DESIGN OF A TUNABLE REPLICA OSCILLATOR (TRO) FOR DYNAMIC FREQUENCY ADJUSTMENT IN A 28 NM CMOS PROCESS

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Degree work presented as a requirement to qualify for the title of Electronic Engineer

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Dedicated to our families and friends.

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First and foremost, I want to thank God for all the blessings He has brought into my life.
I would like to express my deepest gratitude to my parents Lina and Fabián, who were present in every moment and stage of my life, for their unconditional love, their dedication, and for shaping me into the person I am today. In the most difficult moments, they were always there, and without them this achievement would not have been possible. And not only them, but my entire family, especially my siblings Silvia, Rouss, and Santiago, who have also been a fundamental driving force in my life.
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Finally, I would also like to thank the Onchip research group and all its members, who contributed and made me feel part of a process where knowledge was always growing; my advisor Eduardo, whose dedication has been a driving force in my life to keep improving; and Professor Javier Ardila, who believed in me and offered teachings that inspired me throughout my academic journey.

With appreciation, **Johan Camilo Estevez Espinosa**

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With appreciation, **Andres Felipe Ballesteros Santos**

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RESUMEN

TÍTULO: DISEÑO DE UN OSCILADOR RÉPLICA AJUSTABLE (TRO) PARA EL AJUSTE DINÁMICO DE FRECUENCIA EN UN PROCESO CMOS DE 28 NM [*]

AUTORES: JOHAN CAMILO ESTEVEZ ESPINOSA
ANDRES FELIPE BALLESTEROS SANTOS [**]

Palabras clave: UVFR, TRO, Reloj Adaptativo, Seguimiento del Camino Crítico, Gestión de Potencia, Oscilador en Anillo.

DESCRIPCIÓN:

El grupo de investigación OnChip se encuentra desarrollando un regulador unificado de voltaje y frecuencia (UVFR) con el objetivo de mejorar la eficiencia en la gestión de potencia en circuitos digitales integrados. Un componente clave de esta arquitectura es el Oscilador Replica Ajustable (TRO), el cual ajusta dinámicamente la frecuencia de reloj para seguir el retardo del camino crítico en un circuito digital.

Sin embargo, el diseño del TRO presenta desafíos asociados a la sensibilidad frente al voltaje de alimentación y a la capacidad de replicar con precisión el comportamiento temporal del camino crítico. Este trabajo se enfoca en el diseño de un TRO, abordando su análisis, exploración, diseño y validación mediante simulaciones rigurosas en un proceso CMOS estándar de 28 nm de TSMC.

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[*] Trabajo de Grado

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ABSTRACT

TITLE: DESIGN OF A TUNABLE REPLICA OSCILLATOR (TRO) FOR DYNAMIC FREQUENCY ADJUSTMENT IN A 28 NM CMOS PROCESS [*]

AUTHORS: JOHAN CAMILO ESTEVEZ ESPINOSA
ANDRES FELIPE BALLESTEROS SANTOS [**]

Keywords: UVFR, TRO, Adaptive Clocking, Critical Path Matching, Power Management, Ring Oscillator.

DESCRIPTION:

The OnChip research group is developing a Unified Voltage and Frequency Regulator (UVFR) system to improve energy management efficiency in integrated digital circuits. A key component of this system is the Tunable Replica Oscillator (TRO), which dynamically adjusts the clock frequency to match the delay of the critical path in a digital circuit. However, the design of the TRO presents challenges related to power supply sensitivity and accurate replication of the critical path. This work focuses on the design of a TRO circuit that involves analyzing, exploring, designing, and validating the system through rigorous simulations using a 28 nm TSMC standard CMOS process.

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[*] BSc Thesis

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1. INTRODUCTION

Integrated digital circuits are the foundation of modern electronic devices, and as their functional complexity and operating frequency increase, so does their power consumption. Optimizing this consumption has therefore become a fundamental challenge, not only to reduce energy impact but also to ensure long-term reliability[1].

A major difficulty in addressing this challenge arises from variations in operating conditions. In particular, during dynamic operation, supply voltage drops may occur, which increase the critical path delay [2]. This increment can lead to timing errors when the clock frequency is fixed and does not account for such fluctuations.

To prevent this, the operating frequency is set considering worst-case dynamic scenarios to guarantee reliable operation under any condition[3]. While this approach ensures correct operation, it introduces conservative safety margins, known as guardbands, to cover these scenarios. However, since most integrated circuits operate under nominal conditions, where worst-case scenarios rarely occur, these margins consequently limit the performance and energy efficiency of conventional designs [4][5].

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[1] Shaik Jani BABU et al. Extending Silicon Lifetime: A Review of Design Techniques for Reliable Integrated Circuits. In: *arXiv preprint arXiv:2503.21165*. 2025. DOI: 10.48550/arXiv.2503.21165.

[2] K. A. BOWMAN et al. A 45 nm Resilient Microprocessor Core for Dynamic Variation Tolerance. In: *IEEE Journal of Solid-State Circuits*. 2011, vol. 46, no. 1, pp. 194–208. DOI: 10.1109/JSSC.2010.2089657.

[3] Dae-Young KIM et al. Adaptive Clocking Using Supply Tracking Clock Modulator With Background-Calibrated Supply Sensitivity. In: *IEEE Solid-State Circuits Letters*. 2022, vol. 5, pp. 86–89.

[4] Tetsutaro HASHIMOTO et al. An adaptive-clocking-control circuit with 7.5% frequency gain for SPARC processors. In: *IEEE Journal of Solid-State Circuits*. 2018, vol. 53, no. 4, pp. 1028–1037. DOI: 10.1109/JSSC.2017.2786250.

[5] Xun SUN et al. An All-Digital Fused PLL-Buck Architecture for 82% Average Vdd-Margin Reduction in a 0.6-to-1.0-V Cortex-M0 Processor. In: *IEEE Journal of Solid-State Circuits*. 2019, vol. 54, no.

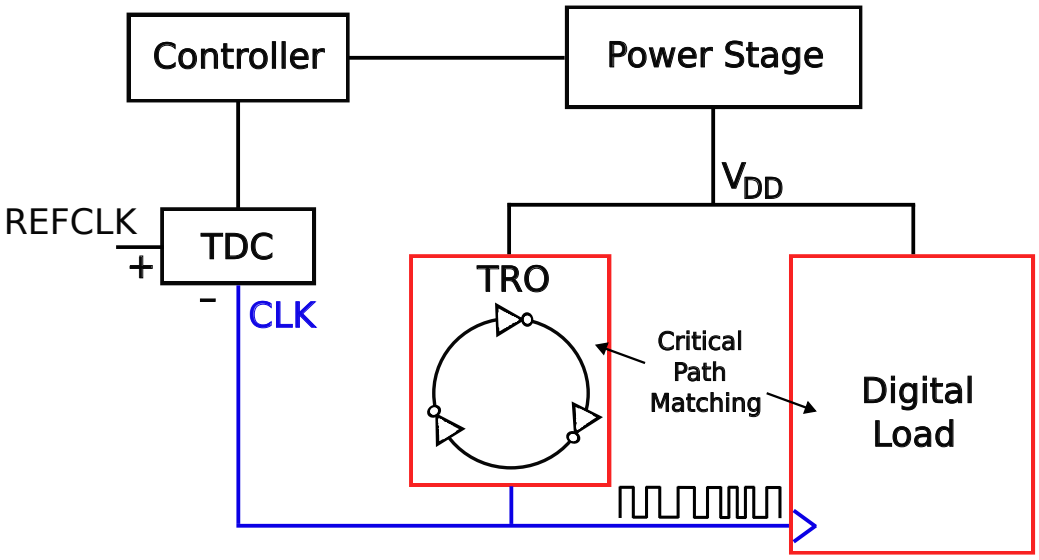
To overcome these limitations, adaptive approaches have been proposed in which parameters such as supply voltage and clock frequency are dynamically adjusted according to real-time conditions. Architectures that coordinate both parameters, such as the Unified Voltage and Frequency Regulator (UVFR) illustrated in Figure 1.1, have demonstrated significant reductions in guardbands and improvements in energy efficiency. Within these architectures, the block responsible for replicating the temporal behavior of the critical path is the Tunable Replica Oscillator (TRO). The TRO is an oscillator whose primary function is to replicate the critical path delay of the digital circuit, thereby generating a clock signal whose frequency depends on the supply voltage [6][7]. Based on this approach, this work focuses on the design and validation of a TRO aimed at replicating the critical path delay of a digital load under dynamic variations, enabling the reduction of guardbands without compromising timing integrity.

11, pp. 3215–3225.

[6] M. CHO et al. Postsilicon Voltage Guard-Band Reduction in a 22 nm Graphics Execution Core Using Adaptive Voltage Scaling and Dynamic Power Gating. In: *IEEE Journal of Solid-State Circuits*. 2017, vol. 52, no. 1, pp. 50–63. DOI: 10.1109/JSSC.2016.2601319.

[7] K. A. BOWMAN et al. A 16 nm All-Digital Auto-Calibrating Adaptive Clock Distribution for Supply Voltage Droop Tolerance Across a Wide Operating Range. In: *IEEE Journal of Solid-State Circuits*. 2016, vol. 51, no. 1, pp. 8–17.

Figure 1.1. Block diagram of the UVFR.



1.1. OBJECTIVES

GENERAL OBJECTIVE

To design a Tunable Replica Oscillator (TRO) for dynamic clock regulation in 28 nm CMOS process.

SPECIFIC OBJECTIVES

To select the appropriate architecture for the TRO based on a detailed analysis of the state of the art.

To design a TRO circuit for dynamic clock regulation based on the selected architecture.

To validate the performance of the TRO through post layout simulations with PVT and Monte Carlo analysis.

2. PROJECT OVERVIEW

2.1. SYSTEM DESCRIPTION

2.1.1. UVFR The UVFR, as illustrated in Figure 1.1, is proposed as an energy management circuit in which the digital load supply voltage and the operating frequency are directly related, allowing the clock frequency to be dynamically adjusted as a function of V_{DD}[8]. This approach relies on adaptive tracking of circuit conditions to regulate performance and energy consumption[9]. The system consists of a power stage that generates the supply voltage shared by both the digital load and the TRO, as well as a control loop that adjusts both the operating frequency and the supply voltage.

In this framework, the dynamic adjustment of the frequency, known as *adaptive clocking*, allows the clock period to adapt to system variations. As supply voltage droops become a major limitation in high-performance systems[10], adaptive clocking techniques dynamically modify the clock frequency to maintain timing integrity[3]. As observed in Figure 2.1, a reduction in V_{DD} leads to an increase in the critical path delay, which translates into an increase in the clock period to avoid timing violations. In this way, the operating frequency follows the circuit behavior.

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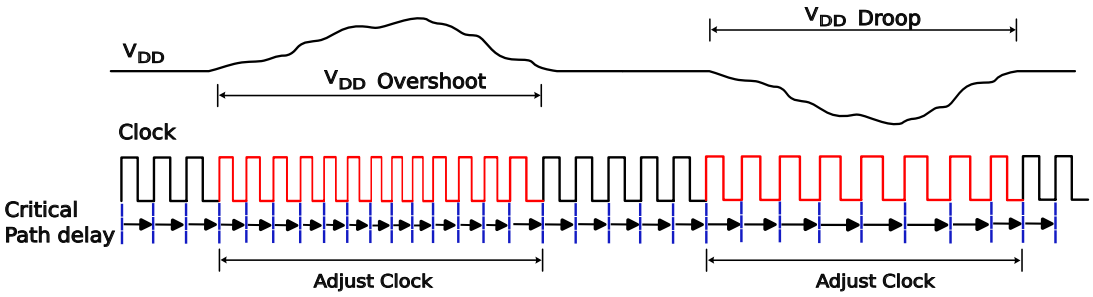
[8] Jae-Won KIM et al. UVFR: A Unified Voltage and Frequency Regulator with 500MHz/0.84V to 100kHz/0.27V Operating Range, 99.4% Current Efficiency and 27% Supply Guardband Reduction. In: *IEEE International Solid-State Circuits Conference (ISSCC)*. 2017, pp. 298–299.

[9] Fahim ur RAHMAN et al. Computationally Enabled Minimum Total Energy Tracking for a Performance Regulated Sub-Threshold Microprocessor in 65-nm CMOS. In: *IEEE Journal of Solid-State Circuits*. 2020, vol. 55, no. 2, pp. 494–504.

[10] Michael S. FLOYD et al. 26.5 Adaptive clocking in the POWER9 processor for voltage droop protection. In: *2017 IEEE International Solid-State Circuits Conference (ISSCC)*. 2017, pp. 444–445.

Figure 2.1. Example of dynamic clock frequency adaptation.

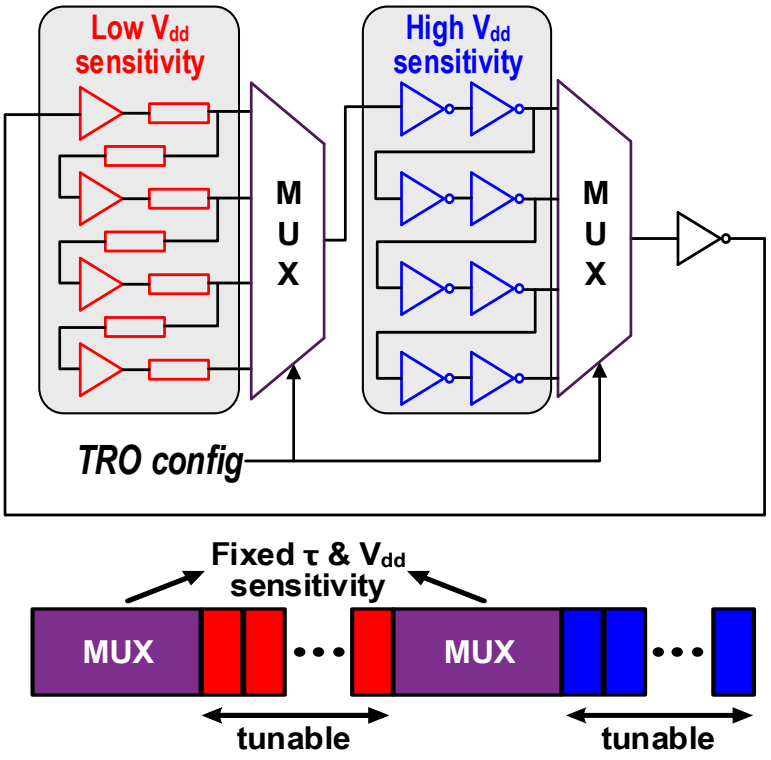


2.1.2. TRO The TRO is a block responsible for replicating the temporal behavior of the critical path through its oscillation frequency. It is based on a ring oscillator that acts as a calibrated Voltage Controlled Oscillator (VCO), whose frequency varies as a function of the supply voltage, emulating the critical path delay.

The classical TRO topology, shown in Figure 2.2, employs delay cells with different sensitivity to V_{DD}, which can be selected or combined using multiplexers. This enables the adjustment of both the oscillation delay and its sensitivity to the supply voltage, allowing it to match the behavior of the critical path under varying operating conditions [11].

[11] X. SUN et al. UniCaP-2: Phase-Locked Adaptive Clocking with Rapid Clock Cycle Recovery in 65nm CMOS. In: *2020 IEEE Symposium on VLSI Circuits*. 2020, pp. 1–2. DOI: 10.1109/VLSICircuits18222.2020.9162982.

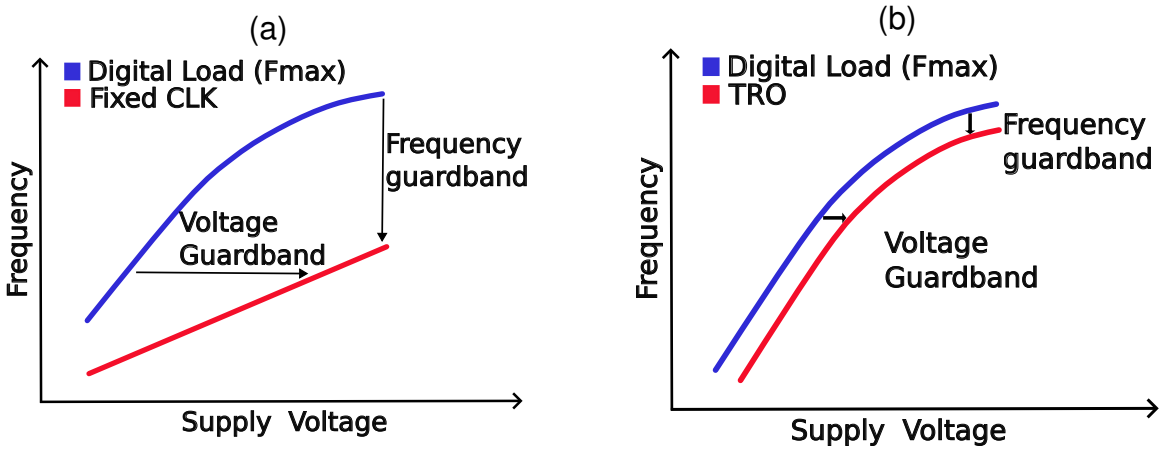
Figure 2.2. Basic TRO topology.



2.2. GUARDBAND REDUCTION

In conventional approaches, the operating frequency is defined considering worst-case conditions, which introduces a significant safety margin. As shown in Figure 2.3(a), the clock frequency is fixed below the maximum achievable frequency, resulting in a guard-band that ensures correct operation under unfavorable conditions. This fixed frequency is typically provided by a Phase-Locked Loop (PLL), whose output remains constant once configured. After applying adaptive clocking, the system behavior changes, as illustrated in Figure 2.3(b). In this case, the operating frequency dynamically follows the circuit conditions, reducing the difference between the achievable frequency and the applied clock frequency. This adjustment leads to a reduction of the guardband, allowing the system to operate closer to the limit imposed by the critical path without relying on overly conservative margins.

Figure 2.3. (a) Conventional fixed clock (b) Adaptive clocking with guardband reduction.



2.3. REFERENCE FREQUENCY–VOLTAGE CHARACTERIZATION CURVES

Given that the present work focuses exclusively on the design of the TRO and does not consider the development of the load, a characterization of the frequency–voltage (F–V) relationship of a digital circuit is required. The curve used was extracted from the frequency–voltage characterization of a digital load reported by Du et al [12], and is employed as the reference characterization for the analysis and validation of the TRO behavior.

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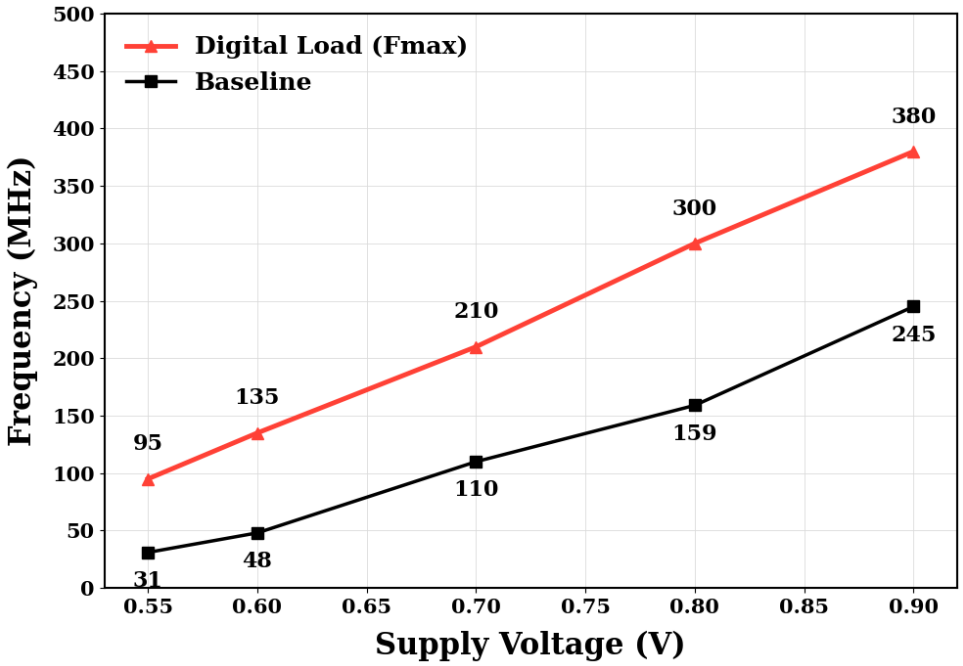
[12] Y. DU et al. DSC-TRCP: Dynamically Self-Calibrating Tunable Replica Critical Paths Based Timing Monitoring for Variation Resilient Circuits. In: *IEEE Journal of Solid-State Circuits*. 2024, vol. 59, no. 7, pp. 2286–2296. DOI: 10.1109/JSSC.2023.3347469.

Figure 2.4. Frequency–voltage curves under (a) slow–slow and (b) nominal conditions.

(a)



(b)

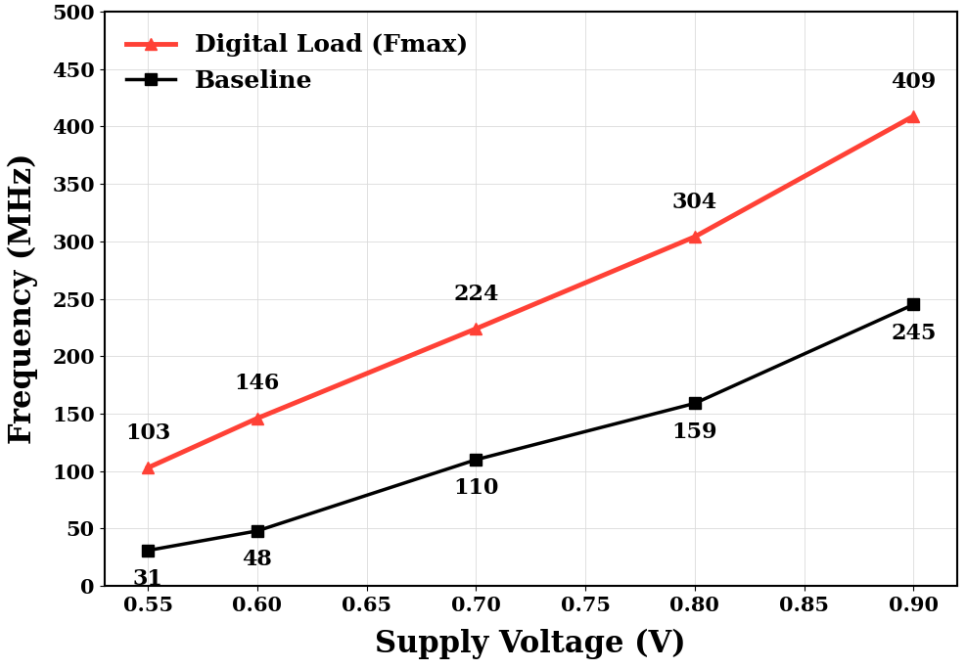


Figure 2.4 illustrates the performance of the digital load under different operating conditions. The baseline corresponds to the fixed operating frequency achieved without adaptive clocking, using a conservative guardband, whereas the curve labeled as “digital load” represents the maximum operating frequency of the digital logic. Additionally, it can be observed that this curve exhibits an approximately linear relationship between frequency and supply voltage.

2.4. DESIGN SPECIFICATIONS

To define the TRO design requirements, different architectures reported in the state of the art were taken as reference. Table 2.1 summarizes the target parameters for this design. The maximum operating frequencies are set to 103 MHz at 0.55 V and 409 MHz at 0.9 V, covering the intended supply voltage range, in order to ensure that the oscillator can adequately track circuit variations and prevent timing errors. The maximum power consumption is set to 440 µW, considering the consumption of all internal blocks of the TRO. The target phase noise of -90 dBc/Hz at 1 MHz offset is established based on values reported for ring oscillators in the state of the art, since the TRO is based on that topology.

Table 2.1. TRO specifications.

Parameter	**Unit**	**Design Target**		
		Min	**Typ**	**Max**
Supply Voltage	V	0.55	-	0.9
Output Frequency ($V_{DD} = 0.55$ V)	MHz	-	-	103
Output Frequency ($V_{DD} = 0.9$ V)	MHz	-	-	409
Guardband Reduction	%	-	TBM	-
Average Power Consumption	μW	-	-	440
Energy Per Cycle	pJ/Cycle	-	-	1.20
Phase Noise @ 1 MHz offset	dBc/Hz	-	-90	-
Cycle-to-Cycle Jitter (RMS)	ps	-	TBM	-
Period Jitter (RMS)	ps	-	TBM	-
Average Current ($E = 1$)	μA	-	-	480
Average Current ($E = 0$)	nA	-	TBM	-
Peak Current	mA	-	TBM	-

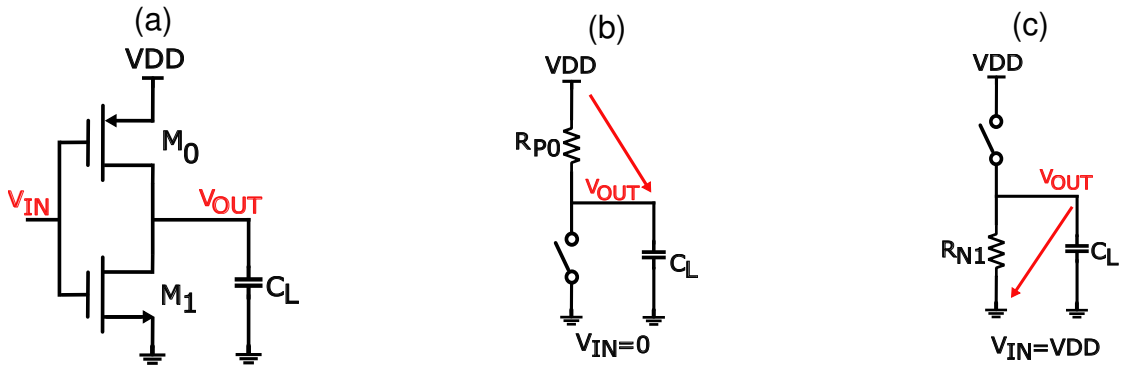
3. DESIGN METHODOLOGY

3.1. CMOS INVERTER MODELING

The CMOS inverter is a key element in delay based circuits, as its dynamic behavior determines the propagation delay of each stage and, consequently, the performance of architectures constructed from their concatenation, such as the ring oscillator.

Figure 3.1(a) shows the schematic of a CMOS inverter composed of a complementary pair of transistors driving a load capacitance C_L at the output node. This capacitance accounts for both intrinsic parasitic effects and the loading introduced by subsequent stages. The transient behavior and the corresponding RC models associated with the output transitions are illustrated in Figure 3.1(b) and Figure 3.1(c).

Figure 3.1. (a) CMOS inverter (b) RC model in low-to-high transition (c) RC model in high-to-low transition.



As a consequence of the switching behavior, the output voltage cannot change instantaneously and follows an exponential response that can be approximated by a first-order RC model. The transient behavior during charging and discharging can be expressed as:

$$V_{out}(t) = V_{DD}\left(1 - e^{-t/(R_{p0}C_L)}\right) \qquad (1)$$

$$V_{out}(t) = V_{DD}e^{-t/(R_{n1}C_L)} \qquad (2)$$

where R_{P0} and R_{n1} represent the effective resistances of the PMOS and NMOS transistors, respectively.

The propagation delay of the inverter is defined as the time required for the output voltage to reach half of the supply voltage. Based on this definition, the delay for both transitions can be derived by solving the previous expressions, yielding:

$$t_{PLH} = R_{p0} C_L \ln(2) \quad (3) \qquad t_{PHL} = R_{n1} C_L \ln(2) \quad (4)$$

The overall propagation delay is defined as the average of both transitions:

$$td = \frac{t_{PLH} + t_{PHL}}{2} \quad (5)$$

For analytical modeling, the inverter can be represented using a single equivalent resistance R_{eq}, leading to the expression:

$$t_d = \ln(2) \cdot C_L \cdot R_{eq} \quad (6)$$

This formulation shows that the propagation delay is determined by the RC time constant of the output node.

3.2. ANALYTICAL MODELING OF RING OSCILLATOR

The TRO employs a ring oscillator architecture, as it enables direct control of the oscillation frequency through the delay of its stages. Additionally, the ring oscillator exhibits an approximately linear frequency dependence on the supply voltage, which is similar to the frequency-voltage (F–V) relationship observed in the reference curve in Figure 2.4.

For an N-stage oscillator, the oscillation frequency depends on the delay of each stage (t_d), defined as:

$$f = \frac{1}{2Nt_d} \tag{7}$$

Where td is the propagation delay of a single stage, as defined in Eq. (6), and depends on the load capacitance and the equivalent resistance of the transistors. The equivalent resistance can be modeled as in Eq. (8).

$$R_{eq} \approx \frac{1}{\mu C_{ox} \frac{W}{L}(V_{DD} - V_{th})} \tag{8}$$

In this expression, μ is the carrier mobility, C_{ox} is the oxide capacitance, W and L are the transistor dimensions, and V_{th} is the threshold voltage.
Substituting these expressions, the oscillation frequency can be approximated as given in Eq. (9).

$$f \approx \frac{\mu C_{ox} \frac{W}{L}(V_{DD} - V_{th})}{2N \ln(2) C_L} \tag{9}$$

This formulation shows that the propagation delay is determined by the RC time constant of the output node. This formulation confirms that the frequency exhibits a linear relationship with the supply voltage, meaning that V_{DD} acts as a design parameter of the circuit, since a variation in the supply voltage directly translates into a change in the oscillation frequency, which can be expressed in simplified form as given in Eqs. (10) and (11).

$$f \approx m \cdot (V_{DD} - V_{th}) \tag{10}$$

$$m = \frac{\mu C_{ox}(W/L)}{2N \ln(2) C_L} \tag{11}$$

From this model, the slope m of the curve F-V can be adjusted by modifying the number of stages N, while the horizontal shift of the curve is determined by the transistor threshold voltage V_{th}. Therefore, the TRO enables a supply voltage sensitive relationship, while also allowing both the slope and the position of the curve to be tuned.
The dynamic power consumption of the ring oscillator is described by Eq. (12):

$$P_{dyn} = N \cdot C_L \cdot V_{DD}^2 \cdot f \tag{12}$$

In this expression, N represents the number of stages in the oscillator, while C_L corresponds to the load capacitance of each stage. The equation shows that power consumption is directly proportional to both the operating frequency (f) and the capacitance.

3.3. TELESCOPIC TRO ARCHITECTURE

Conventional TRO architectures implement frequency tuning by selecting different delay paths through multiplexers. In this approach, each delay configuration corresponds to one input of the multiplexer, so the tuning resolution is directly determined by the number of implemented configurations. Achieving finer control requires increasing this number, which leads to larger multiplexers and increased circuit complexity.

As a result, multiplexers introduce an additional delay within the oscillation loop that is not part of the intrinsic delay of the delay cells. This degrades the accuracy of critical path delay replication, since the total delay includes the contribution of the multiplexer. In addition, the sensitivity of the delay cells is fixed, so tuning is performed by selecting predefined delay paths.

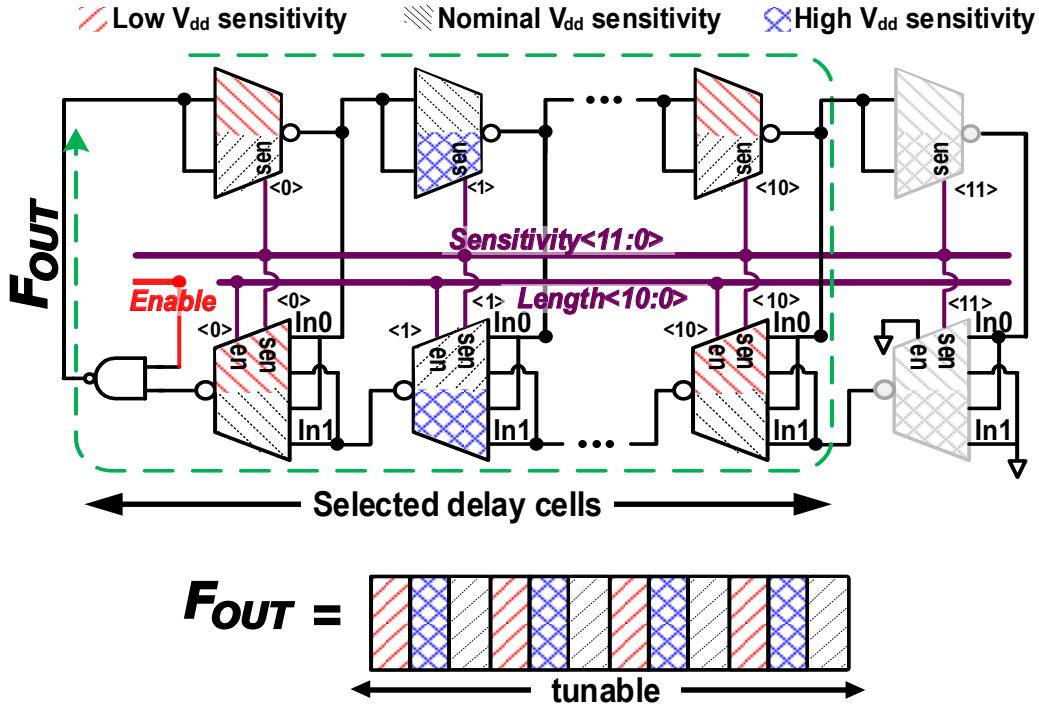
In contrast, the Telescopic TRO architecture, illustrated in Figure 3.2, consists of a closed-loop structure employing delay cells based on inverting multiplexers. Instead of relying on large multiplexers, the tuning mechanism is distributed across multiple delay cells, enabling local control of both the effective delay and the sensitivity. This approach avoids the fixed-sensitivity delay overhead observed in conventional architectures (Figure 2.2) and enables a more flexible distribution of the effective delay.

The main differences between both approaches are summarized in Table 3.1, where it can be observed that the telescopic architecture reduces the impact of multiplexing structures on the critical path while enabling finer and more distributed tuning.

Table 3.1. Architectural Comparison: Conventional vs. Telescopic TRO.

	Conventional TRO	**Telescopic TRO**
Delay overhead	Fixed MUX-induced delay in the loop	Avoids fixed MUX overhead
Sensitivity per cell	Fixed (Predefined by path)	Configurable (Cell-level control)

Figure 3.2. Telescopic TRO architecture.



As shown in Figure 3.2, the TRO integrates a NAND gate that receives the enable signal, which is used as a controlled startup mechanism by enabling the feedback loop and allowing oscillation. Since this logic gate acts as the first inverting stage of the loop, the rest of the chain is configured with an even number of delay cells, thereby ensuring an odd total number of inversions, which is a necessary condition for oscillation in ring oscillator structures.

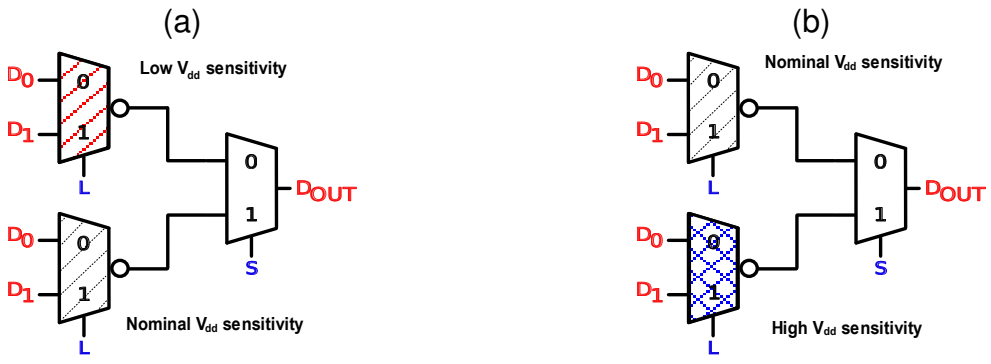
The oscillator configuration is digitally controlled through two main control buses, $Length$ and $Sensitivity$.The Length bus defines which delay stages are active by

enabling or disabling pairs of cells, thereby modifying the total loop delay and the oscillation frequency. Meanwhile, the Sensitivity bus does not change the number of stages, but acts on the active delay cells by selecting transistors with different threshold voltage (V_{th}), which allows tuning the delay sensitivity to variations in V_{DD}. The combination of both mechanisms provides more precise control of the oscillator delay and, consequently, its frequency.

The design consists of two arrays of delay cells based on 2:1 and 4:1 inverting multiplexers, where both architectures are available in two sensitivity variants. The high-sensitivity variant, allows switching between a nominal configuration and a high-V_{th} transistors. Meanwhile, the low-sensitivity variant, enables selection between a nominal configuration and a lower-sensitivity configuration using low-V_{th} transistors. This organization allows the output signal F_{OUT} to be formed by a tunable sequence of these cells.

Internally, the 4:1 delay cells are composed of two inverter multiplexers 2:1 and an output multiplexer, whose implementation variants are detailed in Figure 3.3.

Figure 3.3. (a) Low-sensitivity delay cell (b) high-sensitivity delay cell.

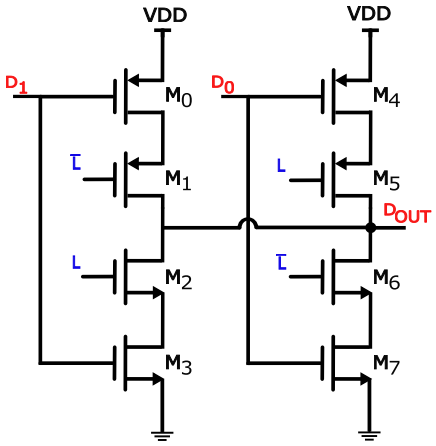


As shown in Figure 3.3, both variants process the input signals D_0 and D_1 in parallel through 2:1 inverting multiplexers implemented with different V_{th} combinations depending on the sensitivity mode. An output multiplexer, controlled by the sensitivity signal S, selects the active path and defines the final output D_{OUT}.

The 2:1 inverting multiplexer is implemented using two parallel tri-state inverters whose outputs are connected to a common node. This topology was selected over pass-transistor logic due to the absence of threshold voltage degradation, which helps maintain full-swing operation. Compared to transmission-gate implementations, the tri-state approach reduces the number of internal nodes, thereby lowering parasitic capacitance. The resulting structure and its corresponding truth table, which describes the selection of the active propagation path depending on the control signal L, are shown in Figure 3.4(a) and Figure 3.4(b), respectively.

Figure 3.4. (a) Inverting multiplexer, (b) truth table of inverting multiplexer.

(a)



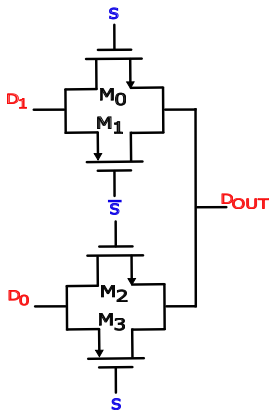
(b)

L	D_0	D_1	D_{out}
0	D_0	D_1	$\overline{D_0}$
1	D_0	D_1	$\overline{D_1}$

In the 4:1 delay cells, both tri-state inverters operate using transistors with the same V_{th} for a given sensitivity configuration, forming the 2:1 inverting multiplexer. In contrast, in the 2:1 delay cells, the two tri-state inverters employ different threshold voltages depending on the selected variant. Specifically, one inverter is implemented with nominal-V_{th} transistors, while the other is configured with either low-V_{th} or high-V_{th} transistors. Finally, Figure 3.5(a) shows the output multiplexer implemented using transmission gates, which is responsible for selecting the corresponding signal path without altering its polarity. The logical behavior is summarized in the truth table shown in Figure 3.5(b).

Figure 3.5. (a) Multiplexer, (b) truth table of multiplexer.

(a)



(b)

S	D_0	D_1	D_{out}
0	D_0	D_1	D_0
1	D_0	D_1	D_1

The 2:1 inverting multiplexer is implemented using tri-state inverters, as shown in Figure 3.4(a), where the selection between D_0 and D_1 is controlled by the signal L. Its behavior under different supply voltage conditions is presented in Tables 3.2 and 3.3. The 4:1 inverting multiplexer follows the same principle, as illustrated in Figure 3.3, employing the control signals L and S to select the corresponding input. Its behavior under different supply voltage conditions is presented in Tables 3.4 and 3.5.

Table 3.2. 2:1 inverting multiplexer (high V_{DD} sensitivity).

S	D_0	D_1	D_{out}
0	D_0	D_1	$\overline{D_{0\text{NVth}}}$
1	D_0	D_1	$\overline{D_{1\text{HVth}}}$

Table 3.3. 2:1 inverting multiplexer (low V_{DD} sensitivity).

S	D_0	D_1	D_{out}
0	D_0	D_1	$\overline{D_{0\text{LVth}}}$
1	D_0	D_1	$\overline{D_{1\text{NVth}}}$

Table 3.4. 4:1 inverting multiplexer (high V_{DD} sensitivity).

LS	D_0	D_1	D_{out}
00	D_0	D_1	$\overline{D_{0\text{NVth}}}$
01	D_0	D_1	$\overline{D_{0\text{HVth}}}$
10	D_0	D_1	$\overline{D_{1\text{NVth}}}$
11	D_0	D_1	$\overline{D_{1\text{HVth}}}$

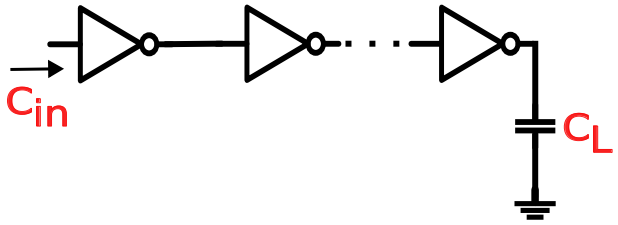
Table 3.5. 4:1 inverting multiplexer (low V_{DD} sensitivity).

LS	D_0	D_1	D_{out}
00	D_0	D_1	$\overline{D_{0\text{LVth}}}$
01	D_0	D_1	$\overline{D_{0\text{NVth}}}$
10	D_0	D_1	$\overline{D_{1\text{LVth}}}$
11	D_0	D_1	$\overline{D_{1\text{NVth}}}$

3.4. BUFFER

The TRO is connected to a digital load, as shown in Figure 1.1, whose input capacitance modifies the oscillation frequency. To address this, a tapered buffer is implemented (see Figure 3.6) to isolate the oscillator from the loading effects.

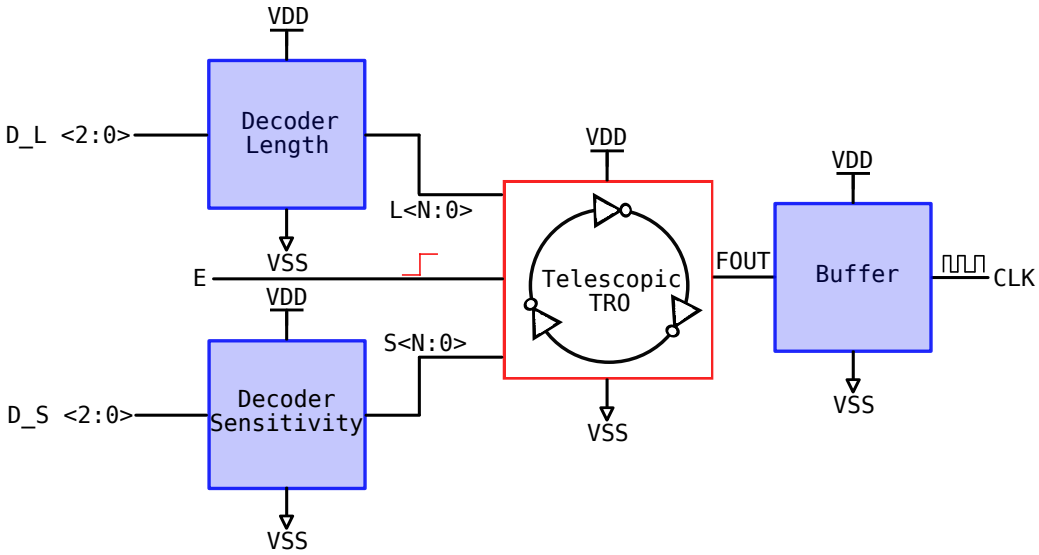
Figure 3.6. Tapered buffer structure.



3.5. DECODER

To reduce the number of control bits, decoders are used to generate the selection signals for the delay stages and sensitivity levels. In this design, the sensitivity control is reduced from 12 bits to 3 bits, and the length control from 11 bits to 3 bits. Figure 3.7 shows the complete TRO architecture, including these decoders and the output buffer.

Figure 3.7. Complete TRO architecture.



4. CIRCUIT IMPLEMENTATION

4.1. VERILOG-A MODELING

The circuit design process began with a Verilog-A modeling stage, aimed at defining the expected electrical behavior based on the mathematical model presented in Chapter 3. This approach enabled the establishment of the system's functional characteristics prior to its transistor-level implementation.

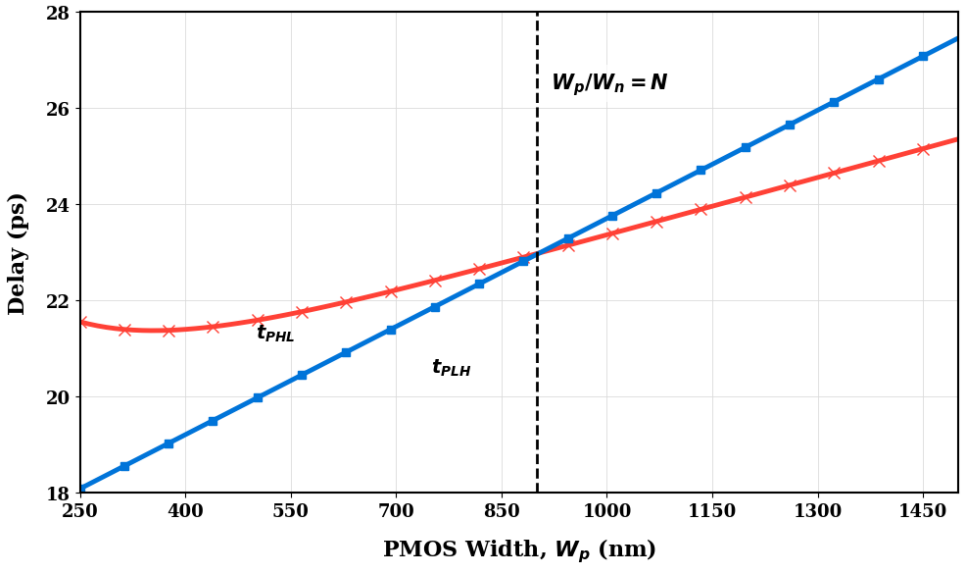
4.2. DESIGN POINT SELECTION

To achieve an operating frequency of 409 MHz, the number of stages N was determined using Eq. (7), evaluating configurations of 17, 37, and 79 stages. From the slope m extracted from the F–V curve of the critical path (Figure 2.4b) in the range of 0.8 V to 0.9 V, the initial NMOS transistor W/L ratio was obtained using Eq. (11). The parameters μC_{ox} and the load capacitance C_L were estimated from transistor characterization simulations.

4.3. BASE INVERTER SIZING

Since each configuration imposes a different propagation delay to operate at 409 MHz, the inverters were sized independently for each case. Starting from the W/L ratio obtained in the previous section, a sweep of L was performed to determine the value that meets the required delay. Then, W_p was swept to match the rise and fall times with an error below 5%, ensuring the condition $t_{PLH} \approx t_{PHL}$, as shown in Figure 4.1.

Figure 4.1. Inverter delay matching.

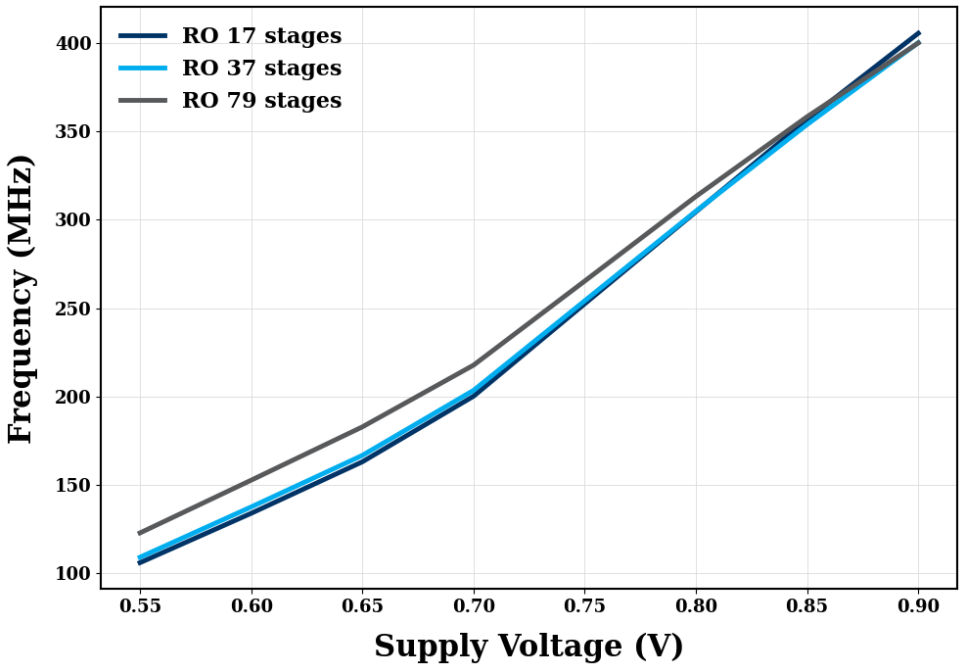


4.4. NUMBER OF STAGE SELECTION

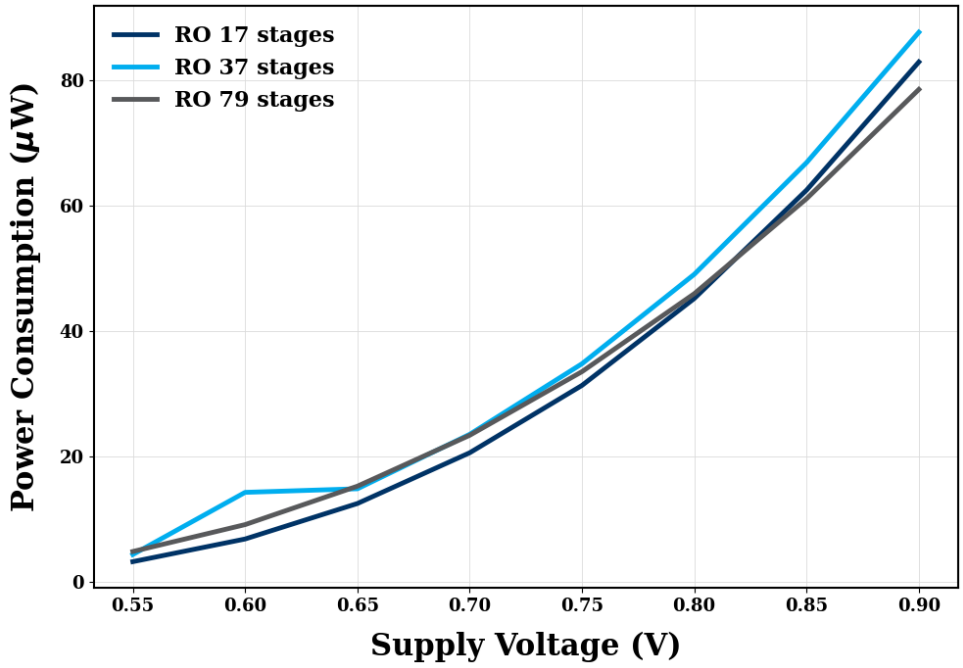
The three ring oscillator stage counts were evaluated through a supply voltage sweep, as shown in Figure 4.2. The 79 stage configuration was selected as it represents an adequate balance between power consumption and available delay margin: since the integration of additional components in each TRO stage increases the delay compared to the base inverter, a configuration with sufficiently low nominal delay is required to absorb this increase and maintain the operating frequency.

Figure 4.2. (a) Frequency vs supply voltage, (b) power vs supply voltage for different numbers of stages.

(a)



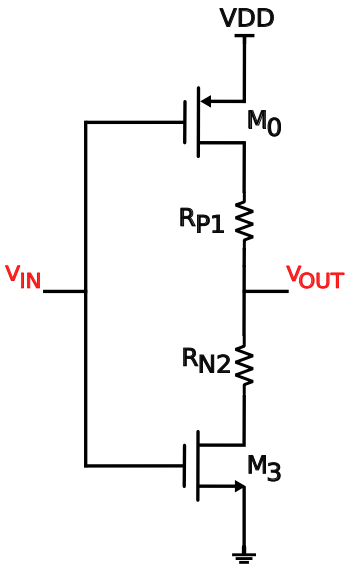
(b)



4.5. TRI-STATE INVERTER CONFIGURATION

After defining the inverter design, it was adapted to a tri-state configuration by inserting enable transistors in series with the pull-up and pull-down networks. Since these additional devices introduce a series resistance when activated, as shown in Figure. 4.3, their dimensions were set to the minimum channel length in order to mitigate their impact on propagation delay. During this stage, the original sizing criteria of the inverter were preserved, ensuring delay symmetry to maintain the condition $t_{PLH} \approx t_{PHL}$.

Figure 4.3. Tri-state inverter model.



Based on this structure, the multiplexers were implemented using tri-state inverters with different threshold voltages (`mac`, `mac_lvt`, `mac_hvt`). The original width (W) and length (L) dimensions were preserved, ensuring that the propagation delay is primarily governed by the threshold voltage.

4.6. TRANSMISSION GATE DESIGN

Minimum channel length was used in the transmission gates to reduce propagation delay. Additionally, the same width W was applied to both NMOS and PMOS transis-

tors. As discussed by Weste and Harris [13], increasing the PMOS width only provides a marginal reduction in conduction resistance while increasing the associated parasitic capacitance.

4.7. OUTPUT BUFFER DESIGN

The output buffer is based on a cascaded inverter structure to drive the external capacitive load. According to the methodology presented by Baker [14], delay-optimized design suggests an ideal tapering factor of $A = e \approx 2.718$. However, since the buffer is the most power-consuming block, energy efficiency is prioritized. As discussed by Villar et al [15], there is a trade-off between driver switching losses and load transition time. Therefore, a two-stage topology ($N = 2$) was selected to reduce switching current, and the tapering factor is defined in Eq. (13).

$$h = \sqrt[N]{\frac{C_{load}}{C_{in1}}} \tag{13}$$

where h is the tapering factor, C_{load} is the external load capacitance driven by the buffer, and C_{in1} is the input capacitance of the first inverter stage. The output waveform is shown in Figure 4.4.

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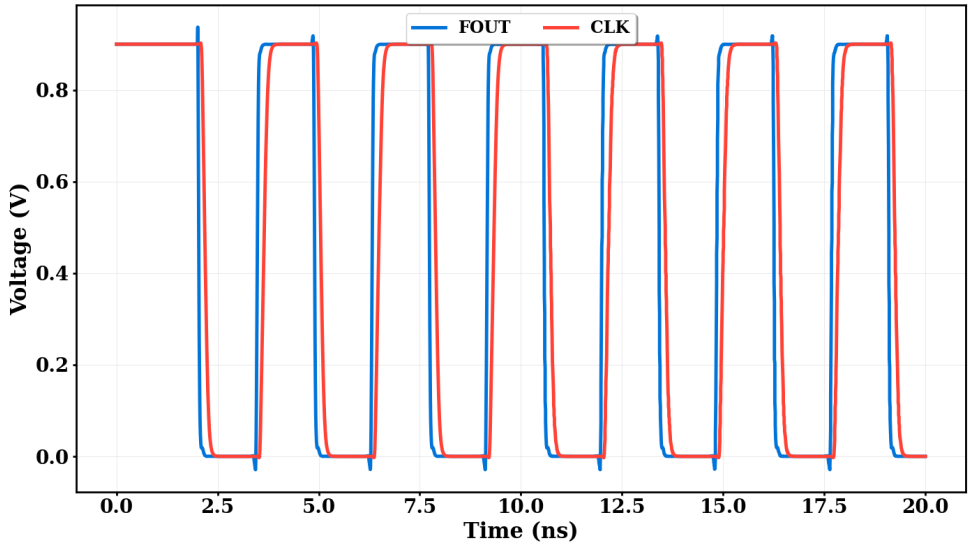
[13] Neil H. E. WESTE et al.. *CMOS VLSI Design: A Circuits and Systems Perspective*. Fourth Edition. Addison-Wesley, 2010.

[14] R Jacob BAKER. *CMOS: circuit design, layout, and simulation*. John Wiley & Sons, 2019.

[15] Gerard VILLAR et al. Energy optimization of tapered buffers for CMOS on-chip switching power converters. In: *2005 IEEE International Symposium on Circuits and Systems*. 2005, pp. 4453–4456.

Figure 4.4. Output buffer waveform at nominal operating conditions.



4.8. START-UP NAND GATE DESIGN

The start-up NAND gate was designed such that its propagation delay closely matches that of the multiplexers implemented with nominal V_{th} transistors. Based on the RC switch model shown in Figure 4.5, the transistor dimensions were selected considering the impact of series and parallel configurations in the conduction networks on the resistance.

This sizing approach enables comparable switching characteristics between the NAND gate and the oscillator delay cells. The resulting delay approximations are summarized in Table 4.1.

Figure 4.5. (a) NAND gate schematic (b) RC switch model.

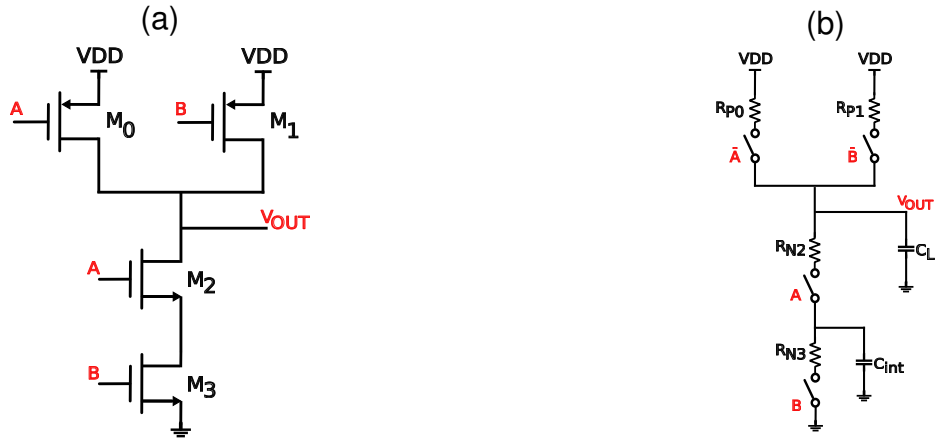
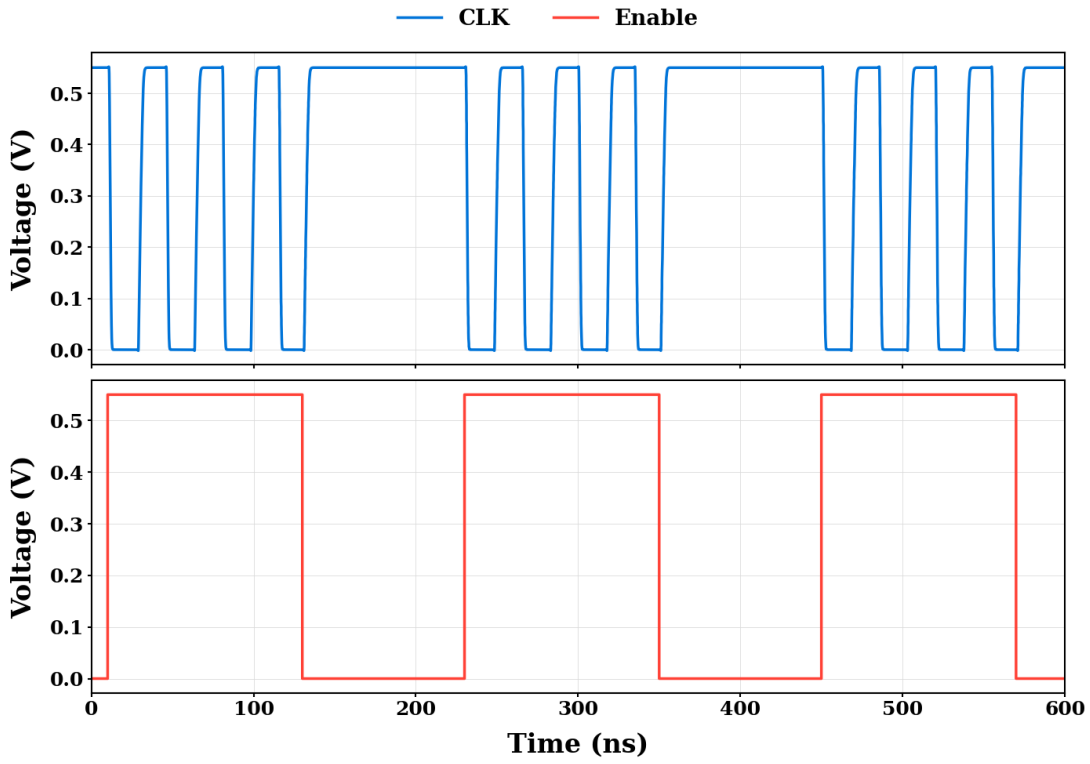


Table 4.1. NAND gate truth table and propagation delay.

A	B	F	Resistance	Approximate Delay
0	0	1	$R_p/2$	$0.69 \cdot R_p/2C_L$
0	1	1	R_p	$0.69 \cdot R_pC_L$
1	0	1	R_p	$0.69 \cdot R_pC_L$
1	1	0	$2R_n$	$0.69 \cdot 2R_nC_L$

In Figure 4.6, the worst case start-up behavior is observed during the transition of the enable signal from 0 to 1.

Figure 4.6. TRO start-up under enable control.



4.9. DECODER DESIGN

Two 3-to-8 decoders were designed to manage the *Length* and *Sensitivity* control words of the TRO. The design was based on Boolean algebra simplification to obtain the required output combinations.

4.10. PVT CALIBRATION

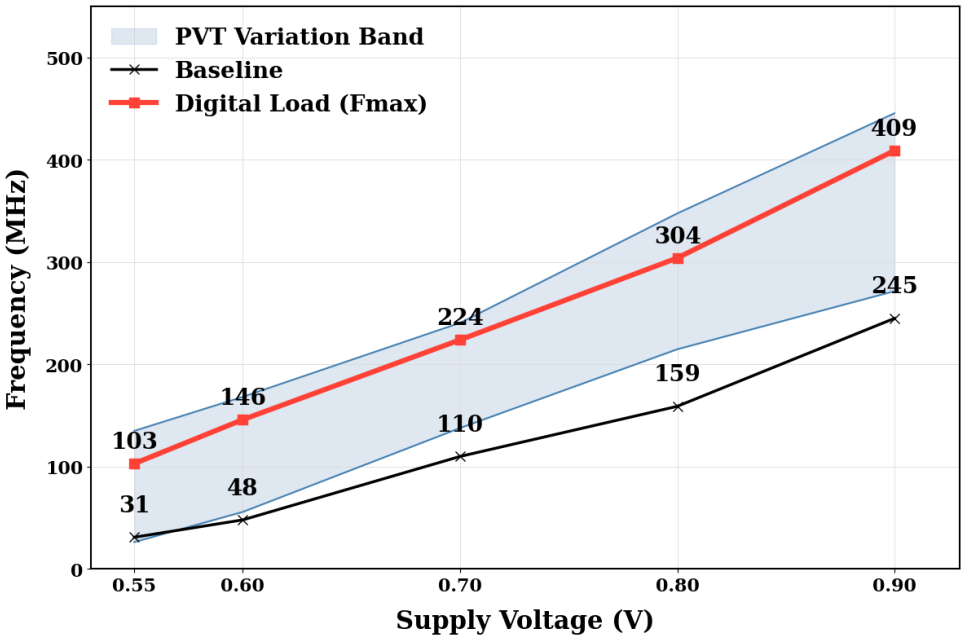
The (F-V) relationship of the TRO before and after calibration is presented in Figure 4.7, considering process, voltage, and temperature (PVT) variations across SS, FF, FS, and SF corners, using the TT condition as the reference. Before calibration, the TRO frequency lies above the digital load curve. The calibration process is performed by modifying the control words associated with the sensitivity and length buses. These settings

affect the effective threshold voltage and the number of active oscillator stages, allowing the TRO oscillation frequency to be adjusted and compensated for PVT variations. After calibration, the frequency remains below this curve within the evaluated operating range, preventing timing violations.

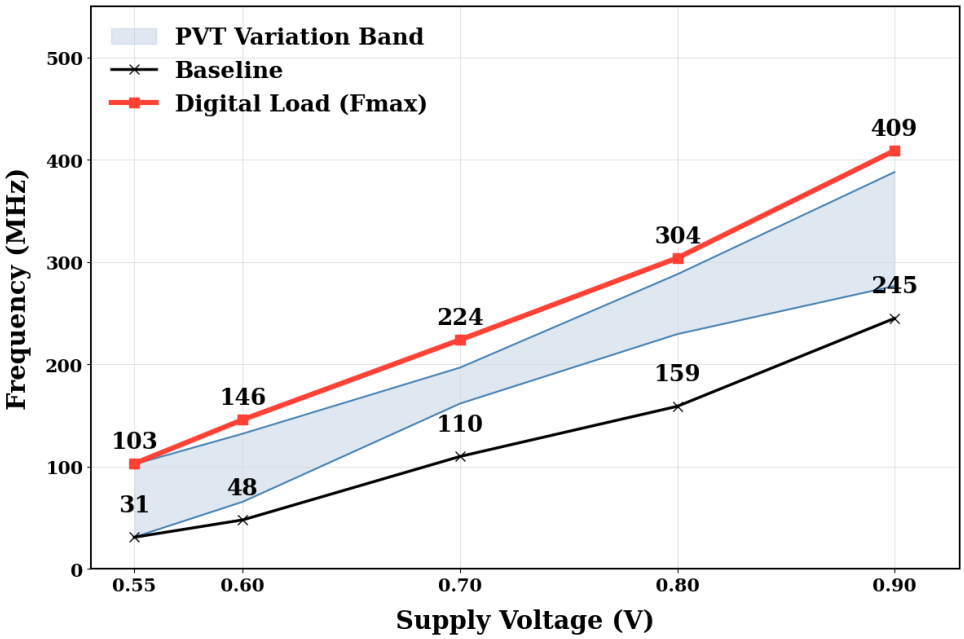
The initial configuration of 79 stages corresponds to a ring oscillator composed only of inverters. As additional elements associated with the multiplexing cells, such as tri-state inverters and transmission gates, are incorporated into each stage, the propagation delay per stage increases. As a result, the total number of stages is reduced, leading to a final configuration of 25 stages used in the TRO.

Figure 4.7. TRO frequency behavior (a) before calibration and (b) after calibration.

(a)



(b)



5. RESULTS

5.1. PRE-LAYOUT SIMULATION

This section presents the pre-layout results of the TRO to validate its performance under different operating conditions. Table 5.1 summarizes the main parameters used in the PVT simulations, which encompass the process corners Slow-Slow (SS), Fast-Fast (FF), Fast-Slow (FS), and Slow-Fast (SF) and the typical condition (TT), along with voltage and temperature variations. The $(F - V)$ curves of the digital load under TT and SS conditions serve as a reference for result comparison.

The evaluation also considers voltage corners; however, specific values are selected for certain measurements. Output frequency is evaluated at 0.55 V and 0.9 V, while power, energy, current, phase noise, and jitter metrics are evaluated at 0.9 V. Guard-band reduction is analyzed at 0.8 V. The enable signal (E) controls the activation of the TRO, where $E = 1$ corresponds to the active state and $E = 0$ to the disabled state.

Table 5.1. TRO evaluation conditions.

Parameter	**Condition**
Output Frequency ($V_{DD} = 0.55$ V)	$V_{DD} = 0.55$ V
Output Frequency ($V_{DD} = 0.9$ V)	$V_{DD} = 0.9$ V
Guardband Reduction	$V_{DD} = 0.8$ V
Average Power Consumption	$V_{DD} = 0.9$ V
Energy per Cycle	$V_{DD} = 0.9$ V
Phase Noise @ 1 MHz offset	$V_{DD} = 0.9$ V
Cycle-to-Cycle Jitter (RMS)	$V_{DD} = 0.9$ V
Period Jitter (RMS)	$V_{DD} = 0.9$ V
Average Current ($E = 1$)	$V_{DD} = 0.9$ V
Average Current ($E = 0$)	$V_{DD} = 0.9$ V
Peak Current	$V_{DD} = 0.9$ V
Process Corners	SS, SF, FS, FF
Temperature	$-40°$C, $25°$C, $125°$C

Table 5.2 summarizes the PVT simulation results, showing that the proposed design meets the target specifications.

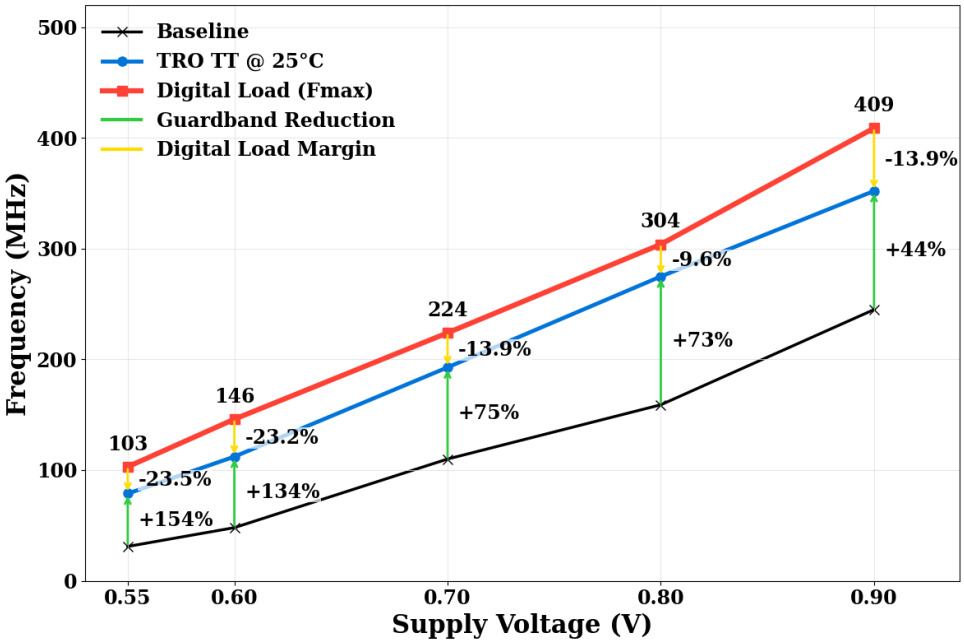
Table 5.2. Simulation results under PVT variations.

Parameter	**Units**	**Target**			**Pre-Layout**			**Judge**
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V	0.55	-	0.90	0.55	-	0.90	Pass
Output Frequency ($V_{DD} = 0.55$ V)	MHz	-	-	103	31.1	78.8	102.3	Pass
Output Frequency ($V_{DD} = 0.9$ V)	MHz	-	-	409	276.6	352.1	388	Pass
Guardband Reduction	%	-	TBM	-	44	73	81	Pass
Average Power Consumption	μW	-	-	440	286	352.1	380.6	Pass
Energy Per Cycle	pJ/Cycle	-	-	1.20	0.97	0.99	1.03	Pass
Phase Noise @ 1 MHz offset	dBc/Hz	-	-90	-	-100.40	-97.71	-96.90	Pass
Cycle-to-Cycle Jitter (RMS)	ps	-	TBM	-	21.41	26.45	34.95	Pass
Period Jitter (RMS)	ps	-	TBM	-	26.69	32.13	41.40	Pass
Average Current ($E = 1$)	μA	-	-	480	317.8	391.2	396.6	Pass
Average Current ($E = 0$)	nA	-	TBM	-	2	15	1383	Pass
Peak Current	mA	-	TBM	-	4.2	5	5.9	Pass

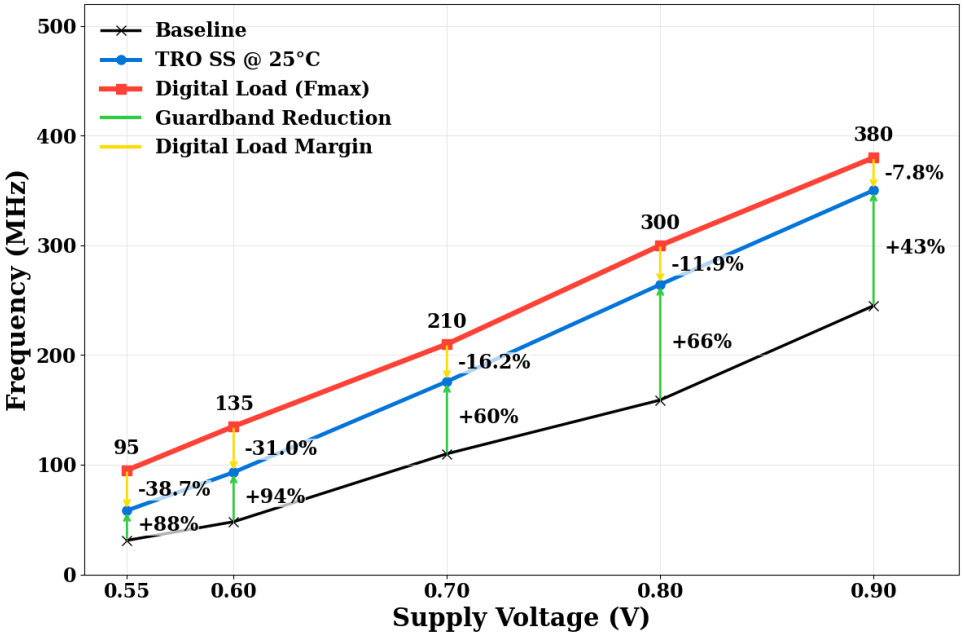
The TRO frequency as a function of V_{DD} is presented in Figure 5.1 for both typical and SS conditions. The analysis of all process corners (SS, SF, FS, FF) and their respective calibrations across different frequency and temperature ranges is detailed in Annex 6.2. Across all operating conditions, the TRO operates above the digital load baseline.Since each process corner and thermal condition exhibits distinct dynamics, an independent calibration was applied to each case. The obtained results show a typical guardband reduction of 73% within a range from 44% to 81%,thereby tracking the critical path without exceeding the safe operating frequency.

Figure 5.1. Pre-layout TRO frequency as a function of V_{DD} for (a) typical case and (b) slow-slow process corner.

(a)



(b)

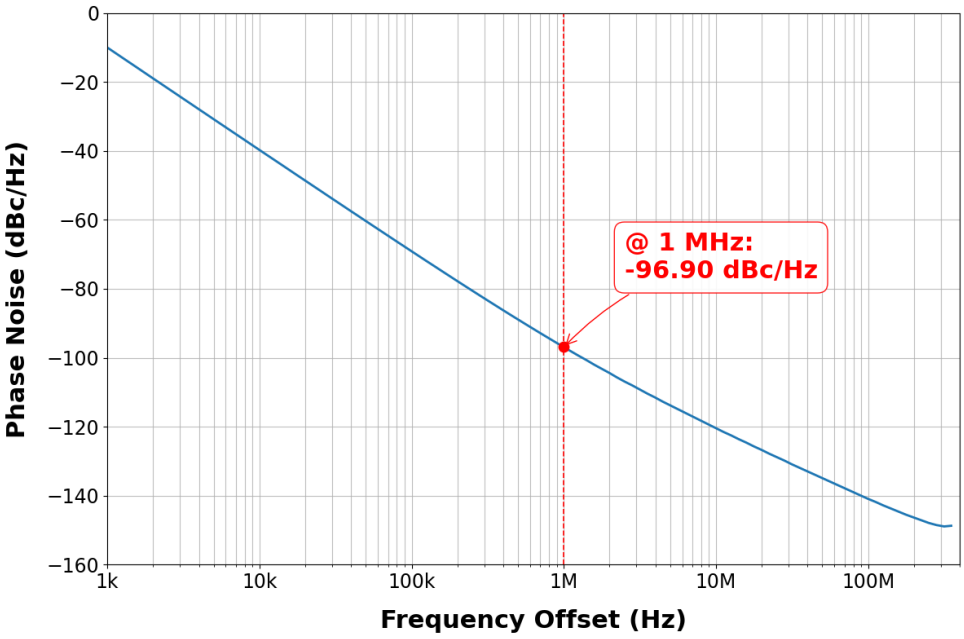


The leakage current of the design exhibits a strong dependence on temperature. Under typical conditions (TT at 25°C), it is approximately 15 nA, increasing to 39 nA in the fast corner (FF at 25°C), which represents a 160% increase. At 125°C (FF), the leakage reaches 1.383 μA, a 3446.15% increase compared to the value at 25°C. This behavior is expected, as leakage current depends exponentially on temperature. This is compounded by the use of LVT transistors in the design, which exhibit higher leakage levels due to their lower V_{th}. The buffer accounts for 40% of this total leakage due to its dimensions. Nevertheless, this worst-case leakage represents only 0.35% of the 396.6 μA maximum dynamic current.Regarding dynamic power, the buffer is the primary contributor, dissipating 329.4 μW, which accounts for 86.53% of the total 380.6 μW. Although dynamic efficiency was prioritized during its sizing, this block remains the largest contributor to the circuit's total power budget.

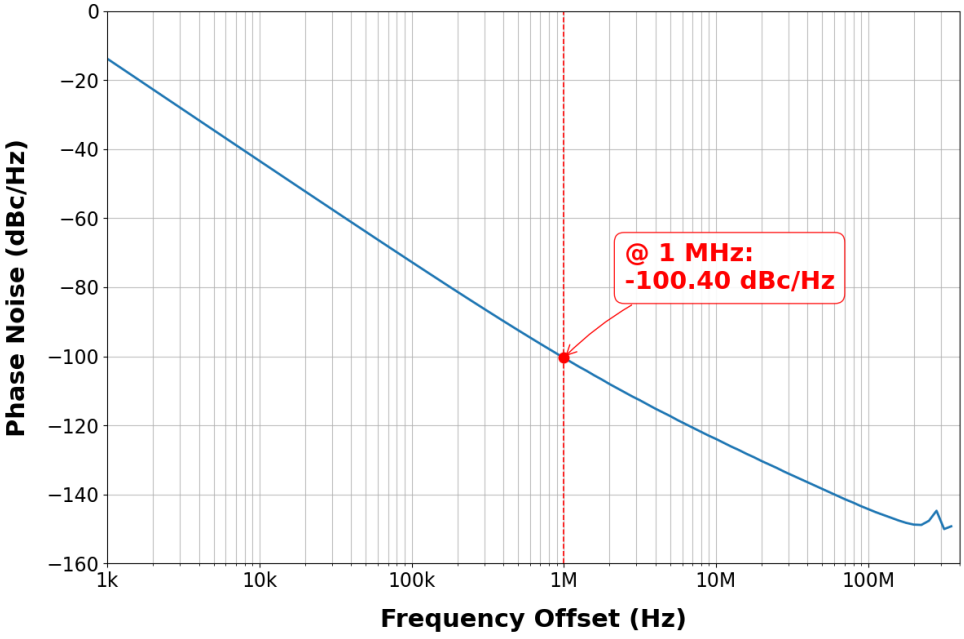
Figure 5.2 presents the simulated phase noise at a 1 MHz offset. The results show a value of -96.90 dBc/Hz for the worst case (a) and -100.40 dBc/Hz for the best case (b). Such values indicate high spectral purity, where the noise power is significantly lower than the carrier power, ensuring a clear and stable oscillation signal.

Figure 5.2. Phase noise pre-layout @ 1MHz (a) worst case and (b) best case.

(a)



(b)



A global Monte Carlo analysis was performed using 100 samples at a supply voltage of

0.8 V, corresponding to the operating point where guardband reduction is reported. The resulting histogram is shown in Figure 5.3. From these 100 samples, 10 were selected to illustrate the TRO calibration procedure, with the corresponding results presented in Figure 5.4.

Figure 5.3. Pre-layout Monte Carlo histogram of the TRO frequency at 0.8 V.

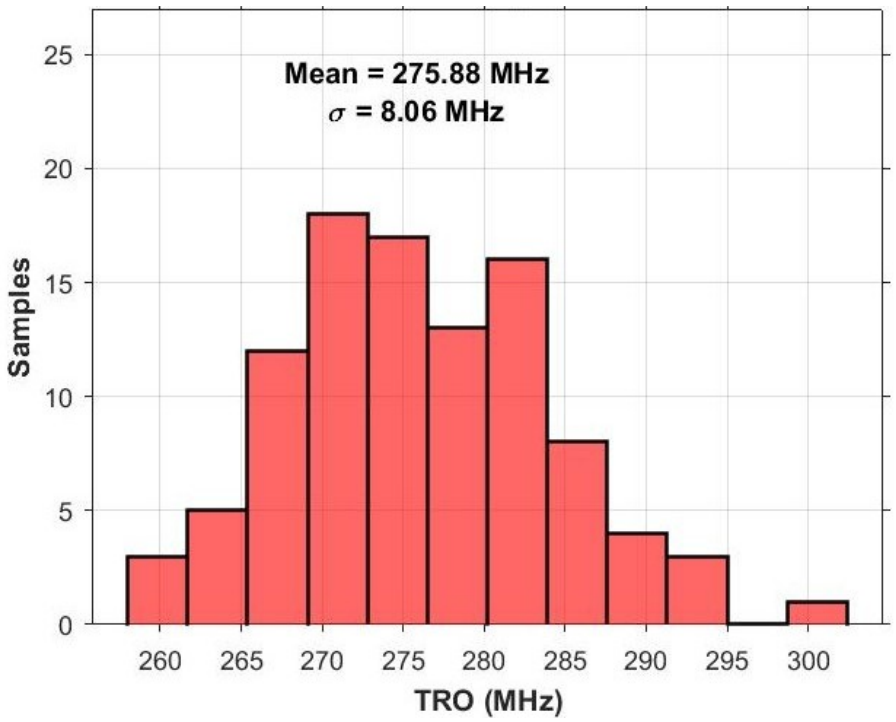
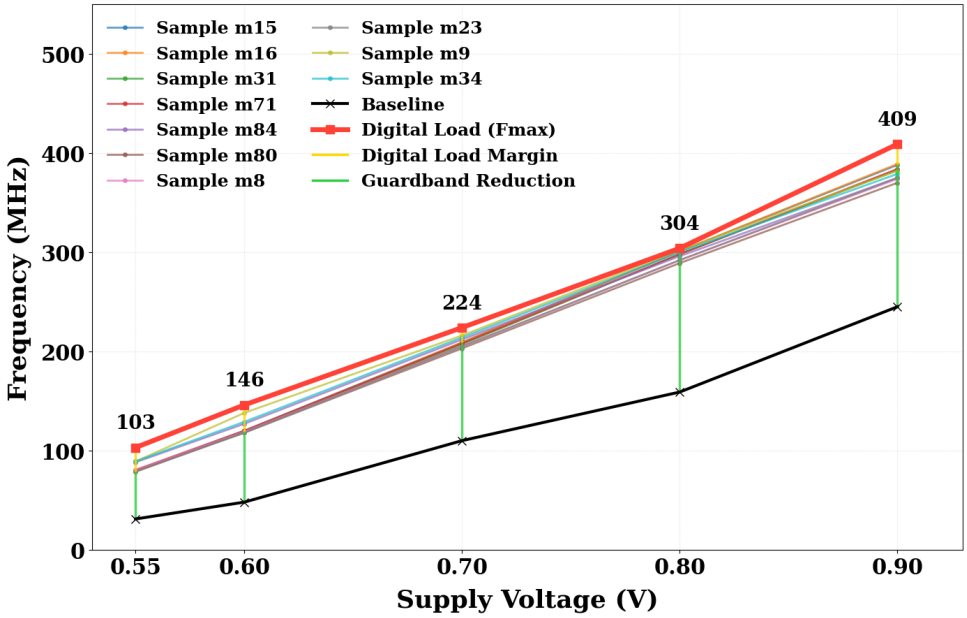


Figure 5.4. Pre-layout Monte Carlo calibration.



5.2. FINAL DIMENSIONS

The TRO architecture. consists of a decoder, and Telescopic TRO, and an output buffer. Their transistor dimensions are summarized in Tables 5.3 and 5.4, where M denotes the transistor multiplier.

The decoder uses NAND, NOR, and inverter gates, while the oscillator core includes tri-state inverters, a NAND gate, and transmission gates with consistent inverter sizing.

Table 5.3. Transistor dimensions of the decoder and TRO oscillator

(a) Decoder Transistor Dimensions

Name	L [μm]	W [μm]	M
Nand			
M_0	0.12	0.12	1
M_1	0.12	0.12	1
M_2	0.12	0.24	1
M_3	0.12	0.24	1
Nor			
M_0	0.12	0.16	1
M_1	0.12	0.16	1
M_2	0.12	0.12	1
M_3	0.12	0.12	1
Inverter			
M_0	0.08	0.16	1
M_1	0.08	0.16	1

(b) Telescopic TRO

Name	L [μm]	W [μm]	M
Tri-State Inverter			
M_0	0.14	0.45	1
M_1	0.03	0.45	1
M_2	0.03	0.25	1
M_3	0.14	0.25	1
Nand			
M_0	0.1	0.3	1
M_1	0.1	0.3	1
M_2	0.1	0.49	1
M_3	0.1	0.49	1
Transmission Gate			
M_0	0.03	0.12	1
M_1	0.03	0.12	1

The inverter used in the decoder is also employed to generate the complementary selection signals required by the multiplexers, maintaining consistent transistor sizing.

Table 5.4 summarizes the dimensions of the output buffer.

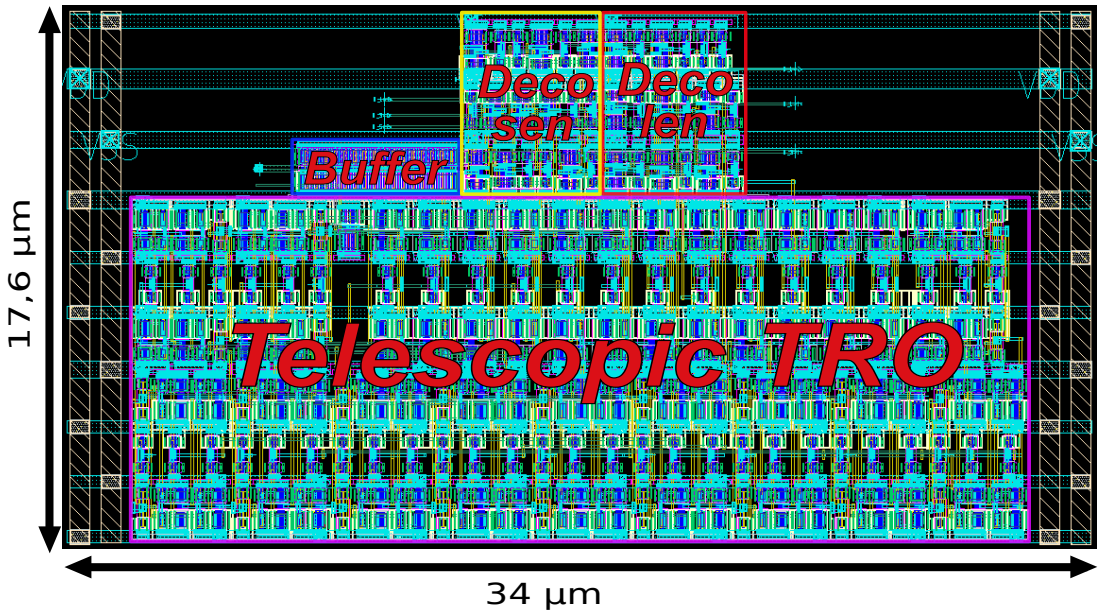
Table 5.4. Buffer transistor dimensions.

Name	L [μm]	W [μm]	M
M_0	0.06	0.48	2
M_1	0.06	0.4	2
M_2	0.06	0.48	30
M_3	0.06	0.4	30

5.3. LAYOUT

The layout of the TRO is shown in Figure 5.5. It consists of three main blocks: the sensitivity decoder (Deco_Sen), the length decoder (Deco_Len), and telescopic TRO.

Figure 5.5. TRO layout circuit.



Key Considerations

- The layout was organized following a standard cell structure for the logic gates to maintain a uniform cell height and consistent alignment, which facilitates the integration of the TRO blocks and allows for more organized signal routing.
- Special emphasis was placed on routing symmetry for critical signals by designing physical connections that follow the schematic's topology, ensuring that delay paths remain balanced and the oscillation preserves the defined timing characteristics.
- To avoid degrading the signal path, lower metal layers were used with a width of 0.05 μm, reducing the metal area and mitigating parasitic capacitance to prevent impacts on the oscillator's operating frequency.
- Due to the current consumption in the output buffer, electromigration criteria were applied to define the width of its traces using a value of 0.21 μm, ensuring the integrity of the metal against the block's current flow.

- The power rails were strategically placed at the sides of the layout instead of crossing through the center of the design to ensure their associated capacitance does not interfere with the TRO signal path.

5.4. POST-LAYOUT

Table 5.5 summarizes the post-layout PVT simulation results, showing that the proposed design meets the target specifications.

Table 5.5. Post-layout simulation results under PVT variations.

Parameter	**Units**	**Target**			**Post-Layout**			**Judge**
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V	0.55	-	0.90	0.55	-	0.90	Pass
Output Frequency ($V_{DD} = 0.55$ V)	MHz	-	-	103	21.3	69.2	102.4	Pass
Output Frequency ($V_{DD} = 0.9$ V)	MHz	-	-	409	294.7	363.2	393	Pass
Guardband Reduction	%	-	TBM	-	52	74	79	Pass
Average Power Consumption	μW	-	-	440	330	389.2	419	Pass
Energy Per Cycle	pJ/Cycle	-	-	1.20	1.05	1.07	1.12	Pass
Phase Noise @ 1 MHz offset	dBc/Hz	-	-90	-	-98.98	-96.10	-95.08	Pass
Cycle-to-Cycle Jitter (RMS)	ps	-	TBM	-	23.42	29.58	38.45	Pass
Period Jitter (RMS)	ps	-	TBM	-	29.90	36.29	47.35	Pass
Average Current ($E = 1$)	μA	-	-	480	367.1	432.5	465.6	Pass
Average Current ($E = 0$)	nA	-	TBM	-	2.04	14.86	1435	Pass
Peak Current	mA	-	TBM	-	5.44	6.29	7.32	Pass

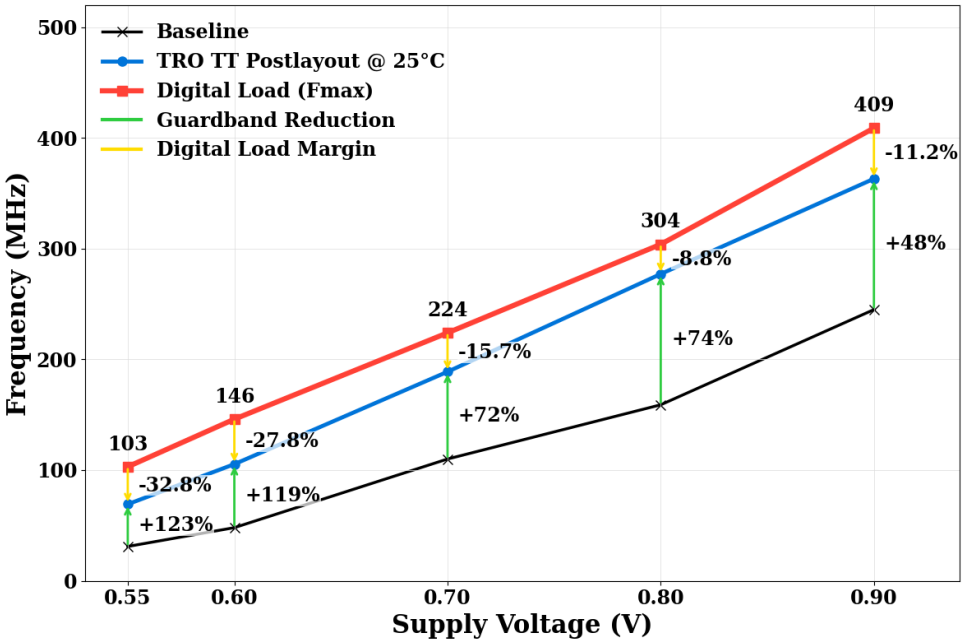
In post-layout, parasitic capacitances increase the propagation delay; therefore, to compensate for this effect, the number of stages in the TRO was reduced. This enables the adjustment of the operating frequency but increases the slope of the frequency–voltage relationship. Compared to pre-layout results, the output frequency improves by up to 6.5% at 0.9 V, while at 0.55 V it degrades by approximately 31.5% in the worst case. This variation results from the adjustment made to ensure tracking of the critical path and is necessary to guarantee that the oscillator frequency does not exceed the

operational limit of the digital load.

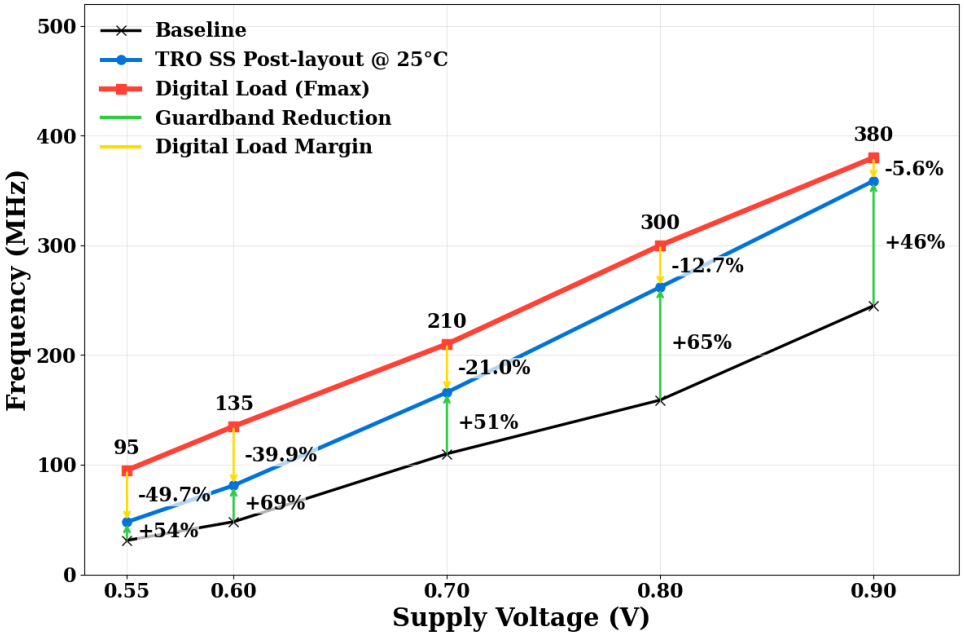
Similar to the pre-layout case, the post-layout results confirm the effectiveness of the calibration strategy in reducing the guardband under different operating conditions, as shown in Figure 5.6. For the TT, a guardband reduction of 74% is achieved, with the TRO operating at 69.2 MHz at 0.55 V and 363.2 MHz at 0.9 V. In the SS corner, a guardband reduction of 65% is obtained, with operating frequencies of 47.78 MHz at 0.55 V and 358.85 MHz at 0.9 V.

Figure 5.6. Post-layout TRO frequency as a function of V_{DD} for (a) typical case and (b) slow-slow process corner.

(a)



(b)

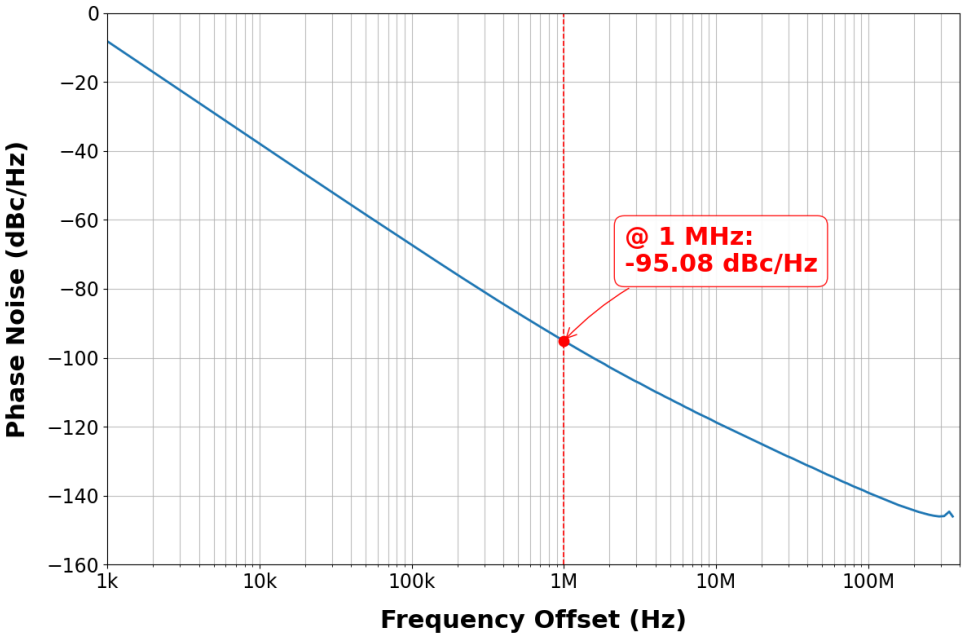


Figures 5.1 and 5.6 illustrate the TRO frequency behavior for the pre-layout and post-layout versions under nominal conditions, with the circuit calibrated in each instance. Across these versions, the TRO curve remains correctly below the digital load and above the baseline, ensuring the necessary operating margin and an effective guard-band reduction. This enables operation at higher frequencies for a given supply voltage.

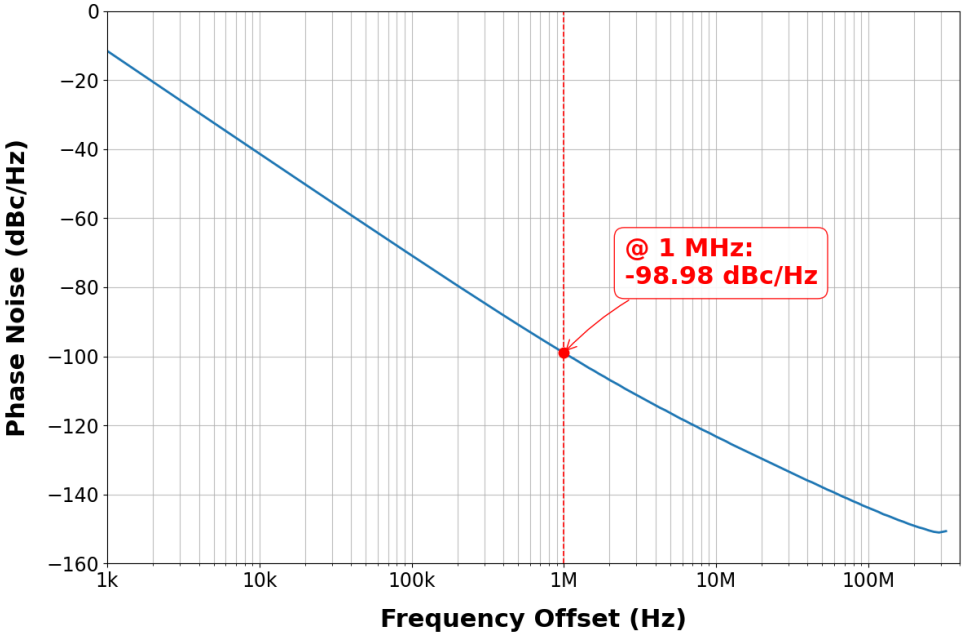
Figure 5.7 presents the simulated phase noise at a 1 MHz offset. The results show a value of -95.08 dBc/Hz for the worst case (a) and -98.98 dBc/Hz for the best case (b). Similar to the pre-layout analysis, these results demonstrate high spectral integrity, as the noise power remains significantly lower than the carrier power.

Figure 5.7. Phase noise post-layout @ 1MHz (a) worst case and (b) best case.

(a)



(b)



The global Monte Carlo simulation results for the post-layout are shown in Figure 5.8.

Figure 5.8. Post-layout Monte Carlo calibration.

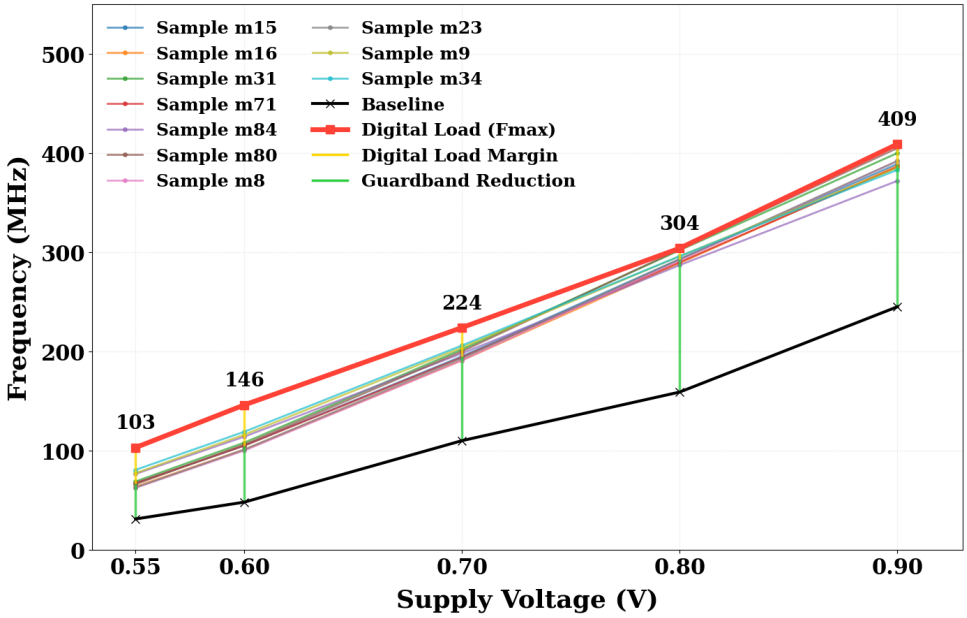


Table 5.6. Comparisons with the state-of-the-art work.

Parameter	**This Work**	**TCAS-I'23**[16]	**VLSI'20**[17]	**JSSC'24**[18]	**TVLSI'26**[19]
Process	28 nm	65 nm	65 nm	28 nm	110 nm
Validation	Post-Layout	Silicon	Silicon	Silicon	Silicon
V_{DD} (V)	0.55–0.9	0.45–0.9	0.6–1.0	0.45–0.9	0.8–1.35
f_{max} (MHz)	103–409	5.98–334.7	∼112–419	N/R	N/R
f_{TRO} (MHz)	69.2–363.2	5.26–283.3	110–415	10–420	8–60
Guardband (%)	8.8–32.8	12–15.4	1–8.9	0.8–2.1	∼10.0

As shown in Table 5.6 the performance of the proposed TRO is compared with the state of the art. While this work reports post-layout simulation results and the reference works are based on silicon measurements, the obtained frequency range (69.2 MHz–363.2 MHz) and operating voltage (0.55 V–0.9 V) remain consistent with prior implementations in 28 nm and 65 nm nodes.

The guardband ranges from 8.8% to 32.8%, which is higher than in some reported works. This is primarily because the TRO frequency is calibrated to remain below the

digital load based only on a limited characterization (TT and SS at 25 ℃). Consequently, the selected nominal condition must account for thermal uncertainties, leading to a conservative margin.

This guardband reflects a trade-off between operational security and efficiency. Although it ensures reliable operation against process and temperature uncertainties, the resulting margin is directly associated with a calibration process based on limited conditions. Consequently, a more detailed characterization of the digital load would reduce uncertainty, allowing for a more precise margin adjustment through a calibration strategy that accounts for these variations.

6. CONCLUSIONS AND FUTURE WORK

6.1. CONCLUSIONS

This work presents the post-layout validation of a telescopic TRO in 28 nm CMOS technology, evaluated under PVT variations and Monte Carlo analysis. The design integrates a calibration capability adaptable to various operating conditions, allowing the oscillator to track the frequency-voltage ($F - V$) curve of the critical path across all evaluated conditions. The results demonstrate that this adjustment reduces the guardband to a range between 52% and 79% compared to a fixed worst-case clock frequency in post-layout. This confirms that the proposed telescopic TRO constitutes a viable solution for tracking the critical path frequency, reducing the conservative safety margins typical of a fixed clock.

6.2. FUTURE WORK

- Obtain the critical path frequency curves of the digital load for all process corners, in order to enable a complete calibration of the TRO across all available operating conditions.
- Incorporate the TRO within the UVFR system to validate its integrated performance, verifying that the TRO operates correctly within the complete system.
- Fabricate the TRO and perform silicon testing to validate its performance and functionality.

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APPENDICES

APPENDIX A. Supplementary material

This appendix provides supplementary information to the Circuit Implementation chapter.

APPENDIX B. Simulation results

This appendix provides supplementary information supporting the Results section.