# DYNAMIC COMPARATOR DESIGN FOR A REGULTED CHARGE PUMP CIRCUIT IN 130nm CMOS TECHNOLOGY

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## RESUMEN

**Título** DISEÑO DE UN COMPARADOR DINÁMICO PARA UNA BOMBA DE CARGA REGULADA EN TECNOLOGÍA CMOS DE 130nm*

**Autor** Harry Kenneth Hurtado Contreras**

**Palabras clave** Bomba de carga, CMOS, Comparador Dinámico, eNVM, Latch, Mismatch, Montecarlo, Offset.

**DESCRIPCIÓN**

En este trabajo se presenta el diseño de un comparador dinámico de doble cola para un control de realimentación de voltaje en una bomba de carga en tecnología CMOS de 130nm. La bomba de carga entrega una tensión de referencia para una memoria no volátil embebida (eNVM). Se consideran el offset referido a la entrada y el tiempo de retardo durante el proceso de diseño, incluyendo simulaciones de Montecarlo y esquinas para la verificación de las características eléctricas del comparador dinámico, los resultados de esta verificación confirman el resultado del análisis, con el fin de alcanzar los requisitos de la bomba de carga. El comparador dinámico diseñado utiliza una fuente de alimentación de 1,2 V, con un tiempo de retardo de 920ps y una frecuencia de operación máxima de 1.087 GHz, un consumo de energía de 142.68 µW a 100 MHz de frecuencia de reloj y un consumo máximo de energía de 772,21 µW a una frecuencia de reloj de 1 GHz con 20fF de carga capacitiva, un offset máximo referido a la entrada de 8mV y un área de *layout* final de 27.12µm × 19.1µm.

Una técnica de compensación de offset digital se implementa como resultado del análisis y comparación de dos alternativas diferentes, mejorando el rendimiento del comparador dinámico para un trabajo posterior; en ambas alternativas el offset inducido se redujo de 40mV a menos de 1mV, mientras que el consumo de energía se elevó un 10% y la máxima frecuencia de operación se redujo un 5% en ambas alternativas.

* Trabajo de grado

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## ABSTRACT

**Title** DYNAMIC COMPARATOR FOR A REGULATED CHARGE PUMP CIRCUIT IN 130NM CMOS TECHNOLOGY*

**Author** Harry Kenneth Hurtado Contreras**

**Keywords** Charge Pump, Device Mismatch, Dynamic Comparator, eNVM, Input Referred Offset, Latch, Montecarlo.

## DESCRIPTION

This paper presents the design of a double tail dynamic comparator for a charge-pump feedback voltage control in 130nm CMOS technology. The charge-pump gives a reference voltage for an embedded non-volatile memory (eNVM). Input referred offset and delay time were considered during the design process, including Montecarlo and corners simulations for verification of the electrical characteristics of the dynamic comparator, the results of this verification confirm the analysis result, in order to achieve the requirements of the charge pump. The dynamic comparator designed uses a power supply of 1.2V, with a delay time of 920ps and maximum operating frequency of 1.087GHz, a power consumption of 142.68 $\mu$W at 100 MHz clock frequency and maximum power consumption of 772.21 $\mu$W at 1 GHz clock frequency with 20fF capacitive load, a maximum input referred offset of 8mV and a final layout area of 27.12$\mu$m *x* 19.1$\mu$m.

A digital offset compensation technique was implemented as a result of the analysis and comparison of two different alternatives in order to improve the performance of the dynamic comparator for a further work; in both alternatives offset induced was reduced from 40mV to less than 1mV while power consumption was elevated 10% and maximum operating frequency was reduced 5% in both alternatives.


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# INTRODUCTION

A non-volatile memory (NVM) is widely used in microelectronics device development because its ability to be implemented for low-power SoC applications. Nowadays, embedded non-volatile memory (eNVM) is implemented on chip. Embedded non-volatile memories (eNVMs) in CMOS technology must be biased with a reference voltage, which is three to ten times higher of the nominal VDD voltage. This reference voltage must be regulated because the process and temperature variations can change the required voltage value to dangerous values for the technology transistors.

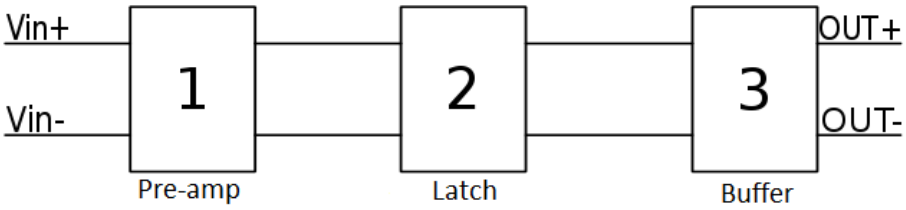
A regulated charge pump is the indicated circuit to generate the bias voltage of embedded non-volatile memories in CMOS technology. A regulated charge pump uses a comparator and a stable voltage reference to generate the feedback control of the output voltage. A bandgap circuit is commonly used to define a reference voltage stable to temperature and process variations. The comparator that composes the feedback voltage control can be implemented with a dynamic topology or a static topology. Static topologies do not need a clock signal to perform the inputs signal comparison, but they have excessive power consumption and low speed. Dynamic architectures require a clock signal and they offer low power consumption and high speed.

In modern CMOS technology the comparator offset can introduce considerable output voltage variations of the charge pump circuit. 25mV of input referred offset of the comparator can trigger 250mV of output voltage increase in a charge pump circuit with 10x of multiplier factor. The comparator offset depends on the temperature, process variation and transistor mismatch which are considerably higher in modern technologies. The offset reduction techniques should be included in the comparator design to avoid this type of effect. This work proposes a dynamic comparator design for a regulated charge pump circuit, which is applied to eNVM in 130nm CMOS technology

# 1. DYNAMIC LATCHED COMPARATOR

A dynamic comparator has a great advantage for the possibility of being implemented in applications with low voltage, besides being fast, allowing it to be used at high frequencies and have low power consumption with zero static dissipation.

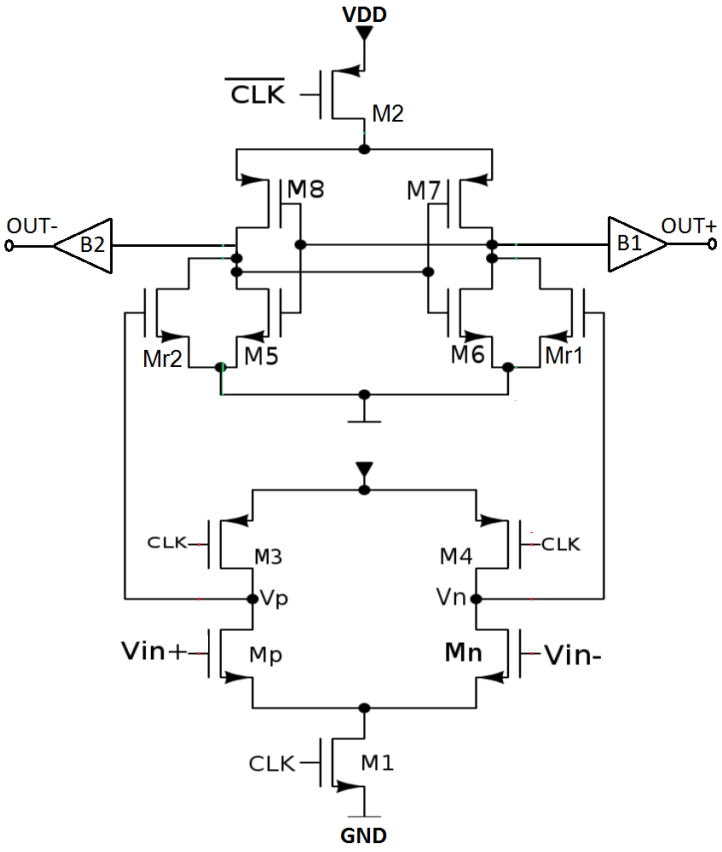
**Figure 1. Block Diagram Comparator**




The dynamic comparator topology is defined by three stages generally arranged in cascade shown in Fig. 1. The first is pre-amplification stage, that is commonly implemented with a differential pair to amplify differences of small magnitude. The second stage is latch stage, current positive feedback is the most used in this block, which defines the signal that is greater and amplifies the difference; the final stage is responsible for conditioning the output signal is regenerative block of the comparator, which takes the decision of the previous block and load the different outputs to the respective high and low levels (VDD and 0) depending on the sign of the difference, that is, has the same behavior of a buffer, (B1 and B2 in figure 2).

The topology shown in Fig. 2 corresponds to a conventional double-tail dynamic comparator. This circuit provides good insulation for kickback noise, generated due to high frequency oscillations which are produced by the circuit in the continuous establishment of high and low. This isolation prevents noise return to inputs. The delay time of this comparator is divided in two parts, one of them is defined by the load time in the capacitance coupled to each output and the other by the time of establishment of the cross-coupled inverters.

**Figure 2. Schematic diagram of the double-tail dynamic comparator.**




## 1.1 DYNAMICS COMPARATOR

In the presence of a clock signal (CLK) circuit operation is conditioned by duality on the clock. This imposes two phases or two states in the device; for LOW values in the clock (CLK = 0) is called reset phase, while for HIGH values (CLK = VDD) we have the comparison phase. For reset phase transistors M1 and M2 both are cut off, making the Vp and Vn nodes are loaded with VDD and output nodes (OUT+ and OUT-) are discharged to ground through transistors Mr1 and Mr2. Once reset phase finish, comparison phase starts, when CLK = VDD transistors M1 and M2 turn on, Vp and Vn nodes start the discharge to different time constant which is proportional to each input voltage. This is, both depend on $I_{M1-M2}/C_{Vp-Vn}$ (where $I_{M1-M2}$ is transistor M1 − M2 drain current, and $C_{Vp-Vn}$ is Vp and Vn node capacitance), thereby defining a differential voltage between Vp and Vn nodes, which depends on voltages applied to the gates of transistors Mn and Mp (comparator input).

For example, assuming that input voltage in Mp transistor is greater than the input voltage in Mn transistor, this indicates that the transistor Mp drain current is greater than the transistor Mn drain current. Therefore, in comparison phase, Vp node is discharged faster than Vn node causing the voltage difference between them, so this differential voltage is applied to the gate of transistors Mr1 and Mr2 which set the shield for kickback noise between output and input; in turn lead to decision and regeneration phase which takes place in the cross-coupled inverters, where the higher voltage is settled and amplified. Considering that voltage in V p node is higher than V n node voltage, output OUT+ is charged to VDD while the output OUT- is discharged to ground (by direct action of the cross-coupled inverters connected to the respective outputs) if the relationship is inverse (Vn voltage greater than Vp voltage), the voltage outputs values will be reversed.

## 1.2 DESIGN OF DOUBLE-TAIL DYNAMIC COMPARATOR

To design the comparator should consider some characteristics depending on the application, such as input common mode range, power consumption, delay time, gain and offset.

Offset could be the characteristic which affects more the design performance. Transistor mismatch is a non-ideality in the fabrication process, it's produces offset. Transistor mismatch is more considerably in modern technologies because the differences between devices are more representatives. In a dynamic comparator topology, the differential pair affected for transistor mismatch produces a higher offset.

Considering transistor mismatch in the circuit design, the differential pair that can be more affected, is found in the pre-amplification stage directly connected to the input. To reduce transistor mismatch in differential pair, the transistors must be as large as possible. This contributes also to increase the gain of this stage achieving the comparator is able to recognize small differences. Nevertheless, increasing size transistors implies a higher power consumption and parallel increase parasitic capacitances, influencing the speed of the circuit making it slower.

Analysis for delay time is based on the analysis obtained by S. Babayan-Mashhadi and R. Lotfi in 2014.

$$t_{delay} = t_0 + t_{latch} \quad \textbf{(1)}$$

Equation (1) shows two parts; the first $t_0$, represents the capacitive charging of the load capacitance ($C_L$) connected at the outputs of comparator, this time depends on $I_{M5-M6}$ (drain current transistor M5 and M6), which can be approximate to the half of the tail

current ($I_{M2}$). The second part is regeneration time ($t_{latch}$), and is the time that outputs takes to charging at VDD or drop to ground.

$$t_0 \approx 2 * \frac{V_{thn} C_L}{I_{M2}} \quad (2)$$

$$t_{latch} = \frac{C_L}{g_{m,eff}} * \ln\left(\frac{VDD/2}{\Delta V_0}\right) \quad (3)$$

In equation (2), $V_{thn}$ responds to threshold voltage in comparison stage when transistor M5 or M6 turns on. In equation (3), $\Delta V_0$ is the voltage difference between OUT+ node and OUT- node in $t = t_0$, during the comparison stage when regeneration begins.

If we wish make the comparator faster, power consumption increases and if we want low offset, transistor should be bigger, but comparator will be slower and power consumption will be greater. In the design of the comparator will take into account the tradeoff between the different features, and set up each one to achieve a better behavior of the comparator for applying at the problem.

**Table 1. Transistor size**

| TRANSISTOR | W ($\mu$m) | L ($\mu$m) | FINGERS |
|---|---|---|---|
| M1 | 2.5 | 0.18 | 2x |
| M2 | 7 | 0.18 | 2x |
| Mp and Mn | 2.5 | 0.18 | 1x |
| M3 and M4 | 7 | 0.18 | 1x |
| Mr1 and Mr2 | 2.5 | 0.18 | 1x |
| M5 and M6 | 2.5 | 0.18 | 1x |
| M7 and M8 | 7 | 0.18 | 1x |

The sizes of transistors after the considerations previously mentioned are listed in Table 1. The size ratio between the NMOS transistors and the PMOS transistors is maintained for the entire circuit, also maintain the same size in all transistors of the same type (either NMOS or PMOS) facilitates the work at the time of the layout while allowing use techniques layout decreasing the abrasive effects of the manufacturing process.

The minimum length of channel permitted by the technology was not used, since executing the simulation of the comparator with the charge pump, the currents handled by the circuit demanded voltages which aren't supported for L = 130nm showing

unsatisfactory results. To achieve better results, increasing this factor to L = 180nm where the simulation threw results expected chords to features designed.

# 2. OFFSET COMPENSATION

In order to decrease the offset in the designed comparator, offset compensation techniques are studied and a comparative study of them is presented. Offset is a feature of the comparators that disproportionately affects the accuracy of the device, many strategies seek to mitigate this problem cancelling the offset or part of it. In order to improve this issue, phenomena that produce it, should be investigated.

Offset can be classified into two classes; the systematic offset and random offset, the first can be attacked with symmetry in the design and special considerations in the layout; the second is caused by device mismatch in the manufacturing process. Mismatch is inversely proportional to the size of the devices, so one way to reduce their effects is implement larger devices, but this solution involves problems in speed and power consumption of the circuit.

Predictive analysis of offset has been performed for dynamic comparators, where expressions shown offset depending on variations in threshold voltage and current of drain of the transistors ΔVth and Δβ, respectively. In equations (4) and (5), offset voltage and variance are shown.

$$V_{OS} = \sum \Delta V_{th_i} + \sum V_{ov_i} \frac{\Delta \beta_i}{\beta_i} \quad (4)$$

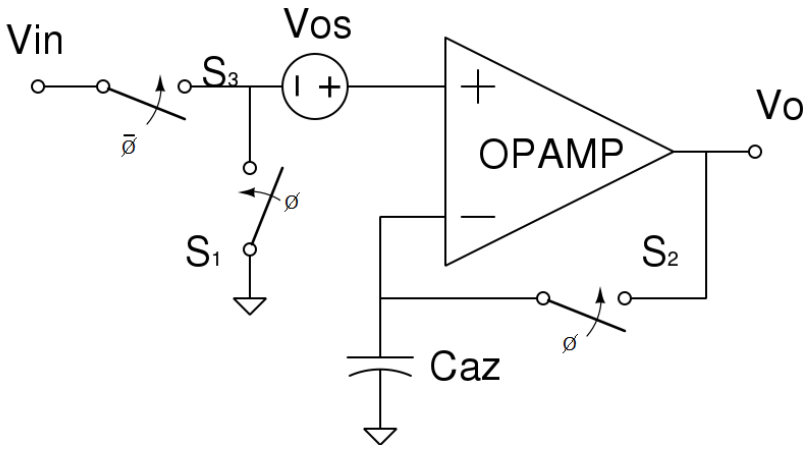
$$\sigma^2_{V_{OS}} = \sum \sigma^2_{V_{th_i}} + \sum V^2_{ov_i} \sigma^2_{\beta_i} \quad (5)$$

Where $i$ responds to Mn, Mp, M3 and M4 transistors in pre amplification stage.

In "*A study on the offset voltage of dynamic comparators*," a predictive analysis for offset was made, part of the analysis was focused on a differential pair, similar to the block in pre-amplification stage of our double-tail dynamic comparator. Prediction in offset value is shown and it will be caused by transistor mismatch in the comparator.
Offset compensation minimizes the offset produced by different techniques, one of them can add offset component with opposite sign to cancel the total offset component, other technique in the case of a differential pair try to balance drain currents of the two branches. Offset compensation can be performed by analog techniques or digital techniques.

- **Analog Techniques:** This compensation is the most used generally, and requires a capacitor for storing the offset, one of the methods used is the auto-zeroing. In the Fig. 3 basic auto-zero technique is shown, Caz is the capacitor which store

**Figure 3. Auto-zero Analog Compensation**

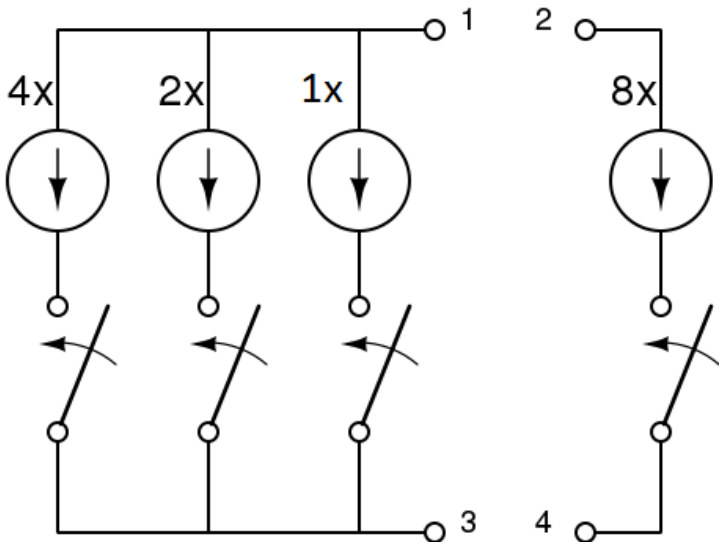



the offset, when ø is a “HIGH”, the amplifier set in a unity gain configuration, Vo is equal to Vos and Caz is charged, when ø is a “LOW”, the input is enabled and the stored offset is subtracted from the initial value and the remaining offset is equal to Vos/A; where Vos is the initial offset and A is the gain of the amplifier. This method has disadvantages as limiting the circuit bandwidth, more power consumption, decrease the comparator speed and by the use of capacitors, layout area of the circuit is increased.

- **Digital Techniques:** This kind of compensation acts on the comparator, compensating the difference at the input produced by the offset. An encoding scheme can tune the offset which is compensated and even if necessary depending on the application to introduce offset in the circuit. This technique does not require capacitors for compensation purposes and have low power consumption and small layout area. Finally, another advantage of digital technique is that speed of comparator is not significantly affected.

  One of the operating principles of offset digital compensation technique is to balance the currents into a differential pair, the presence of offset produces a difference between the currents in each branch of the pair, the technique reduces this difference by adding currents delivered by implementations of current sources connected in parallel to the input transistors how is shown in the Fig. 4. One disadvantage of the technique is the need to measure in advance the offset to encode the circuit with the code suitable, the value is stored in static memory blocks that can be used for this purpose. However, once the offset is measured, these blocks are no longer needed and the circuit is free from any closed loop limitation, which is present all the time in analog technique.

**Figure 4. Principle of operation digital offset compensation.**




According to the above, digital compensation techniques were applied in this paper. Topologies for digital compensation were presented in "*Comparison of digital offset compensation in comparators*", where two of the four topologies studied are chosen according to the characteristics set out in this work and become analyzed in the comparator subject matter of this paper.

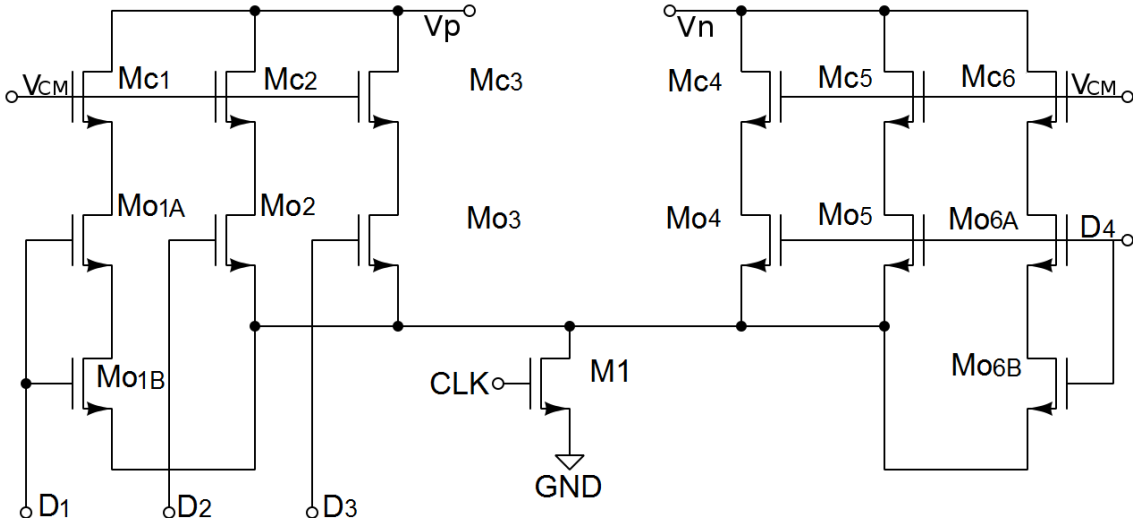
As the offset in the comparator depends on the common mode voltage, linear variation with respect to the common mode voltage is important in the behavior of topology, since this allows that topology has a good effective number of bits and compensation accuracy is not affected.

The nonlinearity in the topologies affects the effective number of bits, which is used to find the worst case overall offset, defined theoretically as the correction range offset divided by the effective number of bits, in simulation this value is found by dividing the largest step level between two. Other features which define a good topology are: sensitivity to variations in VDD, comparator speed and power consumption.

## 2.1 DIGITAL OFFSET COMPENSATION (TOPOLOGY 1).

The figure 5 shows the first topology, this topology has a range of offset compensation defined by $D_{1-3}$, while $D_4$ defines the sign of the settled offset. One of the potential problems of this topology is adding parasitic capacitances in Vp and Vn nodes affecting the speed of the comparator.

**Figure 5. Digital offset compensation Topology 1.**




For topology design, the relationship in each branch of the compensation circuit was considered, as the branch that depends on $D_1$ will be handled as the least significant bit, this consideration sets that transistors in the $D_1$ branch use the smallest or basic value and other branches had a size proportional to first branch. So two scenarios were proposed (1X:2X:3X and 1X: 1,5X: 2X) where numbers are the ratio of width in transistors in the $D_1$, $D_2$ and $D_3$ branches to the minimum transistor width in $D_4$ branch (X). For $D_4$ branch, this must have the same size of the previous branches to maintain symmetry and practice as the sign bit. In the respective simulations, the second ratio has presented better performance, where compensate 40mV maximum offset was one of the design factor (introduced in the simulation) and basic size for transistors branch $D_4$ close to the size of M1.

**Table 2. Topology 1 Transistor size**

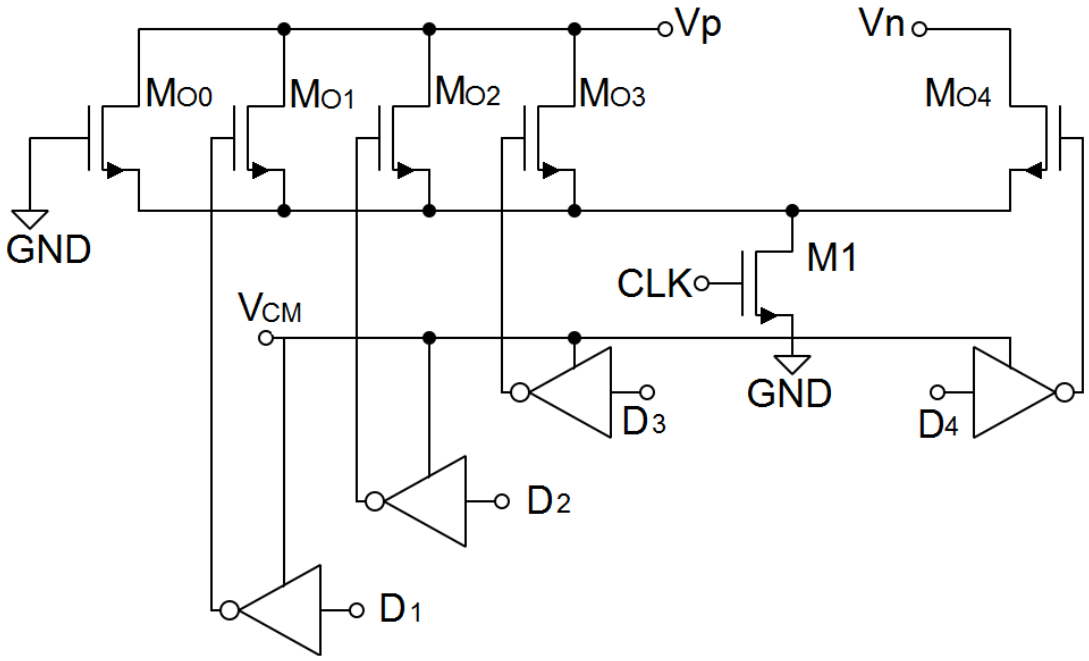
| Transistor | W (μm) | L (μm) |
|---|---|---|
| $M_{C1} - M_{O1A} - M_{O1B}$ | 1.75 | 0.13 |
| $M_{C6} - M_{O6A} - M_{O6B}$ | 1.75 | 0.13 |
| $M_{C2} - M_{O2} - M_{C5} - M_{O5}$ | 2.625 | 0.13 |
| $M_{C3} - M_{O3} - M_{C4} - M_{O4}$ | 3.5 | 0.13 |

## 2.2 DIGITAL OFFSET COMPENSATION (TOPOLOGY 2).

Topology in Fig. 6 is similar to the first topology but this includes inverters which connect the gates of the transistors to Vcm according to the digital code, this implementation

reduce the parasitic capacitance added to the comparator, since this topology has just one transistor per branch. The design of the second topology as

**Figure 6. Digital offset compensation Topology 2.**




suggested by *K. L. J. Wong*, handled the relationship 1x:1x:2x:4x:8x for transistor $M_{O0-4}$ respectively, inverters were taken from the libraries of technology. The base size (X) is handled the same way as the previous topology near the value of M1 with a design consideration in which should compensate 40mV maximum offset.

**Table 3. Topology 2 Transistor size**

| Transistor | W (*µ*m) | L (*µ*m) |
|---|---|---|
| $M_{O0} - M_{O1}$ | 0.98 | 0.13 |
| $M_{O2}$ | 1.96 | 0.13 |
| $M_{O3}$ | 3.92 | 0.13 |
| $M_{O4}$ | 7.84 | 0.13 |

Tables 2 and 3 summarize the topologies design with the above considerations, from them we can infer that there will be less consumption area in topology 2, in addition to affecting less the speed of comparator, since the parasitic capacitance added to Vp and Vn nodes will be lesser than the other topology. Later in the results section other characteristics will be analyzed as compensation range and accuracy between digital levels.

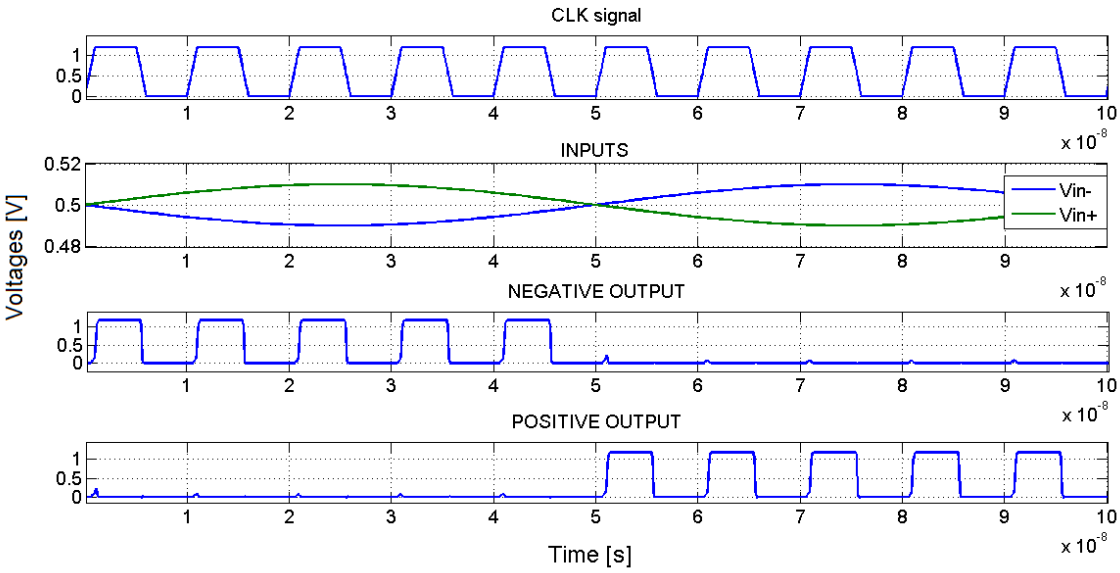
# 3. RESULTS

The results are summarized in two parts: the first showing the characteristics of the double tail dynamic comparator designed, the second part shown the comparative study results of the two topologies of digital offset compensation.

## 3.1 DOUBLE-TAIL DYNAMIC COMPARATOR

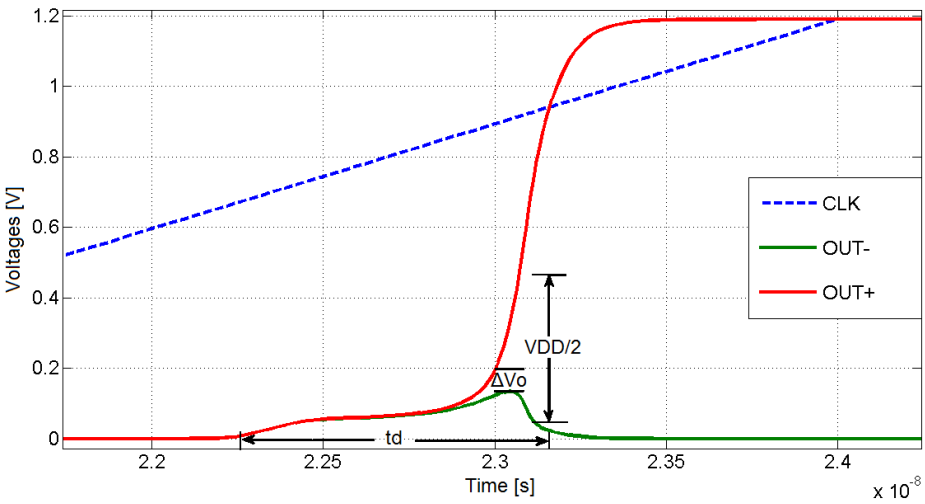
The following characteristics correspond to the double tail dynamic comparator design without offset compensation. In the Fig. 7 is shown the transient analysis of the comparator designed. The two output signals (OUT + and OUT-) are shown with clock signal (CLK) and input signals (Vin+ and Vin-), with the waveform of the voltages in this graph, we can see the desired behavior of the comparator.

**Figure 7. Simulation transient double-tail dynamic comparator @100MHz.**




In Fig. 8 we can obtain delay time, should be noted the two parts of this time; the first call t0, which is charging time in capacitance of output node or load capacitance, second part is settling time, it is regeneration duration and ends when the voltage difference between the two output nodes reaches a value of VDD/2; both can be

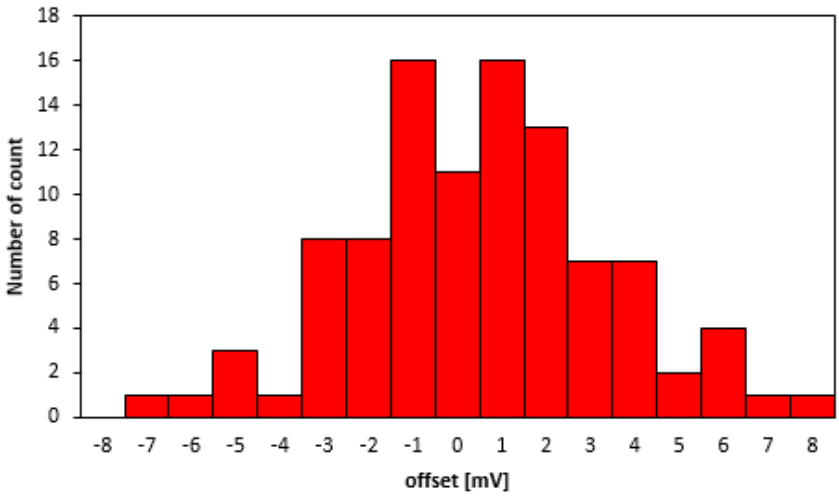
**Figure 8. Analysis delay time double-tail dynamic comparator.**




obtained from the graph. Also both times can be calculated from expressions analyzed previously. Speed of comparator can be obtained from delay time. Corners simulation was made in order to determinate performance and behavior in worst-case supply and temperature sensitive. The circuit pass the test with variations in supply voltage of ±10% and temperature values of −40 °C, 0 °C, 100 °C, besides the nominal values. The results of corners test show variations in output less than 10%.

To obtain the input referred offset, was used a Montecarlo analysis for a run of 100 samples. Fig 9 depicts input referred offset due to variations in all transistors of comparator (transistor mismatch) and an offset standard deviation equal to 2.84mV.

**Figure 9. Histogram diagram of Monte Carlo simulation of the offset in the designed comparator.**



In conclusion the simulations yielded different performance characteristics of the double-tail dynamic comparator designed, these characteristics are shown in table IV.
Fig. 10 shows the respective layout of designed comparator, which looks compact and responds to the design considerations were taken into account, using dummies provides a shield to damages in the manufacturing process for transistors, besides the usage of techniques as common centroid for the location of transistors with connections between them, finally also were used guard rings which offer a kind of isolation between transistors, in this case separates the n-type of p-type giving as a layout result which occupies an area of 27.12µm×19.1µm.

**Figure 10. Layout Double-tail dynamic comparator. Area:27.12µm×19.1µm**

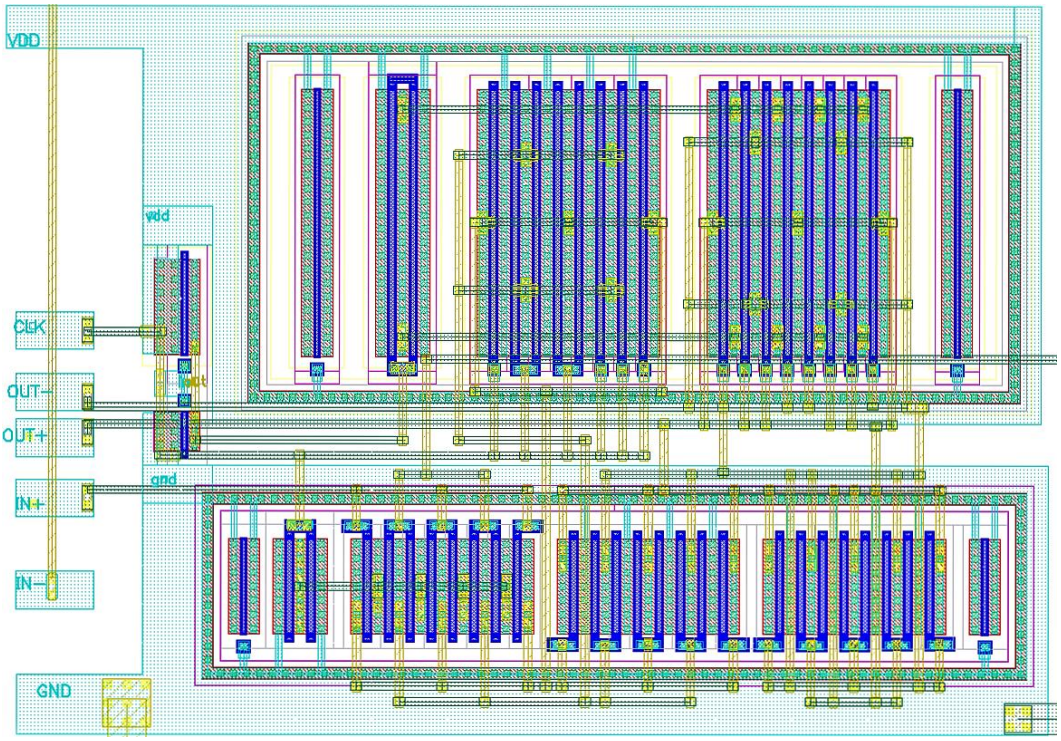


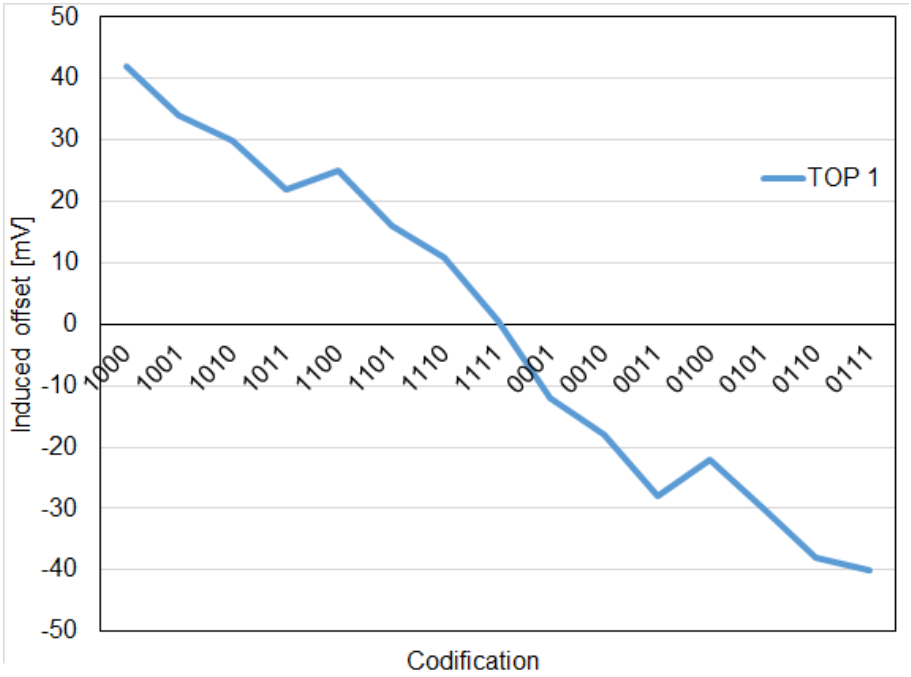

**Table 4. Design characteristics of double -tail dynamic comparator.**

| | |
|---|---|
| **Technology** | CMOS 130nm |
| **Supply voltage** | 1.2V |
| **Power Consumption @ 100MHz** | 139.95$\mu$W |
| **Power Consumption @ 1GHz** | 772.21$\mu$W |
| **Delay time** | 920ps |
| **Maximum operating frequency** | 1.087GHz |
| **Input referred offset (worst-case)** | 8mV |

## 3.2 COMPARATIVE STUDY OF DIGITAL OFFSET COMPENSATION TECHNIQUES.

Analysis of digital compensation was made, offset was induced in the designed comparator, showing the results of the behavior of the two topologies. In Fig. 11 is shown the induced offset that compensates the topology 1, for different digital codes. In Fig. 12 offset compensation of topology 2 is shown. The linearity in topology 2 is better than in topology 1, and topology 2 has better resolution between the digital levels, the offset compensation range is similar in both implementations.

**Figure 11. Linearity of digital offset compensation in topology 1.**




Comparator implemented with the topology 1 had a power consumption of 150.2µW while with the topology 2 the power consumption was 149.03µW. The delay time of comparator implemented whit the different topologies of digital offset compensation was not very deflected; the initial delay time was affected less than 5%.

Fig. 13 shows the microphotograph of the chip where the double-tail dynamic comparator was implemented.

**Figure 12. Linearity of digital offset compensation in topology 2.**

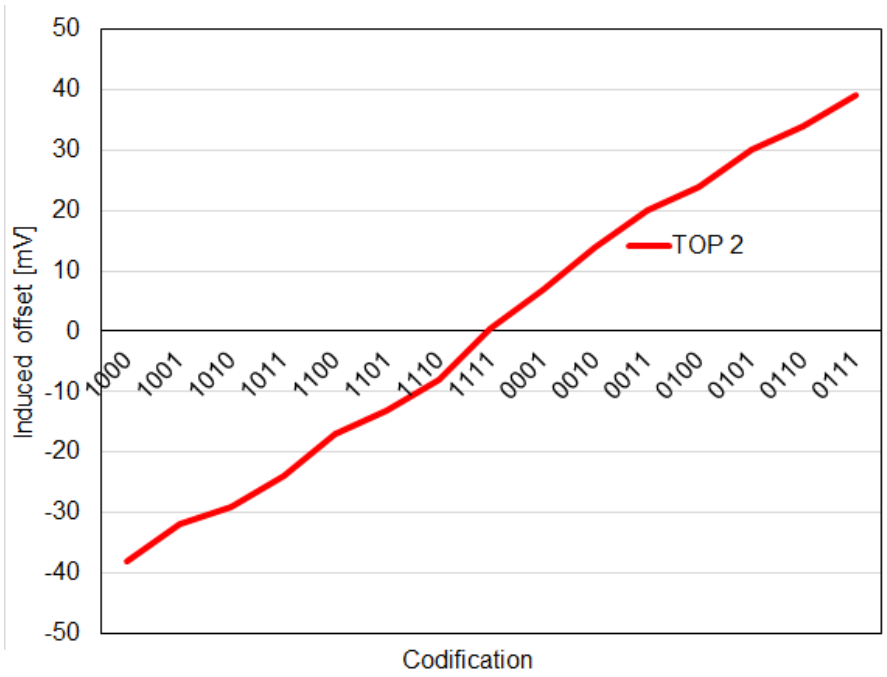
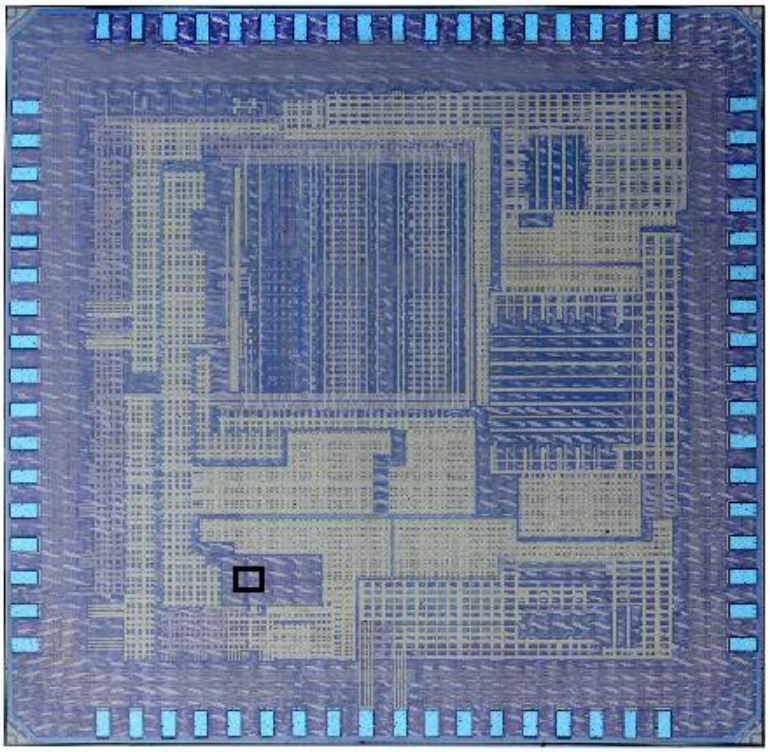



**Figure 13. Microphotograph of the chip.**



# 4. CONCLUSION

In this paper a dynamic comparator design was presented, which is simulated in 130 nm CMOS technology where delay time and input referred offset were features considered, the last using Montecarlo analysis. Layout of the circuit was carefully made in order to avoid systematic offset. Two topologies of digital offset compensation were compared, linearity for each topology and offset compensated are obtained from simulation. Offset compensation reduced the induced offset from 40mV to 0.5mV while the speed and power consumption of comparator were affected less than 10%.

## REFERENCES


A. C. Pinto and J. R. Fernandes, “A study on the offset voltage of dynamic comparators,” Proceedings of Design of Integrated Circuits and Systems Conference (DCIS) 28th Ed., vol. 28, no. 2, Nov 2013.

A. Lahariya and A. Gupta, “Design of low power and high speed dynamic latch comparator using 180 nm technology,” in Signal Processing, Computing and Control (ISPCC), 2015 International Conference on, Sept 2015, pp. 129–134.

B.-D. Yang, “250-mv supply subthreshold CMOS voltage reference using a low-voltage comparator and a charge-pump circuit,” IEEE Transactions on Circuits and Systems II: Express Briefs, pp. 850 – 854.

B. Razavi, Design of Analog CMOS Integrated Circuits. McGraw-Hill, 2000.

C. J. Solis and G. O. Ducoudray, “High resolution low power 0.6 um CMOS 40mhz dynamic latch comparator,” in 2010 53rd IEEE International Midwest Symposium on Circuits and Systems, Aug 2010, pp. 1045–1048.

D. Dzahini and H. Ghazlane, “Auto-zero stabilized CMOS amplifiers for very low voltage or current offset,” in Nuclear Science Symposium Conference Record, 2003 IEEE, vol. 1, Oct 2003, pp. 6–10 Vol.1.

D. Schinkel, E. Mensink, E. Klumperink, E. van Tuijl, and B. Nauta, “A double-tail latch-type voltage sense amplifier with 18ps setup+hold time,” in 2007 IEEE International Solid-State Circuits Conference. Digest of Technical Papers, Feb 2007, pp. 314–605.

J. Lu and J. Holleman, “A low-power dynamic comparator with time domain bulk-driven offset cancellation,” in 2012 IEEE International Symposium on Circuits and Systems, May 2012, pp. 2493–2496.

K. L. J. Wong, “Comparison of digital offset compensation in comparators,” Master’s thesis, University of California, Los Angeles, 2002.

K. L. J. Wong and C. K. K. Yang, “Offset compensation in comparators with minimum input-referred supply noise,” IEEE Journal of Solid-State Circuits, vol. 39, no. 5, pp. 837–840, May 2004.

L. C. Anna Richelli, Luca Mensi and Z. Kova, “A 1.2v-5v high efficiency CMOS charge pump for non-volatile memories,” Circuits and Systems, 2007. ISCAS 2007. IEEE International Symposium on, pp. 2411 – 2414.

L. M. Dhal and A. Pradhan, “Study and analysis of different types of comparators,” national Institute of Technology, Rourkela 2012-2013.

M.-F. hang and P.-C. Chen, “Embedded non-volatile memory circuit design technologies for mobile low-voltage SoC and 3d-ic,” Solid State and Integrated Circuit Technology (ICSICT), 2010 10th IEEE International Conference on, pp. 13 – 16.

P. Chandrahash, “Study of comparator and their architectures,” international Journal of Multidisciplinary Consortium June 2014.

R. J. Baker, CMOS Circuit Design, Layout and Simulation, 3rd ed. Wiley - IEEE Press, 2010.

S. Babayan-Mashhadi and R. Lotfi, “Analysis and design of a low-voltage low-power double-tail comparator,” IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 22, no. 2, pp. 343–352, Feb 2014.