DESIGN METHODOLOGY FOR A VOLTAGE-CONTROLLED OSCILLATOR (VCO) IN A 28 NM CMOS NODE

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Degree work presented as a requirement to qualify for the title of Electronic Engineer

Advisors:
JAVIER FERNEY ARDILA OCHOA
PhD in Microelectronics

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Dedicated to my family and friends.

And to my brother Laude Fernández who introduced me to this amazing journey.

ACKNOWLEDGMENTS

I would like to begin by acknowledging the lifelong dedication and support of my parents, from the moment I was born until now, which has allowed me to achieve this milestone in my life. I owe who I am today to them, as well as to the rest of my family, who have always encouraged me to pursue my dreams.

I am also deeply grateful to all the colleagues who were part of my training over these five years, especially Victor Muñoz, Brayan Martinez, Sebastian Hernandez, and Over Amaya, with whom I maintained a strongly enriching friendship since we began studying microelectronics. I would also like to extend my thanks to Jorge Angarita for the interesting and thought-provoking conversations on circuits, and to Professor Juan Moya for his teachings and his helpfulness.

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[1] Behzad RAZAVI. *Design of Analog CMOS Integrated Circuits*. 2nd. McGraw-Hill Education, 2017.

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[3] Behzad RAZAVI. *RF Microelectronics*. 2nd. Prentice Hall, 2011.

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RESUMEN

TÍTULO: METODOLOGIA DE DISEÑO PARA UN (VCO) EN UN NODO CMOS DE 28 NM [*]

AUTOR: DANIEL JOSÉ FERNÁNDEZ MARTÍNEZ
[**]

PALABRAS CLAVE: VCO, Metodologia de diseño, Ruido de fase, Consumo de potencia, Sintonizacion discreta.

DESCRIPCIÓN:

El grupo de investigación Onchip está motivado para explorar sistemas de enlaces de alta velocidad. Estos sistemas requieren la implementación circuital de transmisores y receptores, los cuales utilizan circuitos como el Phase-Locked Loop (PLL) o el Clock and Data Recovery (CDR) para serializar y deserializar los datos, ya que estos se encargan de generar y recuperar la señal de reloj mediante un Voltage-Controlled Oscillator (VCO).

Este proyecto plantea una metodología de diseño para un VCO en 28 nm, la cual se pone a prueba con el diseño de un ejemplar para una aplicación de comunicaciones ópticas dentro de un CDR. Esta metodología se compone principalmente de un diagrama de flujo cuyo objetivo es ajustar de manera óptima el punto de operación del VCO para, de esta forma, conseguir un buen desempeño en todas y cada una de las especificaciones. Luego del proceso de diseño, se realiza una comparación con otros diseños publicados en el estado del arte.

Esta metodología simplifica el trabajo del diseñador y también podría ser automatizada mediante un algoritmo. Al ingresar las especificaciones del diseño, el algoritmo realizaría el proceso y generaría un diseño final de forma automática.

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[*] Trabajo de Grado

[**] Facultad de Ingenierías Físico-Mecánicas. Escuela de Ingenierías Eléctrica, Electrónica y de Telecomunicaciones. Director: JAVIER FERNEY ARDILA OCHOA

ABSTRACT

TITLE: DESIGN METHODOLOGY FOR A VOLTAGE-CONTROLLED OSCILLATOR (VCO) IN A 28 NM CMOS NODE [*]

AUTHOR: DANIEL JOSÉ FERNÁNDEZ MARTÍNEZ [**]

KEYWORDS: VCO, Design Methodology, Phase Noise, Power Consumption, Discrete Tuning.

DESCRIPTION: The Onchip research group is motivated to explore high-speed link systems. These systems require the circuit implementation of transmitters and receivers, which utilize circuits such as the Phase-Locked Loop (PLL) or the Clock and Data Recovery (CDR) to serialize and deserialize data, as they are responsible for generating and recovering the clock signal through a Voltage-Controlled Oscillator (VCO).

This project proposes a design methodology for a VCO in 28 nm, which is tested with the design of a prototype for an optical communications application within a CDR. This methodology mainly consists of a flowchart that aims to optimally adjust the operating point of the VCO to achieve good performance in every specification. After the design process, a comparison is made with other designs published in the state of the art.

This methodology simplifies the designer's work and could also be automated by an algorithm. By entering the design specifications, the algorithm would perform the process and generate a final design automatically.

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[*] BSc Thesis

[**] Facultad de Ingenierías Físico-Mecánicas. Escuela de Ingenierías Eléctrica, Electrónica y de Telecomunicaciones. Advisor: JAVIER FERNEY ARDILA OCHOA

INTRODUCTION

In our daily lives, we frequently utilize serial communication in interfaces such as HDMI and SATA, among others. To facilitate this communication, high-speed links are required to transmit and receive data streams [1] with the utmost precision and bit rate possible. It's noteworthy that when receiving data, deserialization is necessary. This task is performed using a demultiplexer controlled by a clock signal generated by a VCO, which is integrated into a PLL to achieve phase and frequency lock.

With the aforementioned, we can recognize the need for VCO design but at the same time, we must consider its limitations and restrictions in the design process. It is important to take into account concepts such as phase noise and jitter, which arise from process variations and overall loop misalignments.

This paper proposes a novel design methodology to optimize the oscillator cross-coupled pair with Nmos transistors at the 28 nm technology node, which is one of the most fundamental topologies in oscillator design [2]. This approach is based on an exhaustive study of existing oscillator designs and summarized in a design flowchart that seeks to optimize the operating point of the VCO to achieve good performance in each of the specifications.

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[1] B. CASPER and F. O'MAHONY. "Clocking Analysis, Implementation and Measurement Techniques for High-Speed Data Links—A Tutorial]". In: *IEEE Transactions on Circuits and Systems I* 56.1 (2009), pp. 17–39.

[2] C.LIM and H. RAMIAH. "A high-Q spiral inductor with dual-layer patterned floating shield in a class-B VCO achieving a 190.5-dBc/Hz FoM". in: *IEEE International Symposium on Circuits and Systems (ISCAS)* (2016), pp. 2759–2762.

After having defined the design specifications and having completed the series of steps of the design methodology, we continue with a validation of the circuit under process voltage and temperature variations (PVT) and Monte Carlo simulations to validate the operation. Finally, a comparison is made with the designs found in the state of the art using a figure of merit (FoM) which gathers the most important characteristics of a VCO.

This design methodology can be optimized through an algorithm to facilitate the design of VCOs and reduce the time spent by a designer when considering this task.

OBJECTIVES

0.1. General Objectives

- To describe a design methodology for a VCO in the 28nm technological node standard CMOS process.

0.2. Specific Objectives

- To study and define the circuit specifications for the selected VCO topology based on the system requirements for a high-speed link receiver in a standard TSMC 28nm CMOS process design kit.
- To design a VCO using a 28nm CMOS standard process.
- To validate the performance of the VCO using different types of simulations such as Monte Carlo and process, voltage, and temperature (PVT) variation corners.

1. VCO FUNDAMENTALS

A VCO is a type of oscillator whose oscillation frequency can be adjusted through a control voltage, which redefines the oscillator's phase by directly or indirectly varying certain circuit parameters. VCOs are typically based on either LC or ring oscillators. In the case of ring oscillators, the control voltage directly modifies the circuit's supply voltage, whereas in LC oscillators, the control voltage indirectly alters the resonator's capacitance via a varactor[3].

1.1. Oscillation Start-Up.

There are two points of view from which the oscillators can be analyzed to obtain an expression of their start-up condition and their oscillation frequency, one of them is the one-port view (see Figure (**1.1**)), from which the negative resistance seen from the resonator to the transconductor is calculated and finding an inequality that allows having a negative equivalent resistance (including the inductor losses) in parallel to the resonator[3].

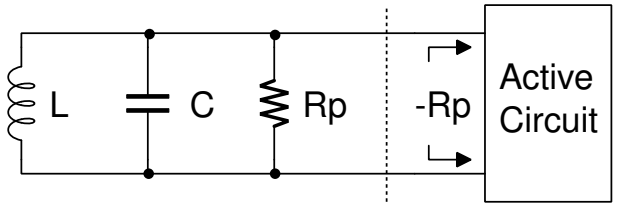

Figure 1.1. One-Port View.

L is the value of the inductance of the resonator, C is the capacitance in parallel to the resonator and R_p represents the total losses of the resonator. The second method

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[3] Behzad RAZAVI. *RF Microelectronics*. 2nd. Prentice Hall, 2011.

from which the oscillators can be analyzed is from the feedback point of view (see figure (**1.2**)). To perform the analysis from this point of view, the small-signal loop gain of the oscillator is required.

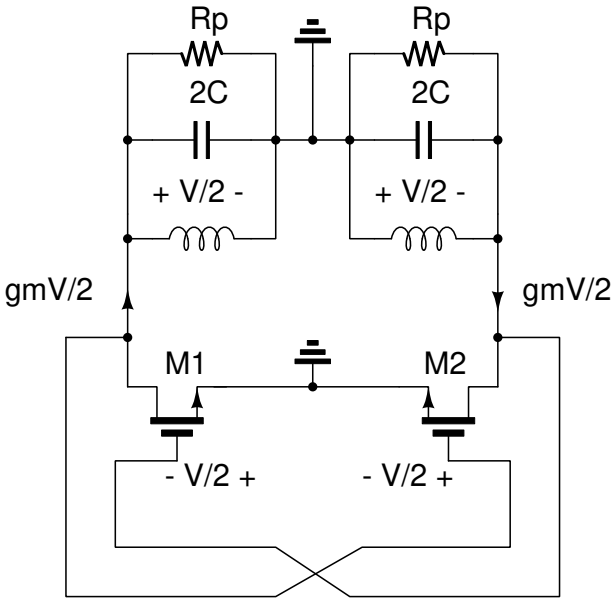

Figure 1.2. Feedback Model of the cross-coupled pair oscillator.

gm is the small signal transconductance of the transistor and V represents the total voltage swing (V_{Swing}) of the differential output. To find the small signal loop gain, you can break the loop at one of the transistor pair gates and then find its respective magnitude response and meet the following condition [4]:

$$|H(\omega_c)| > 1 \tag{1}$$

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[4] Behzad RAZAVI. *Fundamentals of microelectronics*. 2nd. WILEY, 2014.

1.2. Mathematical Model

he mathematical model of the VCO can be defined by the linear relationship between the output frequency and the input voltage. Figure (**1.3**) illustrates how the output frequency changes as the control voltage increases from an initial value V_1 to V_2. Correspondingly, the output frequency varies from ω_1 to ω_2. This relationship is described by the following equation[3]:

$$\omega_{out} = \omega_0 + K_{VCO} * V_{cont}. \tag{2}$$

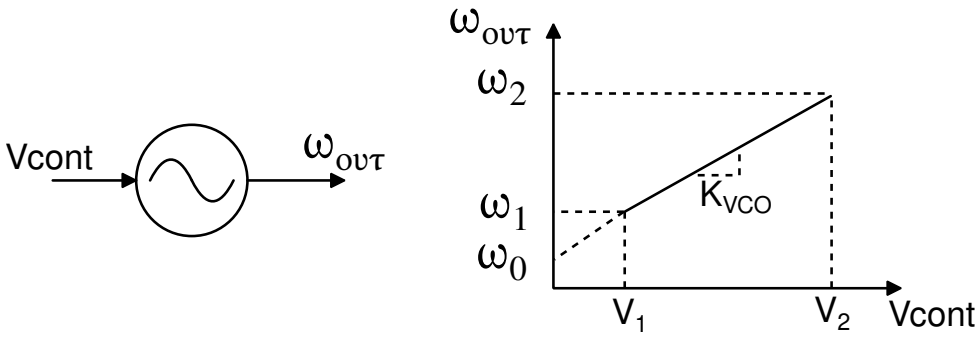

Figure 1.3. VCO Characteristics.

Consider the output signal as a sine wave, $V_{out} = V_0 \sin(\omega t)$. The phase ωt increases linearly in time with a slope ωt; therefore, the instantaneous frequency is defined as the derivative of the instantaneous phase as follows:

$$\omega(t) = \frac{d\phi}{dt}, \tag{3}$$

solving for the instantaneous phase, we have:

$$\phi(t) = \int \omega(t)\, dt + \phi_0, \tag{4}$$

the initial phase is neglected, and therefore the output signal can be expressed as

follows:

$$V_{out} = V_0 \sin\left(\int \omega_{out}(t)\, dt\right), \tag{5}$$

$$V_{out} = V_0 \sin\left(\omega_0 t + K_{VCO} \int V_{cont}\, dt\right). \tag{6}$$

In equation (**6**), it can be seen that the output signal of a VCO is a frequency modulation with a sensitivity coefficient equivalent to the VCO gain (K_{VCO}), and a message signal, which in this case is the control voltage (V_{cont}). Thus it can be concluded that the VCO is a frequency modulator.

1.3. Phase Noise theory

To get an overview of phase noise in electrical oscillators, the reader should review the time-variant analysis made by Ali Hajimiri and Thomas Lee [5]. The phase noise of an oscillator depends on the impulse sensitivity function (ISF), which describes how much noise from the circuit is converted into phase noise in the close-in frequency of the oscillator, as shown in the following equation:

$$L[\Delta\omega] = 10 \log\left(\frac{ISF_{rms}^2 i_n^2}{2q_{max}^2 \Delta\omega^2}\right) [dBc/Hz], \tag{7}$$

The phase noise $L[\Delta\omega]$ in harmonic oscillators at an offset frequency $\Delta\omega$ from the carrier can be expressed as [6]:

$$L[\Delta\omega] = 10 \log\left(\frac{\sum_{i=1}^{n} N_i}{2q_{max}^2 \Delta\omega^2}\right) [dBc/Hz], \tag{8}$$

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[5] Hajimiri A and Lee T. “A general theory of phase noise in electrical oscillators”. In: *JOURNAL OF SOLID-STATE CIRCUITS* 33.2 (1998), pp. 174–194.

[6] Mazzanti A and Andreani P. “Class-c harmonic cmos vcos, with a general result on phase noise”. In: *JOURNAL OF SOLID-STATE CIRCUITS* 43.12 (2008), pp. 2716–2729.

where N_i is the effective noise generated by the losses in each tank and by each MOS transistor. The expressions for those noise sources are defined as:

$$N_R = \frac{K_B T}{2R_p}\left[\frac{A^2}{Hz}\right], \qquad N_M = \frac{K_B T}{2R_p}\gamma F\left[\frac{A^2}{Hz}\right], \tag{9}$$

where N_R represents the effective noise generated by the resonator losses and N_M represents the effective noise generated by the transconductor transistors. K_B is the Boltzmann constant, R_p represents the inductor losses, T is the temperature, γ is the MOS channel noise factor, and F is a noise factor that depends on the ratios between the transconductor and resonator voltages and vice versa. Consequently, the amount of effective noise delivered to the resonator strongly depends on the resonator quality factor and the oscillator's topology.

The upcoming chapters will outline the progression of the project. Chapter two will present the chosen topology, reviewing its operational principles and the necessary devices for the implementation. Chapter three will provide a design methodology for the chosen topology, clarifying all design considerations and trade-offs. Chapter four will consolidate all achieved results and compare them with other VCOs presented in the literature. Lastly, chapter five will present conclusions and future work.

1.4. Chapter Summary

- A brief explanation of Voltage-Controlled Oscillators (VCOs) was presented.
- The foundations of VCOs, including the start-up condition and the different perspectives from which it can be analyzed were reviewed.
- A mathematical model representing the functionality of the VCO was introduced.
- A brief introduction of phase noise theory in electrical oscillators was provided.

2. VCO TOPOLOGY AND MODELING

2.1. Topology

The selected topology for this project is the cross-coupled pair oscillator with NMOS transistors (see figure (**2.1**)). Although there are various VCO topologies, each with its advantages and drawbacks, a detailed discussion of which is superior would go beyond the scope of this research. However, selecting the topology is a key step in this work. After a thorough review of the state of the art, the cross-coupled pair topology was chosen due to its simplicity. The active part (transconductor) consists of only two transistors that compensate for the resonator losses, which is simply an inductor in parallel with a variable capacitance. Other setups require the use of transformers. Furthermore, a current source based on a basic current mirror is used, which is widely applied in oscillators for its ability to remain in saturation with a reduced voltage margin. This topology also has the peculiarity that it allows achieving large output amplitudes since it does not present so many nonlinearities because the output nodes do not have upper limits because the inductors allow any voltage between their terminals, which does not occur in the complementary topologies [7] in which have PMOS transistors connected between each output node and V_{dd}.

Other topologies may offer advantages, such as better phase noise performance by reshaping the signals, but they typically require more extensive modeling efforts, as parasitic capacitances affect the shape of the channel current, or they necessitate the use of transformers to reshape the voltage signal at the oscillator outputs. Therefore, it is concluded that the chosen topology offers the best balance of simplicity and func-

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[7] Mazzanti A and Andreani P. “A Push–Pull Class-C CMOS VCO”. in: *JOURNAL OF SOLID-STATE CIRCUITS* 48.3 (2013), pp. 724–732.

tionality for developing a design methodology.

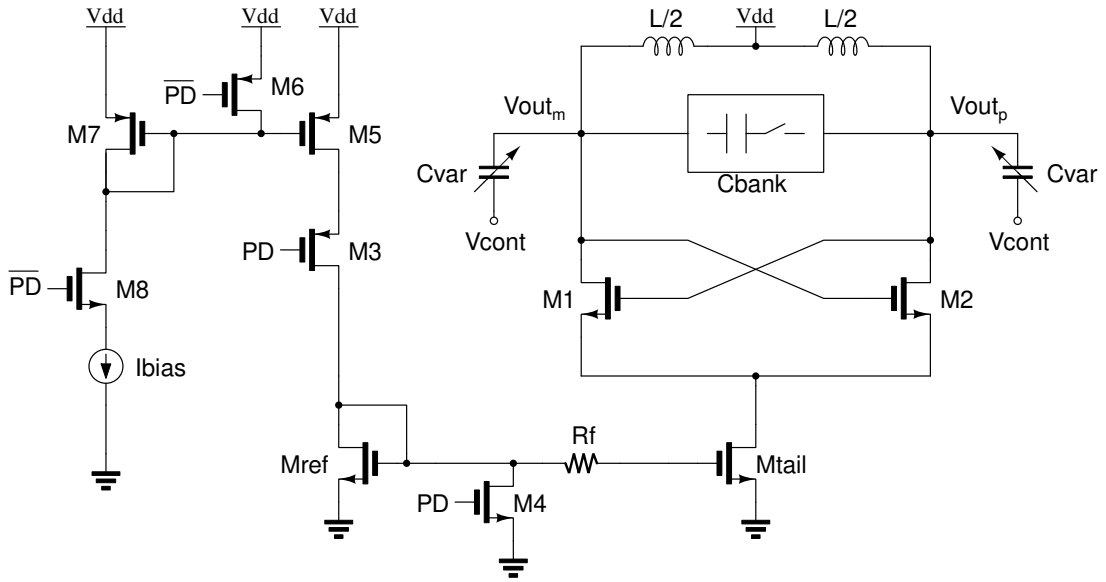

Figure 2.1. Cross-Coupled Pair Topology.

2.2. Design Equations

The oscillation frequency of the chosen topology is presented below.

$$F_C = \frac{1}{2\pi\sqrt{L\left(C + C_{var}\right)}}, \tag{10}$$

where C_{var} represents the capacitance of the varactors. The resonator's quality factor can be expressed as the parallel combination of the quality factors of the inductor and the capacitance. However, at radio frequencies, capacitors typically exhibit much higher quality factors than inductors [3]. Consequently, the inductor's quality factor becomes the dominant factor in the resonator. The quality factor is calculated using the fundamental definition, which relates the imaginary and real parts of the impedance.

$$Q = \frac{L\omega}{R_s}. \tag{11}$$

At frequencies close to the resonance frequency, the following approximation can be used to change the inductor model with a series resistance to an inductor model with a parallel resistance as shown in figure (**2.2**).

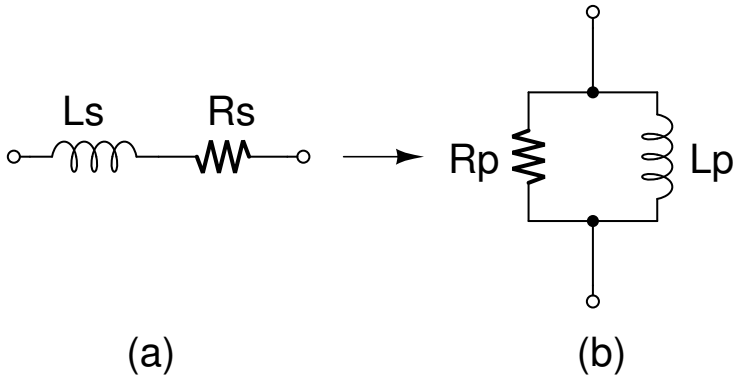

Figure 2.2. (a) Series Model, (b) Parallel Model.

The resistance in the parallel model can be written as follows:

$$R_p \approx Q^2 R_s, \tag{12}$$

the inductance in the parallel model approaches the same value as the inductance in the series model.

$$L_p \approx L_s, \tag{13}$$

the quality factor now is defined as:

$$Q = \frac{R_p}{L_p \omega}. \tag{14}$$

2.2.1. Start-Up Condition To obtain the start-up condition of the chosen topology it can be chosen any of the two points of view mentioned in the previous chapter, for more clarity we will use the feedback point of view, the small signal loop gain of the

chosen topology is made up of two common sources in cascade which have a resonator in their loads, the result is presented below:

$$H(j\omega) = \left(\frac{gm}{\frac{1}{R_p} + 2Cj\omega - \frac{2}{Lj\omega}} \right)^2, \tag{15}$$

from the equation (**1**), the start-up condition can be extracted for which the magnitude of the loop gain must be greater than 1 at the resonance frequency.

$$|H(j\omega)| = \left(\frac{gm}{\sqrt{(\frac{1}{R_p})^2 + (2Cj\omega - \frac{2}{Lj\omega})^2}} \right)^2, \tag{16}$$

with the magnitude of the loop gain function, the next step is to evaluate it at the resonance frequency and use the inequality that implies the start-up condition.

$$gmR_p > 1. \tag{17}$$

2.2.2. Phase Noise The equations (**8**) and (**9**) can be used to analyze the phase noise of the chosen topology. The noise factor is equal to 1 because the resonator output is directly connected to the transconductor output and the transconductor input is directly connected to the transconductor output, therefore we arrive at the following expression for the oscillator phase noise:

$$L[\Delta\omega] = 10\log\left(\frac{2N_R + 2N_M}{2q_{max}^2 \Delta\omega^2} \right)[dBc/Hz], \tag{18}$$

$$L[\Delta\omega] = 10\log\left(\frac{K_B T(1+\gamma)}{2R_p q_{max}^2 \Delta\omega^2} \right)[dBc/Hz]. \tag{19}$$

Keeping the M_{tail} transistor in saturation is important to degenerate the pair transistors

and thus reduce the amount of noise they deliver to the resonator [8]. The above analysis assumes that all the transistors are in saturation and only allows us to estimate the amount of phase noise contributed by the pair transistors and the resonator itself, the phase noise generated by the current source can be estimated using equation (**7**) for which we require the ISF of the common node between the transistors of the pair to determine how much is the conversion from noise at that node to phase noise at the output, the precise calculation of that function can be a very complicated process and it is not within the scope of this project to determine the exact phase noise of the topology, for this reason, we take the following conclusions as design strategies to improve the phase noise of the VCO:

- Designing an inductor with a high-quality factor to increase R_p
- Keep the M_{tail} transistor in saturation.
- Generate as little noise as possible in the circuit (reduce transconductances and add filtering techniques).

2.2.3. Voltage Swing To obtain the voltage change of this oscillator topology at the output it is necessary to recognize that the resonator works as a filter at the resonant frequency, at that frequency each resonator behaves as a resistance of value R_p which is multiplied by the value of the fundamental component of the current (I_1) to obtain the voltage at each output node (V_0).

$$V_0 = I_1 R_p, \tag{20}$$

To determine the fundamental harmonic value of the current, it is crucial to analyze the current waveform over time. It should be noted that the oscillator currents are differential and depend on the output signal, as illustrated in Figure (**2.3**).

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[8] Ayoub Ait IHDA. “Low power, high-reliability class-C voltage-controlled oscillator for space application in 28 nm FD-SOI technology”. PhD thesis. Bordeaux, France: Université de Bordeaux, 2022.

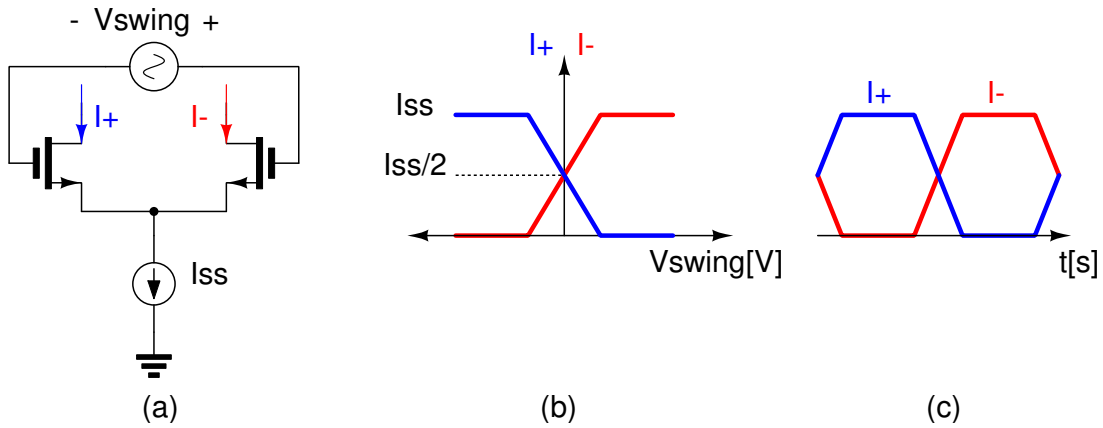

Figure 2.3. (a) Differential Pair, (b) Currents vs Voltage Swing, (c) Currents vs Time[9].

With the above, it can be concluded that the waveform of the currents in time approximates a square signal as long as the output oscillation is large, using the Fourier series expansion of a square signal the following expressions are obtained [10]:

$$I_+ \approx \frac{I_{SS}}{2} + \sum_{n=1,3,5...}^{\infty} \frac{2}{n\pi} I_{SS} \cos(n\omega_c t), \tag{21}$$

$$I_- \approx \frac{I_{SS}}{2} - \sum_{n=1,3,5...}^{\infty} \frac{2}{n\pi} I_{SS} \cos(n\omega_c t), \tag{22}$$

With $n = 1$, the value of the fundamental component of the current can be obtained.

$$I_{+1} \approx +\frac{2}{\pi} I_{SS}, \tag{23}$$

$$I_{-1} \approx -\frac{2}{\pi} I_{SS}, \tag{24}$$

to obtain the voltage swing at the output of the VCO the amplitude of each node of the differential output is required and then multiply it by 2 or perform the respective differential operation between the two voltages as follows:

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[10] Alan V. OPPENHEIM, Alan S. WILLSKY, and S. Hamid NAWAB. *Signals and Systems*. 2nd. Prentice Hall, 1997.

$$V_{Swing} = V_0 - (-V_0) = \frac{4}{\pi} I_{SS} R_p, \tag{25}$$

this linear relationship between V_{swing} and I_{SS} is only valid in the current limited region [11], but the output signal cannot grow infinitely due to the nonlinearities that the circuit presents as the current source which requires a minimum voltage (V_{dsat}) to deliver the necessary current, this effect can be seen reflected in figure (**2.4**) where it can be seen the variation of the output signal with respect to the current I_{SS}.

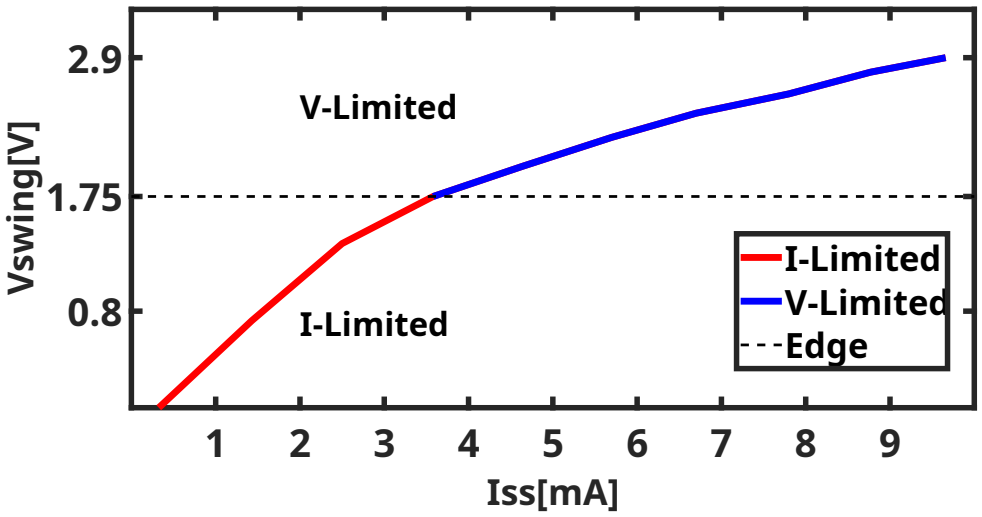

Figure 2.4. I-V Limited Regions.

2.3. Inductor Modeling

To perform the VCO simulations it's needed to generate a circuit model of the inductor that can represent the results obtained in the design tool, in figure (**2.5**) you can see

[11] Hajimiri A and Ham D. "Concepts and Methods in Optimization of Integrated LC VCOs". In: *JOURNAL OF SOLID-STATE CIRCUITS* 36.6 (2001), pp. 896–909.

the circuit model of a differential inductor [12].

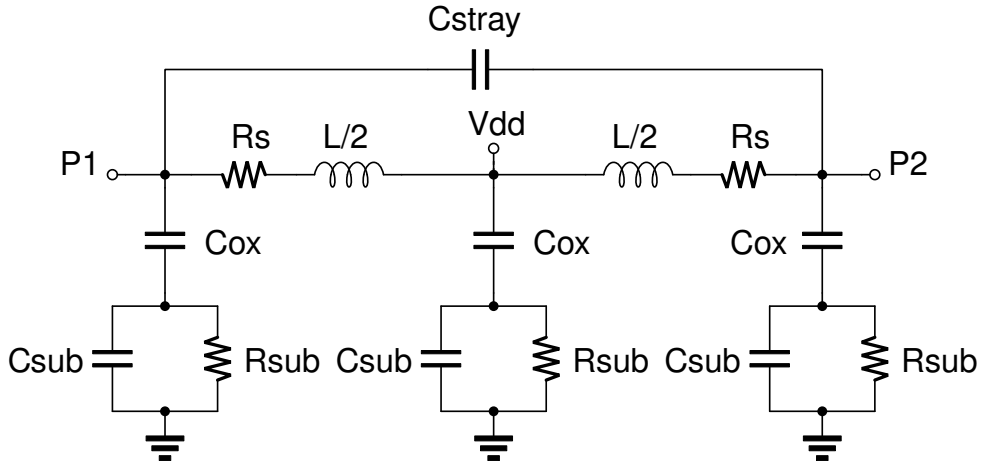

Figure 2.5. Differential Inductor Model.

Performing electromagnetic (EM) simulations to obtain a model represented by S-parameters is a common practice in the design of integrated inductors. These S-parameters can then be transformed into a pi-model using Y-parameters. However, due to certain limitations in the TSMC 28nm PDK used version, these simulations are not available. Consequently, inductor modeling poses a challenge for this project. Nevertheless, obtaining an accurate inductor model is not among the primary objectives. To address this, we opted to use the RFIC-GPT tool [13], which is open source and enables the automatic generation of the inductor layout based on the provided specifications, as long as it is feasible to create the desired inductor. Figure (**2.6**) illustrates the use of this tool.

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[12] SONNET SOFTWARE INC. *Inductor Model Extractor, Sonnet User's Guide*. Accessed: 30-Sept-2024. 2024. URL: https://sonnetsoftware.com/support/help-18/users_guide/Sonnet%20User's%20Guide.html?PIModel.html.

[13] RFIC-GPT. *Inductor Design Tool*. Accessed: 2023-11-20. 2023.

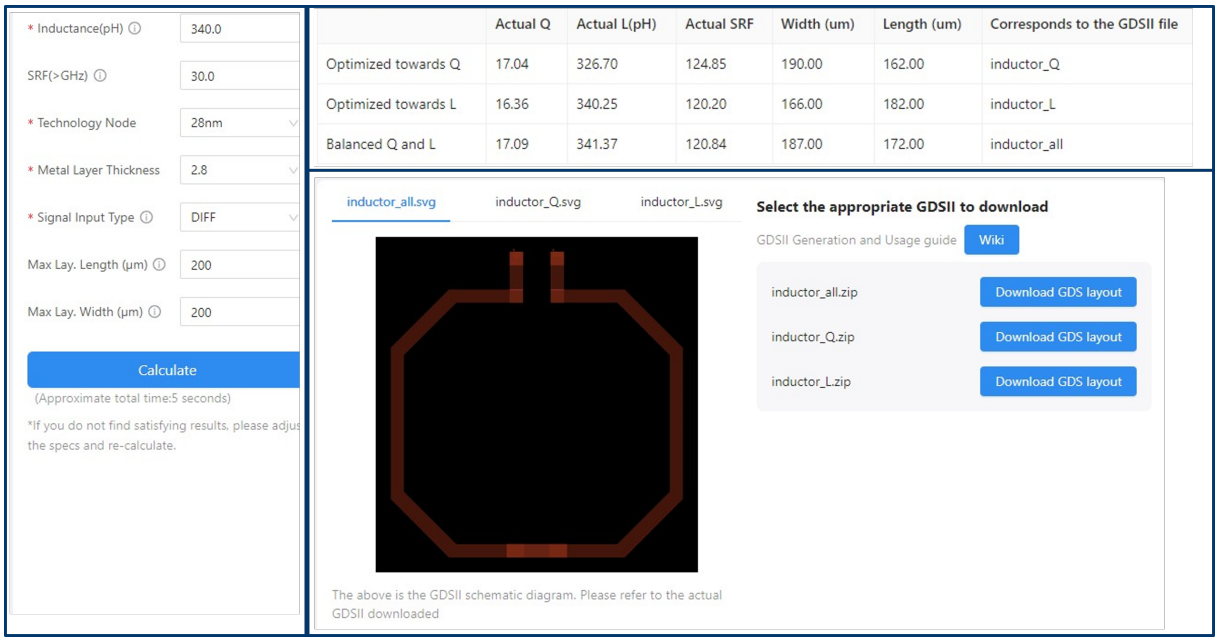


Figure 2.6. Inductor design tool.

After specifying all the inputs, the design tool generates three inductor models that differ in their optimization. One model is optimized for the quality factor, aiming to achieve a value closer to the specified target, albeit with some neglect of the other specifications. A similar approach is taken for the model optimized for inductance. To obtain a balanced model that yields results closely aligned with all specified criteria, the ”Balanced Q and L” model was selected.

The values of the elements composing the model have been derived from the outcomes produced by the design tool shown in Figure (**2.6**), which provides the inductance value and the quality factor. In addition to these results, it was necessary to analyze those obtained in the state of the art to closely resemble the frequency profile of both the inductance and the quality factor of the model with others derived from accurate electromagnetic simulations. Figure (**2.7**) illustrates the frequency profile of the inductor quality factor.

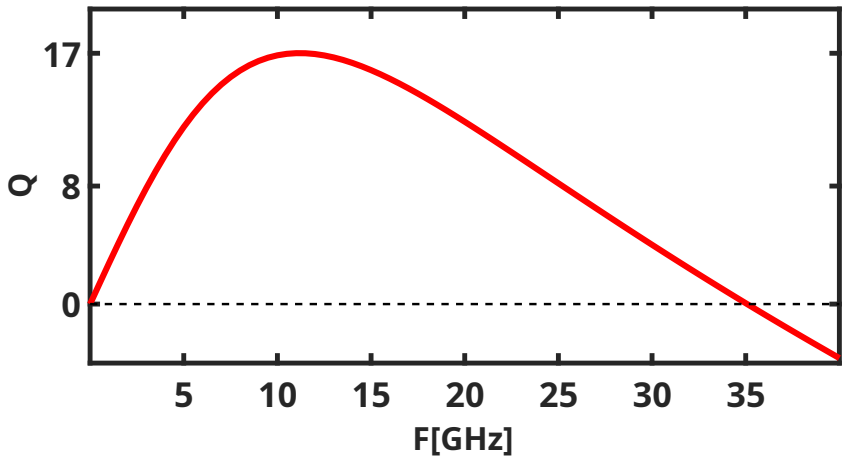


Figure 2.7. Quality factor vs frequency.

Likewise, Figure **2.8** shows the frequency profile of the inductance value, which has an ascending behavior

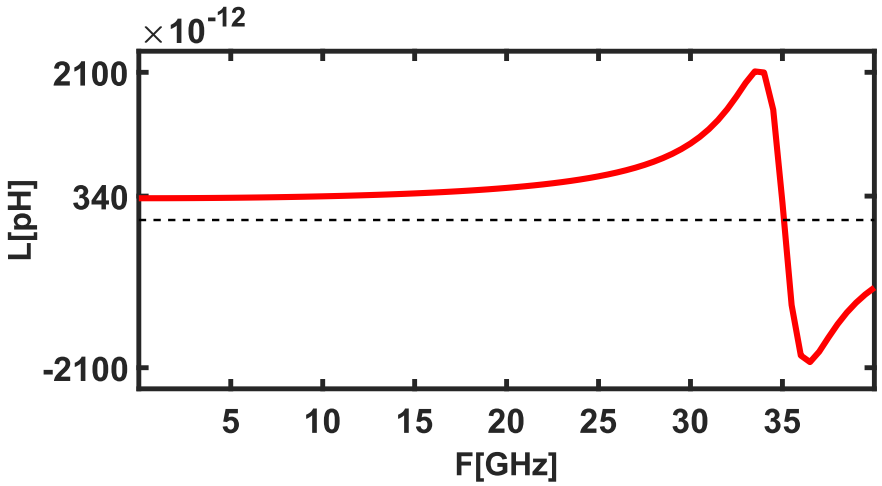


Figure 2.8. Inductance vs frequency.

in frequency as shown in Figure (**2.9**), where the zoom is just in the frequency range where the VCO design will finally be. This effect opposes the tuning of the VCO because when the varactors try to reduce their value to increase the frequency, the in-

ductance increases, which tries to keep the LC product fixed.

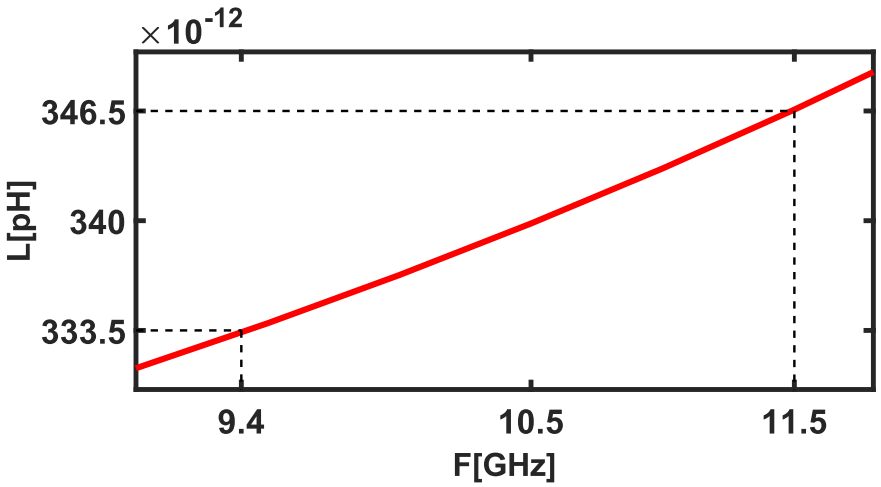


Figure 2.9. Inductance change in the tuning range..

2.4. Varactor Design

Initially, varactors were implemented as P-N junctions [14], which were reverse-biased to exploit their junction capacitance by varying their value with the reverse voltage of the P-N junction. By the late 1990s, transistors began to be employed as varactors, wherein the diffusions were shorted, and the voltage between the gate and the transistors was controlled [15]. The varactors utilized in this design are the ”Accumulation-Mode MOS Varactors,” as illustrated in Figure (**2.10**).

---

[14] B. De Muer N. ITOH and M. STEYAERT. “Low supply voltage fully integrated CMOS VCO with three terminals spiral inductor”. In: *Proceedings of the 25th European Solid-State Circuits Conference* (1999), pp. 194–197.

[15] S. Manzini F. SVELTO and R. CASTELLO. “A three terminal varactor for RF IC’s in standard CMOS technology”. In: *IEEE Transactions on Electron Devices* 47.4 (2000), pp. 893–895.

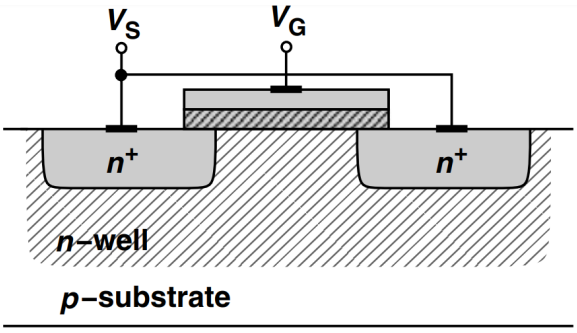


Figure 2.10. Acumulation-Mode Varactor [16].

These varactors exhibit a slight modification compared to conventional transistor varactors (Inversion-Mode MOS Varactors), as they are implemented with two N-diffusions in an N-well. This modification enhances their linearity; under negative V_{GS} voltages, electrons are repelled from the gate/oxide surface, resulting in a series combination of the oxide capacitance and the capacitance generated by the depletion of electrons. Consequently, this configuration allows them to maintain an increasing profile in the capacitance-voltage (C-V) curve, as illustrated in Figure (**2.11**).

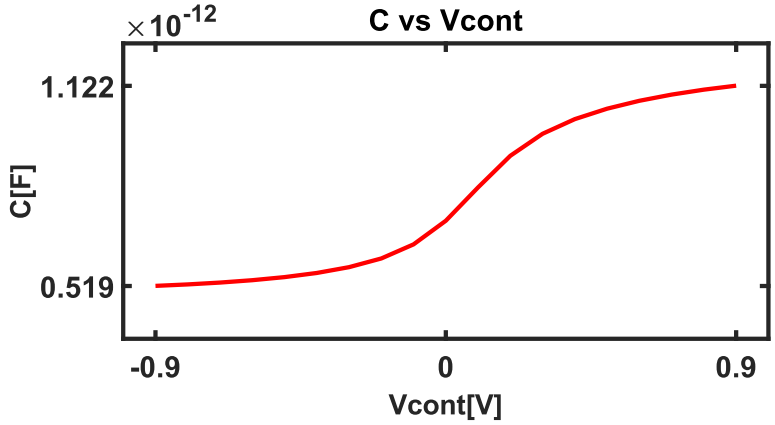


Figure 2.11. Capacitance vs Control Voltage.

The effective control voltage can vary within a range of 0.9V. Consequently, one must select between two ranges: -0.9V to 0V or 0V to 0.9V. Each range presents its advan-

tages and drawbacks. The range that offers a higher quality factor typically exhibits less capacitance variation, while the opposite is true for the other range. This choice ultimately depends on the designer's requirements. In this case, the range between 0V and 0.9V was selected to prioritize the tuning range.

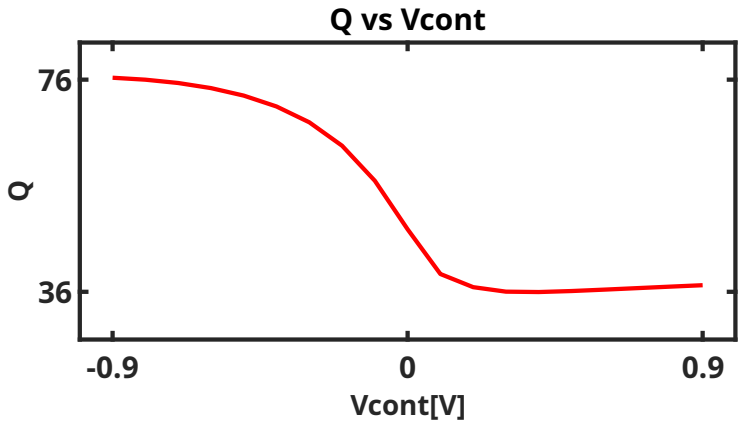


Figure 2.12. Quality factor vs Control Voltage.

Regarding the dimensions of the varactors, it is advisable to utilize the minimum length permitted by the technology to achieve a greater quality factor. This approach reduces the series resistance exhibited by the model, as illustrated in Figure (**2.13**).

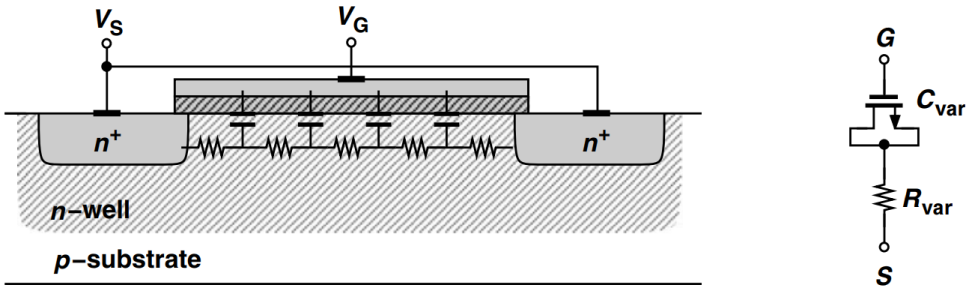


Figure 2.13. Acumulation-Mode Varactor [17].

2.5. Chapter Summary

- The basic design equations for the chosen topology such as the oscillation frequency, start-up condition, amplitude of the differential output, and phase noise were presented.
- The modeling of the inductor was performed by using the RFIC-GPT tool and also by comparison with the models obtained in the state of the art.
- A review of the different ways of implementing varactors was presented and the choice of the accumulation mode varactors was made, explaining their advantages, followed by a discussion of design strategies.

3. DESIGN METHODOLOGY

3.1. Design Specifications

This chapter presents the design specifications based on the chosen application, as well as the detailed design methodology.

3.2. Design Specifications

After conducting an extensive review of the state-of-the-art designs, the following circuit specifications have been established.

Table 3.1. Design specifications

Symbol	Parameter	Units	Min	Typ	Max
V_{dd}	DC Supply Voltage	V	0.81	0.9	0.99
T	Temperature	°C	-40	27	125
I_{bias}	Bias Current	uA	-	10	-
Q	Quality Factor	-	-	17	-
V_{Swing}@9.45GHz	Output Swing	V	0.7	1.4	1.7
V_{Swing}@11.5GHz	Output Swing	V	1.3	1.6	2
P_{DC}@9.45GHz	DC Power	mW	-	-	5.5
P_{DC}@11.5GHz	DC Power	mW	-	-	5.5
TR	Tuning Range	%	14.5	-	-
F_C	Carrier Frequency	GHz	-	10.5	-
PN@1MHz from 9.45GHz	Phase Noise	dBc/Hz	-	-110	-
PN@1MHz from 11.5GHz	Phase Noise	dBc/Hz	-	-110	-

These specifications are based on a specific application [18], in which a VCO is designed for a full-rate CDR, compliant with the G.8251 communication standard [19]. The quality factor was selected as the maximum achievable in 28nm technology at a frequency of 10.5[GHz], corresponding to the intermediate frequency. This value was obtained using the RFIC-GPT tool [13].

3.3. Current Source Design

The source transistors must have the maximum channel length (L) to ensure that the current source operates closer to ideal conditions, thereby minimizing flicker noise. The width of the transistors must be designed to generate the required current with a gate-source voltage $V_{GS} < V_{dd}(0.7)$, to maintain a sufficient voltage margin for V_{SD}. This margin allows the PMOS current mirror, which generates the reference current, to properly generate the reference current I_{ref} with the necessary bias current of 10[µA]. Figure (**3.1**) shows the complete current source circuit.

---

[18] Xuehui CHEN and Yingmei CHEN. "A 9.95-11.5Gb/s Full Rate CDR with Jitter Attenuation PLL in 65-nm CMOS Technology". In: *IEEE 13th International Conference on Communication Technology* (2011), pp. 273–276.

[19] ITU-T. *The control of jitter and wander within the optical transport network (OTN)*. tech. rep. G.8251. International Telecommunication Union, Nov. 2022.

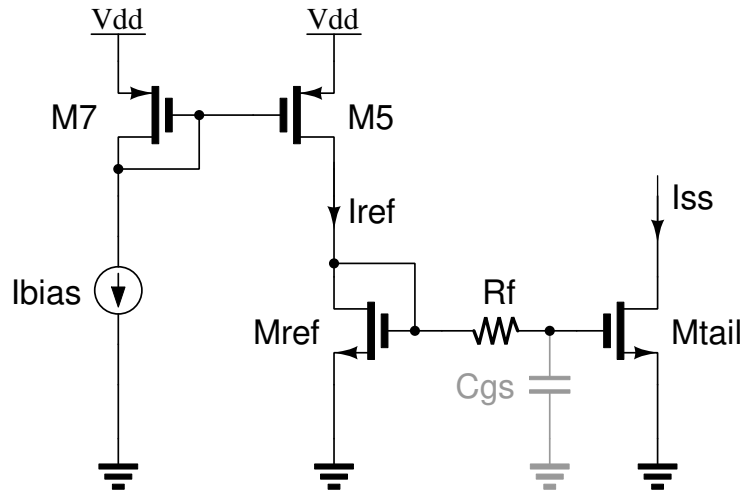


Figure 3.1. Current Source.

The RC filter, composed of the capacitor C_{gs} and the resistor R_f, is essential for filtering the flicker noise generated by the reference transistor. Since the current I_{SS} must be on the order of milliamps (mA), this necessitates a high gain in the current mirror ratio. Without filtering, the flicker noise would modulate the amplitude of the VCO, and the varactors would subsequently convert this modulation into phase noise [20]. An initial value of $I_{SS} = 4$[mA] was selected, considering that in process corners this current may vary, potentially exceeding the maximum power limit of 5.5 [mW], given a supply voltage of 0.9 [V].

3.4. Hand Calculations

The maximum frequency of the range was selected as the initial design frequency. This ensures that when the varactors are added, they can lower the frequency to the desired minimum value. To begin, the limiting parallel resistance is determined such

[20] B.RAZAVI. "The Design of a Millimeter-Wave VCO [The Analog Mind]". In: *IEEE Solid-State Circuits Magazine* 14.3 (2022), pp. 6–12.

that $V_{Swing} < 2.3 \times 0.9$, where 0.9 is a confidence factor that accounts for PVT variations. From equation (**25**):

$$V_{Swing} = \frac{4}{\pi} I_{SS} R_p < 2.3(0.9)[V], \tag{26}$$

hence, the limiting value of the resistance is found as $R_p < 400[\Omega]$. The inductance value is then calculated using equation (**14**).

$$L = \frac{R_p}{Q\omega} = \frac{400}{17(2\pi \cdot 11.5 \times 10^9)} = 325[pH], \tag{27}$$

next, the minimum gm required for the oscillation to start is determined using equation (**17**).

$$gm > \frac{1}{R_p} = \frac{1}{400}[S], \tag{28}$$

with this result, each transistor of the differential pair M_1 and M_2 must be designed to generate at least the minimum gm. Figure (**3.2**) presents a test that can be used for this purpose.

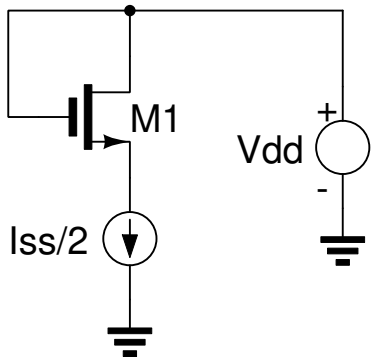


Figure 3.2. Transistor Design.

A DC analysis provides the parameters of the transistor's operating point, including the small-signal transconductance. Equation (**29**) presents an approximate expression for

the transconductance, from which the slope can be extracted to determine the necessary scaling of W to achieve the desired transconductance value.

$$gm = \sqrt{I_{SS}\mu_n C_{ox}\frac{W}{L}}[S] \tag{29}$$

3.5. Transistors Sizing

Once the initial hand calculations have been completed, the design process proceeds with the steps illustrated in the flowchart in figure (**3.3**). These steps facilitate transistor sizing, ensuring stable and optimal circuit operation. The objective is to optimize performance across all design specifications by fine-tuning transistor dimensions to establish a reliable operating point. Each step in the flowchart encapsulates decisions and adjustments required to meet the key specifications of the VCO.

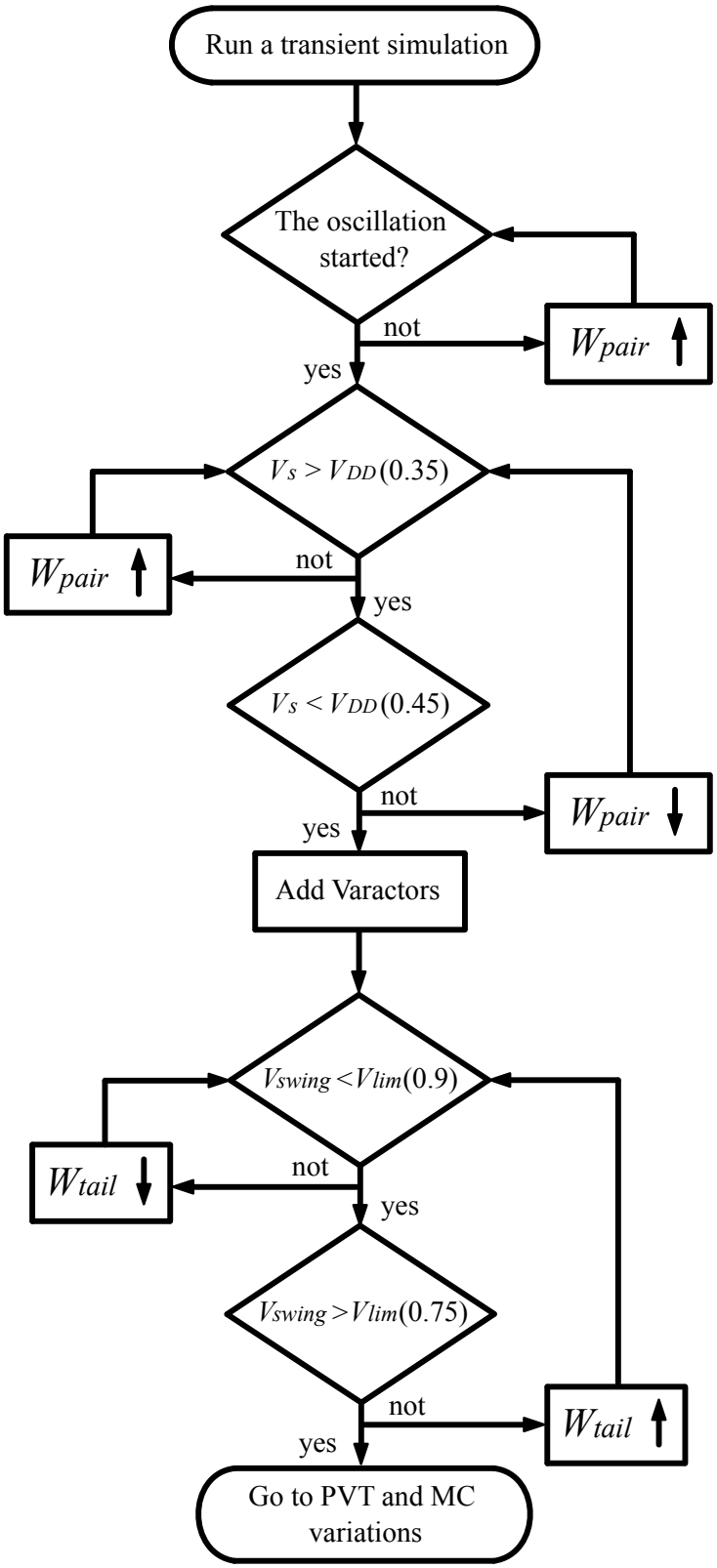


Figure 3.3. flow chart.

V_S represents the source voltage of the differential pair transistors, 2.3[V] is the maximum voltage that the transistors can withstand between the gate and drain according to the Save Operating Area Check (SOAC) of the 28nm technology, the mirror ratio refers to I_{SS}. When adding varactors the number of multipliers should be increased until the maximum frequency of the tuning range is reached, in case the initial inductance value together with the parasitic capacitances are already generating a carrier frequency lower than the design frequency then it is necessary to reduce the inductance and repeat the flowchart.

3.6. Design For PVT Variations

Maintaining a stable I_{SS} current under PVT variations is critical for ensuring reliable circuit performance. Variations in the supply voltage directly affect the V_S voltage, influencing the accuracy of the I_{SS} current replication. Process variations, particularly at the SS and SF corners, alter the overdrive of the source transistors due to the increased threshold voltage (V_{TH}). Moreover, temperature variations impact the resistivity of the circuit, thereby affecting the current. To address these issues, it is necessary to increase the channel length of the source transistors by stacking additional transistors. Given that the maximum L allowed by the technology is 400[nm], stacking transistors emulates the effect of having a longer channel length, as illustrated in Figure (**3.4**).

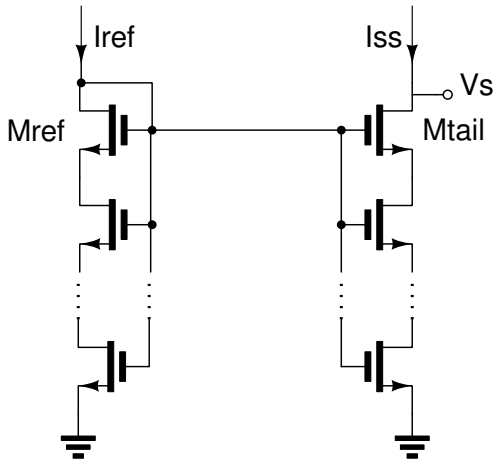


Figure 3.4. Transistors in stack.

The process of stacking each transistor is followed by re-evaluating the flowchart without incorporating the varactors. This procedure is repeated with the objective of positioning V_S within the desired range, specifically $V_{dd}(0.35) < V_S < V_{dd}(0.45)$. The goal is to ensure that the current I_{SS} remains constant enough to meet the specifications as long as the area constraints are not affected.

3.7. The Inductance Value

The inductance value obtained from hand calculations may not represent the optimal inductance for the VCO [11]. Consequently, at this stage, the designer must plot the phase noise as a function of the inductance value. For each inductor value, the flow diagram must be reiterated. Figure (**3.5**) illustrates the results of this iterative process.

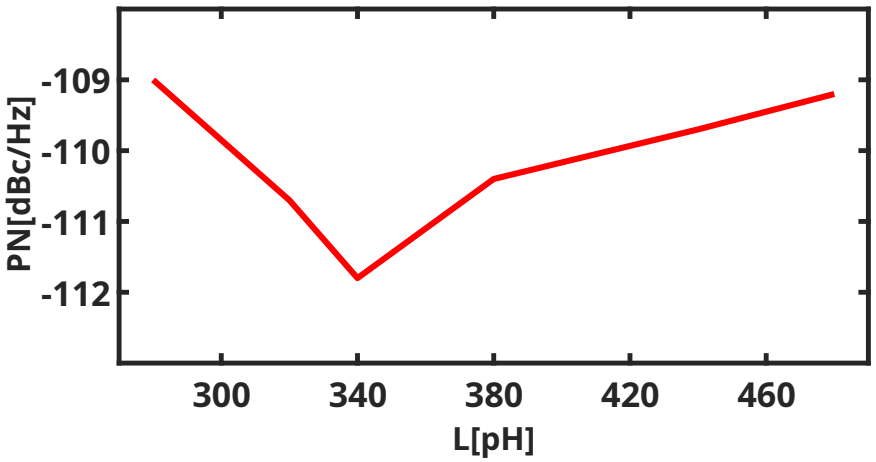


Figure 3.5. Phase noise (PN) vs the inductance value (L).

All phase noise measurements were taken at 1[MHz] offset with respect to the lowest VCO frequency.

3.8. Discrete-Tuning

At this stage, the final design of the VCO is likely complete, unless the varactors with the voltage range of V_{cont} are unable to tune the VCO from the designated high frequency to the lowest frequency. To address this issue, discrete tuning is employed, which involves adding or removing extra capacitance from a capacitor bank to achieve the lowest frequency within the specified range. The switches are implemented differentially to minimize the degradation of the resonator's quality factor. Figure (**3.6**) illustrates the implementation of the differential switches [20].

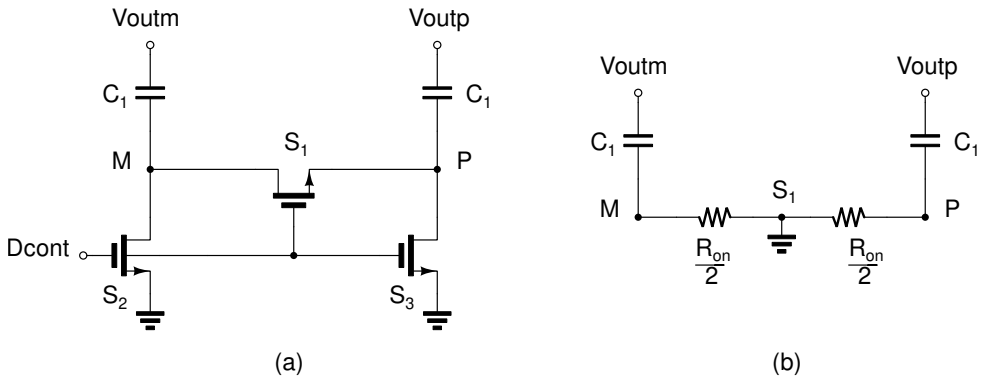


Figure 3.6. (a)Differential switch, (b) Equivalent circuit.

Regarding the design of switch S1, it is advisable to use the minimum length L. As the width W is increased, the quality factor improves due to a reduction in the on-resistance R_{on}; however, this also leads to an increase in parasitic capacitance when the switch is off, resulting in less capacitance variation. For switches S2 and S3, it is also recommended to utilize minimum dimensions to minimize parasitic capacitance, as their primary function is to bias switch S1.

Each differential switch implemented corresponds to a control bit and is operated by the digital control signal D_{cont}. In this design, three switches were utilized, allowing for eight possible combinations that represent a frequency band in which the varactors can continuously control the frequency. An overlap between the bands must be maintained to ensure continuous tuning, as illustrated in Figure (**3.7**).

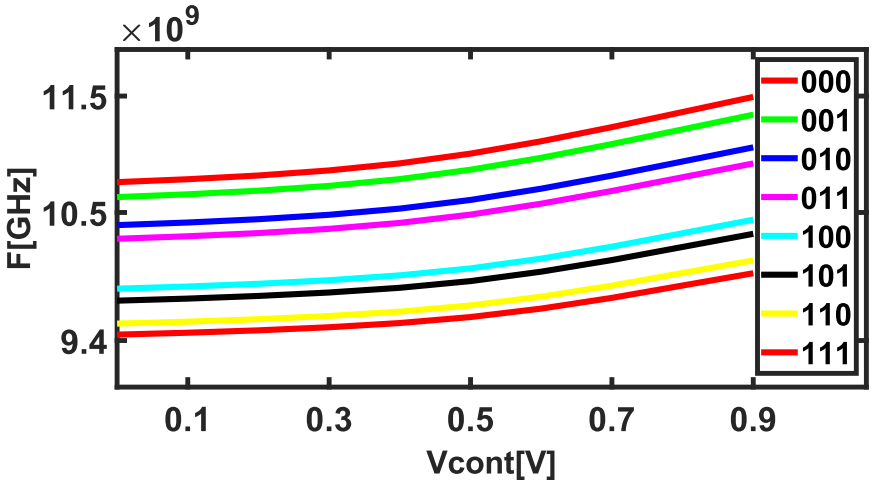


Figure 3.7. Frequency bands.

3.9. Chapter Summary

- Specifications for a VCO in a CDR were defined for an optical communication standard.
- A comprehensive design methodology for the selected VCO topology was outlined, beginning with the design of the current source and a series of hand calculations. This was followed by the flowchart detailing the transistor sizing process and the design for PVT variations
- The options for adjusting the inductor value and implementing discrete tuning to address any specifications that may not be fully satisfied were presented.

4. RESULTS

This chapter presents the results of the device sizing process. Additionally, it provides the results obtained from PVT and Monte Carlo simulations. Finally, it presents a comparison of the achieved design with the state-of-the-art.

4.1. Device Sizes

Table (**4.1**) summarizes all the dimensions and parameters of the transistors and capacitors used in the design, the C_1, C_2, C_3 capacitors and S_1, S_2, S_3 switches are part of the differential switches that make up the discrete preset tuning. See figure (**3.6**). Four-terminal RF transistors were used, along with MOM capacitors.

Table 4.1. Sizes and values of the VCO transistors and capacitors.

Name	$Fing_W[\mu m]$	$Fing_L[nm]$	N_{Mult}	N_{Fing}	N_{Stacks}	$Layers$	$Fing_S[nm]$
M_1	1	150	7	18	1	-	-
M_2	1	150	7	18	1	-	-
M_3	6.9	150	-	-	1	-	-
M_4	3	150	2	4	1	-	-
M_5	6.9	400	10	15	1	-	-
M_6	6.9	150	2	4	1	-	-
M_7	6.9	400	5	5	1	-	-
M_8	6.9	150	2	4	1	-	-
M_{tail}	6.9	400	10	27	6	-	-
M_{ref}	6.9	400	1	4	6	-	-
S_1	6.9	150	2	22	1	-	-
S_2	1	150	1	4	1	-	-
S_3	1	150	1	4	1	-	-
C_1	2u	50	20	-	-	1-6	50
C_2	2u	50	37	-	-	1-6	50
C_3	2u	50	80	-	-	1-6	50

Table (**4.2**) shows the dimensions of the varactors. The used varactors were the Accumulation-Mode ones.

Table 4.2. Sizes of the VCO varactors.

Name	$OD_W[nm]$	$Poly_L[nm]$	OD_{group}	N_{Mult}	$C_{var}(0V)[fF]$	$C_{var}(0.9V)[fF]$
C_{var}	600	200	1	13	372	584

Table (**4.3**) shows the values of the elements that make up the model of the inductor in figure (**2.5**). All these elements are ideal.

Table 4.3. Inductor model values.

Name	$L[pH]$	$R_S[m\Omega]$	$C_{stray}[fF]$	$C_{ox}[pF]$	$C_{sub}[fF]$	$R_{sub}[\Omega]$
Value	310	352.61	18	3	100	500

Table (**4.4**) shows the dimensions of the R_f resistance. The used resistor was the 3-terminal polysilicon resistor.

Table 4.4. Dimensions of the R_f resistance.

Name	$Segment_{Width}(nm)$	$Segment_{Length}(\mu m)$	$N_{Multiplier}$	$N_{segments}$
R_f	100	24.64	1	20

4.2. PVT and Monte Carlo Simulations

PVT and Monte Carlo simulations are performed after the design phase to ensure robust performance. Process variations affect components like transistors and resistors, while voltage and temperature vary by ±10% and from -40 to 125 $[^{\circ}C]$, respectively. Table (**4.5**) shows the simulation results.

Table 4.5. PVT simulation

Parameter	Units	Target			Results			Judge
		Min	Typ	Max	Min	Typ	Max	
V_{dd}	[V]	0.81	0.9	0.99	0.81	0.9	0.99	-
Temperature	[^{o}C]	-40	27	125	-40	27	125	-
I_{bias}	[uA]	-	10	-	-	10	-	-
Quality Factor@10.5GHz	-	-	17	-	-	16.75	-	-
V_{Swing}@9.45GHz	[V]	-	-	2.3	0.487	1.244	1.744	O
V_{Swing}@11.5GHz	[V]	-	-	2.3	1.302	1.813	2.199	O
P_{DC}@9.45GHz	[mW]	-	-	5.5	2.23	3.46	5	O
P_{DC}@11.5GHz	[mW]	-	-	5.5	2.33	3.51	5	O
Tuning Range	[%]	14.5	-	-	18.1	20	21.3	O
F_C	[GHz]	-	10.5	-	9.7	10.5	11.36	O
PN@1MHz from 9.45GHz	[dBc/Hz]	-	-110	-	-114.1	-110.7	-104.4	O
PN@1MHz from 11.5GHz	[dBc/Hz]	-	-110	-	-110.8	-109	-106.6	O

Table (**4.6**) presents the results of 1400 random samples of the possible process variations in the circuit.

Table 4.6. Monte Carlo simulation

Parameter	Units	Results				Judge
		Min	Mean	Max	σ	
V_{Swing}@9.45GHz	[V]	1.195	1.244	1.295	0.015	O
V_{Swing}@11.5GHz	[V]	1.778	1.814	1.849	0.0107	O
P_{DC}@9.45GHz	[mW]	3.32	3.5	3.63	0.04	O
P_{DC}@11.5GHz	[mW]	3.34	3.52	3.63	0.0375	O
F_C	[GHz]	10.48	10.5	10.52	0.0005	O
PN@1MHz from 9.45GHz	[dBc/Hz]	-112.5	-110	-99.71	0.606	O
PN@1MHz from 11.5GHz	[dBc/Hz]	-117.9	-109	-100.3	0.476	O

The results obtained are sufficient in each of the specifications proposed by the application for which the use of the VCO is intended [19], in addition, these results are comparable with those obtained in [18] where the design of a VCO for the same application is also proposed.

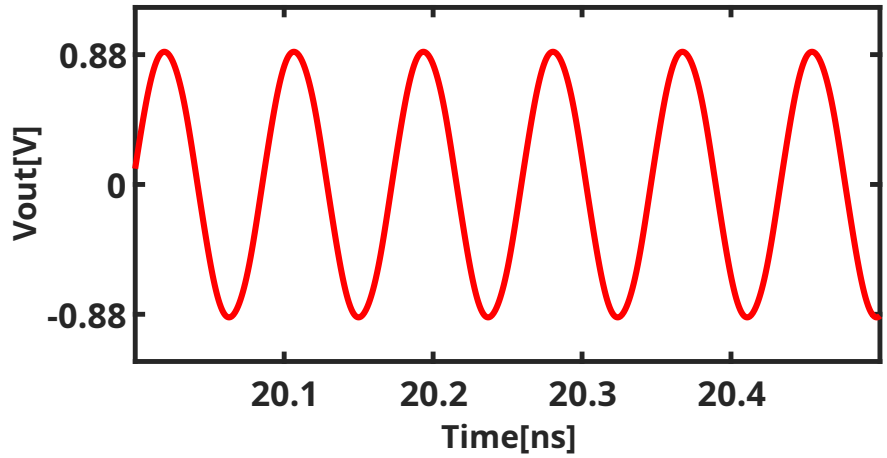
4.3. VCO Mesurements

This section presents the graphs from which the VCO measurements were obtained, except for the tuning range, which is already shown in Figure (**3.7**).

4.3.1. Voltage swing

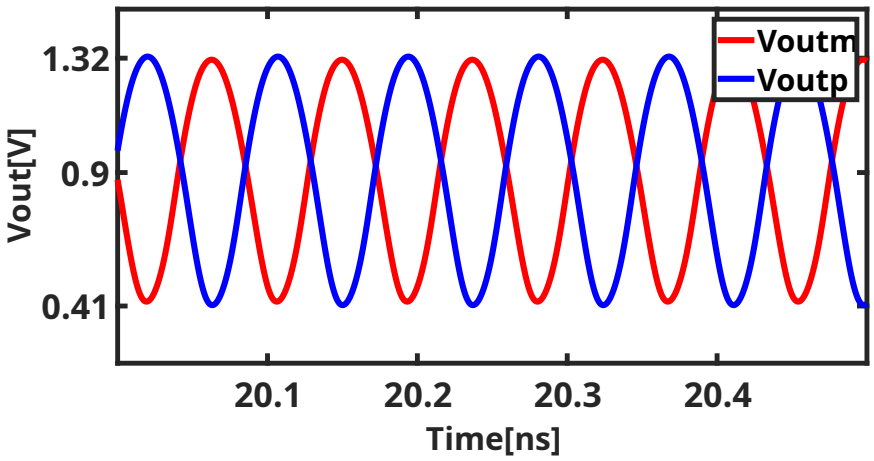
The voltage swing is obtained by measuring the difference between the maximum and minimum of the output signal in a steady state. In Figure (**4.1**), the output signal of the VCO at the highest frequency of the range, corresponding to 11.5 [GHz], can be observed.

Figure 4.1. Differential output signal.



This signal is obtained after performing the differential operation between the output nodes, which can be observed in Figure (**4.2**).

Figure 4.2. Voltage at each output node.



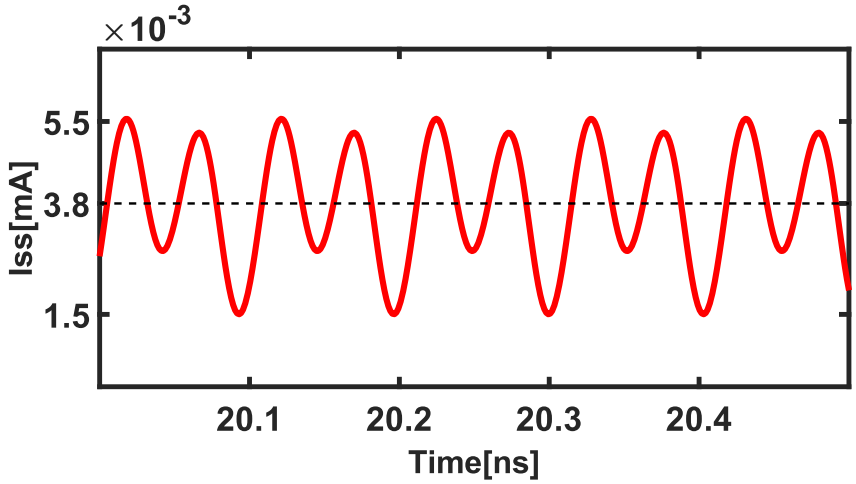
As shown in Figure (**4.2**), each output node is centered at V_{dd}. This is because the inductors create a short circuit between V_{dd} and each output node in DC. Additionally, from a signal perspective, each output resonator behaves like a bandpass filter that

generates a sinusoidal signal from the current pulses coming from the transconductor.

4.3.2. Power consumption

To measure the power consumption, only the current that powers the VCO core is considered. The average value of this current over time is taken and multiplied by the supply voltage V_{dd}. Figure (**4.3**) shows the current over time in steady state.

Figure 4.3. VCO core current.



The average value is obtained from a function that takes the signal over time and performs an integration.

4.3.3. Phase noise

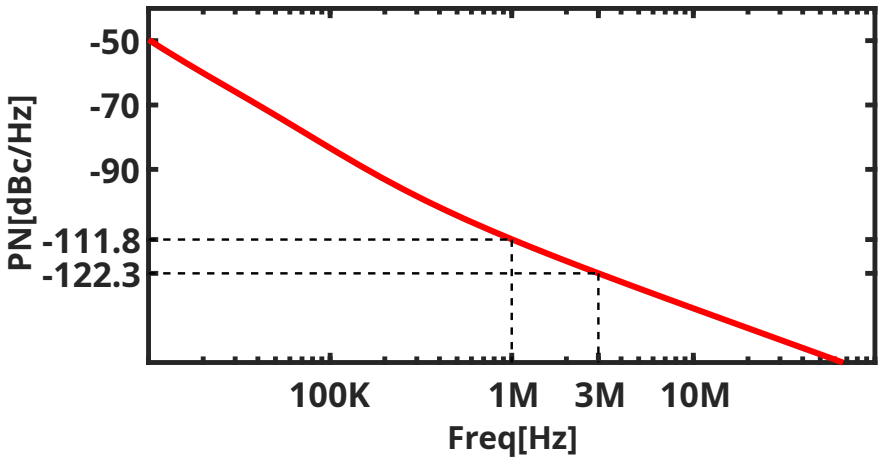
In Equation (**30**)[21], the expression that determines the phase noise of an oscillator can be seen.

$$L[\Delta f] = \frac{S_v(\Delta f)}{\frac{V^2}{2}}[dBc/Hz], \tag{30}$$

[21] Hajimiri A and Ham D. "Virtual Damping and Einstein Relation in Oscillators". In: *IEEE JOURNAL OF SOLID-STATE CIRCUITS* 38.3 (2003), pp. 407–418.

where $S_v(\Delta f)$ is the output spectrum. The simulator internally performs this operation for each frequency offset for which a measurement is requested. Figure (**4.4**) presents the phase noise from a 10.3[GHz] carrier.

Figure 4.4. Phase noise from a 10.3[GHz] carrier.



4.4. State-of-art comparison

To know how the design is positioned concerning the other state-of-the-art designs, a comparison is made based on a figure of merit (FoM) [11] which is very popular in the art and encompasses the most important parameters of a VCO. This FoM has two variations, one considering the tuning range and the other one that does not consider it, both expressions are presented as follows:

$$FoM = 20\log\left(\frac{F_C}{\Delta\omega}\right) - PN[\Delta\omega] - 10\log\left(\frac{P_{DC}}{1mW}\right) \tag{31}$$

$$FoM_T = FoM + 20\log\left(\frac{TR}{10}\right) \tag{32}$$

Table (**4.7**) shows the comparison of the results obtained in this work with those obtained in other comparable state-of-the-art designs.

Table 4.7. State-of-art comparison.

Specification	[22]**	[23]*	[24]*	**This Work****
Technology [nm]	28	65	28	28
V_{dd}[V]	0.95	1	N/A	0.9
F_C [GHz]	30	10.5	10.5	10.5
TR [%]	13.5	19	17.8	**20**
PN@1MHz [dBc/Hz]	-100	-110	-111.8	**-112**
P_{DC} [mW]	2	5	4.88	3.4
FoM [dB]	186.5	183	186.33	**186.84**
FoM_T [dB]	189.1	188.57	191.33	**192.87**

*On silicon**On Schematic

As we can see in Table (**4.7**), this design outperforms the other designs in both FoMs. It is important to highlight that the measurements of this VCO were carried out at the schematic level, as was the case with one of the comparison designs, which uses the same topology, differing only in the center frequency and reference current, where approximately 760 [mW] is consumed while in this work, the power consumption due to the reference current is 57.6 [mW], attributed to the filtering strategy implemented using the resistor R_f. The designs measured on silicon use more complex topologies to enhance performance. From this, it can be concluded that the design methodology significantly optimizes the chosen topology.

5. CONCLUSIONS AND FUTURE WORK

5.1. Conclusions

A design methodology for a VCO using the cross-coupled pair topology with NMOS transistors in the 28 nm CMOS technology node was described. This methodology consists of a series of steps, beginning with hand calculations based on the design specifications to establish an initial design point. The process then proceeds with an initial sizing of the transistors, followed by a flowchart that adjusts the dimensions to achieve an optimal operating point for the circuit.

The circuit specifications were defined based on the study of the Safe Operating Area Check (SOAC) for TSMC's 28 nm technology and a publication **??** in which a VCO is designed for a full-rate CDR in a high-speed link receiver. In this work, it is established that the phase noise at a 1 [MHz] frequency offset should be -110 [dBc/Hz] and the tuning range should span from 9.95 [GHz] to 11.5 [GHz], in accordance with the G.8251 optical communication standard [19].

The design of a VCO using the standard 28 nm CMOS process was completed, achieving a state-of-the-art *FoM* of 186.6 [dB] and a FoM_T of 192.72 [dB]. The phase noise measured at 1 [MHz] was -111.8 [dBc/Hz], with a tuning range from 9.45 [GHz] to 11.5 [GHz] and a power consumption of 3.4 [mW].

The performance of the VCO was validated under PVT variations, ensuring reliable circuit startup and maintaining the output amplitude below 2.3[V]. This validation was carried out over a temperature range of -40 to 125 [$^\circ$C], alongside process variations in each device and a 10% supply voltage fluctuation. Additionally, a Monte Carlo analysis

was performed using 1400 samples per test, yielding a standard deviation of the output voltage of 0.0142 [V].

5.2. Future Work

In future work, I would like to encourage the reader to implement an algorithm based on this design methodology to accelerate the design process. Additionally, it would be interesting to develop a design methodology for other VCO topologies.

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