DESIGN OF A DIGITAL-TO-ANALOG CONVERTER IN 180nm CMOS TECHNOLOGY FOR SoC APPLICATION

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Dedicado a

Mis padres que con su esfuerzo, ayuda y apoyo hicieron posible matener y culminar mi proceso en la universidad.

Mis amigos, aquellos que conocí a lo largo de estos años, personas que siempre fueron una compañía grata y con quienes compartí muchas experiencias amenas.

Todas aquellas personas que contribuyeron con este proyecto y que a pesar de sus ocupaciones dedicaron un tiempo para ayudar a la culminación del mismo.

Eder Zamir Chacón Sanchez

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Glossary

Below are some concepts used in the work developed:

DNL: DNL error is defined as the difference between an actual step width and the ideal value of 1LSB.

INL: INL error is described as the deviation, in LSB or percent of full-scale range (FSR), of an actual transfer function from a straight line. The INL-error magnitude then depends directly on the position chosen for this straight line.

RESUMEN

Título: Diseño de convertidor digital a analógico en tecnología CMOS en 180nm para aplicaciones en SoC[1].

Autor: Eder Zamir Chacón Sanchez[2].

Palabras Clave: error DNL, condensador divisor, condensador unitario, calibración, DAC, condensador MOM.

DESCRIPCIÓN:
Este artículo presenta el diseño de un convertidor digital a analógico (DAC) de 12 bits basado en una arquitectura capacitiva diferencial (CDAC) con *split-capacitor* construido mediante el arreglo de un capacitor en paralelo con dos capacitores en serie de valor unitario. El DAC se implementó utilizando una tecnología CMOS estándar de 180 nm. Se usaron capacitores de metal-óxido-metal (MOM) para implementar un diseño interdigitado con distribución centroide común y capacitores *dummy* para reducir el acoplamiento y los efectos de desajuste. Se aplica un método de calibración mediante asignación de una palabra digital con capacidad de ser modificada según sea conveniente para mejorar el error de DNL existente, la calibración utiliza una máquina de estados finitos y un banco de condensadores adicionales ubicados en el lado del bit menos significativo del diseño con una resolución de un cuarto de capacitor unitario. Las simulaciones *post-layout* muestran una no linealidad integral y diferencial menor que 1 LSB respectivamente, a una frecuencia de muestreo de 10 MHz. El circuito diseñado ocupa un área total de $0.0544mm^2$(160μm X 340μm), con un consumo actual de 3.046μA. El DAC se puede utilizar para fines de *trimming* y calibración de circuitos analógicos de señal mixta en aplicaciones de Sistemas en Chip (SoC).

[1]Trabajo de Grado

[2]Facultad de Ingenierías Físico-Mecánicas. Escuela de Ingenierías Eléctrica, Electrónica y de Telecomunicaciones. Director: Adres F. Amaya Beltraán, MSC. Codirector: Elkim F. Roa Fuentes, PhD.

ABSTRACT

Title: Design of a Digital-to-Analog Converter in 180nm CMOS Technology for SoC Application[1].

Authors: Eder Zamir Chacón Sanchez [2].

Key Words: split-capacitor, DNL error, unit capacitor, calibration, DAC, MOM capacitor.

DESCRIPTION:
This paper presents the design of a 12-bit digital-to-analog (DAC) converter based on a differential capacitive architecture (CDAC) with split-capacitor built by arranging a capacitor in parallel with two capacitors in series. The DAC was implemented using a standard CMOS 180nm technology. Metal-oxide-metal (MOM) capacitors were used to implement an interdigitated layout with common centroid distribution and dummy capacitors to reduce coupling and mismatch effects. A calibration method is applied by assigning a digital word with the ability to be modified as appropriate to improve DNL error, which uses a finite state machine and an extra capacitor bank on the least significant bit side of the design with a resolution of a quarter of a unit capacitor. Post-layout simulations shows an integral and differential nonlinearities smaller than 1 LSB respectively, at a sampling frequency of 10 MHz. The designed circuit occupies and area of $0.0544mm^2$ (160μm X 340μm), with a current consumption of 3.046μA. The DAC could be used for trimming and calibration purposes of analog and mixed-signal circuits in System-on-Chip (SoC) applications.

[1]Bachelor Thesis

[2]Facultad de Ingenierías Físico-Mecánicas. Escuela de Ingenierías Eléctrica, Electrónica y de Telecomunicaciones. Director: Adres F. Amaya Beltraán, MSc. Codirector: Elkim F. Roa Fuentes,PhD.

INTRODUCTION

DACs are crucial blocks for mixed-signal systems because they can be used for on-chip performance trimming and calibration. Their accuracy could determine the overall performance of the entire system because they are used to adjust and test internal circuits. The implementation of DACs as on-chip trimming saves the complexity of external calibrations and does not involve the use of large digital resources. Moreover, implementing a CDAC reduces current consumption as it only demands dynamic power.

Current research projects of OnChip group are related to the design of SoC and microcontrollers based on the RISC-V instruction set. These kind of systems will include peripherals such as power-on-reset (POR), brown-out-detector (BOD), bias generators, and USB interfaces. One common characteristic of listed peripherals is the need of a bias current whose value has to be set regarding PVT variations or speed operation. A DAC is an option for implementing a variable current source, which will help to reduce performance variability.

This work presents the design of a 12bits DAC based on a split capacitive topology [5], which can operate at a sampling frequency of 10MHz. The circuit is designed at circuit and physical level using a standard 180nm CMOS technology, which allows to a rapid implementation between different fabrication processes. Due to the impact of parasitics components on capacitor array, a DNL calibration method was adapted from [7], resulting in a low-complexity algorithm which can be fully synthesized by digital circuits. Most important parameters when designing DACs are glitch energy, settling time and linearity were addressed during circuit design [9].

Chapter 1
DAC ARCHITECTURE

Conventional binary-weighted (CBW DAC) DAC in which number of capacitors increases exponentially with the number of bits imposes a large consumption of switching energy, area, and settling time [4] [9]. One of the most popular solutions is to employ an attenuating capacitor in the binary-weighted array (BWA DAC) [6]. The structure consists in two capacitor arrays (most significant bit (MSB) array and least significant bit (LSB) array) connected by a series capacitor, as Fig. 1 shows.

Each capacitor array is made up of 63 unitary capacitors with their respective switch that allows to connect each element to V_{ref} or VSS, as the case may be required. Its key limitation lies in the parasitic capacitors that affects the desired binary ratio of the DAC array [8], where the conventional charge-redistribution switching degrades linearity [1]. The BWA DAC design was selected because it is better than CBW DAC in almost all the exposed factors (CBW it is only better than BWA in linearity). A differential implementation was selected with the purpose of reduce errors associated to split capacitor and parasitic components, as well as to cancel second order non-linearity [3] [5].

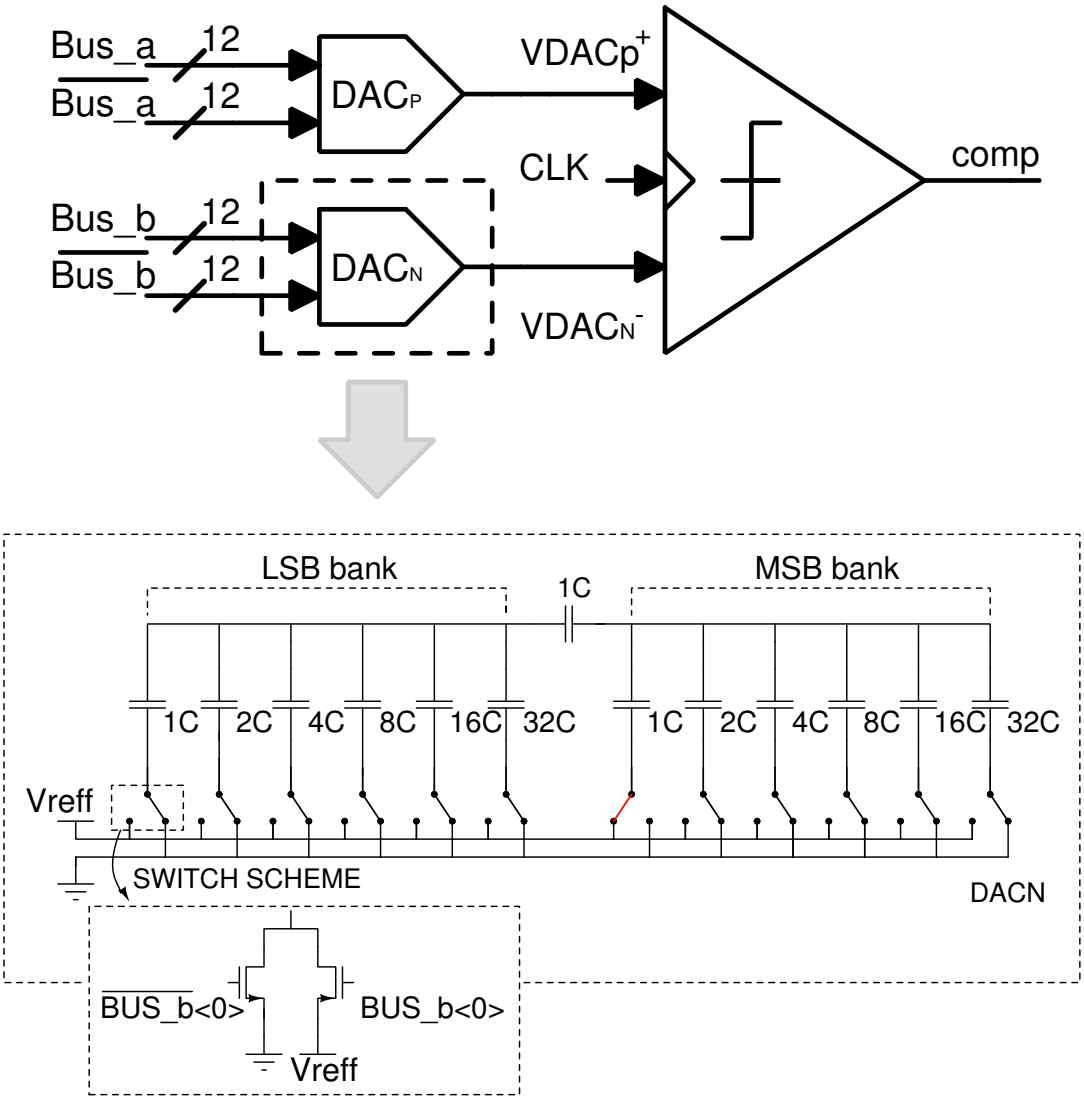
1.1 Unity Capacitor

Selecting a small unit capacitance is the key to reducing the layout area of the capacitor array. To obtain the minimum value of the unit capacitor (C_u), the circuit must be reduced to its minimum expression (RC circuit), and it must be solve the noise error equation with C_T as variable.

$$\text{Thermal Noise} = \frac{kT}{C_T} \tag{1.1}$$

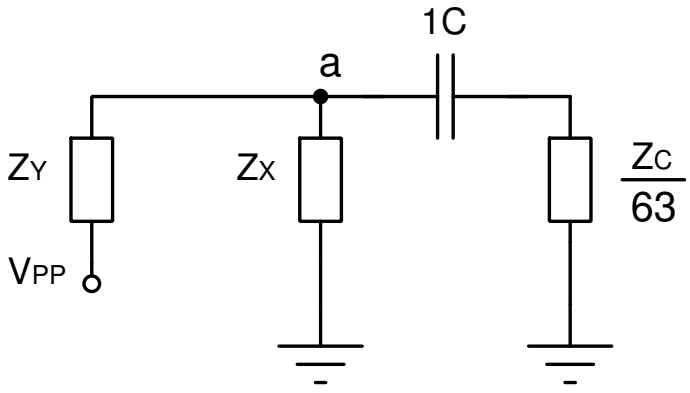
$k = 1.3806x10^{-23}J$ is Boltzmann's constant, T is the operation temperature and C_T is the equivalent capacitor. The initial reduction is showed in the Fig. 2, and it is possible to

Figure 1: Differential 12-bit split-CDAC architecture with unit value bridge capacitor.



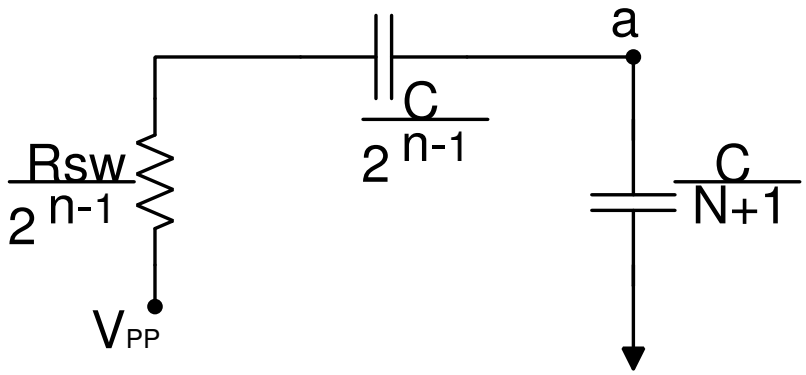
establish a relationship among the impedance contributions seen by each switch in the MSB side.

Figure 2: Equivalent circuit of split CDAC.



Where $Z_y = \frac{z_c}{2^{n-1}}$, $Z_x = \frac{z_c}{N}$ and $N = 64 - 2^{n-1}$. The reduction of the impedance seen from node "a" to ground allows the resistance to be approximated to zero, the inductances in parallel make to switch resistance has a reduction because the final configuration of equivalent resistance is divided by $63 + 2^{n-1}$. It is noted, the equivalent noise power of filtered noise at the output is independent from the switch resistance as manifest a Equation 1.2. Hence the equivalent capacitance is determined (Fig. 3).

Figure 3: Final equivalent circuit.



The equivalent capacitor seen from the LSB is $C_{TL} = \frac{C[(63-2^{n-1})+1]}{64}$. A similar process is performed for the MSB side, and it results in $C_{TM} = \frac{63(63-2^{n-1})C}{2^{n-1}}$. Finally, the thermal error contribution of both sides is added, and the Equation1.2 is solved with C as variable.

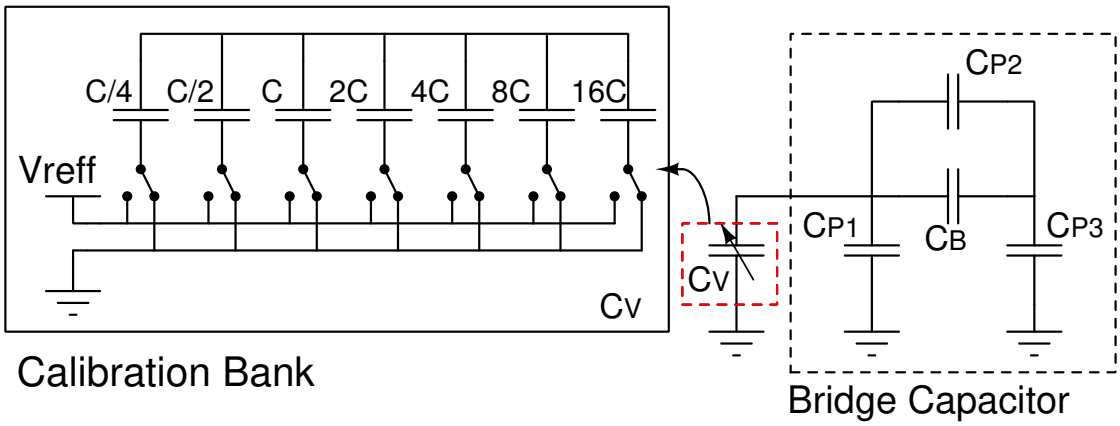
$$V_o^2 = \frac{kT}{C_T} \tag{1.2}$$

The temperature T = 398.15 K was the upper range analyzed in the corners simulations. Being the case with the highest probability of thermal noise, its results establishes the minimum dimension of the unit capacitor. To know the value of the capacitor that covers the requirements of the DAC, it is assumed that the value of the thermal noise must be less than the quantization noise. Then As a final result we have that $C > 1.92fF$ is the minimum value required for the structure of the DAC. Nonetheless, a 25 fF unit capacitor is used for manufacturing recommendations.

1.2 MOM Capacitor

MOM capacitors are formed by interdigitated fingers of several vias-interconnected metals of CMOS process back-end. Its physical principle is the lateral coupling between these fingers (MOMs are included in the side-flux capacitors categorization) [2]. Capacitors values near the DAC's borders differ from the ones positioned far from them. Moreover, coupling between silicon substrate and MOMs terminals increase parasitics, where these capacitances are also affected by variations in MOMs surroundings. These effects produce a mismatch error, and its physical characteristics hinder the layout connexions because it is not possible to pass the tracks through the capacitors in many directions with metals from 1 to 5 forcing to pose a routing strategy.

Figure 4: Parasitic capacitances of MOM Split Capacitor.



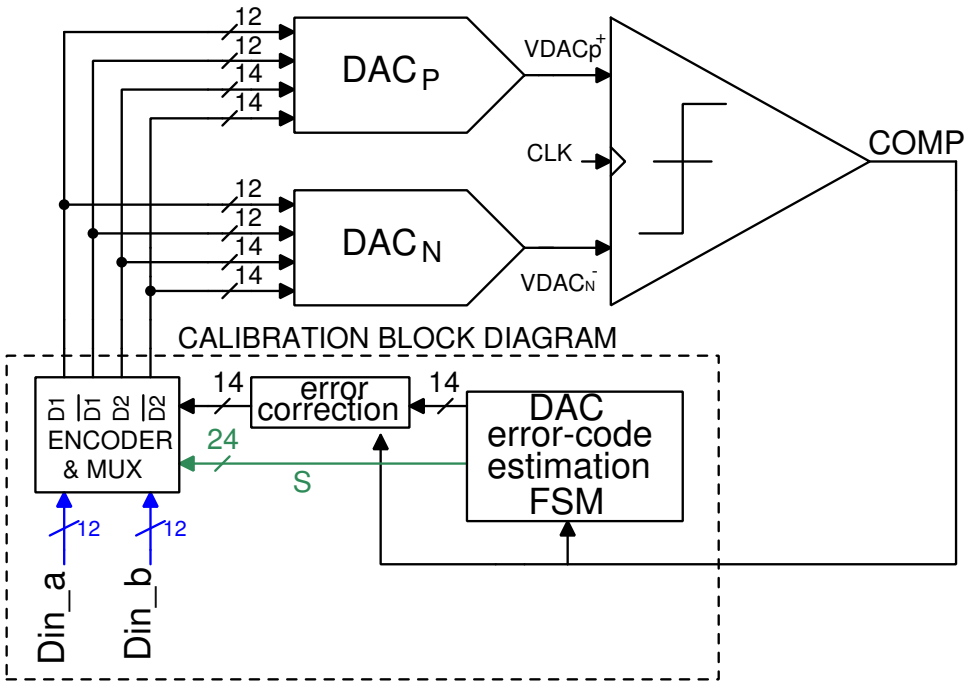
Chapter 2
CALIBRATION

The variations of MOM capacitance seen in the previous section affect the un-even split-capacitor DAC behavior. The parasitic capacitances in Fig. 4 produce DNL error according to its size. To simulated the right side parasitic capacitances Cp1, values from 113fF to 150fF were used. Moreover, a value of 4Cu was used for Cp3 and 0.8fF was used for Cp2. The DNL error imposed by parasites of LSB side is corrected by a FSM, a voltage comparator, and the inclusion of a capacitor bank represented by C_V; FSM and voltage comparator were implemented using Verilog-AMS language. In general, the error is usually periodic and systematic. The idea is to modify the total LSB bank capacitance so that calibration capacitors add extra charge to improve the ratio of ladder steps. When the calibration circuit is added the split capacitor must be re-structured as a series-parallel arrangement of unit capacitors (a unitary capacitor connects in parallel with two unitary capacitors connected in series).

To decide the connection of the calibration capacitors, which is represented by a digital word that controls the switches of calibration bank, it is necessary to find the voltage associated with the parasitic capacitance of the split capacitor. The procedure begins with the connection of the first six branches of the DACp and the seventh branch of DACn to V_{ref} (reference voltage); others capacitors are connected to ground. Then, voltage comparator compares the output of both banks. A counter modifies the calibration circuit of the DACp (C_{Vp}) based on the comparator output. Convergence is achieved when the comparator enters in a meta-stable region i. e. when its output changes continuously from 0 to 1 and vice-versa each clock cycle. Calibration algorithm is based on the work titled "Digital-Domain Calibration of Split-Capacitor DAC with no Extra Calibration DAC for a Differential-Type SAR ADC" [7].

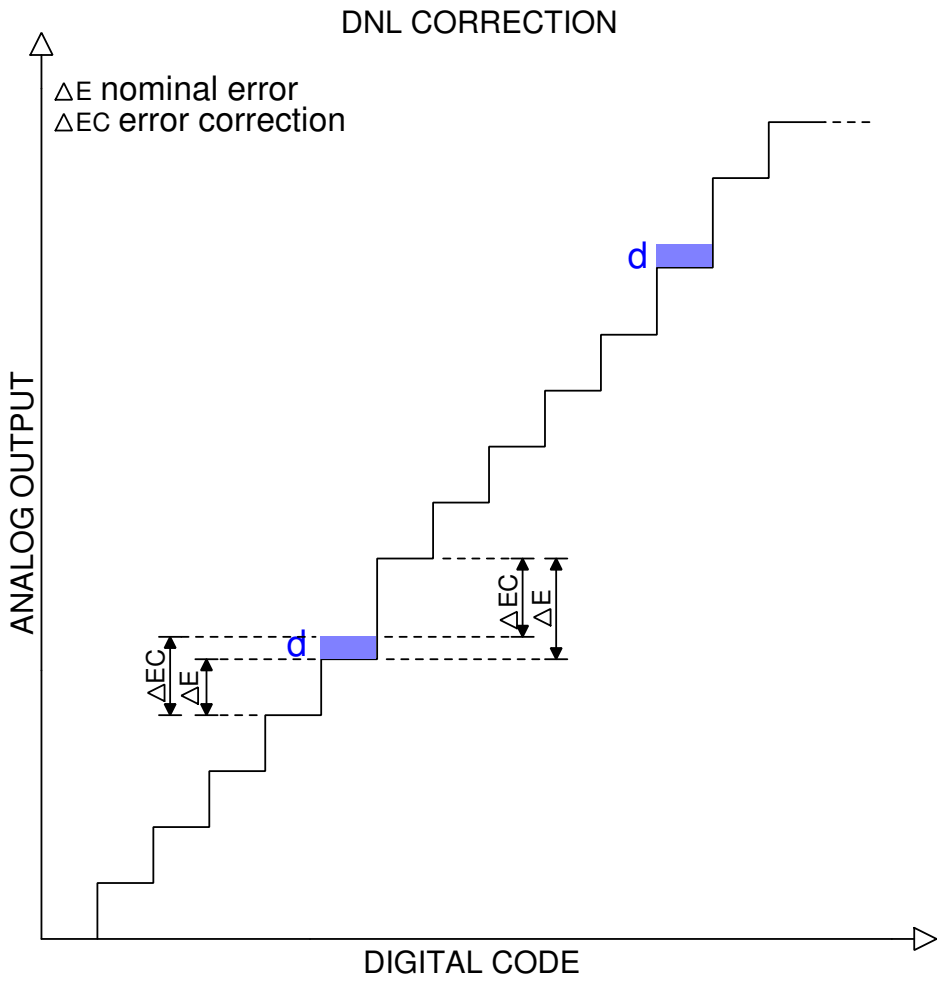
The solid line is the characteristic ladder shape with periodic DNL error, the dotted line is the expected shape after correction, and d is the tension level represented by a digital word needed in each discontinuity to generate the new ladder. It is observed that the calibration consists of modifying a discontinuity by generating an "error distribution", in other words, to decrease the DNL in the identified discontinuity by increasing the error in the previous step

Figure 5: Block calibration scheme.



(Fig. 6), The previous procedure is repeated as many times as discontinuities appear in the ladder, keeping the same number of steps between them fulfilling a pattern. The maximum contribution is when all capacitors refers to Vreff; Therefore, if the discontinuity of the ladder requires a higher voltage to the one provided by the calibration bank, this case will not be successful.

Figure 6: Characteristic ladder with and without DNL correction.



Chapter 3
SIMULATION RESULTS

3.1 Layout

Strategies of common centroid were used in addition to dummy capacitors and interdigitated of components to reduce the presence of parasites effects. Taking into account the above, a distribution of layout of capacitors array was proposed (Fig. 7).

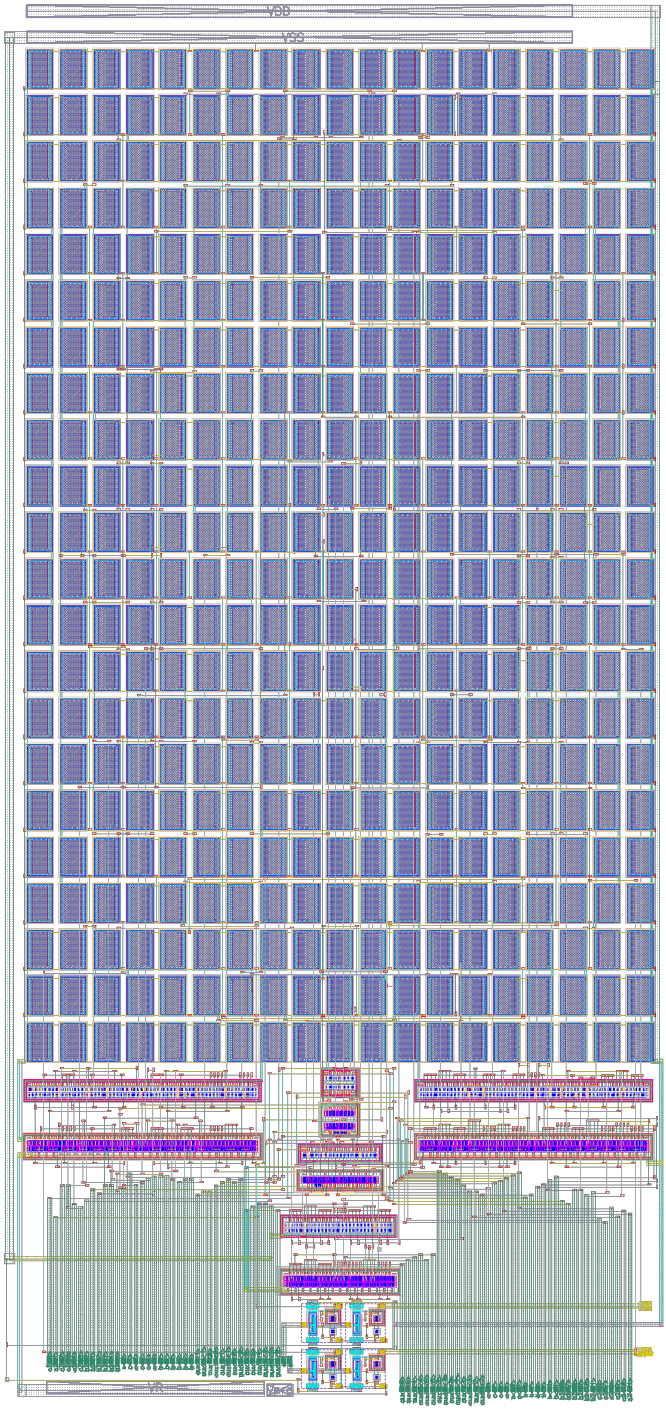
The bank is surrounded by dummy capacitors because ending elements have different boundary conditions to the inner elements. The distribution is not completely common centroid or totally interdigitated due to the difficulty and extension of the routing, so it was decided to make groups of capacitors and interdigitated them as best as possible. The transistors are also interdigitated to reduce mismatch, and guard rings are put in place to avoid latch-up that might exist.

The layout has 0.0544 mm^2 (160 μm x 340 μm), power pins, reference voltage pin, two independent connection for each switch (seventy-seven input pins by control of switches), two pre-charge pins, enable pins, differential output and four capacitors arrays with connection symmetry. Its tracks are as far away as possible to its nearby routes, and its parallel routes have at less a 1 μm among them to avoid parasitic capacitances. Metal from 1 to 5 were used. The metal 5 was necessary to connect the transistor with its respective capacitor. This was the only metal that could pass through the capacitors to create direct routes without greatly affecting them. A useful strategy for reducing parasitic capacitances is to make short routes with the least possible deviations and check the type of metal surrounding them to avoid capacitances by parallel plates. The unit capacitor has an area of 66.66 μm^2 (9,92x6.72 μm), 8 fingers with 280 nm in length and 320 nm of width and metals from 1 to 4. Each switch has an n-type transistor and a p-type transistor with equal dimensions (W = 900 nm and L = 360 nm).

Figure 7: Interdigitated capacitors banks distribution with ring of dummy capacitors (it is only half distribution because it has complete symmetry, and each color represents a capacitor).

D	D	D	D	D	D	D	D	D	D
CC8A	CC2A	CC8A	CCQA	D	D	D	D	D	D
CC1A	CC8A	CCMA	CC8A	CCQA	D	D	D	D	D
CL32B	CM32B	CM32B	CC4	CC4	CC8A	D	D	D	D
CM32B	CM32B	CM32B	CM32A	CM32A	CM32B	CM32B	CM32A	D	D
CL16A	CL16A	CL16A	CM32A	CM32A	CM32B	CM32B	CM32A	D	D
CM16A	CL16A	CL16A	CM16A	CM16A	CM32A	CM32A	CM32B	D	D
CM8A	CM8A	CM8A	CM16A	CM16A	CM32A	CM32A	CM32B	D	D
CL8A	CM8A	CM4B	CM8A	CM32B	CM32B	CM16A	CM16A	D	D
CL1B	CM2A	CM4A	CM8A	CM32B	CM32B	CM16A	CM16A	D	D
CL1A	CM2A	CM4B	CM8A	CM16A	CM16A	CM32B	CM32A	CM32B	D
CS1B	CS2A	CM4A	CM8A	CM16A	CM32B	CM32A	CM32B	CM32A	D
CS1A	CS2B	CM4B	CM8B	CM16B	CM32A	CM32B	CM32A	CM32B	D
CM1A	CM2B	CM4A	CM8B	CM16B	CM16B	CM32A	CM32B	CM32A	D
CM1B	CM2B	CM4B	CM8B	CM32A	CM32A	CM16B	CM16B	D	D
CL8B	CM8B	CM4A	CM8B	CM32A	CM32A	CM16B	CM16B	D	D
CM8B	CM8B	CM8B	CM16B	CM16B	CM32B	CM32B	CM32A	D	D
CM16B	CL16B	CL16B	CM16B	CM16B	CM32B	CM32B	CM32A	D	D
CL16B	CL16B	CL16B	CM32B	CM32B	CM32A	CM32A	CM32B	D	D
CL32A	CM32A	CM32A	CM32B	CM32B	CM32A	CM32A	CM32B	D	D
CM32A	CM32A	CM32A	CC4	CC4	CC8B	D	D	D	D
CC1B	CC8B	CCMB	CC8B	CCQB	D	D	D	D	D
CC8B	CC2B	CC8B	CCQB	D	D	D	D	D	D
D	D	D	D	D	D	D	D	D	D

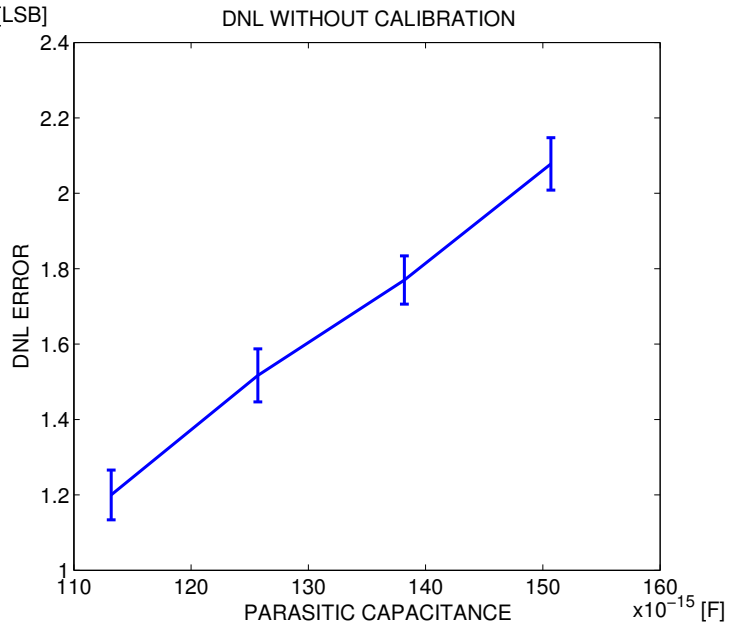
Figure 8: Differential CDAC layout in 180 nm in CMOS technology with MOM capacitors.



3.2 Calibration

Discontinuities are observed in the transfer ladder generate DNL error; therefore, the calibration is used to cause a similar to the one in Fig. 6. The variations of corners are presented and confirm that the calibration continues in operation under any specification of temperature (-40°C, 50°C, 125°C), supply voltage ($V_{DD} \pm 10\%$ [V]) and process variations (slow and fast).Also, it was observed that during the simulations of the calibration, 650 [ns] was the minimum duration to get a digital word.

Figure 9: DNL error associated with C_{P1} variation.



The Fig. 9 shows the DNL behavior of the DAC under no calibration with previous mentioned corners parameters. The error increases with an almost linear behavior and a constant homogeneity.

The Fig. 10 evidences deviations increase and problems in the DNL error correction with values of C_{P1} greater than 150 fF. However, this problem is improved by modifying the way of obtaining the digital word to move the working range of the calibration as Fig. 11. Consequently, when we try to calibrate values outside the range, it will have inefficient results.

Figure 10: DNL error associated with C_{P1} variation and using the DAC calibration with proposal digital word.

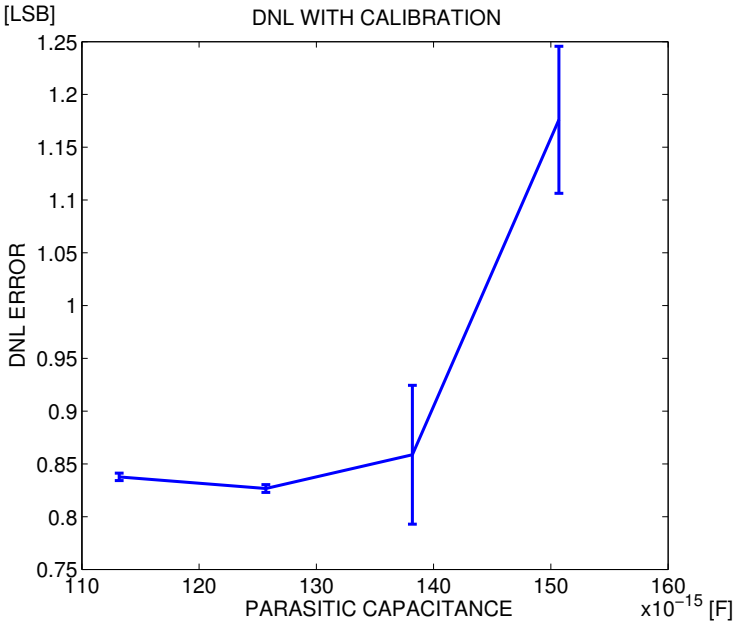
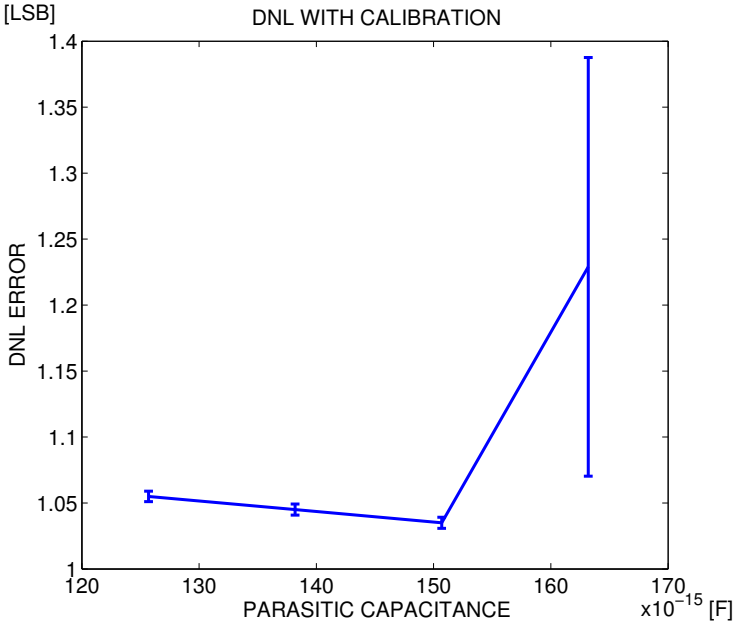


Figure 11: DNL error associated with C_{P1} variation and using the DAC calibration with second proposal digital word.



Chapter 4
POST-LATYOUT RESULTS

In the layout section, some of the steps necessary to achieve the design of a capacitive DAC were presented. A calibration was also shown for the purpose of correcting DNL error. Now, the specifications obtained are presented and compared with the proposed ones (Table 1).

Table 1: Comparative table

Specification	**Proposed**	**Obtained**	**Design [8]**	**Design [9]**	**Design [5]**
Technology	0.18μm	0.18μm	0.35μm	0.90μm	0.18μm
Resolution	12-b	12-b	10-b	10-b	8-b
Supply voltage	1.2 V	1.2 V	-	1.2 V	1.8 V
Frequency	10 MHz	10 MHz	40 MHz	50 MHz	20 MHz
INL	<1 LSB	0.062 LSB	0.74 LSB	0.86 LSB	0.56 LSB
DNL	<1 LSB	0.92 LSB	0.74 LSB	0.86 LSB	0.02 LSB

According to results showed in Fig. 13 the nominal maximum error associated to the circuit is 1.753 LSB. After the calibration, the final DNL is 0.92 LSB (Fig. 14), this result confirms the correct operation of the planted calibration in the previous pre-layout simulations. According to the Fig. 12 the INL error value is quite favorable, this due to the homogeneous distribution of the DNL error. It is important to mention that during the simulation process the DAC showed positive and periodic errors, for that reason, the calibration was adapted only to correct DNL errors with these characteristics. However, the calibration can be improved with the inclusion of a counter that takes a second period into account and by manipulating the digital word to improve the negative error present in Figs. 13 and 14.

Figure 12: Post-Layout INL error (f=10 MHz).

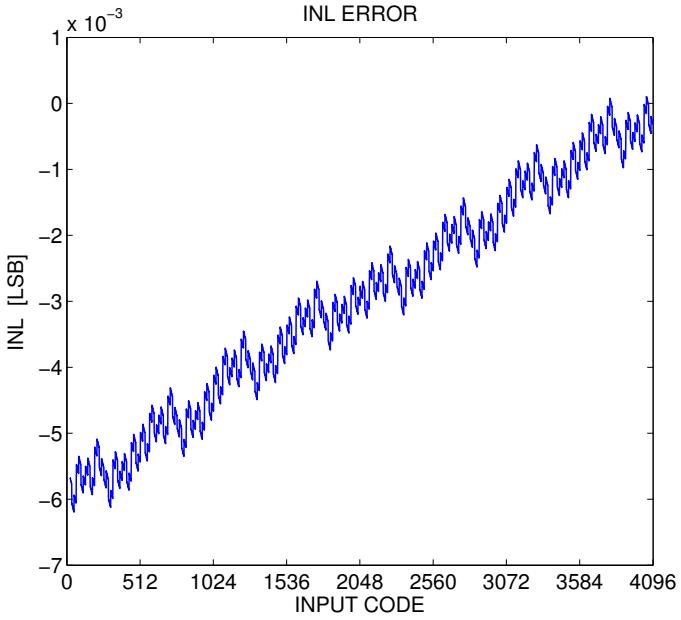


Figure 13: Post-Layout DNL error (f=10 MHz).

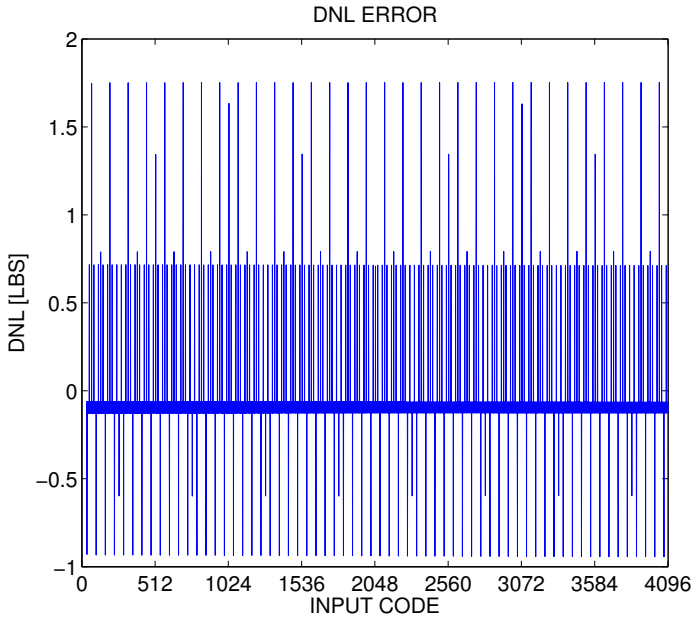
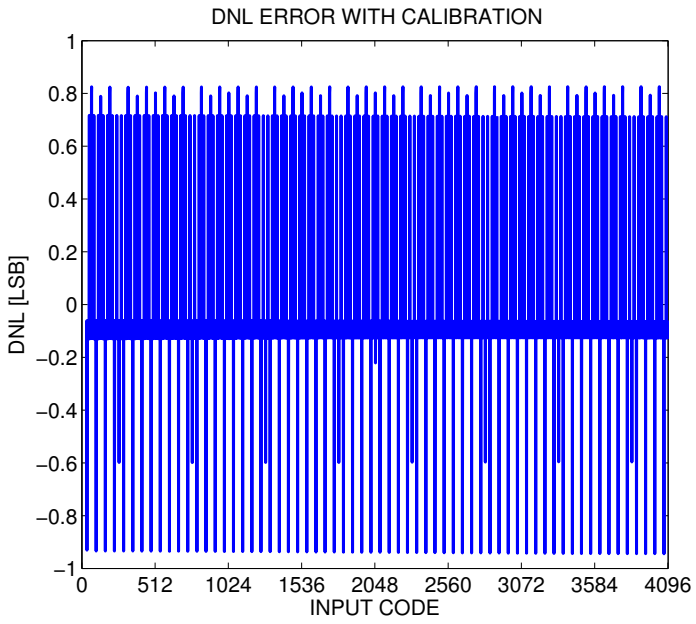


Figure 14: Post-Layout DNL error with calibration implemented (f=10 MHz).



Chapter 5
CONCLUSIONS

A 12-bit digital-to-analog converter was designed in a standard CMOS 180nm technology, which can operate at up 10MHz. A calibration block was included to mitigate the impact of parasitic capacitance on linearity. Calibration range can be adjusted by including a larger calibration bank at a cost o an increment in area an switching power. Moreover, calibration range can be displaced by means of including and offset digital word. Therefore, a double calibration or a dynamic calibration (moving the working range as necessary) could be proposed for a future design. Post-layout simulations shows a final DNL and INL of maximum 0.92 and 0.006 respectively including PVT corners. A differential architecture reduces the effects of non-linearity due to the overlapping at its outputs. Layout design has to be done carefully because parasitic capacitance could also add offset and degrade gain.

Chapter 6
RECOMMENDATIONS FOR FUTURE PROJECTS

- The layout design should be done carefully and be as symmetrical as possible to avoid stray capacitance adding compensation and degrading the gain.
- Capacitors should be made in square form to reduce parasitic capacitances.
- The state machine used for calibration can be reduced in its number of states.

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