DESING OF BASE-BAND CIRCUITS FOR A PWM CONTROLLER IN A DC-DC BUCK CONVERTER IN CMOS TECHNOLOGY

OVER JOSE AMAYA AMAYA
VICTOR HUGO MUÑOZ LOPEZ

UNIVERSIDAD INDUSTRIAL DE SANTANDER
FACULTAD DE INGENIERÍAS FISICOMECÁNICAS
ESCUELA DE INGENIERÍA ELÉCTRICA, ELECTRÓNICA Y DE TELECOMUNICACIONES
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2024

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OVER JOSÉ AMAYA AMAYA
VÍCTOR HUGO MUÑOZ LÓPEZ

Degree work presented as a requirement to qualify for the title of Electronic Engineer

Advisor:
JAVIER FERNEY ARDILA OCHOA
PhD

UNIVERSIDAD INDUSTRIAL DE SANTANDER
FACULTAD DE INGENIERÍAS FISICOMECÁNICAS
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2024

Dedicated to our families and friends.

And to our team, with whom we started and finished this amazing journey.

ACKNOWLEDGMENTS

I would like to express my most sincere gratitude to all the people who have been a fundamental part of this academic and formative journey. First of all, I am deeply grateful to my parents, Lucia and Obedely, for instilling in me the values that guide my life and for their constant support. I also thank myself for never giving up, for always giving my best and for firmly believing that this goal was achievable.

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- Over José Amaya Amaya

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- Víctor Hugo Muñoz López

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RESUMEN

TÍTULO: DISEÑO DE CIRCUITOS DE BANDA BASE PARA UN CONTROLADOR PWM EN UN CONVERTIDOR BUCK DC-DC EN TECNOLOGÍA CMOS [*]

AUTORES: OVER JÓSE AMAYA AMAYA
VÍCTOR HUGO MUÑOZ LÓPEZ [**]

PALABRAS CLAVE: PWM Controller, CMOS, DC-DC Buck Converter, Ramp Generator, Frequency Variation Analysis, Efficiency.

DESCRIPCIÓN:

Este trabajo aborda el diseño de un circuito PWM analógico para un convertidor Buck DC-DC, realizado por el grupo de investigación OnChip. El grupo está trabajando en un nuevo microcontrolador en tecnología CMOS de 28 nm, donde la eficiencia energética es esencial para el rendimiento del sistema en chip (SoC). Se realizó la implementación de un circuito PWM a 2 MHz con una topología del generador de rampa diferente a la convencional, esta implementación se basa en una idea del estado del arte, pero se eligió una solución más simple. Esta topología mejora la precisión tanto en frecuencia como en amplitud, manteniendo un bajo consumo de potencia. Además, se introduce una metodología basada en un presupuesto de error para la frecuencia de conmutación y técnicas de trimming, lo que garantiza una alta robustez frente a variaciones PVT y MC. Los resultados de simulación muestran una variación de menos de $\pm$5.2% sobre la frecuencia en PVT y un consumo de corriente de 114 µA, con un rango de [3.8%-98%] ciclo de trabajo. Las pruebas estadísticas revelan una variación 3σ de menos de $\pm$4.5% en la frecuencia de conmutación. El impacto de esta investigación podría ser significativo para futuros proyectos del grupo OnChip, mejorando la eficiencia y optimizando la gestión de potencia en sistemas integrados.

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[*] Trabajo de Grado

[**] Facultad de Ingenierías Físico-Mecánicas. Escuela de Ingenierías Eléctrica, Electrónica y de Telecomunicaciones. Director: JAVIER FERNEY ARDILA OCHOA

ABSTRACT

TITLE: DESING OF BASE-BAND CIRCUITS FOR A PWM CONTROLLER IN A DC-DC BUCK CONVERTER IN 28NM CMOS TECHNOLOGY [*]

AUTHORS: OVER JÓSE AMAYA AMAYA
VÍCTOR HUGO MUÑOZ LÓPEZ [**]

KEYWORDS: PWM Controller, CMOS, DC-DC Buck Converter, Ramp Generator, Frequency Variation Analysis, Efficiency.

DESCRIPTION:

This work addresses the design of an analog PWM circuit for a DC-DC buck converter, performed by the OnChip research group. The group is working on a new microcontroller in 28 nm CMOS technology, where power efficiency is essential for system-on-chip (SoC) performance. The implementation of a PWM circuit at 2 MHz with a ramp generator topology different from the conventional one was performed, this implementation is based on an idea of the state of the art, but a simpler solution was chosen. This topology improves both frequency and amplitude accuracy while maintaining low power consumption. In addition, a methodology based on an error budget for the switching frequency and trimming techniques is introduced, which ensures high robustness against PVT and MC variations. Simulation results show a variation of less than $\pm$5.2% over frequency at PVT and a current consumption of 114 µA, with a range of [3.8%-98%] duty cycle. Statistical tests reveal a 3σ variation of less than $\pm$4.5% at the switching frequency. The impact of this research could be significant for future OnChip group projects, improving efficiency and optimizing power management in embedded systems.

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[*] BSc Thesis

[**] Facultad de Ingenierías Físico-Mecánicas. Escuela de Ingenierías Eléctrica, Electrónica y de Telecomunicaciones. Advisor: JAVIER FERNEY ARDILA OCHOA

INTRODUCTION

Efficient power management is crucial in modern electronic devices, especially in System on-Chip (SoC) devices, composed of multiple circuit blocks requiring different voltage levels. DC-DC converters are employed to adjust voltage levels efficiently to meet these demands. These converters require precise feedback control systems to maintain consistent voltage output, ensuring energy efficiency and performance. In voltage mode feedback control, the PWM modulator regulates the output voltage and maintains high efficiency. It adjusts the duty cycle to compensate for load or input voltage variations, ensuring a stable output. This project focuses on the design of the PWM circuit.

A constant-frequency PWM circuit design requires a comparator and a sawtooth ramp generator, which regulates both frequency and duty cycle. Conventional topologies for ramp generators often suffer from higher frequency errors and increased power consumption as in [1]. To address this, Implementation is based on [2], idea that improves control over ramp frequency and amplitude errors while reducing power consumption. Additionally, an error budget for the ramp frequency is created to minimize these errors by applying trimming techniques and defining the specifications of the blocks that make up the PWM circuit.

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[1] Cheung Fai LEE and P.K.T. MOK. "A monolithic current-mode CMOS DC-DC converter with on-chip current-sensing technique". In: *IEEE Journal of Solid-State Circuits* 39.1 (2004), pp. 3–14. DOI: 10.1109/JSSC.2003.820870.

[2] H. FORGHANI-ZADEH and Gabriel RINCÓN-MORA. "Low-Power CMOS Ramp Generator Circuit for DC-DC Converters". In: *J. Low Power Electronics* 2 (Dec. 2006), pp. 437–441. DOI: 10.1166/jolpe.2006.084.

The ramp frequency must remain robust against variations in process, voltage, and temperature (PVT), as well as Monte Carlo (MC) simulations, with a tolerance of $\pm$10%. Simulations show a frequency variation of less than ±5.2% under PVT conditions, statistical tests reveal a 3σ variation of less than ±4.5% in the switching frequency, a current consumption of 114 µA. The flow of this work begins with a general introduction, followed by a detailed analysis of the error that can be generated in the frequency of the circuit. Subsequently, the design methodology used is presented, ending with the results obtained in the design.

OBJECTIVES

0.1. General Objectives

- To design an efficient PWM controller for a DC-DC buck converter in CMOS Technology node.

0.2. Specific Objectives

- To investigate PWM control circuits and techniques in DCDC buck converters.
- To design and simulate an efficient PWM controller using standard CMOS technology.
- To validate the design through PVT and Monte Carlo simulations.

1. PROJECT OVERVIEW

The project focuses on power management in microelectronics, particularly in analog design and efficient operation of integrated systems. Minimizing power consumption is critical for modern devices, so the OnChip research group aims to develop a Power Management Unit (PMU) that optimally controls power distribution in the System-on-Chip (SoC) under development. A key element is the DC-DC converter, where the PWM controller plays a vital role in ensuring energy efficiency and precise output voltage regulation. Key considerations in this project include efficiency, precision, PWM frequency, duty cycle, PVT and MC variations, and size and cost.

1.1. DC-DC Buck Converter

A DC-DC buck converter converts the input DC voltage to a lower-magnitude DC output voltage with high efficiency using switches, inductors, and non-dissipative capacitors (Figure 1.1). This allows for the desired output voltage to be obtained, which invariably requires control to produce a well-regulated output voltage in the presence of variations in the input voltage and the load current of the converter.

1.2. Pulse Width Modulator

The PWM modulator is the central circuit in the voltage mode feedback control of a DC-DC converter. In this system, the converter adjusts the duty cycle of the modulator in response to variations in load or line conditions, gradually modifying the duty cycle to maintain a constant output voltage in the converter. A pulse-width modulated signal can be constructed by comparing a control signal V_{ctrl} with a sawtooth carrier signal

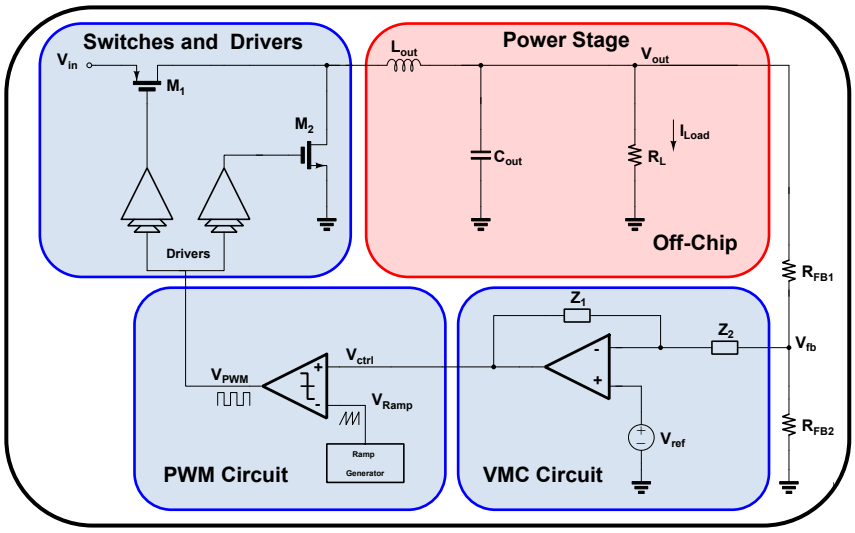

Figure 1.1. DC-DC Buck Converter.

V_{Ramp} [3]. As shown in the Figure 1.2(a) control or modulating signal modulates the pulse width based on the carrier signal. Additionally, the modulated signal will have the frequency of the carrier. The result of the duty cycle depends on V_{ctrl} and V_m which is the amplitude of the ramp signal as shown in (1).

$$D = \frac{V_{ctrl}}{V_m} \tag{1}$$

This is why the ramp generator circuit is particularly critical for controlling the frequency and duty cycle of pulse-width modulated (PWM) switching supplies. In the figure 1.2(b), a graphical representation can be observed when the control signal is at 50% of the ramp signal's amplitude, resulting in a signal modulated at 50%.

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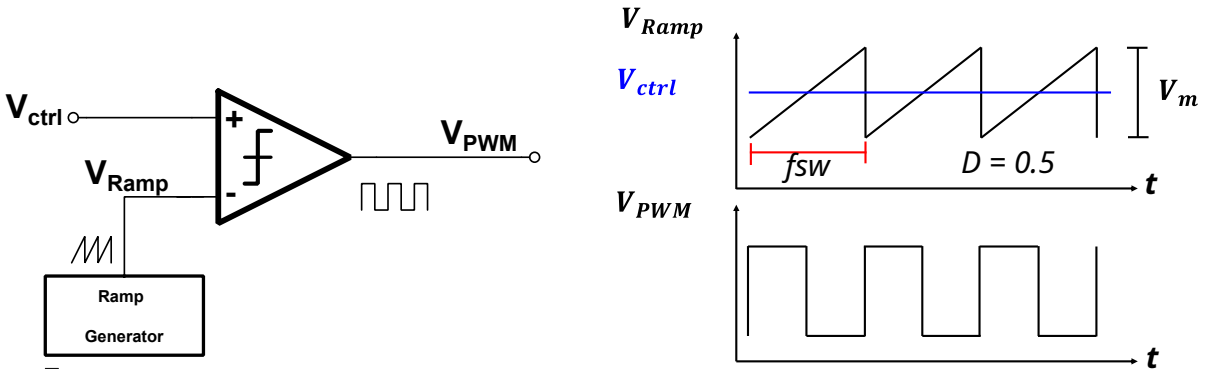
[3] Luigi Iannelli FRANCESCO VASCA. *Dynamics and Control of Switched Electronic Systems*. Prentice Hall, 2012.



(a) PWM Circuit. (b) PWM Signal.

Figure 1.2. PWM Circuit and PWM Signal.

1.3. PWM Circuit Topology

Pulse-width modulation can take different forms [4]. Pulse frequency is one of the most important parameters when defining a PWM method, and it can be either constant or variable. A constant-frequency (CF) PWM signal can be produced simply by comparing a reference signal, r(t), with a carrier signal, c(t). The binary PWM output can be mathematically written as:

$$b_{PWM} = sgn[r(t) - c(t)] \tag{2}$$

Three types of carrier signals are commonly used in constant-frequency PWM [3].

1.3.1. Sawtooth Carrier The leading (rising) edge of PWM output occurs at fixed instants in time while the position of the trailing (falling) edge is modulated as the reference signal level varies (Figure 1.3). Hence the method is also called constant-frequency trailing-edge modulation.

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[4] H.S. BLACK. *Modulation Theory*. Van Nostrand Reinhold, New York, 1953.

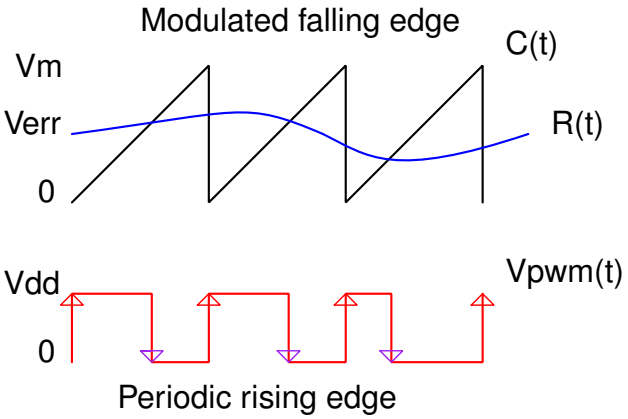

Figure 1.3. Constant-frequency trailing-edge modulation.

1.3.2. Inverted Sawtooth Carrier The trailing (falling) edge of PWM output occurs at fixed instants in time while the position of the leading (rising) edge is modulated as the reference signal level varies (Figure 1.4). The method is usually referred to as constant-frequency leading-edge modulation.

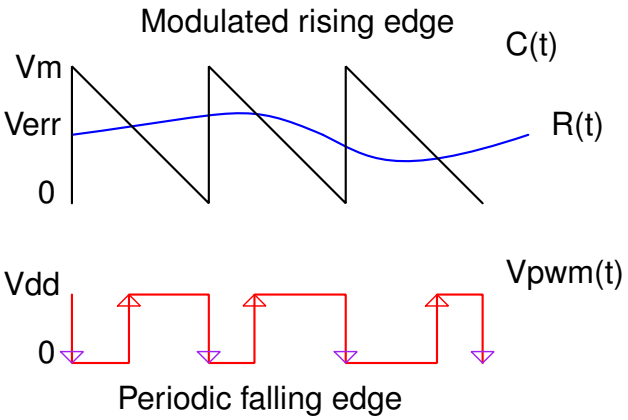

Figure 1.4. Constant-frequency leading-edge modulation.

1.3.3. Triangle Carrier Both the leading edge and the trailing edge of the PWM output is modulated. The rising and falling edge of the triangle are usually symmetric so that the pulse is centred within a carrier cycle when the reference is a constant

(Figure 1.5). The method is called constant-frequency double-edge modulation.

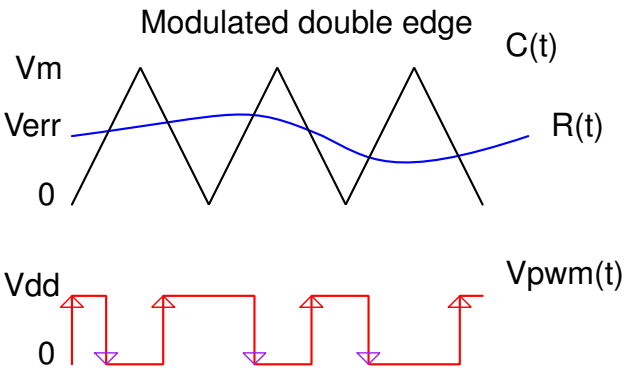

Figure 1.5. Constant-frequency double-edge modulation.

Trailing-edge modulation is most common in DC–DC converters [3]. Double-edge modulation eliminates certain harmonics when the reference is a sine wave and is a preferred method for AC–DC and DC-AC converters where the PWM reference contains a sinusoidal component [3].

In [5] proposes a general frequency-domain model to reflect the effect of trailing-edge and leading edge carrier on the stability of the pulse width modulation (PWM) dc–dc converter.

Based on the results of this model (Figure 1.6) [5] and since it is the most commonly used in the literature for DC-DC converters, the trailing-edge carrier has been chosen. The basic principle of the ramp generator is the charging and discharging of a capacitor employing a current source, using a switch controlled by a clock signal to reset the ramp voltage to ground (see Figure 1.7). Where the amplitude of the ramp signal is given by (3).

Understanding the basic operation of the ramp generator, it can be implemented us-

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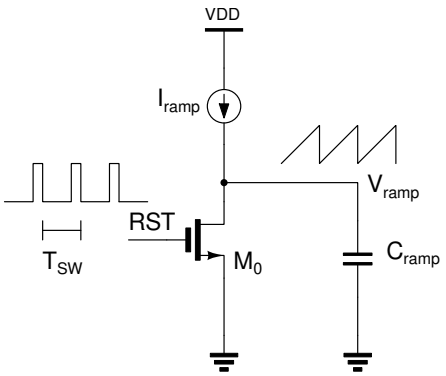
[5] Yuan CHEN et al. “A General Frequency-Domain Model of Trailing-Edge and Leading-Edge Carrier PWM dc–dc Converter Based on Hybrid Continuous and Discrete-Time Descriptions”. In: *IEEE Journal of Emerging and Selected Topics in Power Electronics* 9.4 (2021), pp. 4175–4187. DOI: 10.1109/JESTPE.2020.2982179.

TABLE V
RESULTS OF VERIFICATION

Model	Trailing-edge carrier				Leading-edge carrier			
	Boost	Buck	Buck-Boost	Sepic	Boost	Buck	Buck-Boost	Sepic
SSA	Stable	Stable	Stable	Stable	Unstable	Stable	Unstable	Unstable
DAM	Stable	Stable	Stable	Stable	Unstable	Stable	Unstable	Unstable
DTM	Stable	Unstable	Stable	——	Unstable	Unstable	Unstable	——
Proposed	Unstable	Stable	Unstable	Unstable	Stable	Stable	Stable	Stable
Exact	Unstable	Stable	Unstable	Unstable	Stable	Stable	Stable	Stable

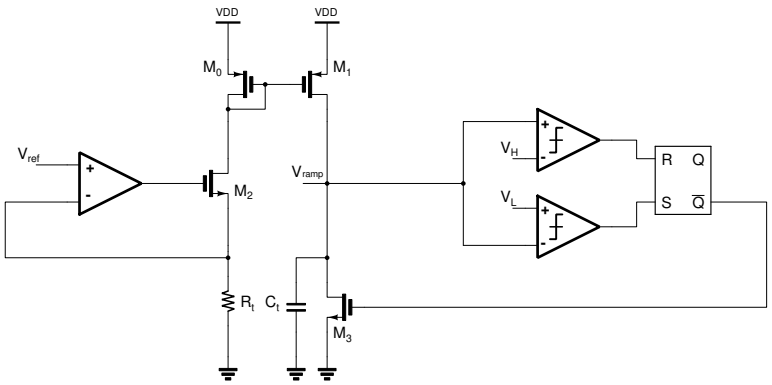
Figure 1.6. Stability of the different converters, for the different modulations.



$$V_m = \frac{I_{ramp}}{C_{ramp} F_{SW}} \tag{3}$$

Figure 1.7. Basic principle of the ramp generation.

ing a voltage-to-current converter that generates a current mirrored by a PMOS current mirror to charge a capacitor. Additionally, an oscillator circuit comprising a window comparator and an SR latch circuit generates a sawtooth signal periodically. This topology is widely employed in the literature (Figure 1.8). [1], Thus, the oscillation frequency of the ramp generator is given by (4).



$$f = \frac{V_{ref}}{R_t C_t (V_H - V_L)} \tag{4}$$

Figure 1.8. Conventional Ramp Generator.

The ramp generator circuit can also be implemented by replacing the oscillation circuit in the conventional topology with a Schmitt Trigger comparator and an inverter to generate the oscillation signal (Figure 1.9), [6]. The Schmitt Trigger Circuit helps generate clean pulses from noisy input signals or designing oscillator circuits. It is like the Inverter Voltage Transfer Characteristic except that it has faster transition regions and hysteresis, this hysteresis is defined by a low and high transission voltage in which when the input exceeds the voltage V_{SPH}, the output switches to a logic zero and holds this value until the input does not fall below V_{SPL}; when this occurs, the output will switch to a logic one and hold until it again exceeds the voltage V_{SPH}. As in the conventional ramp circuit, the ramp frequency will now be defined by the V_{SPH} and V_{SPL} limits of the Schmitt Trigger comparator. Where the oscillation frequency of the ramp generator is given by (5).

Since the frequency strongly depends on these transition voltages, it can vary considerably due to PVT variations. This is why the conventional topology was chosen. It allows for better control of frequency errors and offers greater flexibility in design by allowing the selection of reference voltages.

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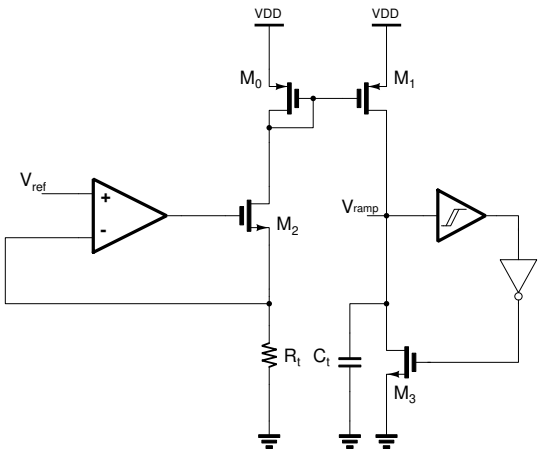
[6] Min-Chin LEE and Yi-Chiuan CHEN. “Implementation of a ramp generator with Schmitt trigger circuit for PWM modulator applications”. In: (2017), pp. 2176–2182. DOI: 10.1109/PIERS-FALL.2017.8293500.

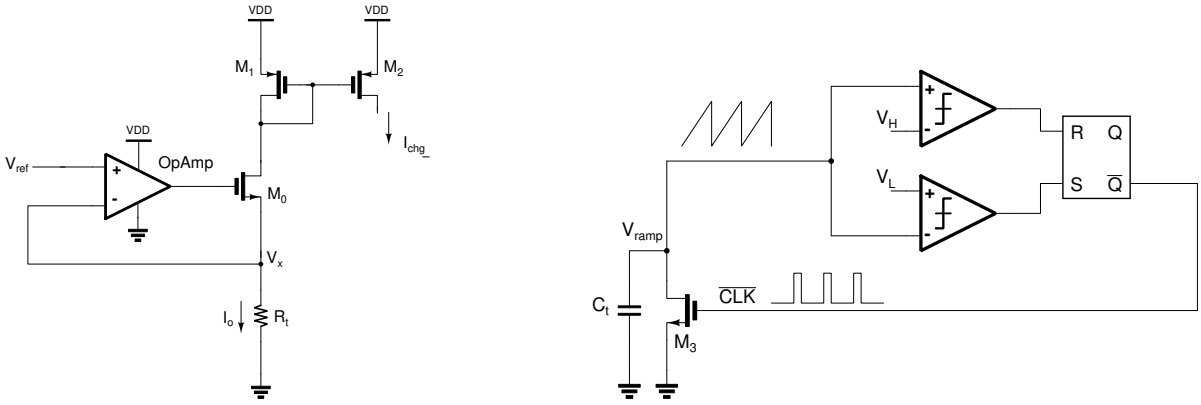


$$f = \frac{V_{ref}}{R_t C_t (V_{SPH} - V_{SPL})} \tag{5}$$

Figure 1.9. Schmitt Trigger Ramp Generator.

The chosen topology can be divided into two fundamental parts: the voltage-to-current converter circuit and the oscillator circuit, as shown in Figure 1.10. The voltage-to-current converter circuit consists of an OpAmp, a transistor in common drain configuration, a resistor, and a P-MOS current mirror (Figure 1.10(a)). The main function of this circuit is to produce a constant current I_o, which is then copied by the P-MOS current mirror to charge the capacitor C_t. The oscillator circuit consists of two static comparators and an SR latch, which causes the ramp to oscillate at a fixed frequency between V_L and V_H. The SR latch generates a clock signal that periodically resets the ramp sequence (Figure 1.10(b)).

The SR Latch circuit governs the ramp sequence, starting with an uncharged capacitor and a V_{ramp} of zero Volts. As V_{ramp} rises, the circuit allows the capacitor to charge until it exceeds the reference voltage V_H, at which point the clock signals switch, causing rapid discharge of the capacitor. The process repeats as V_{ramp} oscillates between V_L and V_H. However, comparator delays introduce errors in the ramp limits(Figure 1.11), these errors in the upper(V_{errH}) and lower(V_{errL}) voltages of the ramp signal depend on the delay of the comparator and the slope of the charging or discharging process (As shown in (6)), whether it is in the upper voltage during charging or the lower voltage during discharging, making it essential to identify the critical delay path (Figure 1.12)



(a) Voltage to Current Converter. (b) Oscillator Circuit.

Figure 1.10. Fundamental parts of the ramp generator.

to minimize these errors. Since the ramp's discharge slope is much steeper than its charging slope, the error voltage produced by the product of this discharge slope with the delay of $cmpL$ identifies the critical delay path, which is shown in red. To minimize these errors, it is necessary to design comparators with low delay and high gain, ensuring that these comparators have good sensitivity in the comparison.

$$V_{\text{errH}} = \left(\frac{dV_{\text{rise}}}{dt}\right) t_{dH} \qquad V_{\text{errL}} = \left(\frac{dV_{\text{fall}}}{dt}\right) t_{dL} \tag{6}$$

Due to this, it became necessary to conduct an in-depth analysis of this issue.

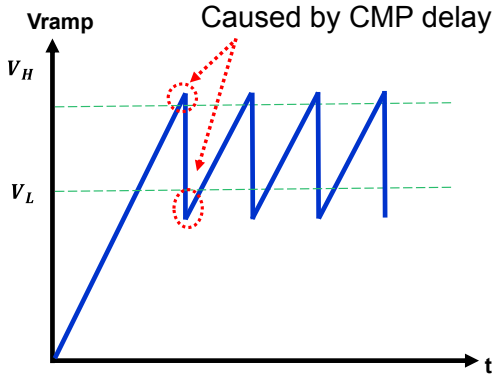


Figure 1.11. Delay Errors.

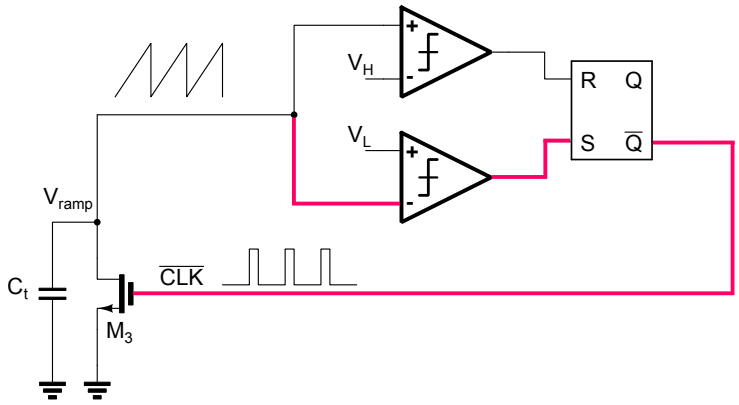


Figure 1.12. Critical delay path.

The conventional ramp generator circuit (Figure 1.13) operates on the basic principle of periodically charging (with a fixed current source) and discharging (directly to ground) a capacitor. This is achieved using an oscillator circuit composed of two comparators and an SR latch circuit, which causes the ramp to oscillate from a voltage V_L to a voltage V_H. The SR latch generates a clock signal that resets the ramp at each oscillation period. Ideally, the oscillation frequency of the ramp is given by:

$$f = \frac{V_{ref}}{R_t C_t (V_H - V_L)} \tag{7}$$

However, due to the delay time of the comparators, an error voltage is generated in the ramp amplitude, which affects the ramp frequency as follows (8).

$$f = \frac{V_{ref}}{R_t C_t [V_H + V_{errH} - (V_L - V_{errL})]} \tag{8}$$

Where these error voltages are given by the charging and discharging slopes, respectively, and by the comparator delays, given by equation (6).

Due to the fact that ideally the discharge slope of the ramp is very steep (since it discharges directly to ground), the error voltage V_{errL} can become excessively large, thereby affecting the oscillation frequency of the ramp. To reduce this error voltage,

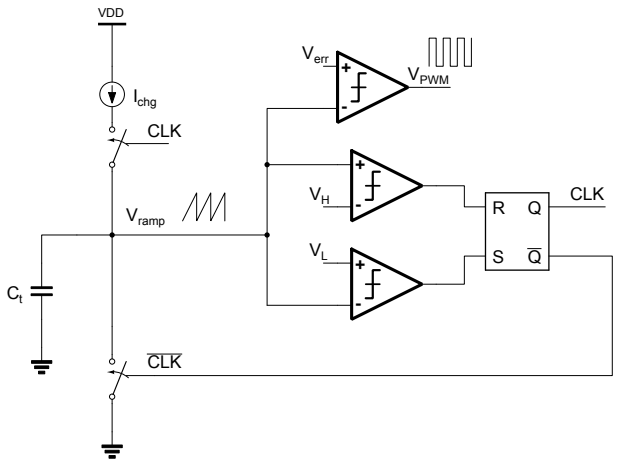


Figure 1.13. Conventional ramp-generator circuit.

it is necessary to significantly sacrifice the power consumption in the comparators in order to considerably reduce the comparator delay and thus decrease the error voltage. This increases the overall power consumption in the PWM circuit, making it an unviable solution for this problem.

Therefore, the ramp generator circuit proposed in [2] was implemented, which changes the capacitor discharge method to a current source 9 times greater than the discharge current, rather than discharging directly to ground. This provides better control of the error voltages produced by the comparator delays without increasing power consumption. This proposed circuit can be seen in Figure 1.14.

The error voltages of the proposed circuit still follow the equations (6), with the difference that we now know the charging and discharging slopes of the ramp signal, providing better control over the error voltages.

$$\frac{dV_{\text{rise}}}{dt} = \frac{I_{\text{chg}}}{C_t} \tag{9}$$

$$\frac{dV_{\text{fall}}}{dt} = \frac{I_{\text{Dchg}}}{C_t} = \frac{9I_{\text{chg}}}{C_t} \tag{10}$$

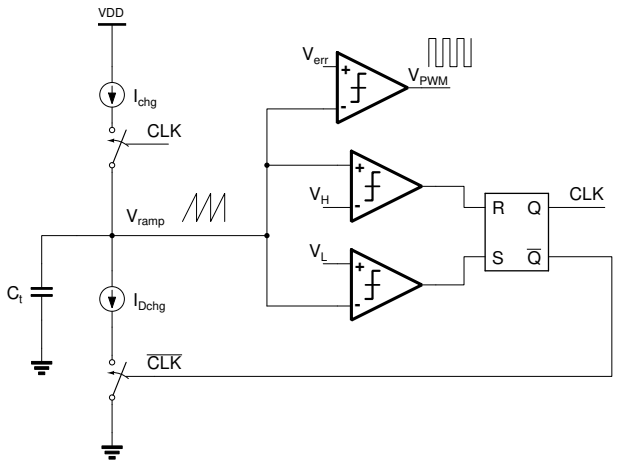


Figure 1.14. Proposed ramp-generator circuit with discharge current source.

Depending on the discharge current relative to the charging current, the discharge slope of the ramp will be either steeper or shallower. Therefore, a value of 90% for the charging period and 10% for the discharge period was used, as it significantly reduces the ramp error voltage while maintaining a sawtooth waveform, preventing it from becoming a triangular signal if the discharge slope is reduced further.
The oscillation frequency for the proposed ramp generator circuit is given by:

$$f_{sw} = \frac{I_{\text{ramp}}}{C_t \left[V_H + V_{\text{errH}} - (V_L - V_{\text{errL}})\right]} \tag{11}$$

$$I_{\text{ramp}} = \frac{1}{\dfrac{1}{I_{\text{chg}}} + \dfrac{1}{I_{\text{Dchg}}}} \tag{12}$$

The ramp oscillation frequency of the implemented topology (Figure 1.15) is given by the following expression:

$$f_{sw} = \frac{0.9 I_{\text{chg}}}{C_t \left(V_H - V_L\right) + I_{\text{chg}} \left(t_{dH} + 9 t_{dL}\right)} \tag{13}$$

A PMOS current mirror was used to replicate the current generated by the voltage-to-

current converter to implement the discharge source. This current is then mirrored using an NMOS current mirror, resulting in a discharge current that is nine times greater. This discharge current is generated by transistor M5, as shown in Figure 1.15.

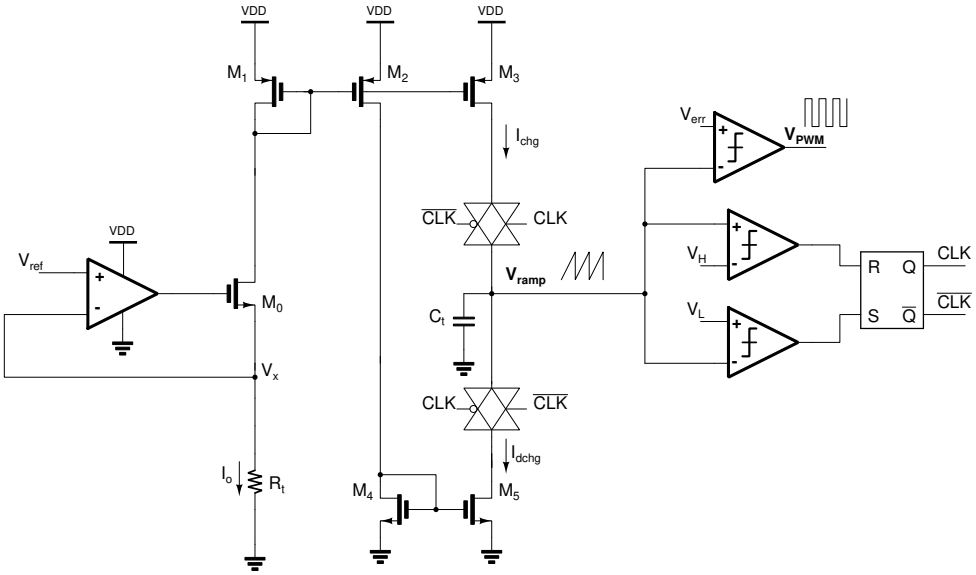


Figure 1.15. Implemented PWM circuit.

2. FREQUENCY VARIATION ANALYSIS

In this section we will make an analysis of the switching frequency, in order to obtain the specifications for each block that make up the PWM, thus obtaining a budget for each variable that affects the frequency.

2.1. Design Specifications

The switching frequency is fundamental in DC-DC converters, as it determines the efficiency and the ripple voltage at the converter's output [7].

Where P_{Loss} is the total loss in the converter, consisting of the sum of conduction losses, losses in the output filter capacitor and inductor, and switching losses, the latter are of particular interest in our project, as they depend on the switching frequency of the DC-DC converter.

$$P_{Loss} = P_{con} + P_{esr} + P_{dcr} + P_{SW} \tag{14}$$

The switching losses are given by [8]:

$$P_{SW} = C_G V_{in}^2 f_{SW} \tag{15}$$

The output voltage ripple in a DC-DC Buck converter is given by:

$$\Delta V_{out} = \frac{(V_{in} - V_{out})D}{16LCf_{SW}^2} \tag{16}$$

This is why the frequency generated by the ramp must tolerate PVT and MC variations, without exceeding a deviation of ±10% from the typical frequency. Therefore, a

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[7] Dragan Maksimović ROBERT W. ERICKSON. *Fundamentals of Power Electronics*. Third Edition. Springer International, 2020.

[8] Wanjin WANG, Rongshan WEI, and Yadong YIN. "Efficiency-based power MOSFETs size optimization method for DC-DC buck converters". In: *2019 20th International Symposium on Power Electronics (Ee)*. 2019, pp. 1–5. DOI: 10.1109/PEE.2019.8923036.

high-precision ramp generator must be designed. For this reason, an analysis of the variations in this frequency was conducted, including an error budget, identifying each independent variable that affects the switching frequency, and reducing its variations to optimal values to meet the specifications outlined in Table **2.1**.

Table 2.1. Design specifications.

Parameter	**Min**	**Typ**	**Max**
V_{DD} [V]	1.62	1.8	1.98
I_{VDD} [uA]	-	-	200
F_{PWM} [MHz]	1.8	2.0	2.2
D [%]	TBD	TBD	TBD
D_{range} [%]	-	TBS	-
V_{ctr} [V]	-	0.8	-
C_L [fF]	-	100	-

2.2. Types Of Errors In The Design

Variability is generally interpreted as a collection of phenomena characterized by uncontrolled parameter variation between individual transistors or components in a circuit; from a statistics point of view, these (time-independent) effects can be subdivided into two classes: **deterministic** and **stochastic** (See Table **2.2**) and in designer's terms: offsets and random mismatch[9]. Deterministic errors can be predicted, either physically. They can occur due to variations in PVT, systematic offsets, etc. stochastic errors are random errors that cannot be predicted in terms of how they will affect our circuit. Examples of random errors include noise or random matching.

[9] M.J.M. PELGROM. *Analog-to-Digital Conversion*. Springer International Publishing, 2022.

Table 2.2. Types of errors.

Deterministic Errors	**Stochastic or Random errors**
Process	Noise(1/f, kT)
Supply voltage	Random Matching
Temperature	Dopant fluctuation
Systematic offsets	Mobility fluctuation

As previously seen, the ramp frequency is affected by the delays of the comparators, as these produce an error voltage that depends on the charging and discharging slopes of the ramp generator and the delay of each comparator. This can be observed in Figure **1.11**. Additionally, the offset referred to the input of the comparators generates an error voltage in the comparison, affecting both the amplitude of the ramp and its frequency. The actual frequency of the ramp generator, considering these errors, is given by:

$$f_{sw} = \frac{0.9 I_{\text{chg}}}{C_t \left(V_H - V_L \pm V_{os}\right) + I_{\text{chg}} \left(t_{dH} + 9 t_{dL}\right)} \tag{17}$$

If we assume the ideal frequency equation **18**, where a charging current and a ramp amplitude are proposed to calculate a capacitor that provides a frequency of 2 MHz, the nominal values are obtained, $I_{chg} = 2\ uA, \quad C_t = 2.25\ pF, \quad V_H = 1\ V, \quad V_L = 0.6\ V$.

$$f_{sw} = \frac{0.9 I_{chg}}{C_t (V_H - V_L)} = 2\ \ MHz \tag{18}$$

However, the comparator delay is always present due to the parasitic capacitances of the transistors that make up the comparators. Therefore, a maximum nominal value must be assumed. Literature shows that the error produced by the comparator delay, even when low, provides the largest source of error because it depends on the

discharge slope. In [10], an error of 10% relative to the ramp amplitude was obtained. For this reason, it is proposed that this error should not exceed 5% of the ideal ramp amplitude.

$$V_{errL} < V_{ramp} \cdot 5\% = 0.4 \cdot 5\% = 20\ mV \rightarrow V_{errL} = \frac{9I_{\text{chg}}}{C_t} tdL < 20\ mV \tag{19}$$

The maximum nominal delay of the low reference comparator is derived from equation 19, resulting in a delay condition of:

$$tdL < 2.5\ ns \rightarrow Nominal \tag{20}$$

Since the error produced by the high comparator delay is several orders of magnitude lower compared to V_{errL}, it was proposed that this results in a 1.25% error in the ramp signal amplitude. From this, the maximum delay condition for this comparator was derived:

$$V_{errL} < V_{ramp} \cdot 1.25\% = 0.4 \cdot 1.25\% = 5\ mV, \quad tdL < 5.5\ ns \rightarrow Nominal \tag{21}$$

Asumming td_H = 5.5 ns and td_L = 2.5 ns, the value of C_t is modified to C_t = 2.11 pF, to center the frequency at 2 MHz.

$$f_{sw} = \frac{0.9I_{\text{chg}}}{C_t\left(V_H - V_L \pm V_{os}\right) + I_{\text{chg}}\left(t_{dH} + 9t_{dL}\right)} = 2\ MHz \tag{22}$$

Deterministic errors in the ramp frequency arise from the accumulation of errors in the independent variables of the ramp frequency as follows:

$$\Delta f_{sw} = \frac{\partial f_{sw}}{\partial I_{chg}}\Delta I_{chg} + \frac{\partial f_{sw}}{\partial C_t}\Delta C_t + \frac{\partial f_{sw}}{\partial t_{dH}}\Delta t_{dH} + \frac{\partial f_{sw}}{\partial t_{dL}}\Delta t_{dL} + \frac{\partial f_{sw}}{\partial V_{os}}\cancelto{0}{\Delta V_{os}} \tag{23}$$

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[10] Yonggen LIU et al. “A 10/30MHz PWM buck converter with an accuracy-improved ramp generator”. In: *2012 IEEE Asia Pacific Conference on Circuits and Systems*. 2012, pp. 420–423. DOI: 10.1109/APCCAS.2012.6419061.

On the other hand, statistical errors usually arise due to random errors such as mismatches between two transistors due to random manufacturing processes. These errors can be determined through Monte Carlo statistical analysis, where the transistors and passive components of the ramp generator and PWM circuit circuits are randomly varied. The random error in the ramp frequency is given by:

$$\sigma_{f_{sw}}^2 = \left(\frac{\partial f_{sw}}{\partial I_{chg}}\right)^2 \sigma_{I_{chg}}^2 + \left(\frac{\partial f_{sw}}{\partial C_t}\right)^2 \sigma_{Ct}^2 + \left(\frac{\partial f_{sw}}{\partial t_{dH}}\right)^2 \sigma_{t_{dH}}^2 + \left(\frac{\partial f_{sw}}{\partial t_{dL}}\right)^2 \sigma_{t_{dL}}^2 + \left(\frac{\partial f_{sw}}{\partial V_{os}}\right)^2 \sigma_{V_{os}}^2 \quad (24)$$

The offset voltage error in PVT variations is negligible and thus excluded from the analysis. Similarly, preliminary simulations show that the capacitor's sigma is insignificant compared to other random variables. To evaluate these errors, partial derivatives of each variable affecting ramp frequency are calculated. These derivatives help identify which errors impact frequency changes most and guide the specification of the PWM modulator's circuits, ensuring frequency variations stay within ±10%.

$$\frac{\partial f_{sw}}{\partial I_{chg}} = \frac{0,9C_t(V_H - V_L \pm V_{os})}{(C_t(V_H - V_L \pm V_{os}) + I_{chg}(td_H + 9td_L))^2} = 938 \times 10^9 \left[\frac{Hz}{A}\right] \quad (25)$$

$$\frac{\partial f_{sw}}{\partial C_t} = \frac{-0,9I_{chg}(V_H - V_L \pm V_{os})}{(C_t(V_H - V_L \pm V_{os}) + I_{chg}(td_H + 9td_L))^2} = -889 \times 10^{15} \left[\frac{Hz}{F}\right] \quad (26)$$

$$\frac{\partial f_{sw}}{\partial td_H} = \frac{-0,9I_{chg}^2}{(C_t(V_H - V_L \pm V_{os}) + I_{chg}(td_H + 9td_L))^2} = -4,44 \times 10^{12} \left[\frac{Hz}{s}\right] \quad (27)$$

$$\frac{\partial f_{sw}}{\partial td_L} = \frac{-8,1I_{chg}^2}{(C_t(V_H - V_L \pm V_{os}) + I_{chg}(td_H + 9td_L))^2} = -40 \times 10^{12} \left[\frac{Hz}{s}\right] \quad (28)$$

$$\frac{\partial f_{sw}}{\partial V_{os}} = \frac{\pm 0,9C_tI_{chg}}{(C_t(V_H - V_L \pm V_{os}) + I_{chg}(td_H + 9td_L))^2} = \pm 4,69 \times 10^6 \left[\frac{Hz}{V}\right] \quad (29)$$

2.3. Switching frequency variation budget

A budget was made for the errors produced in the frequency due to variations in the independent. This analysis will be carried out by obtaining the maximum frequency delta, where the frequency increases. This occurs when the directly proportional variables increase, and the inversely proportional variables decrease. The calculations and analysis proposed for this budget are shown in detail.

Since potential variations in the delay of the low-voltage reference comparator are one of the main sources of deterministic error, it was proposed to induce a 2% variation in the ramp frequency:

$$\Delta f_{sw} = \frac{\partial f_{sw}}{\partial t_{dL}} \Delta t_{dL} = f_{sw} \cdot 2\% \tag{30}$$

Resulting in a Δt_{dL} of -1 [ns], which corresponds to an error of:

$$td_{Lerr} = \frac{|\Delta td_L|}{td_L} \cdot 100\% = 40\% \tag{31}$$

Given that the design of the comparators is the same, the delay of the high-voltage reference comparator could vary by 40%, producing a frequency delta of:

$$\Delta f_{sw} = \frac{\partial f_{sw}}{\partial t_{dH}} \Delta t_{dH} = 9.78 \ \ kHz \tag{32}$$

producing a frequency error of:

$$f_{swerr} = \frac{|\Delta f_{sw}|}{f_{sw}} \cdot 100\% = 0.489\% \tag{33}$$

Regarding the deterministic errors in the capacitor and resistor, since they produce opposing effects on the switching frequency, and the capacitor varies by 25% in process, the resistor by 15% and 3% in temperature, a trimming implementation was carried out

on the resistor to vary it by 25% in process, thereby compensating for the changes in the capacitor. Given that the resistor also changes with temperature, the total error produced by these two variables after applying trimming is given by 35

$$\Delta f_{sw} = \frac{\partial f_{sw}}{\partial I_{chg}} \Delta I_{chg} + \frac{\partial f_{sw}}{\partial C_t} \Delta C_t = 56.33 \ \ kHz \tag{34}$$

$$f_{swerr} = \frac{|\Delta f_{sw}|}{f_{sw}} \cdot 100\% = 2.816\% \tag{35}$$

The total deterministic error in the frequency, taking into account the variations, is calculated in 41

$$\Delta f_{sw} = \frac{\partial f_{sw}}{\partial I_{chg}} \Delta I_{chg} + \frac{\partial f_{sw}}{\partial C_t} \Delta C_t + \frac{\partial f_{sw}}{\partial t_{dH}} \Delta t_{dH} + \frac{\partial f_{sw}}{\partial t_{dL}} \Delta t_{dL} = \ \ 106,1 kHz \tag{36}$$

$$f_{swerr} = \frac{|\Delta f_{sw}|}{f_{sw}} \cdot 100\% = 5.3\% \tag{37}$$

Finally, a budget was made for the random or statistical errors, in which a variation of $3\sigma_{f_{sw}}$ of 3.2% was proposed, due to the standard deviation of the offset referred to the input of the comparators.

$$\sigma_{f_{sw}} = f_{sw} \cdot 1,07\% = 21.4 \ \ kHz \tag{38}$$

Thus, the sigma of the offset of the comparators cannot exceed:

$$\sigma_{V_{os}} = \frac{f_{sw} \cdot 1,07\%}{\left(\frac{\partial f_{sw}}{\partial V_{os}} \right)} \approx \pm 4.5 mV \tag{39}$$

The same analysis was performed for the variation in $3\sigma_{f_{sw}}$ caused by random changes in the load current, proposing a $3\sigma_{f_{sw}}$ of 2.8%, which results in a current sigma of:

$$\sigma_{I_{chg}} = \frac{f_{sw} \cdot 0,93\%}{\left(\frac{\partial f_{sw}}{\partial I_{chg}}\right)} \approx \pm 20nA \tag{40}$$

This $\sigma_{I_{chg}}$ produces a current error of:

$$I_{chg} = \frac{\sigma_{I_{chg}}}{I_{chg}} \cdot 100\% = \pm 1\% \tag{41}$$

Finally, the sigma of the comparator delay was determined, proposing a variation of $3\sigma_{f_{sw}}$ caused by the delay of the low-reference comparator of 1.5% of the nominal frequency, which results in a frequency sigma of:

$$\sigma_{f_{sw}} = \sqrt{\left(\frac{\partial f_{sw}}{\partial td_L}\right)^2 \sigma_{td_L}^2} = \pm 10 \ \ kHz \tag{42}$$

With respect to this, the standard deviation of t_{d_L} was determined, which causes a percentage error calculated in eq:45

$$\sigma_{td_L} = \frac{\pm f_{sw} \cdot 0,6\%}{\left(\frac{\partial f_{sw}}{\partial td_L}\right)} \approx \pm 300 \ \ ps \tag{43}$$

$$td_L = \frac{\sigma_{td_L}}{td_L} \cdot 100\% = \pm 12\% \tag{44}$$

Since the percentage error in the low-reference comparator is 12%, the high-reference comparator will have the same percentage error in delay, which results in a frequency sigma of $\pm$ 2.933 kHz, producing a frequency error at 3σ of:

$$f_{swerr} = \frac{3\sigma_{f_{sw}}}{f_{sw}} \cdot 100\% = \pm 0.4399\% \tag{45}$$

The deterministic and statistical errors were distributed as follows:

$$\Delta f = \frac{\partial f}{\partial I_{chg}}\Delta I_{chg} + \frac{\partial f}{\partial C_t}\Delta C_t + \frac{\partial f}{\partial td_H}\Delta td_H + \frac{\partial f}{\partial td_L}\Delta td_L = 106.04 \ \ kHz \tag{46}$$

$$\begin{aligned} \Delta I_{chg} &= \pm I_{chg} \cdot 28\%, \ \ \Delta C_t = \pm C_t \cdot 25\% \\ \Delta td_H &= \pm td_H \cdot 40\%, \ \ \Delta td_L = \pm td_L \cdot 40\% \end{aligned} \tag{47}$$

$$\sigma_f = \sqrt{\left(\frac{\partial f}{\partial I_{chg}}\right)^2 \sigma^2_{chg} + \left(\frac{\partial f}{\partial td_H}\right)^2 \sigma^2_{td_H} + \left(\frac{\partial f}{\partial td_L}\right)^2 \sigma^2_{td_L} + \left(\frac{\partial f}{\partial V_{os}}\right)^2 \sigma^2_{V_{os}}} = 30.08 \ \ kHz \tag{48}$$

$$\begin{aligned} \sigma I_{chg} &= \pm I_{chg} \cdot 1\%, \ \ \sigma td_H = \pm td_H \cdot 12\% \\ \sigma td_L &= \pm td_L \cdot 12\%, \ \ \sigma V_{os} = \pm 4.5 \ \ mV \end{aligned} \tag{49}$$

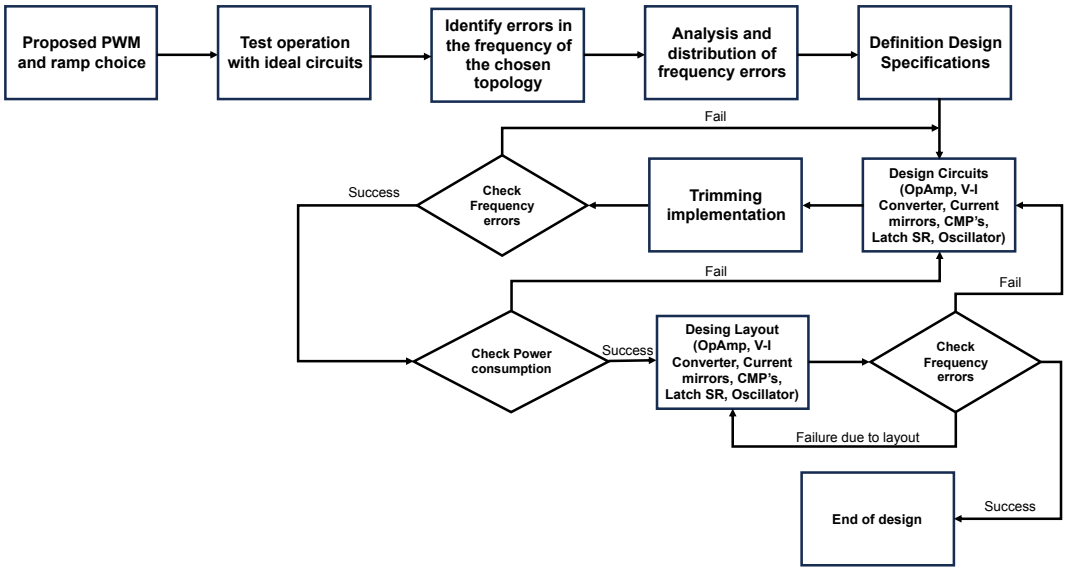
Obtaining a frequency error produced by a deterministic error delta and three sigma of random error, which is:

$$f_{sw_{err}} = \frac{|3\sigma_{f_{sw}} + \Delta_{f_{sw}}|}{f_{sw}} \times 100\% = 9.92\% \tag{50}$$

3. PWM CIRCUIT DESIGN METHODOLOGY

This chapter will address the design methodology proposed for the PWM circuit. It consists of an iterative design flow in which the switching frequency and power consumption are fundamental pillars when approaching the next step in the design.

Figure 3.1. Design methodology.



The initial step, detailed in Section **1.3**, involved selecting the topology for the PWM and ramp generator circuits, optimizing frequency control, power consumption, and design flexibility. Behavioral models in Verilog-A and circuit models were then created to verify the circuit's functionality. Next, errors impacting the switching frequency were analyzed, as described in Section **2.2**. Finally, an error budget, outlined in Section **2.3**, ensured frequency variations stayed within $\pm$ 10% of the nominal value during PVT and Monte Carlo simulations.

3.1. Definition Design Specifications

This section will define the specifications of the blocks that make up the PWM circuit based on the frequency error budget presented in section **2.3**.

We will begin by defining the specifications of the voltage-to-current converter (see in Figure **3.2**), distributing the error in the load current, which depends on various parameters of the error amplifier, such as gain, offset, PSR, as well as the matching of the mirrors responsible for copying the current generated by the V-I converter.

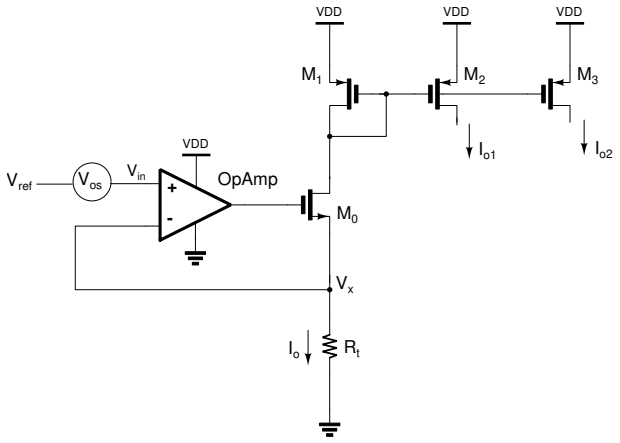


Figure 3.2. Voltage to Current Converter.

3.1.1. Gain OpAmp Considering the deterministic error in the current due to the OpAmp gain, if we want the voltage across R_t, called V_x, to be equal to V_{ref}, the OpAmp must have a high gain. In this way, we can derive the equation for the loop gain.

$$Ao_{CL} = \frac{V_x}{V_{in}} = \frac{A_1 A_{M_0}}{1 + \beta A_1 A_{M_0}} \tag{51}$$

$$A_{M_0} = \frac{R_t}{\frac{1}{gm_0} + R_t} \tag{52}$$

Where A_1 is the gain of the OpAmp and A_{M_0} is the gain of the common drain. This circuit has a negative feedback loop with β equal to 1. We know that A_{M_0} tends to 1 if the drain resistance (R_t) is large. However, in this case, the resistance is in the order of kΩ, similar to $1/gm_0$, so we say it has a gain of 0.7, based on previous simulations indicating that gm_0 has a value of 15 µS and R_t a value of 150 kΩ. Therefore:

$$Ao_{CL} = \frac{A_1 0.7}{1 + A_1 0.7} \tag{53}$$

We want this error to be small, so we choose a 0.1% error to make it negligible, opting for a high-gain OpAmp topology. Therefore:

$$Ao_{CL} = \frac{A_1 0.7}{1 + A_1 0.7} = 0.999 \rightarrow 0.1\% \ \ error \tag{54}$$

Therefore, a minimum gain in the OpAmp of:

$$A_1(min) = 1427 \ \frac{V}{V} \rightarrow 63 \ \ dB \tag{55}$$

3.1.2. Input reference offset OpAmp The input-referred offset voltage is a statistical error in the OpAmp. This voltage randomly affects the load current, as it directly influences the voltage V_x. By assuming only the statistical error of the input-referred offset voltage with infinite gain for the amplifier, the input voltage will be given by:

$$V_{in} = V_{ref} \pm V_{os} \tag{56}$$

Any voltage in V_{os} will either add to or subtract from V_{ref}, and this will be the voltage we observe at the V_x node. This will change the current I_o, and this error will be

proportional to the current. For example, if V_{os} is 1% of V_{ref}, the current I_o will change by 1%.

In the budget, it was decided that the load current I_{chg} would change by 1% of its nominal value, 2 µA, so a sigma of 20 nA was chosen. Therefore:

$$\sigma V_{os} = V_{ref} \times 1\% \tag{57}$$

In the design, a reference voltage of 300 mV was used, so the standard deviation of the input-referred offset of the OpAmp must be less than 3 mV, which gives us an input-referred offset voltage at 3σ for the amplifier of:

$$3\sigma V_{os} = \pm 9 \ mV \tag{58}$$

Regarding the deterministic and random errors in the P-MOS current mirrors in the design, these will be minimized by improving the matching of the transistors so that these errors become insignificant compared to other errors occurring in the load current. Therefore, in this analysis, the mirrors are assumed to be ideal.

3.1.3. Power Supply Rejection(PSR) OpAmp It is a deterministic error of the OpAmp that affects the voltage V_x in a predictable manner. We can express the PSR as $PSR = \dfrac{V_x}{V_{dd}}$.

$$A_{vdd} = \frac{V_x}{V_{dd}} = \frac{PSR_1 A_{M_0} + PSR_{M_0}}{1 + \beta A_1 A_{M_0}} \tag{59}$$

Where PSR_1 is the power supply rejection of the OpAmp, and PSR_{M_0} is the PSR of the common drain stage at the output V_x of the Voltage-to-Current converter.

$$PSR_{M_0} \approx \frac{R_t}{R_t + ro_0(1 + R_t g m_0)} \tag{60}$$

Assuming that the PSR gain is a maximum of -60 dB, this means that when there is

a 10 mV change in V_{dd} at the V_x node, we will observe a 10 µV change in V_x, with $r_{o_0}(min) = 1M\Omega$. Using the previous values, solving from equation (**76**):

$$PSR_1 \leq 2.6 \ dB \tag{61}$$

We will now define the specifications of the oscillator circuit, starting with the specifications of the comparators that make up the PWM circuit and the ramp generator. To define the specifications of the comparators that make up the ramp generator and PWM circuit, frequency variation analysis was used. This included determining the maximum delay of each comparator, the minimum required gain, and the maximum input-referred offset voltage.

3.1.4. Delay Comparators The maximum delay of the comparators is the largest source of error in the circuit. Therefore, based on the analysis performed in section 2.3, the maximum delay for the high and low reference comparators, as observed in Figure **3.3**, is determined by:

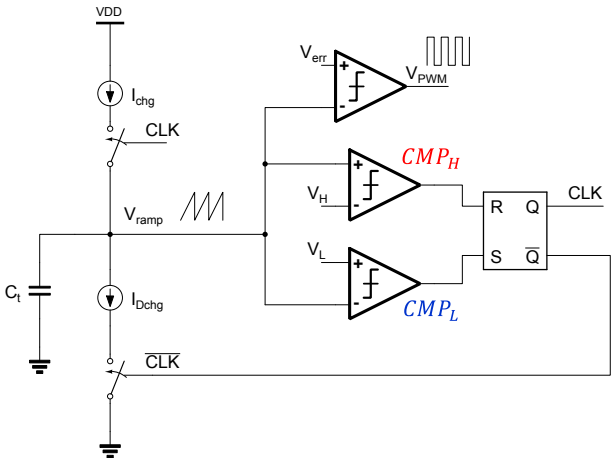


Figure 3.3. Oscillator Circuit.

$$td_H[max] = td_H + |\Delta td_H| \approx 7.5 \ ns \rightarrow V_{in} = 5 \ mV \tag{62}$$

$$td_L[max] = td_L + |\Delta td_L| \approx 3.5\ \ ns \rightarrow V_{in} = 20\ \ mV \tag{63}$$

The delay of the comparators can also vary statistically. Therefore, in the frequency error analysis, it was proposed to obtain a 3σ for the comparator delay of:

$$3\sigma td_H = \pm 660\ \ ps \tag{64}$$

$$3\sigma td_L = \pm 300\ \ ps \tag{65}$$

3.1.5. Input reference offset voltage Comparators It is the main statistical error in the ramp frequency. A voltage V_{os} at 3σ was defined as:

$$3\sigma V_{os} = \pm 13.5\ \ mV \tag{66}$$

3.1.6. Gain of Comparators The minimum gain of the comparators is determined by the comparator resolution $V_{in(min)}$:

$$A_o = 20log\left(\frac{V_{OH} - V_{OL}}{V_{in(min)}}\right) \tag{67}$$

This resolution can be derived by calculating the minimum error voltages produced by the delay of each comparator (see figure **3.4**).

$$V_{errH}[min] = \frac{I_{chg}}{C_t} \cdot (td_H - |\Delta td_H|) \tag{68}$$

$$V_{errL}[min] = \frac{9I_{chg}}{C_t} \cdot (td_L - |\Delta td_L|) \tag{69}$$

Since the error voltage of the CMPH is smaller than the error voltage produced by the CMPL, the former is chosen as the minimum value. This value is divided by one-tenth

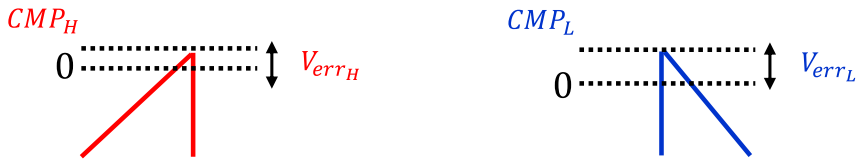


Figure 3.4. Resolution Comparators.

to find a value for the sensitivity of the comparator to be designed as:

$$V_{in(min)} = 625.6 \ \ uV \tag{70}$$

The minimum gain of the comparators must be at least 80 dB to meet the comparator resolution requirements.

$$A_o > 70 \ \ dB \tag{71}$$

3.1.7. Design specifications OpAmp and Comparators

Having defined the specifications for the OpAmp and Comparator In 3.1, the following summary table is shown in Table 3.1.

Table 3.1. Design specifications OpAmp and comparators.

OpAmp				**Comparator**			
Parameter	**Min**	**Typ**	**Max**	**Parameter**	**Min**	**Typ**	**Max**
V_{DD} [V]	1.62	1.8	1.98	V_{DD} [V]	1.62	1.8	1.98
I_{bias} [uA]	-	1	-	I_{bias} [uA]	-	1	-
C_L [fF]	-	50	-	C_L [fF]	-	50	-
A_o [dB]	63	-	-	A_0 [dB]	70	-	-
G_M [dB]	10	-	-	BW [MHz]	2.2	-	-
P_M [º]	45	-	-	td_{HL} [ns] @ΔV_{in} = 5 mV	-	-	7.5
PSR [dB]	-	-	2.6	td_{LH} [ns] @ΔV_{in} = 5 mV	-	-	7.5
V_{os} [mV] @3σ	-9	-	9	td_{HL} [ns] @ΔV_{in} = 20 mV	-	-	3.5
				td_{LH} [ns] @ΔV_{in} = 20 mV	-	-	3.5
				V_{os} [mV] @3σ	-13.5	-	13.5

3.2. Design Blocks and TOP Level Circuit

This section will address the design of the different blocks that make up the PWM circuit and the ramp generator, as well as the circuit at a top-level view.

3.2.1. OpAmp Topology and Design

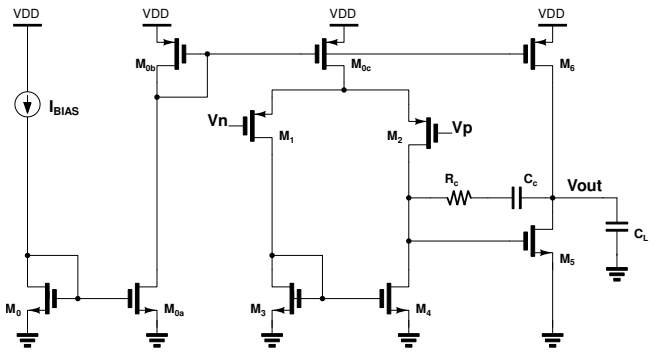
The design of the OpAmp for the voltage-to-current converter was carried out considering the specifications previously obtained through the analysis of frequency errors in the ramp (see section **2.3**) to ensure optimal converter operation. The most relevant specifications include the open-loop gain and the offset referred to as the input of the OpAmp.

Table 3.2. Comparison OpAmp.

	Telescopic	**Folded cascode**	**Two stage with Miller compensation**
Gain	Medium	Medium	High
Offset	Low	Medium	Low
Power core	Low	Medium	Medium
Bias Voltage	Medium	High	Low
Output Swing	Medium	Medium	Highest
Speed	Highest	High	Low

A study of various OpAmp topologies was first conducted(see Table **3.2**). The two-stage topology with Miller compensation (see figure **3.5**) and a P-MOS differential input was chosen, characterized by its high gain, low power consumption considering the power consumed by the core and the number of bias voltages used in the core, and low offset. The P-MOS input was selected because we will use a low input voltage.

Figure 3.5. OpAmp Topology.



After selecting the topology, we will design the OpAmp to meet the specifications in Table **3.2**. We will start with the design of the OpAmp gain, which was calculated using

the small-signal model (see equation **72**).

$$A_0 = gm_{1,2}(r_{0_{1,2}}||r_{0_{3,4}})gm_5(r_{0_5}||r_{0_6}) \tag{72}$$

The dominant poles and the zero generated by Miller compensation were calculated (see equation **73**).

$$P_1 = -\frac{gm_{1,2}}{A_0 C_c}, P_2 = -\frac{gm_5}{C_L}, Z_1 = \frac{1}{C_c\left(\frac{1}{gm_5} - R_c\right)} \tag{73}$$

For the low-frequency gain design, the input of the differential pair was operated in weak inversion, as this provides the highest g_m for a given current. Additionally, the r_0 values were optimized to be large to achieve high gain. In the design of Miller compensation, the zero created by the Miller resistor and capacitor was adjusted to cancel the second pole. An N-MOS transistor was used for the resistor R_c, making the design more area-efficient. The value of this resistor is given by equation **74**, thereby achieving the phase margin required by the specifications.

$$R_c = \frac{1}{k'\frac{W}{L}(Vgs_N - Vth_N)} \tag{74}$$

For the input-referred offset voltage design, equation **75** was considered. Since the gain design aimed to maximize $g_{m_{1,2}}$, followed the approach in [11], which states that the standard deviation of the threshold voltage is inversely proportional to the transistor area. This was applied to minimize the transistors without affecting the previously

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[11] A. C. J. Duinmaijer M. J. M. PELGROM and A. P. G. WELBERS. “Matching properties of MOS transistors”. In: *IEEE Journal of Solid-State Circuits* 24 (1989), pp. 1433–1439.

achieved specifications.

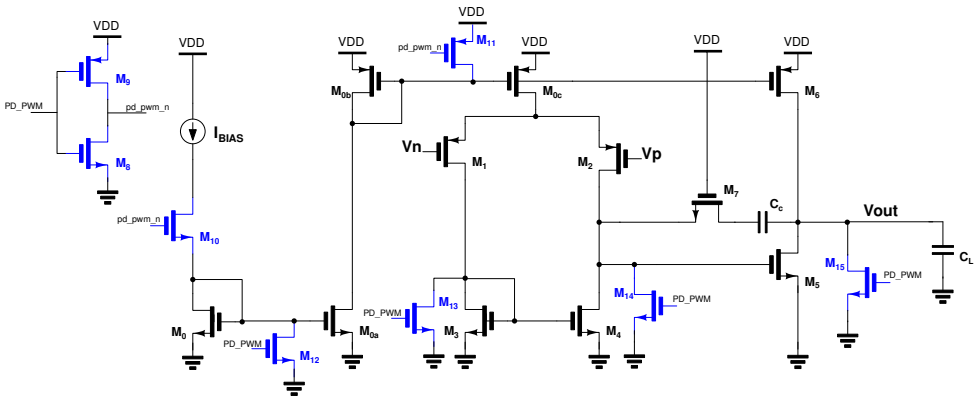
$$(\sigma_{V_{os}})^2 \approx (\sigma_{V_{th_{1,2}}})^2 + \left(\frac{gm_{3,4}}{gm_{1,2}}\right)^2 (\sigma_{V_{th_{3,4}}})^2 \tag{75}$$

For the PSR, equation **76** was considered, and the small-signal resistance r_{0_6} was designed to be large.

$$PSR_{DC} \approx \frac{r_{0_5}}{r_{0_5} + r_{0_6}} \tag{76}$$

Finally, the power-down feature of the OpAmp was designed (see Figure **3.6**). The transistors used for power-down are shown in blue. This feature allows the OpAmp to be turned off when not in use and turned on when needed, reducing power consumption during idle periods. To achieve this, the gates of the N-MOS transistors are connected to the ground, and the gates of the P-MOS transistors are connected to the supply voltage to turn them off. Additionally, the output of the OpAmp is connected to the ground through M_{15}, ensuring minimal power consumption when the power-down mode is activated.

Figure 3.6. OpAmp Topology with power down.



3.2.2. Comparators Topology and Design

In designing the comparators for the ramp generator and PWM circuit, specifications from the variational analysis of ramp frequency errors were considered, focusing on input-referred offset voltage, delay time, and required gain for sensitivity. A literature

review was conducted to select the optimal comparator topology, prioritizing low delay time, low offset, high gain, high speed, and low power consumption. A comparative table was created to evaluate three types of comparators: the Two-Stage, Open-Loop Comparator [12], Source Coupled Differential Pair with Positive Feedback (Hysteresis-Based Comparator) [1], and a High-Speed Three-Stage Comparator [13].

Table 3.3. Comparison Comparator.

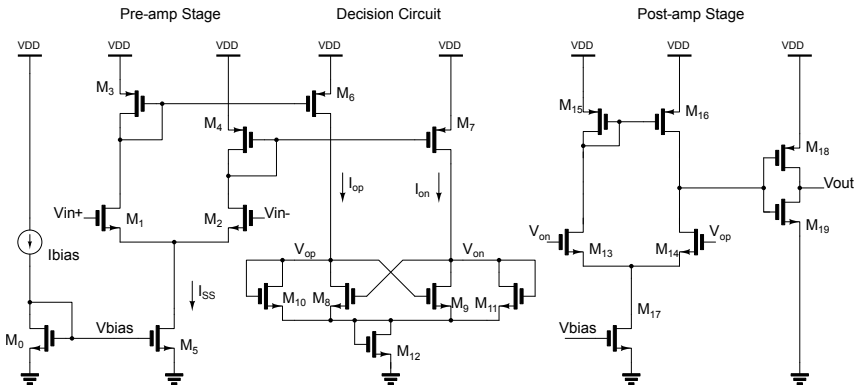
	Two-Stage Open-Loop Comparator	**Hysteresis-Based Comparator**	**A high-speed three-stage Comparator**
Gain	Medium	High	High
Speed	Low	Highest	High
Delay	High	Low	Lowest
Offset	Low	Medium	Medium
Power	Low	High	Low
Area	Low	Medium	Medium

Thus, the high-speed three-stage Comparator topology was chosen, as it provides suitable specifications for our application. This topology is shown in Figure **3.7**.
This comparator consists of three stages. The first is the pre-amplification stage, which amplifies the input signal to improve the comparator's sensitivity and isolates the input from the switching noise from the comparator's positive feedback stage. The positive feedback stage determines which of the input signals is larger. The output buffer amplifies this information and outputs a digital signal [13]. The pre-amplification stage shown in Figure **3.7** was designed considering the diff-amp transconductance g_m and the input capacitance. Since this transconductance determines the gain of this stage, the input

[12] D. R. H. Phillip E. ALLEN. *CMOS Analog Circuit Design*. OXFORD UNIVERSITY PRESS, 2011.

[13] R. Jacob BAKER, Harry W. LI, and David E. BOYCE. *CMOS. Circuit design layout and simulation*. Fourth Edition. IEEE Press, 2019.

Figure 3.7. Comparators Topology.



pair transistors M1 and M2 were set in weak inversion, and their width W was maximized. The minimum length L was also used to maximize the comparator's bandwidth. We can relate the input voltages to the output small-signal AC currents i_{op} and ion:

$$i_{op} = \frac{I_{ss}}{2} + \frac{gm_{1,2}}{2}(V_{in+} - V_{in-}), \quad i_{on} = \frac{I_{ss}}{2} - \frac{gm_{1,2}}{2}(V_{in+} - V_{in-}) \tag{77}$$

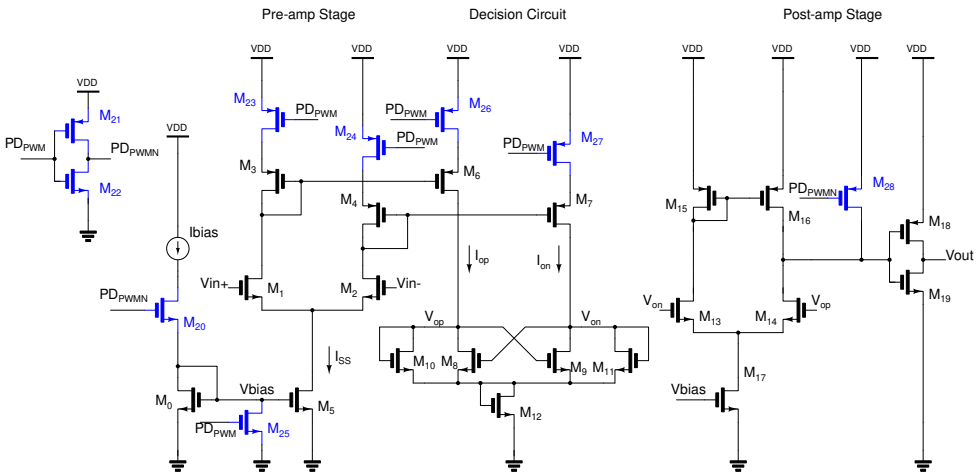
For the decision stage (see figure **3.7**), the transistors M_{8-11} were initially designed with equal sizes, as hysteresis is not desired in our application, and minimum sizes were used to reduce the delay in the comparator. However, the lengths L were increased to reduce the offset and the hysteresis caused by random variations. The switching point voltages when the comparator has hysteresis (if $\beta_A \neq \beta_B$) are given by:

$$V_{SPH} = \frac{I_{ss}}{gm_{1,2}} \frac{(\beta_A - \beta_B)}{(\beta_A + \beta_B)} for \beta_B, \quad V_{SPL} = -V_{SPH} \geq \beta_A \tag{78}$$

In the previous stage, transistor M_{12} was added to elevate the DC level of the output signals from the decision stage to the common-mode input range of the buffer stage, enhancing its behavior and speed. The sizes of the transistors in the output buffer

were minimized to prevent significant increases in the comparator's delay. Additionally, the bias current in this stage was increased to enhance the comparator's speed. Throughout the various stages of the comparator, a trade-off was made between delay and input-referred offset voltage, thus improving the offset without compromising delay performance. Finally, the power-down of the comparators was implemented to reduce power consumption when they are not in use. This implementation was based on the power-down technique described in [14]. (See Figure **3.8**).

Figure 3.8. Power Down implementation Comparators.



3.2.3. Latch SR Topology and Design and Switch Implementation

For the SR latch circuit, the topology shown in Figure **3.9(a)** was chosen, which eliminates two transistors from conventional topologies made with cross-coupled NOR or NAND gates [15], reducing the area and parasitic capacitances without compromising

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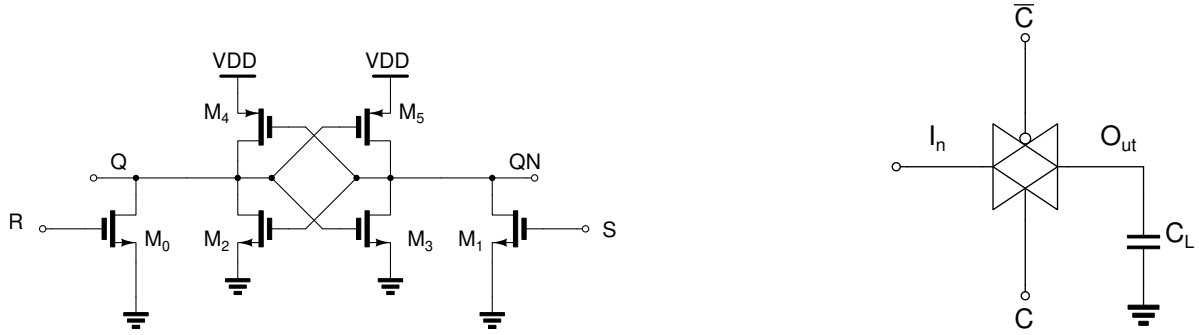
[14] Daniel Felipe BARRIOS RUEDA and Nestor Ivan MATAJIRA ORTIZ. "Design of Energy-Efficient Voltage Comparators for a System-on-Chip Using a CMOS Technology Node of 28nm". Bachelor's thesis. Universidad Industrial de Santander, May 15, 2024.

[15] J.P. UYEMURA. *CMOS Logic Circuit Design*. [ProQuest Ebook Central]. Springer US, 1999.

speed. The switches were implemented using transmission gates (see Figure **3.9(b)**), since an NMOS switch passes a logic zero better and a PMOS switch passes a logic one better. Combining their qualities makes a much faster switch obtained [13].

Figure 3.9. Latch SR Circuit and Transmission Gate.



(a) Latch SR Circuit. (b) Transmission Gate.

3.2.4. Voltage to Current Converter Design

Properly designing the common drain stage and P-MOS transistor-based current mirrors in this circuit is crucial to ensure system performance. Accurate matching of the current mirrors leads to precise current replication, which directly influences the overall functionality of the circuit. For the common drain stage, a strong inversion regime configuration was selected. For the P-MOS current mirrors, saturation current (**79**) was taken into account to ensure stability and accuracy in transistor operation.

$$I_d = \frac{1}{2}\mu C_{ox}(V_{sg} - |V_{th_p}|)^2 \tag{79}$$

Two key factors affecting current mirror matching were addressed in designing the current source, as noted in [16]. First, the relation $V_{ov} = V_{sg} - |V_{th_p}|$ was used to reduce mismatching by increasing V_{sg}, making variations in $|V_{th_p}|$ less impactful. Additionally,

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[16] Jeison Herney ACEVEDO VELASQUEZ and Eduardo CABALLERO BARAJAS. "Design of a Bandgap Voltage Reference in a 28 nm CMOS Process". Bachelor's thesis. Universidad Industrial de Santander, Nov. 10, 2023, pp. 36–39.

the device area was increased, as $\sigma_{V_{th_p}}$ is inversely proportional to the area, reducing threshold voltage variation. These considerations ensure highly accurate matching in the current mirrors.

3.2.5. Oscillator Circuit Design

The oscillator circuit controls each oscillation cycle in the ramp generator. This circuit comprises two static comparators and an SR Latch circuit, where the delay was minimized while performing a trade-off to ensure low offset in the comparators.

3.3. Trimming Implementation

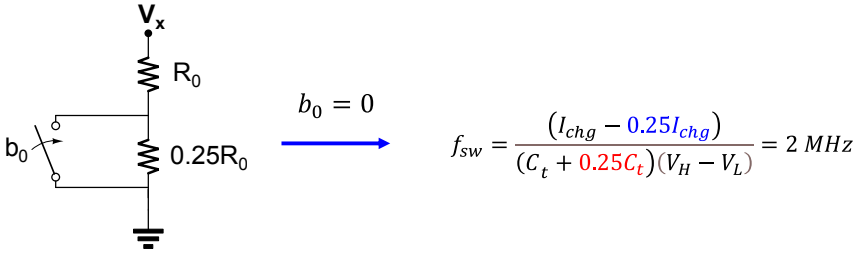
In the design corners of the PWM, where variations in Process, Voltage, and Temperature (PVT) are considered, the most significant changes affecting the switching frequency are related to the process. Two components are susceptible to these variations: the resistance R_t, which generates the current I_0 and is used to create I_{chg} and I_{dchg}, and the capacitor C_t, that charges and discharges to generate the ramp oscillation signal at a fixed frequency of 2 MHz. Under process variation conditions, R_t can vary by approximately ±15%, and C_t can vary by ±25%. These fluctuations are especially critical in the FF (fast) and SS (slow) process corners. For instance, a -25% variation in C_t would alter the ramp frequency (**80**). In this design, the independent variable values for switching frequency are $I_{chg} = 2, \mu A$, $C_t = 2.25, pF$, $V_H = 1, V$, and $V_L = 0.6, V$, using the ideal frequency equation and assuming no delays in the comparators.

$$f_{sw} = \frac{0.9Ichg}{C_t(V_H - V_L)} = 2Mhz, \quad f_{sw} = \frac{0.9Ichg}{(C_t - 0.25C_t)(V_H - V_L)} = 2.66Mhz \tag{80}$$

The solution to this problem involves trimming in R_t, allowing the modification of I_{chg} and adjusting the switching frequency. Figure **3.10** shows a basic trimming setup where

a digital signal controls a switch (b_0) to activate or deactivate a resistor. In the nominal state, $b_0 = 1$, resulting in $I_{chg} = \frac{V_x}{R_0}$. However, in the FF process corner, where the capacitor decreases by 25% and the resistance remains typical, b_0 is set to 0. This adjusts $I_{chg} = \frac{V_x}{R_0 + 0.25R_0}$, allowing the frequency to be corrected. This 25% reduction in I_{chg} compensates for the capacitor variation (see Figure **3.10**).

Figure 3.10. Trimming implementation basic.



The first step involves considering the possible combinations of process corners. In the resistive and capacitive elements, there are three primary corners: Typical (TT), Fast (FF), and Slow (SS). By combining these corners we obtain nine possible combinations. (See Table **3.4**).

Table 3.4. Process corner combination for resistor and capacitor.

Corner	R	C
TT-TT	typical(TT)	typical(TT)
TT-SS	typical(TT)	Slow(SS)
TT-FF	typical(TT)	Fast(FF)
SS-TT	Slow(SS)	typical(TT)
SS-SS	Slow(SS)	Slow(SS)
SS-FF	Slow(SS)	Fast(FF)
FF-TT	Fast(FF)	typical(TT)
FF-SS	Fast(FF)	Slow(SS)
FF-FF	Fast(FF)	Fast(FF)

The trimming design was executed in Table **3.5**. The 'Corner' column lists the different process corner combinations. The 'R_{trimm}' column indicates the resistance in $k\Omega$ at its typical value, used to adjust the current I_{chg} by adding or removing resistance. 'R_{new}' shows the effective resistance, calculated as $R_{new} = R_t + R_{trimm}(1 \pm 15\%)$, reflecting process variations. The 'R_t' and 'C_t' columns contain the effective resistance and capacitance due to process changes. The 'f' column displays the frequency without trimming, calculated using equation **17**. Finally, 'f_{trimm}' represents the frequency after trimming, using the same equation but with R_{new} and C_t, considering the delays from the comparator and a reference voltage of 300 mV.

Table 3.5. Design Trimming.

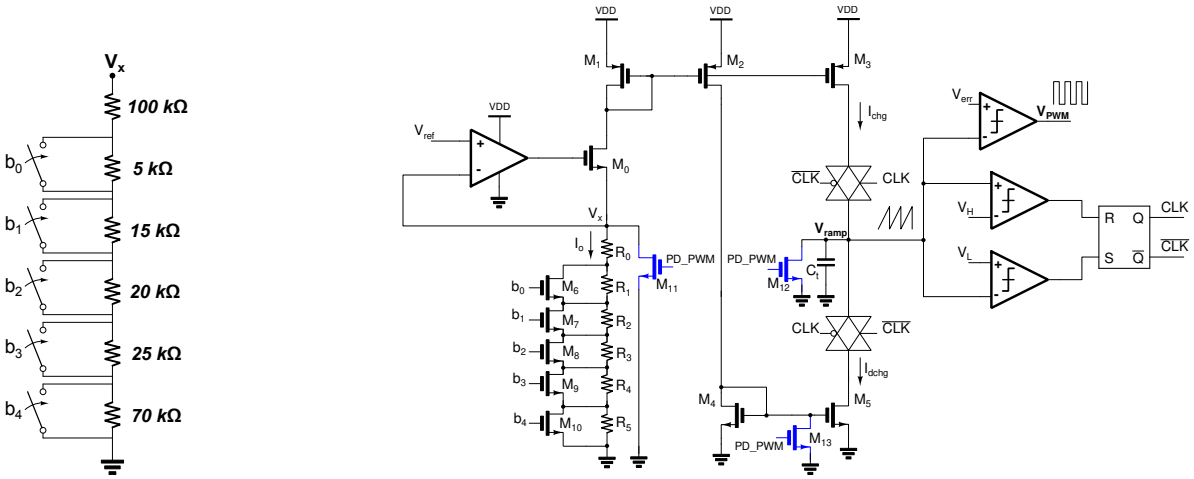
Corner	$R_{trimm}(k\Omega)$	$R_{new}(k\Omega)$	$R_t(k\Omega)$	$C_t(pF)$	$f(MHz)$	$f_{trimm}(MHz)$
TT-TT	00.0	150.0	150.0	2.115	2.000	2.000
TT-SS	-30.0	120.0	150.0	2.644	1.696	2.000
TT-FF	50.0	200.0	150.0	1.586	2.615	2.010
SS-TT	-20.0	149.5	172.5	2.115	1.753	2.006
SS-SS	-45.0	120.8	172.5	2.644	1.417	1.988
SS-FF	25.0	201.3	172.5	1.586	2.297	1.999
FF-TT	25.0	148.8	127.5	2.115	2.328	2.027
FF-SS	-10.0	119.0	127.5	2.644	1.889	2.016
FF-FF	85.0	199.8	127.5	1.586	3.054	2.010

After determining the resistance adjustment, the final values for the typical corner were calculated (see Table **3.6**, column $R = R(TT) + R_{trimm}$). Additionally, a value of 1 is retained to account for changes in the load capacitor due to parasitic capacitance from other blocks at that node. The proposed resistance values for bits b_0, b_1, b_2, b_3, and b_4 are $5k\Omega$, $15k\Omega$, $20k\Omega$, $25k\Omega$, and $70k\Omega$, respectively. Figure **3.11(a)** illustrates the implementation of trimming in the circuit. The final PWM circuit is as follows (see figure **3.11(b)**).

Table 3.6. Words for each process corner combination.

Corner(R - C)	$R(k\Omega)$	$b_0(5k\Omega)$	$b_1(15k\Omega)$	$b_2(20k\Omega)$	$b_3(25k\Omega)$	$b_4(70k\Omega)$
TT-TT	150	1	1	0	0	1
TT-SS	120	1	0	1	1	1
TT-FF	200	1	1	1	0	0
SS-TT	130	1	1	1	0	1
SS-SS	105	1	1	1	1	1
SS-FF	175	0	1	1	1	0
FF-TT	175	1	1	1	1	0
FF-SS	140	1	0	0	1	1
FF-FF	235	1	0	0	0	0

Figure 3.11. Proposed Trimming and Proposed PWM circuit with trimming.



(a) Proposed Trimming.

(b) Proposed PWM circuit with trimming.

3.4. Power Consumption Considerations

This section will address the considerations to ensure a low-power PWM Circuit design. Primarily, implementing the discharge source in the ramp generator by reducing the discharge slope to a lower and more constant value relieves the delay specifications in the comparators, allowing for the use of lower bias currents, which drastically

reduces power consumption. The current generated by the voltage-to-current converter was minimized by using a low reference voltage so that the resistance R_t is in the magnitude of $K\Omega$, occupying the least possible area with low current. A low-power current amplifier (4uA) was also designed, maximizing the amplifier's output resistance R_{out} to achieve a high gain. Furthermore, with the implementation of switches, the charge or discharge current is disconnected depending on the oscillation cycle state (ramp charging or discharging) to avoid consuming this current when these sources are not in use.

4. RESULTS

This section shows the sizes of each transistor and the resistor and capacitor values used, as well as the measurements taken for each block and the complete implemented circuit.

4.1. Devices Sizing

This section will show the sizes of the transistors designed for each block that constitutes the PWM circuit. The technology used for this process was TSMC's 28[nm] CMOS using the 1.8[V] standard transistors. A convention for transistor sizing will be used where W is the total width of the transistor and is given by $W = Finger_W * N_{Finger}$, where $Finger_W$ is the width of the finger used and N_{Finger} is the number of fingers employed. L is the length of the transistor, $N_{Multiplier}$ is the number of transistors in parallel, and N_{Series} is the number of transistors in the stack.

4.1.1. OpAmp

Table **4.1** describes the final dimensions of each transistor used in the design of the OpAmp (see Figure **3.6**). A compensation capacitance C_c with a value of $212.8\ \mathrm{fF}$ was used with a MOM capacitor. PVT specifications were satisfactorily met.

Table 4.1. Sizes OpAmp.

Name	$W(\mu m)$	$Figer_W(\mu m)$	$L(\mu m)$	$N_{Multiplier}$	N_{Finger}	N_{Series}
$M_{0,0a}$	0.270	0.270	1.50	1	1	1
$M_{0b,0c}$	0.830	0.415	2.00	1	2	2
M_{1-2}	2.250	0.450	0.40	6	5	1
M_{3-4}	1.600	0.400	2.00	1	4	2
M_5	1.320	0.660	1.50	1	2	1
M_6	0.830	0.415	2.00	1	2	2
M_7	0.270	0.270	2.00	1	1	3
M_{8-15}	0.270	0.270	0.15	1	1	1

4.1.2. Comparator's, Latch SR and PWM circuit

For the comparator design (Figure **3.8**), the SR latch (Figure **3.9(a)**), and the PWM circuit (Figure **3.11(b)**), the transistor sizes for each circuit are shown in Table **4.2**. In the PWM circuit, we used polysilicon resistors: $R_0 = 100k\Omega$, $R_1 = 5k\Omega$, $R_2 = 15k\Omega$, $R_3 = 20k\Omega$, $R_4 = 25k\Omega$, and $R_5 = 70k\Omega$, along with a MOM capacitor of $C_t = 2.11\text{pF}$.

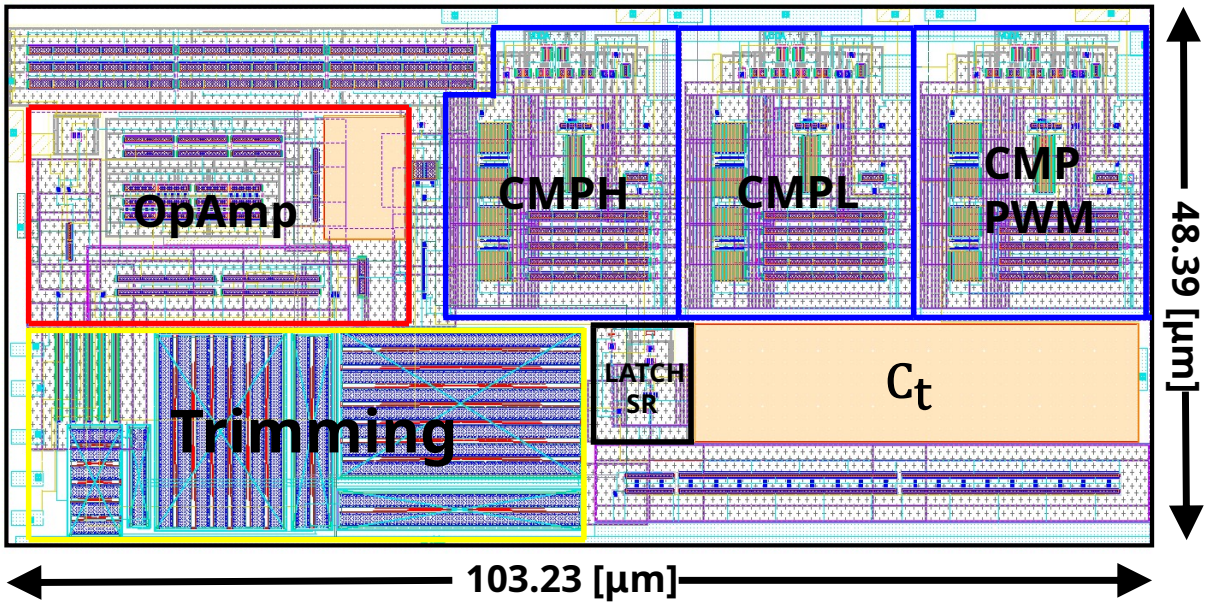
Table 4.2. Sizes for the Comparator's, Latch SR and PWM circuit.

Name	$W(\mu m)$	$Figer_W(\mu m)$	$L(\mu m)$	$N_{Multiplier}$	N_{Finger}	N_{Series}
			Comparator			
M_0	0.54	0.54	2	1	1	1
M_{1-2}	2.5	2.5	0.15	16	1	1
M_{3-4}	0.6	0.6	0.4	2	1	1
M_5	2.75	0.55	2	2	5	1
M_{6-7}	0.6	0.6	0.4	2	1	1
M_{8-11}	0.27	0.27	0.5	1	1	1
M_{12}	5	5	0.15	4	1	1
M_{13-14}	0.27	0.27	0.15	1	1	1
M_{15-16}	0.41	0.41	0.4	1	1	1
M_{17}	2.75	0.55	0.15	3	5	1
M_{18}	1.015	1.015	0.3	1	1	1
M_{19}	0.27	0.27	0.3	1	1	1
M_{20-22}	0.27	0.27	0.15	1	1	1
M_{23-24}	1	1	0.15	1	1	1
M_{25}	0.27	0.27	0.15	1	1	1
M_{26-27}	1	1	0.15	1	1	1
M_{28}	0.27	0.27	0.15	1	1	1
			LATCH SR			
M_{0-5}	0.27	0.27	0.15	1	1	1
			PWM Circuit			
M_0	3.000	1.500	1.00	1	2	1
M_{1-3}	4.200	0.700	2.00	1	6	3
M_4	0.600	0.300	2.00	1	2	2
M_5	2.565	0.285	2.00	2	9	2
M_{TGP}	0.270	0.270	0.15	1	1	1
M_{TGN}	0.270	0.270	0.15	1	1	1
M_{6-10}	8.000	8.000	0.15	1	1	1
M_{11-13}	0.270	0.270	0.15	1	1	1

4.2. Layout Considerations

After performing the schematic verification of the PWM circuit design, the layout design was carried out, as shown in Figure **4.1**. In this process, various techniques were implemented to minimize parasitic effects that could affect the behavior of the PWM circuit.

Figure 4.1. PWM circuit Layout.



The layout design utilized M1, M2, M3, and M4 layers for general interconnections, while MOM capacitors employed layers M1 to M6 to optimize area usage. A scaled layout was created, ensuring each block functioned correctly. For critical components like the OpAmp differential pairs and comparators, a common centroid approach was implemented for better matching, alongside an interdigitated technique for current mirrors to ensure symmetry. A guard ring was added for bulk connections of similar MOS transistors to reduce resistance and mitigate latch-up. Care was taken to minimize distances between connected components, particularly in the oscillator circuit, to avoid significant delays that could impact performance. After completing the layout connec-

tions, design rule checking (DRC) and layout vs. schematic (LVS) comparisons were conducted, followed by parasitic component extraction (PEX) and simulations to evaluate PWM circuit performance.

4.3. Schematic and Post-Layout Results

In this section, the results of each block composing the PWM circuit will be presented, as well as the complete circuit at the TOP level, where the schematic level design results and post-layout results are shown. The selected corners consider the slow/fast process variation for the MOSFET transistors and the passive devices, such as MOM capacitors and polysilicon resistors. The supply voltage varies ±10%, and the temperature ranges from -40 to 125 ℃. Statistical tests (MC) were performed on 1400 samples. Due to the changes caused by parasitic effects after extraction (PEX), the trimming values are modified as follows(See table **4.3**).

Table 4.3. Words for each process corner combination for schematic and post-layout.

Corner(R - C)	**Schematic**					**Post-Layout**				
	b_0	b_1	b_2	b_3	b_4	b_0	b_1	b_2	b_3	b_4
TT-TT	0	1	0	0	1	1	1	0	0	1
TT-SS	0	0	1	1	1	1	0	1	1	1
TT-FF	0	1	1	0	0	0	0	1	1	0
SS-TT	0	1	1	0	1	0	1	0	1	1
SS-SS	0	1	1	1	1	1	1	1	1	1
SS-FF	1	1	1	1	0	0	0	0	0	1
FF-TT	0	1	1	1	0	1	1	1	1	0
FF-SS	0	0	0	1	1	1	0	0	1	1
FF-FF	0	0	0	0	0	0	1	0	0	0

4.3.1. OpAmp

Based on the specifications Table **3.2** of the OpAmp, Transient, and AC Analysis simu-

lations were performed to observe the operation of the designed OpAmp, verifying that the specifications were met across PVT corners, as well as in MC random variations. Additionally, measurements of other parameters of the OpAmp were taken to verify the final design thoroughly. The schematic and Post-Layout PVT simulation results are shown in Table **4.4**.

Table 4.4. PVT simulation OpAmp.

Parameter	**Condition**	**Tarjet**	**Schematic**			**Post-layout**		
			Min	**Typ**	**Max**	**Min**	**Typ**	**Max**
A_o [dB]		> 63	91.5	96.3	99.4	91.36	96.38	99.45
G_M [dB]		> 10	20.4	39.6	44.0	21.68	37.04	39.89
P_M [º]		> 45	49.7	74.5	103.5	45.5	70.57	95.19
PSR [dB]	@DC	< 2.6	-53.1	-25.6	-14.4	-52.46	-22.76	-3.64
ICMR [V]	$80\%A_o$ criterion	TBS	1.2	1.6	2.0	1.25	1.64	2.06
CMRR [dB]	@DC	TBS	93.12	115.1	138.0	76.82	108.5	128
UGBW [dB]		TBS	6.5	10.8	33.5	6.22	10.32	30.82
T_{ss} [ns]	$\Delta vin = 10mV$	TBS	39.1	53.1	121.3	52.7	52.7	125.4
P_w [uW]		TBS	6.2	7.1	8.2	6.41	7.21	8.02
$Ivdd_{PD}$ [pA]	PD_{PWM}= Vdd	TBS	6.9	16.2	686	8.66	18.01	601.8

The schematic and Post-Layout MC simulation results are shown in Table **4.5**.

Table 4.5. Monte Carlo simulation OpAmp.

Parameter	**Condition**	**Tarjet**	**Schematic**		**Post-layout**	
		σ	**Mean**	σ	**Mean**	σ
V_{os} [mV]		3	0.012	1.784	0.147	1.807

Based on the results from the schematic and post-layout simulations, all the proposed specifications in the frequency variation analysis for the operational amplifier were met, as were the stability criteria.

4.3.2. Comparator's

Based on the specifications table **3.3** of the comparators, Transient, AC, DC, and Noise Analysis simulations were performed to observe the operation of the designed comparator, verifying that the specifications were met across PVT corners, as well as in Monte Carlo (MC) random variations. Additionally, measurements of other parameters of the comparator were taken for a complete verification of the final design. The schematic and Post-Layout PVT simulation results are shown in Table **4.6**. PVT specifications were satisfactorily met.

Table 4.6. PVT simulation Comparator.

Parameter	**Condition**	**Target**	**Schematic**			**Post-Layout**		
			Min	**Typ**	**Max**	**Min**	**Typ**	**Max**
A_o [dB]		> 70	99.54	109.1	116.9	93.73	111	119.7
BW[MHz]		> 2.2	3.167	6.344	6.578	2.204	4,624	4.981
UGBW [GHz]		TBS	1.068	1.471	1.918	0.826	1.177	1.53
td_{LH}[ns]	Vin = 5mV	< 7.5	2.548	3.274	4.342	2.921	4.054	5.05
td_{HL}[ns]	Vin = 5mV	<7.5	2.235	2.897	4.196	3.116	4.089	6.208
td_{LH}[ns]	Vin = 20mV	< 3.5	1.696	2.093	2.787	2.124	2.59	3.35
td_{HL}[ns]	Vin = 20mV	<3.5	1.599	2.008	2.819	1.989	2.507	3.517
SR [V/us]	Vin = 1.8 V	TBS	1251	1951	2704	1175	1817	2502
Static Current Low [uA]	Vinn = 900 mV Vout Low	TBS	32.41	36.65	37.35	32.97	37.8	38.37
Static Current High [uA]	Vinn = 900 mV Vout High	TBS	17.94	22.15	22.83	17.88	22.82	23.43
ICMR [V]		TBS	1.231	1.481	1.621	-	-	-
Ivdd [uA]		TBS	27.78	30.13	31.33	28.27	31.09	32.12
$Ivdd_{PD}$ [pA]	PD_{PWM} = Vdd	TBS	9.621	17.2	1316	11.54	20.29	1108
Pavg [uW]		TBS	45.01	54.31	62.1	45.79	55.95	63.61

The schematic and Post-Layout MC simulation results are shown in Table **4.7**.

Table 4.7. MC simulation Comparator.

Parameter	Condition	Target	Schematic		Post-Layout	
		σ	Mean	σ	Mean	σ
Input Referred Offset [mV]		$\pm$ 4.5	-555.3n	3.822	497.5u	3.864
tdLH[ps]	Vin = 20mV	$\pm$ 300	2133	243.92	2533	261.9
tdHL[ps]	Vin = 20mV	$\pm$ 300	2034	204.68	2645	301.2
Ivdd [uA]		TBS	30.27	1.47	31.16	1.538

The comparator's results at the schematic level indicated that all proposed specifications were met during the analysis of switching frequency variations in both PVT and Monte Carlo simulations. In post-layout simulations after extraction, a deviation of 17 ps from the specification was observed for PVT variations with a 20 mV input. In comparison, Monte Carlo simulations showed a deviation of 1.2 ps. Since these deviations are minor and have a negligible impact on frequency, it can be concluded that all comparator specifications at the post-layout simulation level were successfully achieved.

4.3.3. Ramp Generator

Based on the specifications table **2.1** of the PWM circuit, Transient and phase Noise Analysis simulations were performed to observe the operation of the designed Ramp generator, verifying that the specifications were met across PVT corners, as well as in Monte Carlo (MC) random variations. Additionally, measurements of other parameters of the Ramp Generator were taken to complete the verification of the final design. The schematic and Post-Layout PVT simulation results are shown in Table **4.8**.

Table 4.8. PVT simulation Ramp Generator.

Parameter	Condition	Tarjet	Schematic			Post-layout		
			Min	Typ	Max	Min	Typ	Max
F_{ramp} [MHz]		[1.8, 2.2]	1.909	2.000	2.098	1.907	1.993	2.105
V_m [V]		TBS	0.418	0.421	0.427	0.419	0.423	0.434
V_{errorL} [mV]		TBS	15.17	17.98	24.14	15.15	18.65	29.06
V_{errorH} [mV]		TBS	1.91	3.55	4.12	1.27	4.695	5.33
SR_{rise} [kV/us]		TBS	869	914	954	874	911	957
SR_{fall} [MV/us]		TBS	7.87	8.17	8.96	7.94	8.12	8.95
P_{noise} [dBc/Hz]	@1kHz	TBS	-51.61	-49.6	-44.46	-51.18	-48.1	-46.7
	@10kHz	TBS	-78.96	-76.49	-71.35	-78.27	-74.93	-73.8

The schematic and Post-Layout MC simulation results are shown in Table **4.9**.

Table 4.9. Monte Carlo simulation Ramp Generator.

Parameter	Condition	Tarjet	Schematic		Post-layout	
		σ	Mean	σ	Mean	σ
F_{ramp} [MHz]		0.066	1.998	0.0304	1.993	0.0295
V_{errorL} [mV]		TBS	18.22	3.93	18.73	4.03
V_{errorH} [mV]		TBS	3.69	3.82	4.78	3.73

All specifications proposed in the Ramp Generator Circuit are met based on the results from the schematic and post-layout simulations. A maximum error in amplitude error V_m of 8.5% was obtained, and of this percentage of error in amplitude 7.25% is for the lower voltage, which coincides with the previous analysis, with a σ of 4mV for V_{errorL} and a sigma of 3.7mV for the voltage V_{errorH}.

4.3.4. PWM Circuit

Based on the specifications Table **2.1** of the PWM circuit, Transient Analysis simulations were performed to observe the operation of the designed PWM circuit, verifying that the specifications were met across PVT corners, as well as in Monte Carlo ran-

dom variations. Additionally, measurements of other parameters of the PWM circuit were taken to verify the final design thoroughly. The schematic and Post-Layout PVT simulation results are shown in Table **4.10**.

Table 4.10. PVT simulation PWM Circuit.

Parameter	**Condition**	**Tarjet**	**Schematic**			**Post-layout**		
			Min	**Typ**	**Max**	**Min**	**Typ**	**Max**
F_{ramp} [MHz]		[1.8, 2.2]	1.909	2.000	2.098	1.907	1.993	2.105
Duty Cycle [%]	@Vctrl = 0.8V	TBS	51.34	51.65	52.8	51.39	51.8	53.96
Duty Cycle Min [%]		TBS	2.71	3.53	4.93	2.78	3.76	5.98
Duty Cycle Max [%]		TBS	97.58	97.79	98.32	97.82	98.04	98.18
I_{vdd} [uA]		$<$200	97.12	111.2	114.2	98.15	114.9	117.9
I_{vddPD} [nA]	PD = Vdd	TBS	0.041	0.094	10.43	0.060	0.112	8.7
P_w [uW]		TBS	157.3	200.1	226.2	159	206.7	233.5

The results from the schematic and Post-Layout MC simulations are shown in Table **4.11**.

Table 4.11. Monte Carlo simulation PWM Circuit.

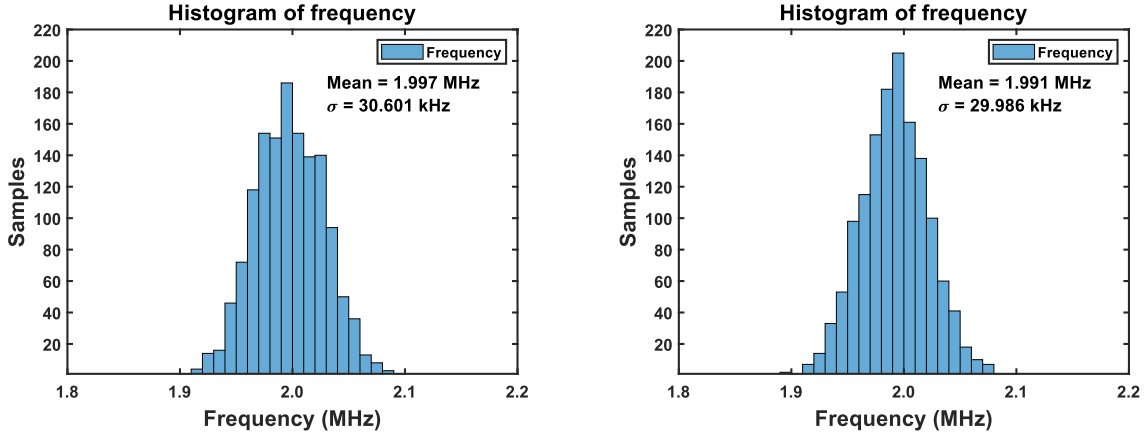
Parameter	**Condition**	**Tarjet**	**Schematic**		**Post-layout**	
		σ	**Mean**	σ	**Mean**	σ
F_{ramp} [MHz]		0.066	1.997	0.0306	1.991	0.02998
Duty Cycle [%]	@Vctrl = 0.8V	TBS	51.66	1.08	51.88	1.036
I_{vdd} [uA]		TBS	111.3	2.76	115.1	2.768

Based on the results from the schematic and post-layout simulations, all specifications proposed in the PWM Circuit are met. A post-layout frequency error of 5.25% was obtained for the maximum frequency and 4.65% for the minimum frequency. The 3σ error was 4.45%, meeting the design specification of 10%, with a maximum error of

9.67%. Additionally, the current consumption specifications were met, with a maximum consumption of 117.9 uA and a σ of 2.7 uA. The power budget for the PWM was 0.1% of the DC-DC converter's load current, which is 200 mA, ensuring an energy-efficient PWM.

Figure **4.2** shows the statistical simulation results for both schematic and post-layout levels. It can be observed that both maintain an average close to 2 MHz, with a standard deviation of 30.6 kHz for the schematic design and 29.98 kHz for the post-layout design. This implies that in the 3σ analysis, the error remains at 4.59% of the nominal switching frequency of 2 MHz for the schematic and 4.49% for the post-layout.

Figure 4.2. Monte Carlo simulation results for the PWM circuit.

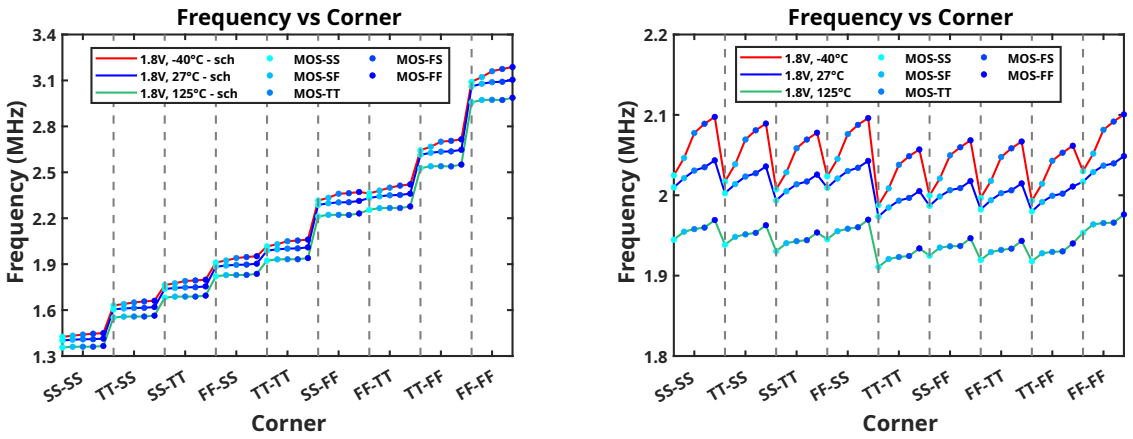


(a) Schematic (b) Post-Layout

In Figure **4.3(a)**, the changes in the switching frequency can be observed due to process variations (transistors and passive elements) and temperature when the ramp generator circuit does not include the trimming implementation. The frequency varies from 1.355 MHz to 3.187 MHz, exceeding the frequency specification required by the buck DC-DC converter. In Figure **4.3(b)**, each combination shown in Table **4.3** can be observed, along with process variations of the transistors in the blocks that make up the PWM circuit and the Ramp generator. This figure shows the post-layout simulation results when trimming is implemented for temperatures of -40 ℃, 27 ℃, and 125

℃, with a supply voltage of 1.8 V. By implementing trimming, the frequency variations are constrained within the specification, leaving a margin of plus or minus 5% for errors caused by Monte Carlo variations. After trimming, the most significant frequency change is due to temperature variations, as this change causes a 3% error in the ramp frequency. In contrast, the error produced in the frequency by process variations of the transistors does not exceed 1%.

Figure 4.3. PVT simulations for Frequency Vs. Corner without trimming and with trimming.

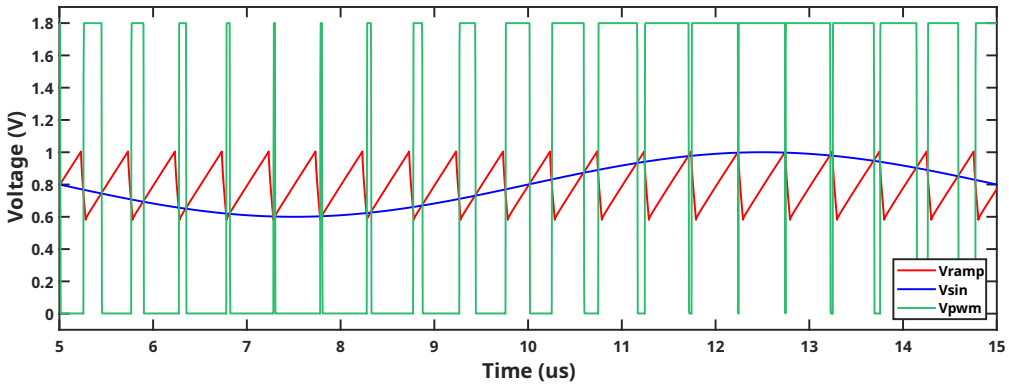


(a) Frquency Vs Corner

(b) Frequency Vs Corner

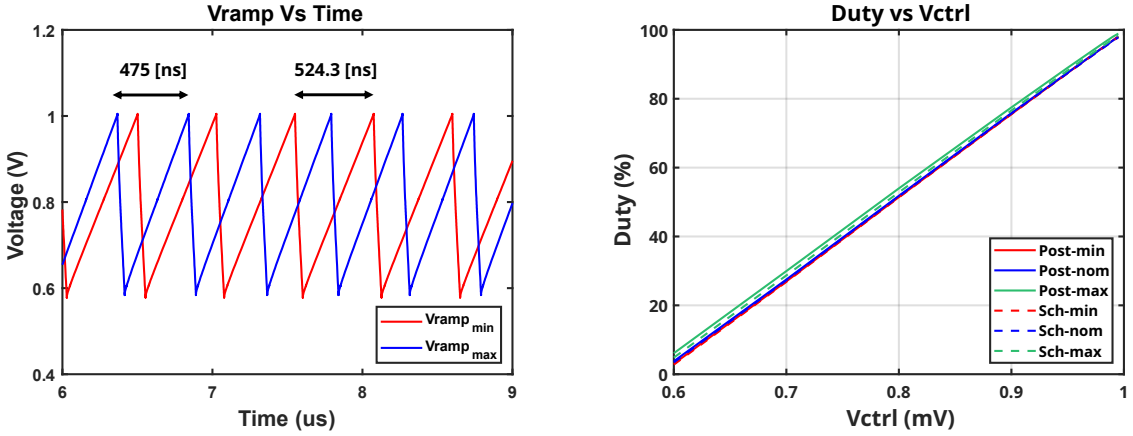
In Figure **4.4**, the waveforms of the PWM and sawtooth signals can be observed, where pulse-width modulation is performed with a sinusoidal modulating signal at a frequency of 125 kHz and a carrier signal at 2 MHz, resulting in a pulse-width modulated (PWM) signal. In **Figure 4.5(a)**, the waveforms of the sawtooth signals in the corners of maximum and minimum period can be observed, corresponding to the upper and lower frequency limits, respectively. A phase shift caused by the difference in switching frequency is observed, and this phase shift would be much more significant without the trimming implementation, resulting in greater efficiency losses in the converter. In Figure **4.5(b)**, where 'sch' is schematic and 'post' is post-layout, the relationship between the duty cycle and the control voltage from the VCM circuit is shown. This signal represents the error voltage, which is the difference between the converter output and the

Figure 4.4. PWM circuit in operation.



reference voltage, where the duty cycle can vary, in the worst case, from 6% to 97%. By adjusting the duty cycle, line and voltage variations in the DC-DC converter can be effectively controlled.

Figure 4.5. PVT simulations for a Maximum and Minimum period and Duty Range graph.



(a) Vramp Vs Time

(b) Duty Vs Vctrl

4.4. Comparison With Other Projects

A comparative analysis of the results obtained by previous projects of PWM circuits and ramp generators, with the results of this work, highlights a greater accuracy in the

switching frequency and the amplitude of the ramp in PVT; also statistical variations were made in Monte Carlo, for a more robust design, since in the other papers such variations were not reported, In addition, the lowest power and area consumption was obtained concerning the compared projects, it should be clarified that in [17] an actual Bandgap reference is used which is part of the power and area consumption, likewise in [10] only the power and area consumption of the ramp generator was reported, at the same time the highest duty cycle range of the comparison was obtained.

Table 4.12. Performance Comparison.

Specification	[**Doloriel**]**	[**Liu**]**	**This Work**
Technology	65nm	130nm	28nm
Supply Voltage (V)	1.2	3.7	1.8
Frecuency (MHz)	1	10	2
Duty Cycle range (%)	47.70	[x - 87.5]	[3.8 - 98]
Ramp amplitude error voltage (%)	-	12.3	5.43
Power Consumption (mW)	0.431	0.240	0.206
Variation of frequency PVT (%)	-	9	5.25
Variation of frequency 3σ (%)	-	-	4.5
Area (mm^2)	0.420	-	0.04995
Waveform	PWM and Ramp	Ramp	PWM and Ramp

**Post-layout.

[17] Chandler Timm C. DOLORIEL and Aileen B. CABEROS. "High Speed CMOS Pulse Generator Based on Analog Ramp Signal Implemented in 65nm CMOS Process Technology". In: *2019 19th International Symposium on Communications and Information Technologies (ISCIT)*. 2019, pp. 578–583. DOI: 10.1109/ISCIT.2019.8905203.

5. CONCLUSIONS AND FUTURE WORK

5.1. Conclusions

This work describes the design of an analog PWM circuit operating at 2 MHz, designed in TSMC 28 nm CMOS technology, for a DC-DC Buck Converter, which will be integrated into a System on Chip (SoC). The project began by conducting an exhaustive analysis of the most optimal topology for applying the PWM circuit, where a high-precision ramp generator was desired. Therefore, a modification of the conventional topology was chosen, adding a discharge source and implementing trimming, resulting in a PWM circuit and a high-precision with low power consumption.

Using the proposed design methodology, based on a budget of both deterministic (PVT) and random (MC) errors in the frequency, and distributing these errors according to their impact on the independent variables that affect the ramp frequency, the specifications for each block that composes the PWM circuit were defined. As a result, a PWM circuit design was obtained with a frequency error due to PVT variations of ±4.9% and an error due to 3σ MC variations of ±4.59%. This allowed the creation of a high precision PWM circuit, robust to PVT + MC variations, maintaining an error margin of less than ±10% with respect to the nominal frequency of 2 MHz. These simulations were performed at schematic level.

Layout design was done, with a total area usage of approximately 48.39x103.23 μm^2; techniques such as common centroid and interdigitated connections were utilized, and an optimal distribution of metal connections was implemented to minimize parasitic capacitances and resistances at the critical nodes of the PWM circuit, thereby minimizing frequency variations caused by these parasitics in the layout.

Post-layout simulations were performed using a new circuit model with parasitic ex-

traction. The deviations were 5.25% at the maximum frequency and 4.65% at the minimum frequency, with a frequency error due to variations in MC at 3σ of 4.497%. This resulted in a high-accuracy PWM circuit, robust against PVT + MC variations, with an error of less than $\pm$10% with respect to the nominal 2 MHz frequency in post-layout simulations. In addition, a maximum voltage error in the ramp amplitude of 8.5% was obtained, caused mainly by the delay of the low reference comparator(VL). The PWM circuit also delivered a worst-case duty cycle between [6% - 97%]. The maximum measured power consumption was 233.5 uW, meeting all required specifications in each PVT corner and in the Monte Carlo tests. Compared to typical specifications of different PWM circuits and ramp generators for DC-DC converters, this design stood out for its higher accuracy and robustness to PVT + MC variations, in addition to low power consumption and reduced design area.

An efficient PWM circuit was designed employing a current budget, obtaining a maximum current consumption of 117.9 uA, representing less than 0.1% of the DC-DC load current, equivalent to 200 mA. This design is considered efficient because the losses produced by the PWM circuit are not considerable at a TOP level in the DC-DC converter due to the low power consumption.

5.2. Future Work

- Designed and implemented the PWM circuit, it is desired to implement real bias circuits, such as Bandgap reference and current references, previously developed in the Onchip research group, to test the performance of the PWM circuit when these circuits are no longer ideal.
- Test the behavior of the Buck DC-DC converter in an IP environment, with all the blocks that compose it, to check its performance and the impact of blocks such as the PWM circuit or the voltage mode compensator (VMC).

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