CHARGE PUMP FOR EMBEDDED NONVOLATILE MEMORY (eNVM) IN 0.13 µm CMOS TECHNOLOGY

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CONTENTS

Page.

LIST OF TABLES

Page

LIST OF FIGURES

Page

RESUMEN

Título BOMBA DE CARGA PARA UNA MEMORIA NO VOLÁTIL EMBEBIDA (ENVM) EN TECNOLOGÍA CMOS 0.13 µm *

Autor Rodrigo Andrés Gómez Pérez **

Palabras clave Bomba de carga, Comparador Dinámico, Corners, eNVM, Layout, Regulación de carga, Regulación de línea.

DESCRIPCIÓN

Este informe presenta el diseño y la caracterización de un circuito de bomba de carga para una memoria no volátil embebida (eNVM) en la tecnología CMOS de 130nm. El diseño propuesto utiliza una bomba de carga dinámica con switch de transferencia de carga (CTS), un comparador dinámico de doble cola y un generador de reloj sin traslape. La bomba de carga se basa en un esquema de aumento de frecuencia para controlar los picos de corriente durante la operación de escritura en la memoria. Durante el proceso de diseño se verificaron la mayoría de los casos críticos de PVT; estas simulaciones de esquinas verifican las características eléctricas del sistema de bomba de carga para cumplir con los requisitos de escritura y borrado de la memoria eNVM. El circuito de bomba de carga diseñado utiliza una fuente de alimentación de 1,2 V, tensión de referencia de 0,6 V y frecuencia máxima de operación de 100 MHz. Los resultados experimentales muestran una tensión de salida de 5,5 V con una tensión de rizado de salida de 39 mV para una frecuencia de conmutación de 100 MHz. La regulación de línea muestra la robustez del sistema a las variaciones de VIN. Cuando la tensión de entrada desciende 200mV, la variación de voltaje de salida es de aproximadamente 134mV. Un aumento en la tensión de entrada de 300mV implica, en la tensión de salida, una variación de 54mV. Además, la bomba de carga presenta una eficiencia del 83% para una corriente de salida de 10 µA y un tiempo de asentamiento de 5 µs.

* Trabajo de grado

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ABSTRACT

Title CHARGE PUMP FOR EMBEDDED NONVOLATILE MEMORY (eNVM) IN 0.13µm CMOS TECHNOLOGY *

Author Rodrigo Andrés Gómez Pérez **

Keywords Charge Pump, Corners, Dynamic Comparator, eNVM, Layout, Load Regulation.

DESCRIPTION

This report presents the design and characterization of a charge pump circuit for embedded non-volatile memory (eNVM) in 130nm standard CMOS technology. The proposed design uses a charge pump with dynamic charge transfer switch (CTS), a double tail dynamic comparator and a Non-Overlapping Clock Generator. The charge pump is based on a frequency step-up scheme to control the surge current during a memory write operation. The most cases critical of PVT were considered during the design process, these corners simulations verify the electrical characteristics of the charge pump system for achieve to meets the requirements in the write and erase of the Memory eNVM. The Charge pump circuit designed uses a power supply of 1.2 V, referent voltage of 0.6 V and maximum operating frequency of 100 MHz. Experimental results show an output voltage of 5.5 V with an output ripple voltage of 39 mV for a switching frequency of 100 MHz. The line regulation shows the system robustness to VIN variations. When the unregulated supply descends 200mV, the output voltage variation is about 134mV. An increase in the input voltage of 300mV implies, in the output voltage, a variation of 54mV. Moreover, the charge pump presents an efficiency of 83% for an output current of 10 µA, and a settling time of 5 µs.

* Bachelor degree

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INTRODUCTION

Nowadays, the development of portable devices for the Internet-of-Things (IoT) applications is setting a trend in the emerging market. The demand for mobile electronic products has brought great design challenges including more functionalities whereas low power, small size and low cost specifications are maintained. These characteristics are linked to an increase in integration density (i.e. downscaling of CMOS technology), looking for an increment in processing speed and temporary and permanent storage. In the latter case, the embedded non-volatile memories (eNVM) have become essential devices because of its use in storing results of Arithmetic Logical Units (ALU), ICs parameter control (initialization), sensors control and microcontroller programming.

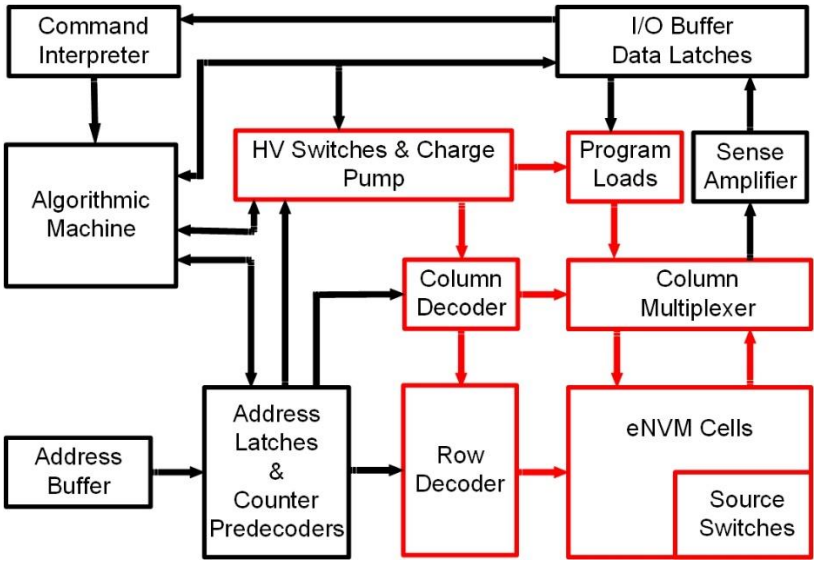
eNVM requires different voltage levels to properly operate, which are generated by a subsystem called charge pump circuit. This circuit establishes an output voltage higher than its input level, being crucial for write and erase operations in this type of memories [1]. Most of the charge-pump circuit designs are based on the topology proposed by Dickson. The Dickson circuit uses two capacitors, two diodes and two clocks signals with a 180º phase difference and a peak amplitude equal to the supply voltage. The diodes of Dickson circuit may be replaced by NMOS transistors increasing the efficiency [2]. However, the modified circuit is limited by the threshold voltage of the NMOS devices and the phenomenon" reverse charge-sharing".

In order to overcome the aforementioned problems, Dickson proposed two improvements to the charge-pump circuit. Dickson charge pump uses dynamic charge-transfer switches CTS's (Design-2), uses (MSx transistors); in this case each of these transistors are controlled by MNx and MPx pass transistors. Thus, the charge transfer switches can be disabled completely when necessary and can be enabled more effectively by having higher voltage in the next step.
In this paper, a study, design, and characterization of a charge pump using dynamic charge-transfer-switch (CTS) is presented [3]. Design issues related to the control system and low-power consumption are described in order to obtain a high performance for embedded non-volatile memories (eNVM). Furthermore, the circuit was fabricated in a TSMC 130nm standard CMOS technology. The paper is organized as follows: section II describes the memory structure and operation principles; section III presents the charge-pump system including charge-pump dynamic Cts's and dynamic comparators; the charge pump circuit implementation and measurement results are given in section IV; finally, section V lists the main conclusions of this work.

1. MEMORY STRUCTURE AND OPERATION PRINCIPLES

The architecture of the eNVM memory is show in Figure 1. The system is composed by a programmable memory eNVM cell array, an I/O buffer data latch, a program load, a charge pump, an address latches and counter, a sense amplifier, a column/row decoders, and a column multiplexer. The operation that it carried out depends on the initialization commands. In the case of a writing operation, the input data are stored in a latch during a period of time. Later, the column and row decoder deliver the high voltages generated by the charge pump to the selected row or column in the cell array of the memory eNVM.

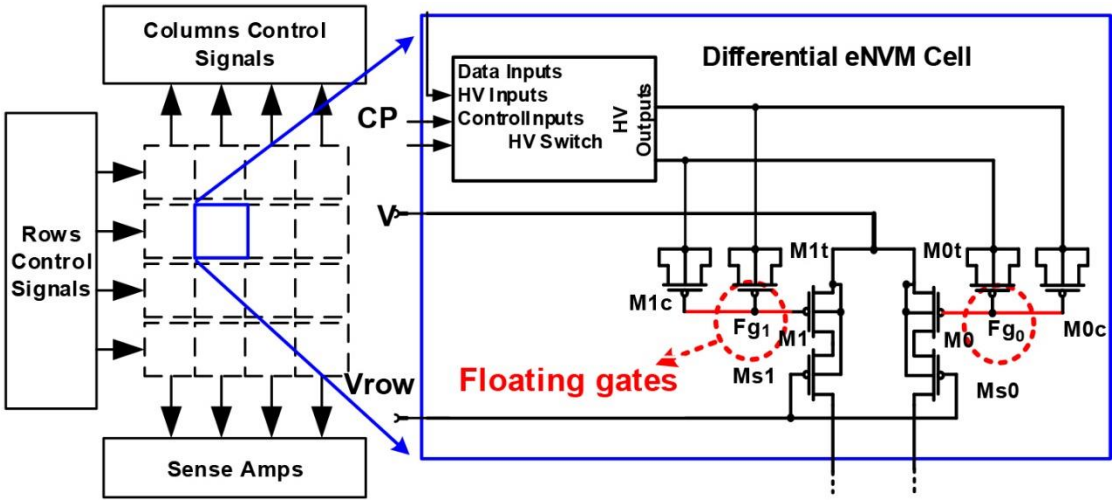
Figure 1. General eNVM architecture.



1.1 CELL STRUCTURE

Figure 1 shows a basic differential pFET eNVM memory cell [4]. This cell has two floating gates denoted Fg0 and Fg1. When the eNVM cell is powered through the terminal denoted “V”, it presents a difference between the readout currents I0 and I1. A conventional current sense amplifier is used to detect the logical value stored in the cells. For example, the condition I0 > I1 may be used to indicate the logic value “0” and the condition I0 < I1 may be used to indicate the logic value “1”.

Figure 2. Architecture of the bit cell array.

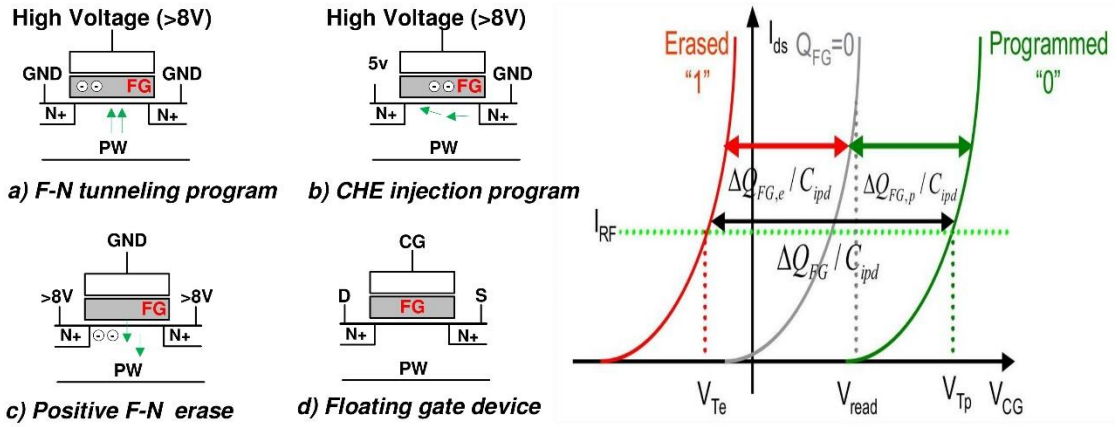


1.2 OPERATION PRINCIPLES

The floating-gate device is similar to a MOSFET transistor except that it has a floating gate (FG in Figure.3-d) surrounded by the insulators between the control gate (CG) and the P − well. Suppose a proof voltage is applied to the control gate CG with no charge stored in the floating-gate FG, the current will flow as long as the source to drain voltage is not zero, just like the operation of a conventional transistor. However, if some charge is stored in the floating-gate, the negative electrical field will counter-act with the positive field generated by the control gate voltage at the surface of the channel. As a result, the control gate voltage must be increased to maintain the current flow.

Figure. 3 shows the operation principles of the eNVM memory. The memory requires a lot of energy for a program (inject electron into FG) or erase (remove the electron from FG) operation. There are two effects that generate these operations, one is called the Channel-Hot-Electron (CHE) Injection [6] , and the other is called the Fowler-Nordheim (F-N) Tunneling [5]. The first one effect is used to program the a memory cell as shown Figure 3-a,b . The injection in this case occurs between the gate and a n+ diffusion. The second effect is shown in Figure 3-c in a erase operation. In this case the tunneling takes place between the gate and a p+ diffusion. Once the cell is programmed, it can be read by applying a moderate voltage (dotted line in Figure 3-e) on the control gate CG and sense the output current. If no current flows, a ”0” is read, otherwise a ”1” is read.

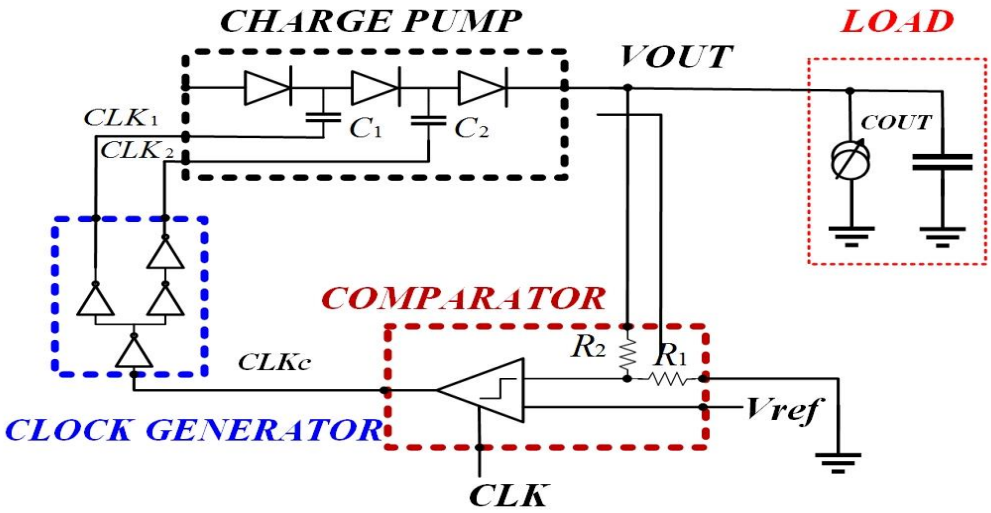
Figure 3. Floating gate NVM with program and erase



2. DESIGN CHARGE PUMP SYSTEM

In this section, the block diagram of the charge pump system is explained. The diagram for get charge pump output regulated are shown in Figure 4.

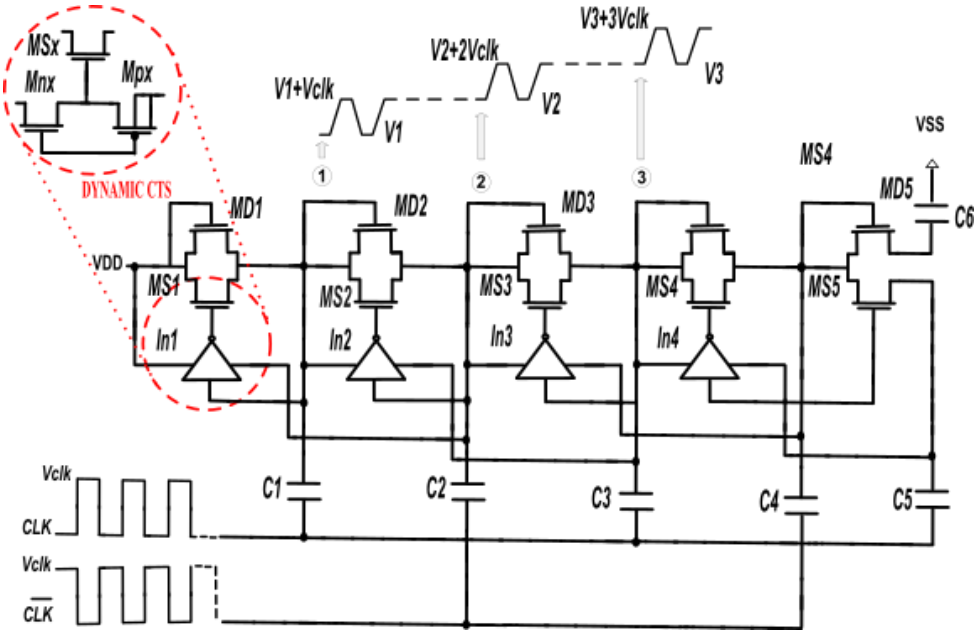
Figure 4. Charge Pump System



The charge pump circuit dynamic CTS'S [7], shown in Figure 5, employ pass transistors MNx and MPx to increase the voltage pumping gain and to dynamically control the charge transfer switch (CTS). The idea of use these multipliers is to use MOS switches with precise on/off characteristics to direct charge flow during pumping rather than using diodes, or diode connected transistors which inevitably introduce a forward voltage drop at each node. Each CTS is accompanied by an auxiliary pass transistor so that the CTS's can be turned off completely in the designated period. The gate control voltage of each CTS is assigned from the succeeding stage to backward control the charge transfer switch, so that the transfer device can be turned on completely as an ideal switch without suffering the limitation of threshold voltage. Finally, taking into account the requirements imposed by the eNVM memory, the output voltage of the charge pump needs to reach 5.1V. So, it is necessary to implement five stages to produce a response between 5.0V and 5.6V.

The operation of the charge pump circuit dynamic CTS'S is explained as follows. In Figure.5, Clk and Clkn are out-of-phase and have the same voltage amplitude Vclk.

Figure 5. Schematic Charge Pump using Dynamic CTS'S



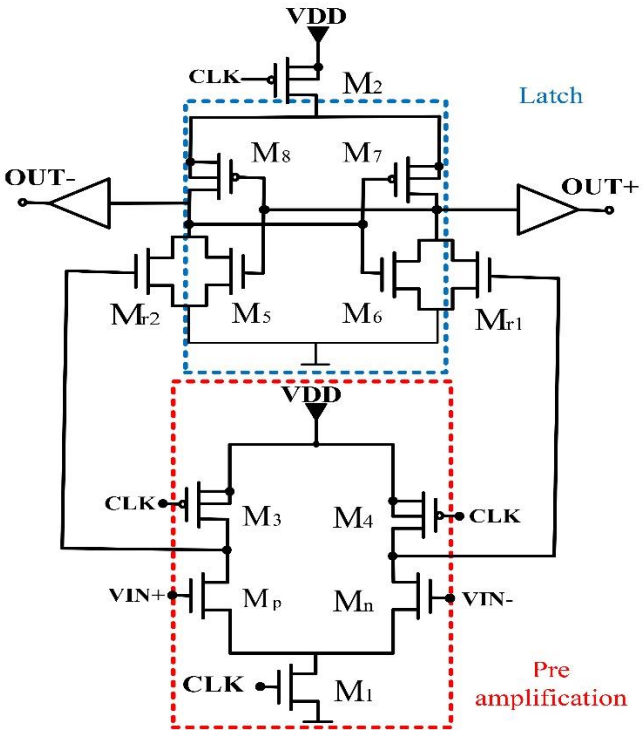
The MOS diode (MDx) is used to establish initial voltages. When Clk is high and Clkn is low, the voltage on node 1 can be transferred as high as V DD + Vclk to turn on MN1 and to turn off MP1. Thus, the gate voltage of MS1 would be at its low level and MS1 can be completely turned off to prevent charges back to the power supply. When Clk is low and Clkn is high, the voltage of nodes 2 and 4 are raised to higher potential levels, the pass transistor MN1 is off and MP1 is on, so it can be considered that the gate of MS 1 and the node 2 are connected. Since Clkn is high, the voltage of node 2 is pumped to high level V DD + 2Vclk . Therefore, by this high voltage of node 2 from succeeding stage, the charge transfer switch MS1 would be completely turned on to transfer charges from the power supply VDD to C1 waiting for the next clock state.

2.1 DYNAMIC COMPARATOR

The topology, shown in Figure. 6, corresponds to a conventional double-tail dynamic comparator. This circuit provides high insulation for kickback noise [10], which is generated due to high-frequency oscillations produced by the continuous establishment of high and low states. This isolation prevents that noise returns to inputs and degrades sensed signals. The delay time of this comparator is divided

into two parts: the first is defined by the load time in the capacitance coupled to each output, and the second is related to the establishment time the cross-coupled inverters regeneration time.

Figure 6. Double-Tail Dynamic Comparator topology.

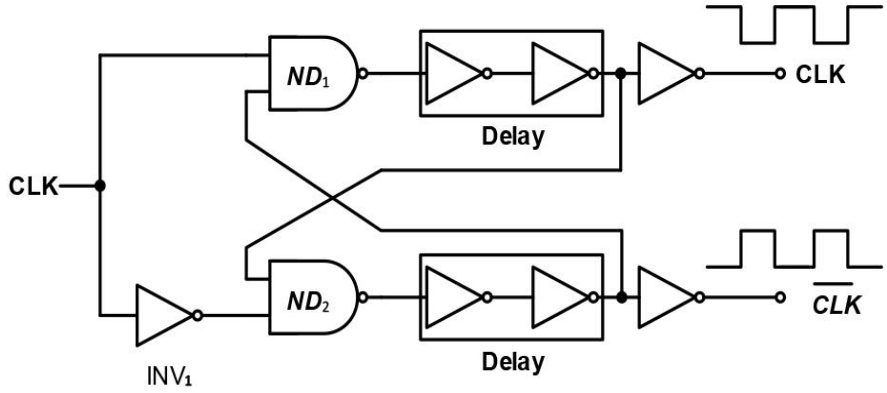


In the presence of a clock signal (CLK) circuit operation is conditioned by duality on the clock. This imposes two phases or two states in the device; for LOW values in the clock (CLK = 0) is called reset phase, while for HIGH values (CLK = VDD) we have the comparison phase. For reset phase transistors M1 and M2 both are cut off, making the Vp and Vn nodes are loaded with VDD and output nodes (OUT+ and OUT-) are discharged to ground through transistors Mr1 and Mr2. Once reset phase finish, comparison phase starts, when CLK = VDD transistors M1 and M2 turn on, Vp and Vn nodes start the discharge to different time constant which is proportional to each input voltage. This is, both depend on IM 1−M 2 CVp −Vn / (where IM 1−M 2 is transistor M1 − M2 drain current, and CVp −Vn is Vp and Vn node capacitance), thereby defining a differential voltage between Vp and Vn nodes, which depends on voltages applied to the gates of transistors Mn and Mp (comparator input).

2.2 CLOCK GENERATION CIRCUIT.

The non-overlapping control signals is used to drive the switched circuits with the objective of to avoid signal leakage during switching. An efficient design of a non-overlapping circuit leads to two requirements, minimize tov and to equalize phase and to maximize the frequency of operation t ov should be zero. This is admissible, if t ov cannot is negative under any circumstances (e.g. local and global process variations, temperature). Therefore, in most applications t ov is chosen to be slightly positive to ensure a certain tolerance margin. The generation of non-overlapping clocks be realized by the circuit shown in Figure 7.

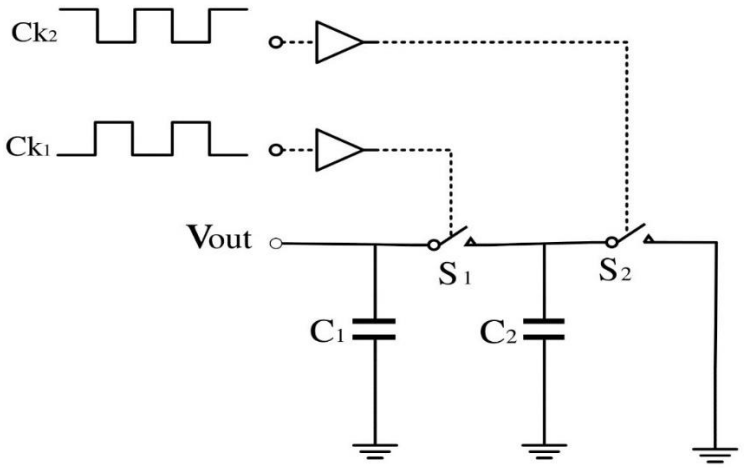
Figure 7. Schematic a Non-overlapping Clock Generator



3. IMPLEMENTATION AND EXPERIMENTAL RESULT

Then, simulations are presented charge-pump circuit based on the design specifications shown in the table I. Where it shows the operation of the circuit and its robustness against variations in the input voltage V in and the load C1. To emulate the loading and unloading of memory was implemented the circuit shown in Fig. 8.

Figure 8. Memory and Pin Model for Simulation Purpose.



3.1 SIMULATION RESULTS

Figure. 9 shows the transient simulation of waveforms of the charge pump circuit of five stages with an output voltage of 5.5 [V] where the simulation conditions are shown in the table 1.

Table 1. Specifications of Design Charge Pump

Specification	Value
Vin	1.2 V
CL	10 pF
Fsw	100 MHz
Ripple	50 mV
Vout	5.5 V

Figure 9. Output voltage vs Time for: TTNN PVT

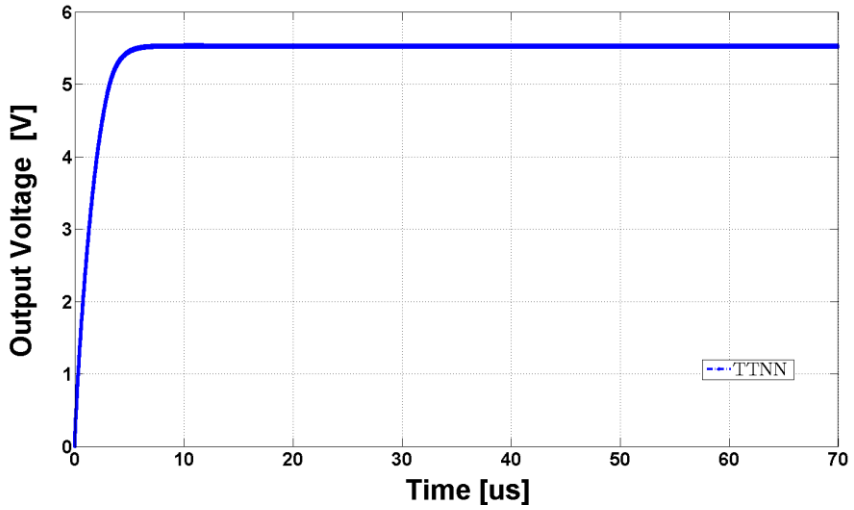


Figure. 10 a shows the simulated average output voltage and the ripple of the designed charge pump. The test conditions include a switching frequency of 100MHz and a load capacitance of 50pF. Furthermore, results include PVT variations for process corners and temperatures between -40 ºC and 120 ºC. In all cases, the output voltage is higher than 5.5V, meeting the requirements of an eNVM; also, the ripple is lower than 41mV, which does not affect write and erase operations.

Figure 10. Average Output Voltage and Ripple vs Temperature for: PVT results

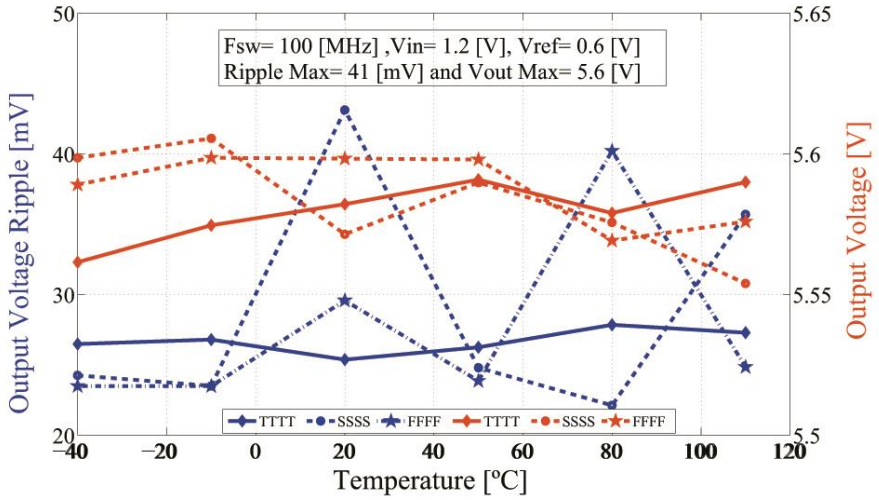
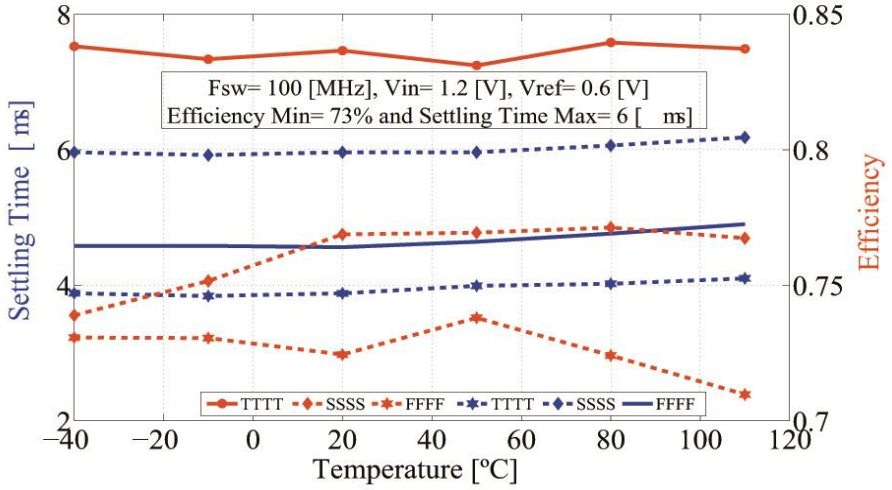


Figure. 11 presents the simulated settling time once the charge pump is turned on, which is lower than 6µs for all PVT cases. Moreover, the same Figure shows the efficiency of the circuit, achieving a minimum value of 70%.

Figure 11. Settling Time and Efficiency vs Temperature for:PVT results



Finally, the charge pump circuit with the dynamic comparator and clock generation circuit were fabricated in a 0.13µm CMOS technology; the charge pump system occupies a total area of 0.295x0.148mm is shown in figure 12.

3.2 EXPERIMENTAL RESULTS

Figure 13 y 14 shows the measured output ripple voltage for a total load capacitance of 30pF (including pads and PCB-wires capacitance) and a output current of 30µA; the maximum ripple is 39mV for an average output voltage of 5.5V. These characteristics prove that the fabricated charge pump meets the requirements for write and erase operations of the eNVM. Moreover.

Figure 12. Layout Charge Pump Circuit and its Control System.

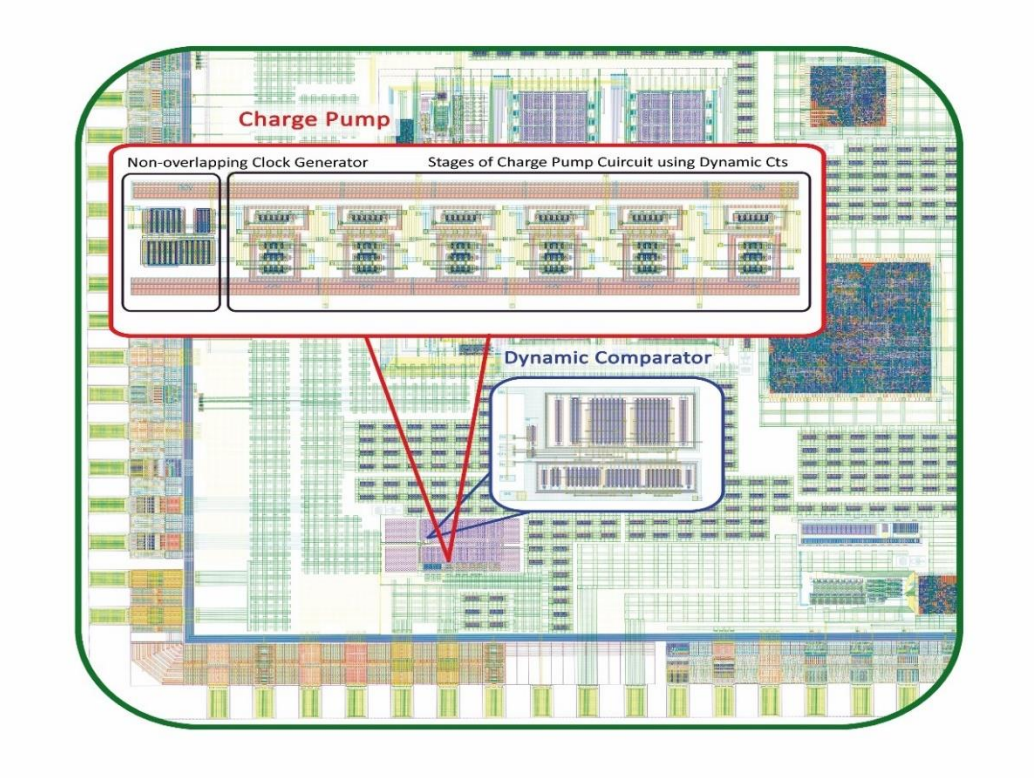


Figure 13. Experimental results for Output Voltage Ripple

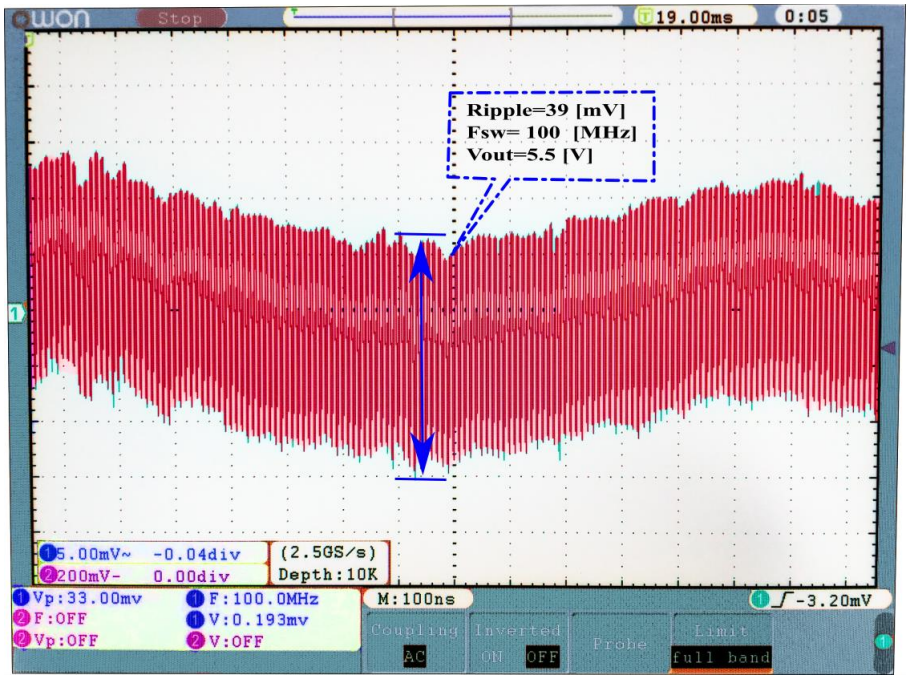
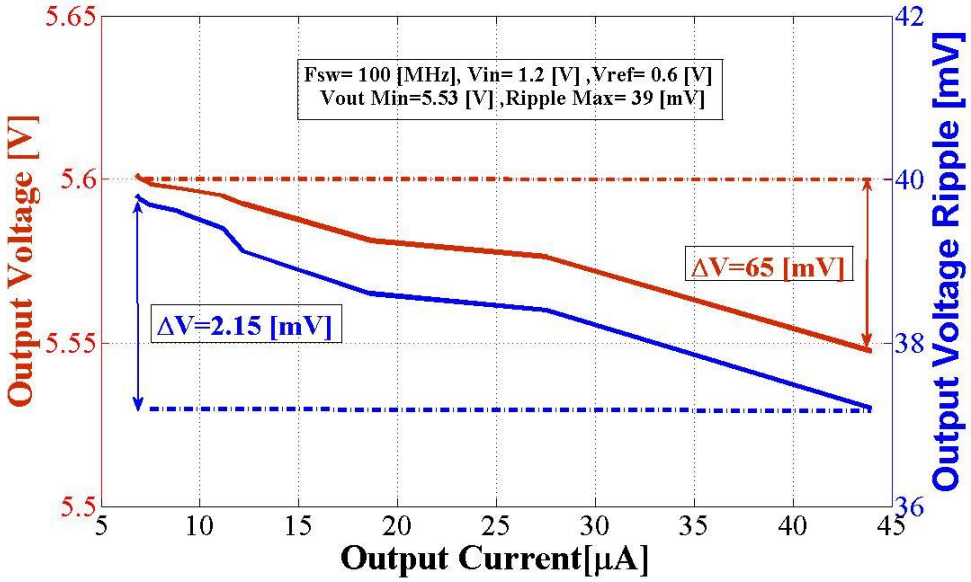


Figure 14. Experimental results for Vout and Ripple Vs Output Current



Figures 15 and 16 presents the load regulation, efficiency and line regulation respectively. The maximum output current is 45μA, reaching a efficiency of 72%; this is a notable aspect because previous designs reported in [8], [9] shows a maximum efficiency of 60% for eNVM applications.

Figure 15. Experimental results for Efficiency vs Output Current

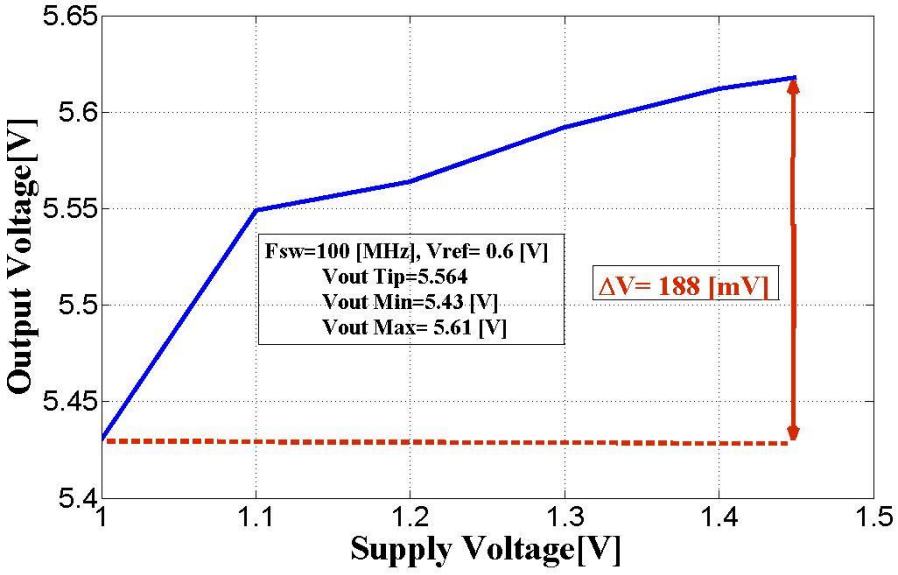
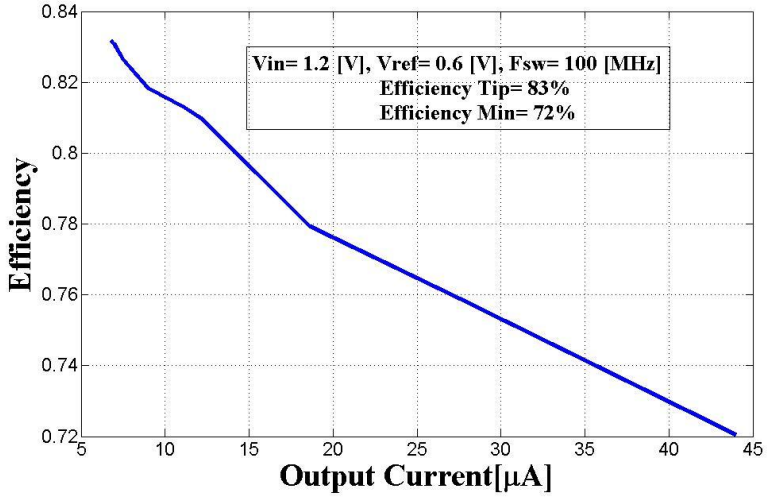
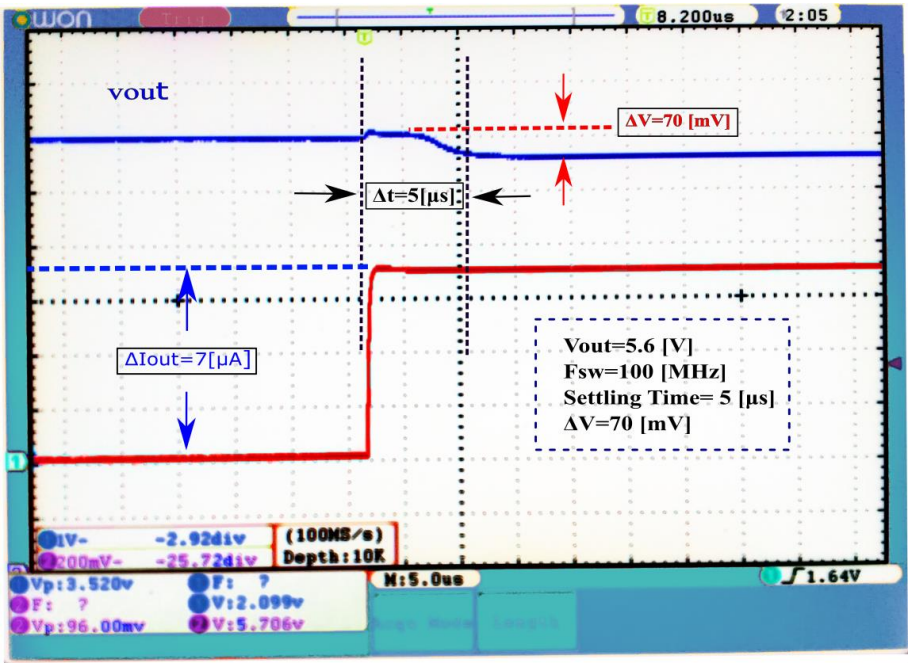


Figure 16. Experimental results for Line Regulation



Furthermore, Figure 17 exposes the transient behavior of the output voltage for a load change from 0 to 15µA; the settling time is 5µs for both charge and discharge process, proving the effectiveness of the control system. Finally, table I summaries the performance of the designed circuit.

Figure 17 Experimental Results for Settling Time



3.3 INTEGRATION WITH MRISC-V PLATFORM

The research group Onchip designed the first 32-bit microcontroller based on the RISC-V instruction set [11] show in figure 18. The 2x2mm chip is shown in figure 19 was taped-out in a 130nm process aiming to be the equivalent of commercial microcontrollers implemented with an ARM M0 core. The first prototype (mRISC-V) includes an AXI4-Lite and APB buses for linking the core to peripherals, a Serial Peripheral Interface (SPI), an 8 I/O GPIO module, a SAR 10-bit analog-to-digital converter, a 12-bit digital-to-analog converter, and supports 4 KBytes RAM.

Figure 18 First 32-bit microcontroller prototype

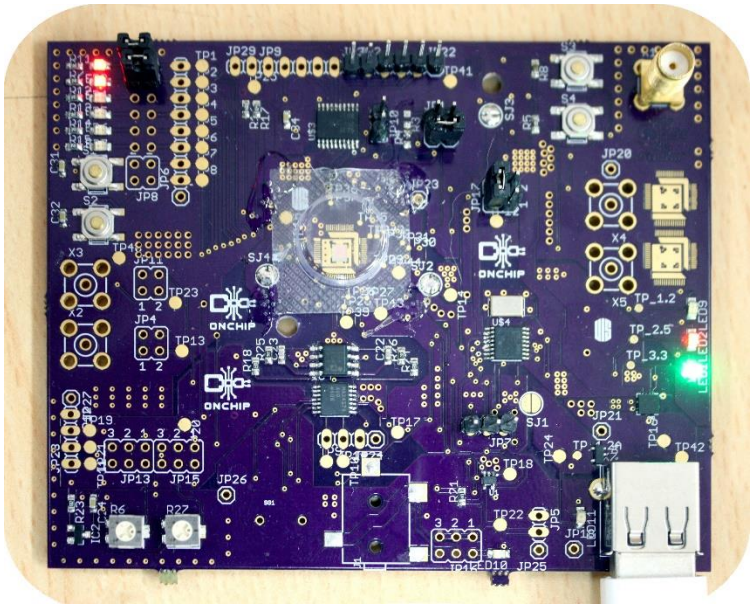
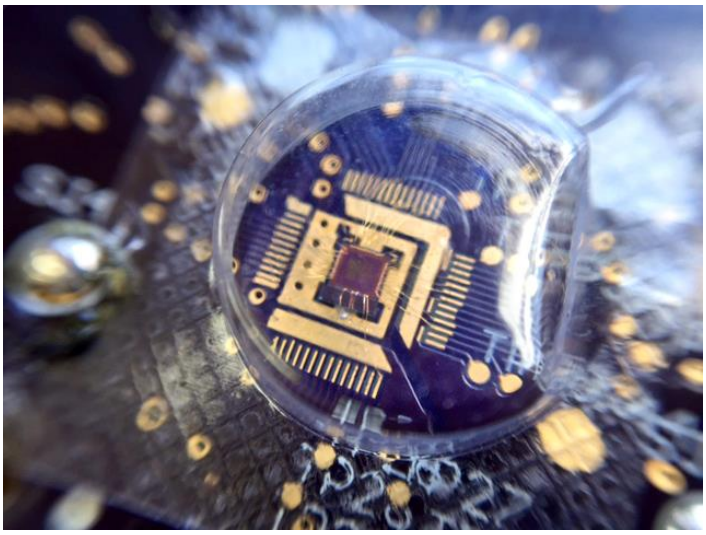


Table 2. Measured Performance of the Charge Pump

Specification	Value
Output Voltage	5.5 V
Ripple	39 mV
Efficiency	83% max
Settling Time	5 µs
Line Regulation	54 mV

Figure 19 First 32-bit microcontroller microcontroller based on the RISC-V instruction set



Currently, the group is designing the second version of the mRISC-V prototype in which Embedded nonvolatile memory (eNVM) will be included shown in figure 20,21 along with the charge pump circuit. Furthermore, it will be designed a complete Arduino-compatible development board with USB communication. For that reason, this first prototype of a charge pump plays an important role for the microcontroller in order to integrate a eNVM memory for enhancing functionality and programming purpose.

Figure 20 Microphotograph of the Charge Pump Circuit

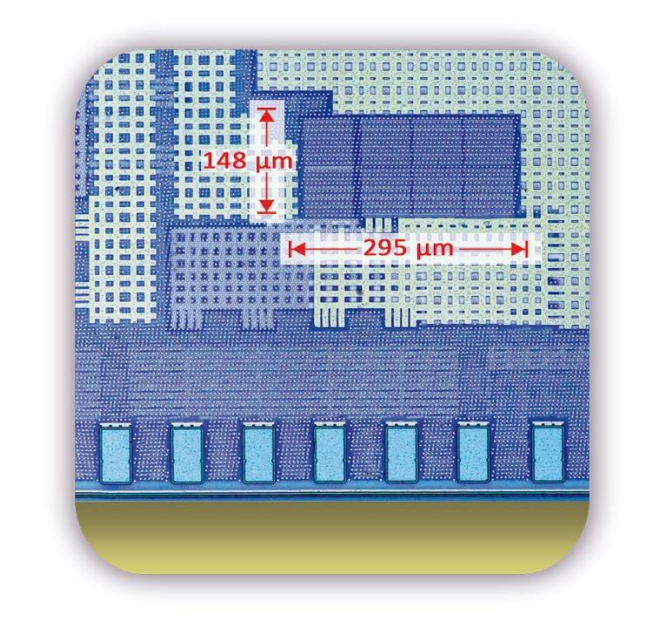
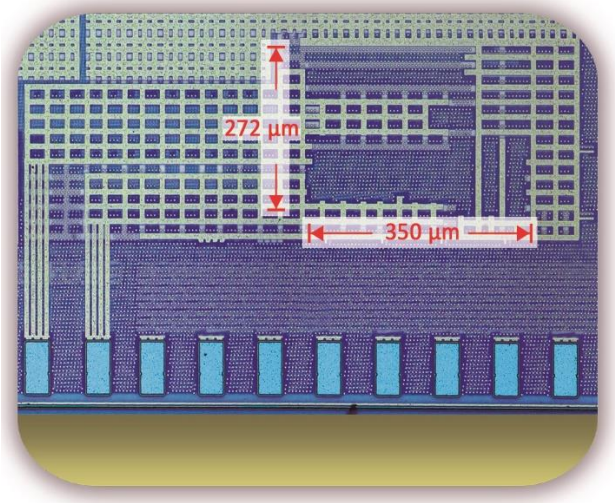


Figure 21 Microphotograph eNVM



4. CONCLUSION

A five stages charge pump system has been designed and tested at Fsw=100MHz, VDD=1.2V and C L =7pF reaching an output voltage of 5.4V, with a ripple of 40 mV, and settling time of 5µs. Experimental results of line regulation show the system robustness to V IN variations. When the unregulated supply descends 200mV, the output voltage variation is about 134mV. An increase in the input voltage of 300mV implies, in the output voltage, a variation of 54mV. The voltage conversion ratio efficiency is 83% for a load of C L =7pF.

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