DESIGN OF A LOW DROP OUT REGULATOR FOR POWER MANAGEMENT IN 28nm CMOS NODE FOR DIGITAL DOMAIN

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Degree work presented as a requirement to qualify for the title of Electronic Engineering

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Dedicated to my family and all members of the research group.

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PALABRAS CLAVE: REGULADOR DE VOLTAJE, MICROELECTRONICS, MICROCONTROLADOR, SoC, SEMICONDUCTORES, DIGITAL, BAJA POTENCIA,LDO.

DESCRIPCIÓN:

Los reguladores de baja caida (LDO) son importantes porque permiten obtener una salida de voltaje estable con una caída de voltaje mínima a través de ellos, incluso cuando el voltaje de entrada está cerca del voltaje de salida. Por lo tanto, los LDO pueden mantener un voltaje de salida constante incluso cuando el voltaje de entrada está fluctuando, lo que los hace ideales para su uso en dispositivos electrónicos portátiles y otras aplicaciones donde la eficiencia energética es prioritaria. Este trabajo presenta el diseño de un LDO para el manejo de energía de una implementación de SoC en tecnología CMOS estándar de 28 nm, abarcando desde la revisión de la literatura hasta la validación del diseño.

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[*] Trabajo de Grado

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ABSTRACT

TITLE: DESIGN OF LOW DROP OUT VOLTAGE REGULATOR FOR POWER MANAGEMENT IN 28nm CMOS NODE FOR DIGITAL DOMAIN. *

AUTHOR: BRYAN ANDRÉS GALVIS CORREA **

KEYWORDS: REGULATOR VOLTAGE , MICROELECTRONICS, MICRO-CONTROLLER, SoC, SEMICONDUCTORS, DIGITAL, LOW POWER, LDO.

DESCRIPTION:

Low-dropout regulators (LDOs) are important because they provide a stable output voltage with a minimal voltage drop across them, even when the input voltage is close to the output voltage. Therefore, LDOs can maintain a constant output voltage even when the input voltage fluctuates, which makes them ideal for use in portable electronic devices and other applications where energy efficiency is a priority. This work presents the design of an LDO for power management in a System-on-Chip (SoC) implementation using standard 28-nm CMOS technology, covering the process from the literature review to the validation of the design.

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* BSc Thesis

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INTRODUCTION

Power management is a critical aspect in the design of modern systems-on-chip (SoC). Low dropout regulators (LDOs) are one of the selected strategies for power management since they can maintain a steady output voltage with minimal power loss, a critical feature for today's high-performance SoCs.

Voltage regulation is a relevant task for the correct performance of an SoC. A malfunction of the LDOs could mean that the other modules on the chip cannot be powered on. Consequently, it is necessary to ensure that the regulation satisfies specific voltage levels and ripple requirements [1]. Another pertinent characteristic of LDOs is their power consumption. That is particularly important in battery-powered systems, where the LDO can help extend the battery life by reducing the amount of wasted power [2]. LDOs are fundamental for maintaining stable voltage output, power conservation, space saving, and current protection in electronic systems [3]. This project seeks to elaborate on that mentioned component, LDOs, for the power management application of an SoC proposal. To align with the miniaturization trend, the design is implemented in 28 nm CMOS technology. In this way, it contributes to the development of this technology. Since it is an industry almost nonexistent in our country, it is a small contribution to making it the opposite. In Chapter 1 we provide an overview of the project, including its

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[1] G. RINCÓN-MORA. "Analog IC Design With Low-Dropout Regulators (LDOs)". In: *Analog IC Design With Low-Dropout Regulators (LDOs)*. McGraw-Hill. 2009. Chap. 1–8.

[2] Kamyar KEIKHOSRAVY and Shahriar MIRABBASI. "A 0.13-μm CMOS Low-Power Capacitor-Less LDO Regulator Using Bulk-Modulation Technique". In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 61.11 (2014), pp. 3105–3114. DOI: 10.1109/TCSI.2014.2334831.

[3] T. NAGATEJA et al. "A 8-ns Settling Time Fully Integrated LDO with Dynamic Biasing and Bulk Modulation Techniques in 40nm CMOS". in: *2020 IEEE International Symposium on Circuits and Systems (ISCAS)*. 2020, pp. 1–4. DOI: 10.1109/ISCAS45731.2020.9181197.

objectives. In Chapter 2, we define the design specifications and present the system modeling. In Chapter 3, the design methodology is discussed, and this chapter details the circuit-level implementation of the LDO. Finally Chapter 4 presents the results.

1. PROJECT OVERVIEW

The Onchip Research Group has been pursuing the technological transition from a microcontroller manufactured using 180-nm CMOS technology to 28-nm CMOS technology. Studying this type of Regulator offers an opportunity to investigate and optimize voltage regulators in more advanced system-on-chip (SoC) technologies, thereby contributing to the advancement of knowledge in the field of integrated circuits and systems. Voltage stability is a critical aspect of modern microelectronics, as integrated circuits are becoming increasingly sensitive to energy variations. In this context, efficient energy management is essential to ensure optimal performance and extend device lifetime. Advances in miniaturization and component integration have increased the importance of maintaining stable, low-noise supply voltages. Voltage fluctuations can lead to reading errors, performance degradation, and even permanent damage to microelectronic devices. Consequently, implementing suitable voltage regulators and advanced energy management techniques has become a critical research area in modern microelectronics. Addressing emerging challenges in this field requires optimizing power consumption, designing efficient regulation circuits, and exploring innovative control strategies.

1.1. OBJECTIVES

1.1.1. General Objective

- To design, at transistor level, a low-dropout voltage regulator (LDO) in 28 nm CMOS technology for powering digital blocks within a System-on-Chip (SoC), achieving the required output voltage, stability, load capability, and power-efficiency targets for reliable SoC operation.

1.1.2. Specific Objective

- To study and define the circuit specifications for analog LDO for a digital domain, based on the system requirements for a 28nm SoC in a standard CMOS technology.
- To design a LDO regulator for the digital domain of a SoC implementing a 28nm CMOS standard process with a good power supply rejection in DC, 1kHz and 1MHz of frequencies.
- To validate the design performance of LDO, using Monte Carlo and process, voltage, and temperature (PVT) corners simulations.

2. SPECIFICATIONS AND MODELING

2.1. SPECIFICATIONS

To characterize the specifications of a voltage regulator, a review of literature and previous works in the field was conducted. Various studies have addressed key aspects such as energy efficiency, input and output voltage range, thermal stability, and transient response to load variations. Table 1 shows the parameters to consider when designing. Consequently, it is necessary to understand each one.

Table 1. Complete Specifications.

Parameters	Units	Design Target		
		Min	Typ	Max
V_{IN}	V	1.62	1.8	1.98
V_{OUT}	V	-	0.9	-
I_{OUT}	mA	0.1	20	50
I_{Qs}	uA	-	-	50
LNR	mV/V	-	2	-
LDR	mV/mA	-	300	-
Ts	ns	-	300	-
$PSR@DC$	dB	-	-60	-20
$PSR@1khz$	dB	-	-60	-
$PSR@1Mhz$	dB	-	-10	-
$Noise_{rms}$	uV	-	200	-
$PhaseMargin$	º	-	55	-
$GainMargin$	dB	10	-	-

The primary function of an LDO is to provide a stable output voltage even when the

input voltage and load current change. A good regulation ensures that the output voltage remains within specified limits despite fluctuations in the load current or supply voltage. In addition to that, it must meet other stability and performance specifications to ensure a good regulation circuit.

The classic typology of a low drop voltage regulator[1] as seen in Figure.1 is made up of three essential blocks. The first block is the pass element, typically implemented using a transistor. The second block is an array of resistors that acts as a voltage divider, and the third block is the error amplifier, preferably implemented as a single-stage amplifier to enhance stability.

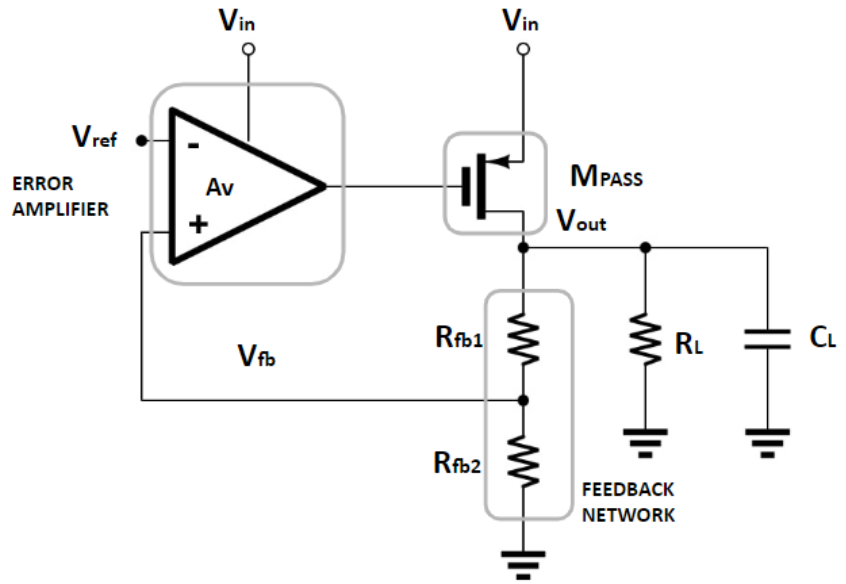

Figure 1. LDO Basic topology.

The pass element is placed in series with the load and is responsible for supplying the current. The voltage divider provides a scaled version of the output voltage V_{out} which is compared with external reference voltage V_{ref}. The error amplifier compares this scaled V_{out} with V_{ref} and adjusts the control voltage that drives the pass element. As a result, V_{out} remains stable despite variations in the load current and input voltage.[1]

The small signal analysis is discussed in A.1.

2.2. LNR

Line regulation quantifies the extent to which the output voltage fluctuates in response to alterations in the stable input voltage, and it is formally characterized as

$$LNR = \frac{\Delta Vout}{\Delta Vin}. \tag{1}$$

Line regulation is a critical parameter of low dropout regulators (LDOs) because it determines how well the regulator can maintain a stable output voltage despite variations in the supply voltage[4]. In the ideal case, the line regulation should be zero but the finite gain of the amplifier set a dependence of V_{out} with V_{in}.[5]

Assuming small variations in V_{in} and from small signal analysis and setting $V_{ref} = 0$ the line regulation can be approximated resulting in:

$$LNR = \frac{\Delta Vout}{\Delta Vin} \approx \frac{1}{A_v \beta}. \tag{2}$$

Where A_v is the gain of the error amplifier and β is the feedback. Note that line regulation primarily depends on the gain of the error amplifier.

To see graphically Vout versus time we have to analyze the transient response, 2 shows the variations of V_{in} versus time, the graph b represents the ideal case when V_{out} is not suffering variations, and c, is the real behavior of V_{out} due to the changes in the supply voltage.

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[4] Glen MORITA. "Understand Low-Dropout Regulator (LDO) Concepts to Achieve Optimal Designs". In: *Analog Dialogue* 48.4 (2014), pp. 27–31.

[5] José María Hinojo Clara Luján Martínez Antonio TORRALBA. *Internally Compensated LDO Regulators for Modern System-on-Chip Design*. https://doi.org/10.1007/978-3-319-75411-6. 2018.

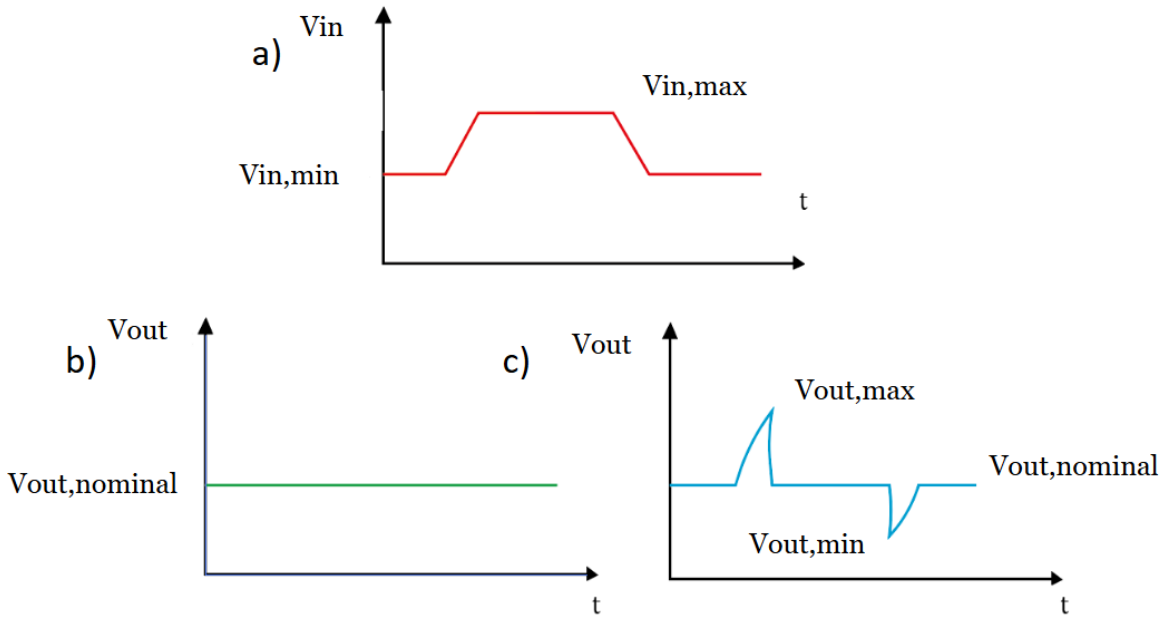

Figure 2. a) Represents the change in the steady state of V_{in} b) Ideal behavior of V_{out} due to changes in V_{in}. c) Natural behavior of V_{out} due to variations to changes in V_{in}.

2.3. LDR

Load regulation can be shown as the changes in V_{out} produced by the variations in the load current, and using the previous small signal analysis can be approximated as:

$$LDR = \frac{\Delta Vout}{\Delta Iload} \approx -\frac{1}{A_v \beta g_{mP}}, \tag{3}$$

where g_{mP} denotes the transconductance of the PMOS pass device. A higher value g_{mP} indicates stronger drive capability and improved LDO load regulation performance.The negative sign reflects that an increase in I_{LOAD} produces a decrease in V_{out}. This occurs because an increase in I_{LOAD} causes a voltage drop in R_{LOAD} and also affects the PMOS response.

2.4. QUIESCENT CURRENT

Power consumption is an important specification of this project and an important design parameter. Selecting a low-quiescent current is one way to reduce power consumption. Quiescent current is the current consumed by the internal control circuitry of an LDO when it is active as its represented in Figure 3 . This can be measured as:

$$I_q[\mu A] = I_{out} - I_{in}. \tag{4}$$

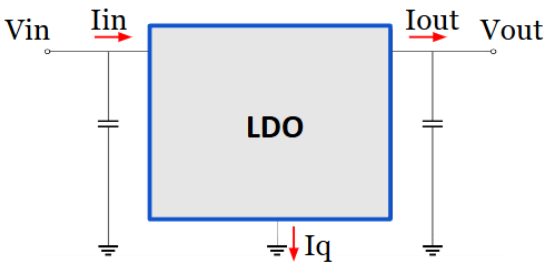

Figure 3. Quiescent current across the system.

2.5. PSR

Another important parameter is power supply rejection is the capacity of the LDO to reject the variation in the supply. Unlike line regulation, PSR measures how well the power supply can filter out unwanted disturbances in the input voltage V_{in}, whether they are low-frequency or high-frequency, to prevent them from affecting the regulated output voltage. Figure 4 shows the different paths that affect the PSR in an LDO regulator and shows the typical frequency response of the PSR, indicating which path

usually dominates in each frequency range.[5-6]

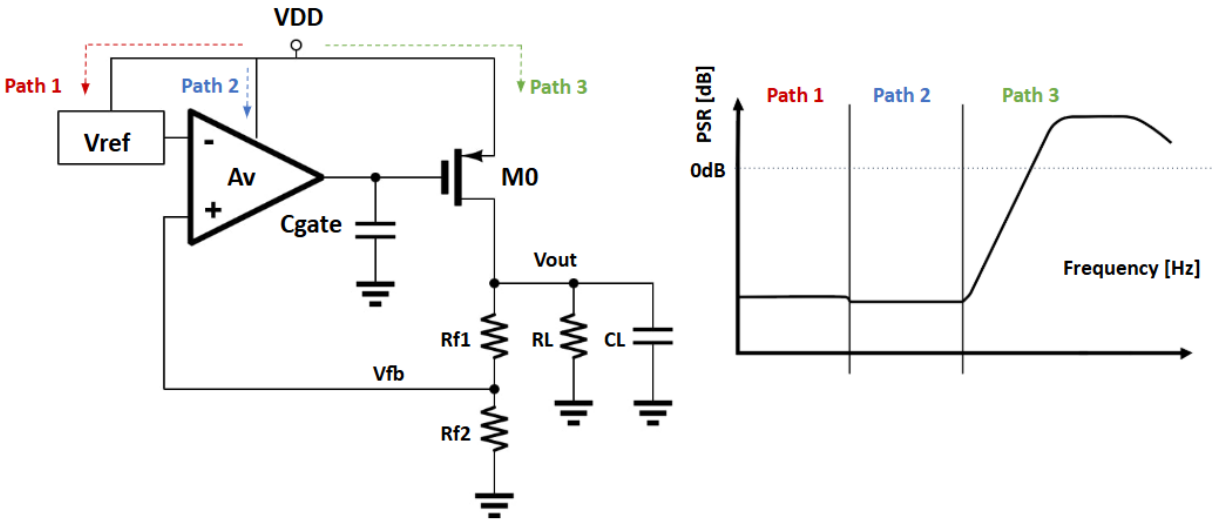

Figure 4. Power Supply Rejection.

$$PSR = 20log(\frac{\Delta Vout}{\Delta Vin}). \tag{5}$$

Note that it is similar to line regulation, the difference is that the PSR is for the frequency ranges while the line regulation is in DC.

2.6. NOISE

Analyze the two main sources of noise in an LDO: thermal noise and flicker noise[7]. Thermal noise is generated by the random motion of electrons due to thermal agitation in a conductor, while flicker noise, also known as $1/f$ noise, exhibits a power spectral

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6 Yasu Lu FENG CHEN and PhilipK. T. MOK. “Transfer Function Analysis of the Power Supply Rejection Ratio of Low-Dropout Regulators and the Feed-Forward Ripple Cancellation Scheme”. In: *IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, VOL. 69, NO. 8* (2022).

7 Qingyun LI et al. “A CMOS Low-Noise, Low-Dropout Regulator”. In: *Asia-Pacific Power and Energy Engineering Conference*. 2010.

density inversely proportional to frequency, being more prominent at low frequencies. Understanding and reduce both types of noise is essential to ensure optimal LDO performance as dicussed in the Annex A.2.[7].

2.7. PHASE AND GAIN MARGIN

2.7.1. Phase Margin Phase margin is the amount of additional phase delay required to bring the system to the brink of instability. It is measured at the frequency where the open-loop gain is equal to one (0 dB).

The phase margin is calculated as:

$$\text{Phase Margin} = 180^\circ - \text{Phase}(\omega_{gc}), \tag{6}$$

where ω_{gc} is the gain crossover frequency (the frequency at which the magnitude of the open-loop transfer function is 1 or 0 dB).
A larger phase margin indicates a more stable system. A phase margin of 45° to 60° is typically considered desirable for good stability and transient response.[8]

2.7.2. Gain Margin Gain margin is the amount by which the system gain can be increased before the system becomes unstable. It is measured at the frequency where the phase angle is -180°.
The gain margin is calculated as:

$$\text{Gain Margin} = \frac{1}{\left|\text{Gain}(\omega_{pc})\right|}, \tag{7}$$

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[8] Behzad RAZAVI. *Design of Analog CMOS Integrated Circuits Second Edition*. McGraw-Hill Education, 2017.

or in decibels,

$$\text{Gain Margin (dB)} = 20\log_{10}\left(\frac{1}{|\text{Gain}(\omega_{pc})|}\right), \tag{8}$$

where ω_{pc} is the phase crossover frequency (the frequency at which the phase of the open-loop transfer function is -180°).
A larger gain margin also indicates a more stable system.

A system is considered stable if both the phase margin and the gain margin are positive. This means that there is enough safety margin before reaching the point where the system oscillates or becomes unstable.

If the phase margin approaches 0° or the gain margin approaches 0 dB, the system is on the verge of instability and may exhibit sustained oscillations. In this condition, even small changes in system parameters or external disturbances can push the system into an unstable state. When the phase margin becomes negative or the gain margin drops below 0 dB, the system is considered unstable, meaning the feedback loop will reinforce oscillations and may eventually result in uncontrolled or undesired behavior.

In a transient response, a higher phase margin generally results in a less oscillatory and more damped transient response. Conversely, a lower phase margin can lead to oscillations and slower settling times[8].

3. DESIGN METHODOLOGY

The methodology shown in Figure 5 describes the analog design process of LDO that meet the required specifications. First, the architectural design can be separated by sections as blocks that recreate a general behavior. These blocks must be selected to obtain optimal behavior. The next step is the circuit design, which determines the circuit topology, device sizes, and bias voltages. Subsequently, the layout phase happens where each module generated is attached to the complete system. At last, the fabrication phase and post-silicon testing exceed the scope of this project.

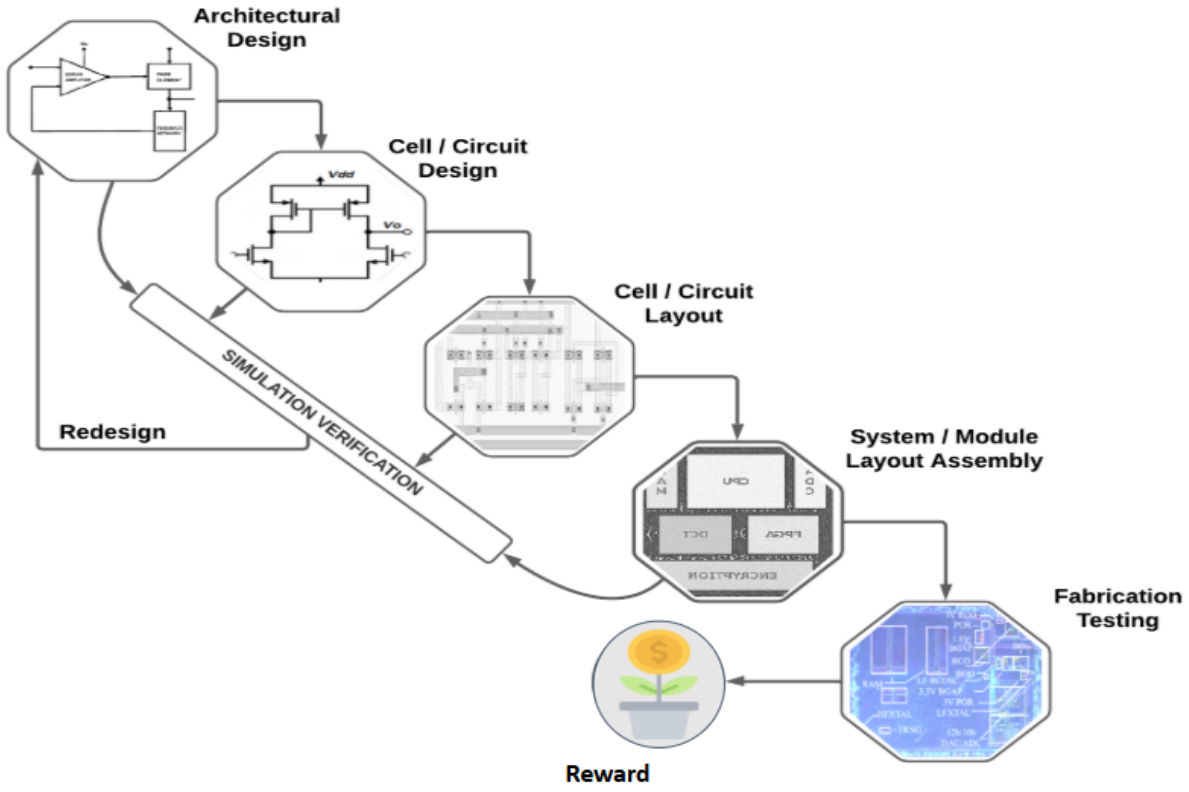

Figure 5. Visual representation of the analog design process.

3.1. FEEDBACK NETWORK

The feedback network in a Low Dropout Regulator helps maintain a stable output voltage by comparing the output voltage to a reference voltage and adjusting the pass device accordingly. The output voltage is sampled using a resistive voltage divider network. This network typically consists of two resistors, R_1 and R_2, connected in series between the output and ground. The divided voltage V_{fb}, taken from the junction of R_1 and R_2, is feedback to the error amplifier. The error amplifier compares the feedback voltage V_{fb}, to the reference voltage V_{ref}. The output of the error amplifier controls the pass device, adjusting its resistance to maintain the output voltage at the desired level. The values of R_1 and R_2 in the voltage divider determine the feedback voltage. The relationship is given by:

$$V_{\text{fb}} = V_{\text{out}} \times \frac{R_2}{R_1 + R_2}. \tag{9}$$

The resistors should be chosen to set V_{fb} equal to V_{ref} when V_{out} is at its desired value.

Consider an LDO with a reference voltage V_{ref} of 600 mV and a desired output voltage V_{out} of 900 mV. The resistors R_1 and R_2 in the feedback network can be calculated as follows:

1. Set the desired output voltage:

$$V_{\text{out}} = V_{\text{ref}} \times \left(1 + \frac{R_1}{R_2}\right). \tag{10}$$

2. Solve for R_1 and R_2: For $V_{\text{out}} = 900mV$ and $V_{\text{ref}} = 600mV$,

$$0.9 = 0.6 \times \left(1 + \frac{R_1}{R_2}\right) \;\Rightarrow\; 2 = \frac{R_1}{R_2} \;\Rightarrow\; R_1 = 0.5\,R_2. \tag{11}$$

3.2. PASS DEVICE

The pass device is integral to the performance of an LDO regulator. It directly influences the key parameters such as dropout voltage, efficiency, thermal performance, load regulation, and transient response. The selection of the appropriate pass device and the optimization of its operation are essential to design efficient and reliable LDOs that meet specific application requirements. Table 2 shows different types of pass devices, each one used for different applications.[9]

PARAMETER	**NMOS**	**NPN**	**PNP**	**PMOS**	**DARLINGTON**
$I_{\text{out-max}}$	Medium	High	High	Medium	High
$I_{\text{quiescent}}$	Low	Medium	Large	Low	Medium
$V_{\text{drop-out}}$	$V_{\text{sat}} + V_{\text{gs}}$	$V_{\text{sat}} + V_{\text{be}}$	$V_{\text{ec}} - V_{\text{sat}}$	$V_{\text{sd}} - V_{\text{sat}}$	$V_{\text{sat}} + 2V_{\text{be}}$
Speed	Medium	Fast	Slow	Medium	Fast

Table 2. Comparison of different transistor types.

One of the primary requirements of an LDO is to achieve a low dropout voltage, as it determines the minimum difference between the input and output voltages required to maintain regulation. Among the devices compared in Table 2, the PMOS transistor provides a significantly lower dropout voltage, since in a source-follower configuration it only requires $V_{SD} - V_{sat}$, whereas NMOS or bipolar devices demand an additional gate-source or base-emitter voltage overhead. This characteristic allows the LDO to operate efficiently even when the supply voltage is only slightly higher than the desired output. Furthermore, the PMOS exhibits a low quiescent current, which is essential for energy constrained applications such as battery powered systems, as it minimizes the static power dissipation of the regulator.

These factors, low dropout voltage and reduced quiescent current, make the PMOS

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[9] Gabriel Alfonso RINCON-MORA and Phillip E. ALLEN. *Study and Design of Low Drop-Out Regulators*. School of Electrical and Computer Engineering Georgia Institute of Technology Atlanta,

transistor the most suitable choice for the pass element in the proposed LDO architecture.

To estimate the appropriate size of the pass device in this design, it is essential to determine the desired region of operation. The process begins with a reference transistor characterized by a width to length ratio:

$$\frac{W}{L} = 2 \tag{12}$$

This reference device is characterized through simulation to obtain a baseline current and transconductance behavior, yielding a reference current of $I_{\text{ref}} = 16.07\ \mu$A.
Based on this reference, the relationship between current and device size is given by:

$$W_{\text{design}} = \left(\frac{I_{\text{design}}}{I_{\text{ref}}} \right) W_{\text{ref}} \tag{13}$$

Based on this reference, the transistor was resized to meet the design specification of a maximum output current $I_{\text{out,max}} = 50\,\text{mA}$
Using simulation results, the required width scaling factor was determined.

3.3. ERROR AMPLIFIER

The error amplifier in a Low Dropout Regulator (LDO) is a key component responsible for regulating the output voltage. Ensure that the output voltage remains stable and within the desired range by comparing the output voltage to a reference voltage and adjusting the pass device accordingly. It was necessary to implement a single-stage gain amplifier, as a multi-stage differential amplifier could be detrimental due to the presence of an additional pole in the gain stage. This can lead to stability issues, as the number of poles can affect the system's total phase, causing a phase shift close to 180°, which could result in oscillation or an unstable response if not properly handled

through compensation techniques, such as frequency compensation.

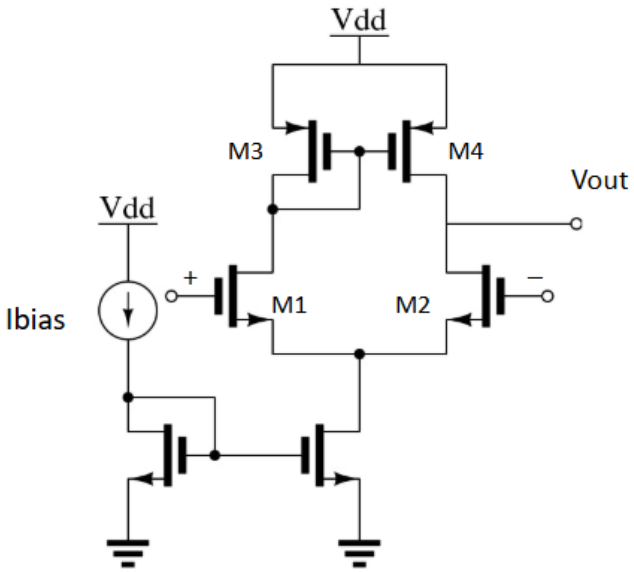

Figure 6. Single stage Amplifier.

Therefore, by using a single-stage amplifier Figure 6, the complexity of multiple poles is avoided, simplifying the analysis and improving stability, although this may come at the expense of the total gain that can be achieved. The gain of the amplifier is:

$$A_v = g_{m1,2} R_{out}, \tag{14}$$

where R_{out} its equal to:

$$R_{out} = r_{o2} || r_{o4}. \tag{15}$$

Voltage Gain Calculation

$$V_{\text{error}} = V_{\text{ref}} - V_{\text{fb}} \tag{16}$$

,

$$V_{\text{fb}} = V_{\text{out}} \times \frac{R_2}{R_1 + R_2}, \tag{17}$$

Given that $V_{out} = 900\,\text{mV}$.

$$A_v = \frac{V_{\text{out}}}{V_{\text{error}}} = \frac{900\,\text{mV}}{1\,\text{mV}} = 900, \tag{18}$$

A voltage error of 1 mV (0.11% of the nominal 900 mV output) was selected to ensure high regulation accuracy and to evaluate the steady state precision of the LDO under strict conditions.

$$A_v(\text{dB}) = 20\log_{10}(900) \approx 59\,\text{dB}. \tag{19}$$

The chosen amplifier was a folded cascode with NMOS input Figure 7,

as it provides high gain due to its large output resistance and increase the transconductance, putting the differential pair in weak inversion.[8]

$$A_v = \ g_{m1,2}\ R_{out}, \tag{20}$$

where R_{out} its equal to:

$$R_{out} = g_{m6}r_{o6}r_{o4}||g_{m8}r_{o8}(r_{o2}||r_{o10}). \tag{21}$$

3.4. COMPENSATION

The stability depends by the location of the poles and zeros of the system; therefore, it is necessary to analyze the open loop of the circuit and find where the dominant poles are located. H1, H2, H3 represent, respectively, the transfer functions of the error amplifier module, the PMOS control module, and the feedback resistor as is shown in the Fig.8 The compensation method that almost all LDOs use is Series Equivalent

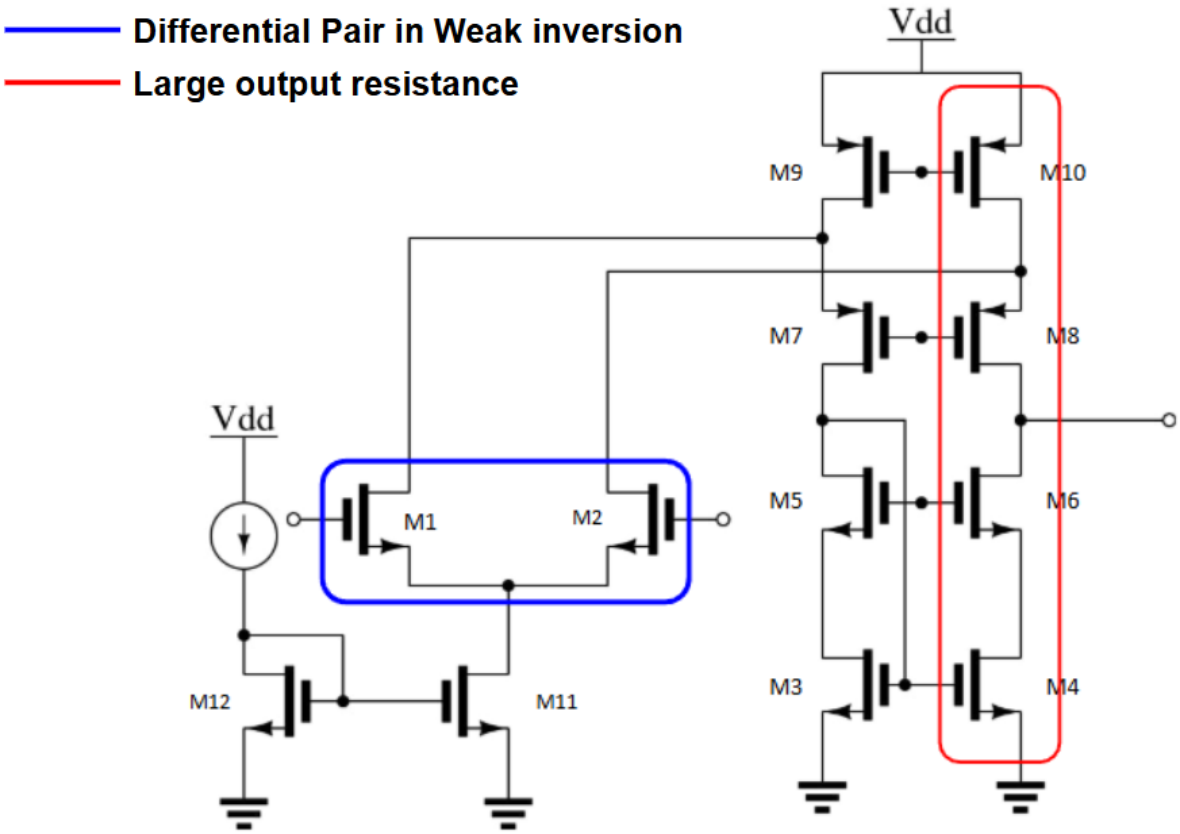

Figure 7. Folded cascode Amplifier.

Resistance (ESR). The main purpose of this compensation is to adjust the H2 transfer function. The AC components of the output impedance in equation (22) introduce both the load pole and a new ESR zero at (23).[10] Figure 9

$$Z_{OUT} = R_{OUT} \parallel \left(\frac{1}{sC_{OUT}} + R_{ESR} \right) = R_{OUT} \cdot \frac{1 + sC_{OUT}R_{ESR}}{1 + sC_{OUT}(R_{OUT} + R_{ESR})}, \qquad (22)$$

[10] Zhongwei Li XUEWEN WANG Fengge Wang. "The Analysis of LDO and the Stability of Loop Compensation". In: *International Conference on Electrical and Control Engineering* (2010), pp. 4369–4371.

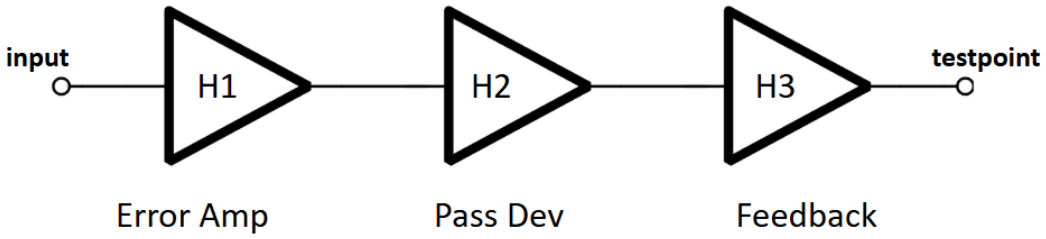

Figure 8. LDO AC Open-loop Block Diagram

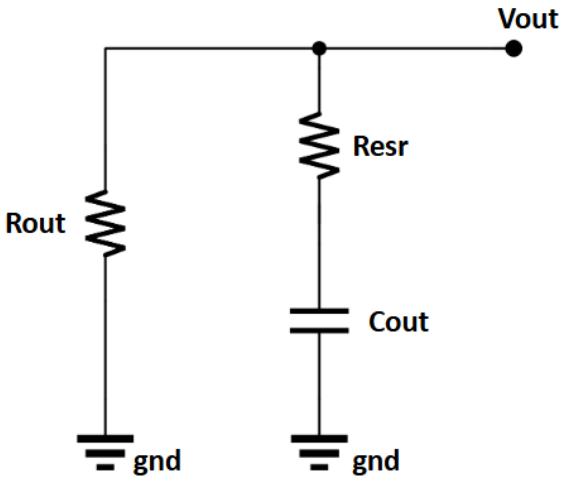

Figure 9. Output Impedance Equivalent Circuit with ESR.

$$Z_{ESR} = \frac{1}{C_{OUT} \cdot R_{ESR}}. \tag{23}$$

If this ESR zero falls within the appropriate frequency range, it can help properly compensate the loop.

To place a zero in the frequency range between $1\,\mathrm{MHz}$ and $10\,\mathrm{MHz}$. A 50 pF output capacitor is used to emulate the typical load capacitance that the regulator would drive in practical on-chip applications.

$$C_{\mathrm{out}} = 50\,\mathrm{pF}. \tag{24}$$

The frequency of the zero generated by the equivalent series resistance (R_{ESR}) is given by:

$$f_z = \frac{1}{2\pi R_{\text{ESR}}\, C_{\text{out}}}, \tag{25}$$

Solving for R_{ESR}:

$$R_{\text{ESR}} = \frac{1}{2\pi f_z\, C_{\text{out}}}, \tag{26}$$

For $f_z = 1\,\text{MHz}$:

$$R_{\text{ESR}} = \frac{1}{2\pi\,(1\times 10^{6})\,(50\times 10^{-12})} \approx 3.18\,\text{k}\Omega, \tag{27}$$

For $f_z = 10\,\text{MHz}$:

$$R_{\text{ESR}} = \frac{1}{2\pi\,(10\times 10^{6})\,(50\times 10^{-12})} \approx 318\,\Omega. \tag{28}$$

In two-stage op-amp Miller compensation, stability is enhanced by shifting the zero from the right-half plane to the left-half plane, which improves the system's phase margin. This adjustment is achieved by controlling the resistance associated with the zero. The compensation specifically targets the transfer function H_1 of the op-amp module.

$$\omega_{p1} \approx \frac{1}{R_{O,EA}\,(C_{GATE} + g_{m,P} R_{OUT} C_C)}, \tag{29}$$

$$\omega_{p2} \approx \frac{1}{R_{OUT} C_{LOAD}} \frac{C_C + C_{GATE}}{C_{GATE} + g_{m,P} R_{OUT} C_C}, \tag{30}$$

$$\omega_{z1} \approx \frac{g_{m,P}}{C_C + C_{gd,P}}. \tag{31}$$

Identifying terms can be concluded that the system has two real poles (39,40) and one

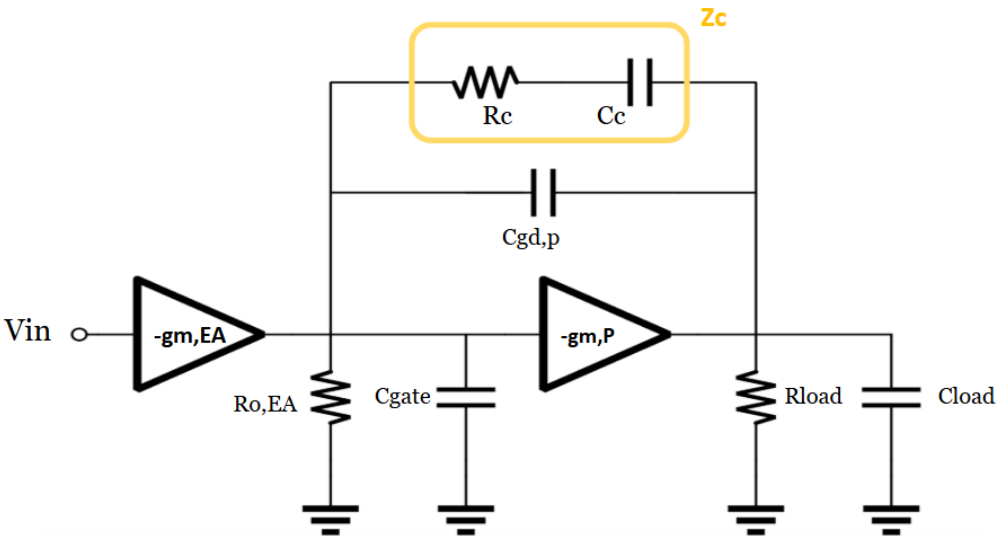

Figure 10. Miller zero compensation.

Right Half-Plane (RHP) zero (41). The latter zero depends on the ratio between gm,P and the total Miller capacitance C_c + $C_{gd,P}$. Unfortunately, as both, $g_{m,P}$ and $C_{gd,P}$ are strongly dependent on I_{LOAD}, the RHP zero location changes several decades when the I_{LOAD} is modified, moving towards the Unity Gain Frequency (UGF) and, hence, degrading the phase margin, to improve this we can put a resistance R_c in series with C_c canceling the zero and improving the stability of the system.[5]

$$f_z = \frac{1}{2\pi \cdot C_c + C_{gd,P} \cdot \left(\frac{1}{g_{m_p}} - R_c\right)}, \tag{32}$$

.

When $R_C = \frac{1}{g_{m2}}$, the generated zero is canceled. If $R_C > \frac{1}{g_{m2}}$, a negative zero is introduced. By further increasing R_C to a suitable value, this negative zero can be positioned to counteract a pole, effectively improving phase compensation.[10]

4. RESULTS

4.1. SIMULATION RESULTS

In this section, the results of the LDO regulator simulation are presented to validate its performance under different operating conditions. The LDO regulator was designed and evaluated under a wide range of operating and environmental conditions to ensure robust performance. Table 3 summarizes the main parameters used during the simulations, including the load current range, supply voltage variation, temperature range, and process corners considered for the PVT analysis.

Table 3. Operating and Simulation Conditions.

Parameter	**Value / Range**
Load Current (I_{LOAD})	$100\,\mu$A (min) – $50\,$mA (max)
External Capacitor (C_{EXT})	$50\,$pF
Supply Voltage (V_{DD})	$1.62\,$V – $1.98\,$V ($\pm 10\%$ of nominal value)
Load Range for Test (I_{LOAD})	$10\,\mu$A – $50\,$mA
Temperature Range	-40°C, 27°C, 125°C
Process Corners	`xxy_lib`; x = s, f, y = l, h slow (**s**), fast (**f**), low-V_{th} (**l**), and high-V_{th} (**h**) devices.

In addition, a validation using *Monte Carlo* simulations to evaluate the impact of random manufacturing variations on device parameters, thus providing insight into the statistical robustness and yield of the design. Annex A.3 summarize the simulation results for line regulation, load regulation, PSR, and transient response across PVT corners.

Table 4. Simulation Results PVT.

Parameters	**Units**	**Target**	**Design Obtained**			[11]	[12]	**Judge**
			Min	*Typ*	*Max*	*Typ*	*Typ*	
V_{IN}	V	1.8	1.62	1.8	1.98	1.8	-	Pass
V_{OUT}	V	0.9	0.9	0.9	0.9	1.2	1.6	Pass
I_{OUT}	mA	20	0.1	20	50	50	50	Pass
I_{Qs}	μA	50	25.95	31.49	40.23	60	0.6	Pass
LNR	mV/V	2	0.3	0.7	2.96	2.18	0.125	Pass
LDR	mV/mA	300	11.58	13.6	142.7	22.1	0.046	Pass
Ts	ns	300	196	203	343	237	-	Pass
$PSR@DC$	dB	-60	-65.36	-60.13	-46.24	-	-	Pass
$PSR@1kHz$	dB	-60	-64.98	-60.06	-46.22	-	-69	Pass
$PSR@1MHz$	dB	-10	-19.59	-17.86	-10.96	-	-	Pass
$Noise_{rms}$	μV	200	130.4	159.2	177.1	-	-	Pass
Phase Margin	º	55	50.88	84.21	85.77	-	83.29	Pass
Gain Margin	dB	10	35.35	37.01	42.42	-	-	Pass

Table 4. shows the results of the PVT simulation values and Table 5 shows the results of the Monte Carlo simulation, both exhibit good performance meeting the specifications desired by the project.

Table 5. Monte Carlo Results.

Parameter	**Min**	**Max**	**Mean**	**Median**	**Std. Dev.**
Vout [mV]	875.9	927.8	900.9	900.8	7.001
Iq [µA]	27.61	36.16	31.47	31.54	1.46
Noise [nV/$\sqrt{\text{Hz}}$]	136.0	211.2	163.5	162.2	9.838
Gain Margin [dB]	32.9	39.7	36.97	37.03	0.9952
Phase Margin [°]	76.99	86.08	84.02	84.19	1.078
PSR @ 1 kHz [dB]	-78.41	-46.54	-61.04	-59.49	6.708
PSR @ 1 MHz [dB]	-20.88	-15.21	-17.78	-17.75	0.8581
PSR DC [dB]	-114.8	-48.55	-61.76	-59.56	8.409

4.2. FINAL DIMENSIONS

The dimensions for the cascode amplifier are presented in Table 6, the dimensions of the pass transistors are presented in Table 7, the resistor values are presented in Table 8, and the compensation capacitor value is presented in Table 9.

Name	W [µm]	L [µm]	Multiplier
M1	5.5	0.27	10
M2	5.5	0.27	10
M3	2.0	0.4	1
M4	2.0	0.4	1
M5	2.0	0.4	1
M6	2.0	0.4	1
M7	4.4	0.5	1
M8	4.4	0.5	1
M9	4.4	0.5	1
M10	4.4	0.5	1
M11	4.8	0.4	1
M12	4.1	0.4	1

Table 6. Transistor dimensions.

Name	W [µm]	L [µm]	Multiplier
MPass	4.1	0.2	50

Table 7. Pass transistor dimensions.

Name	Ohm [kΩ]
Rf1	20
Rf2	40
Rc	1

Table 8. Resistor values.

Name	C [pF]
Cc	1.8

Table 9. Capacitor value.

4.3. LAYOUT

The layout was developed based on the circuit schematic (Figure 11), taking into account key design considerations such as area optimization, device placement, and routing efficiency. Devices with similar functionalities were placed close to each other, common-centroid techniques were applied where appropriate, and routing congestion was minimized. The total layout area measures 58.79 μm $\times$ 45.84 μm.

4.3.1. Layout Limitations The physical layout of the LDO in 28 nm technology was completed following general placement and routing guidelines. However, due to the lack of access to design rule check (DRC) and layout versus schematic (LVS) verification tools, formal validation could not be performed.

It should be noted that DRC and LVS validation were beyond the scope of this project, which focused on schematic design, loop compensation, and performance simulation. Therefore, while the layout may contain minor rule violations, these do not affect the validity of the simulation results or the achievement of the project objectives.

4.4. FIGURE OF MERIT

Annex A.4 presents a comparison of the proposed LDO and previously reported designs in terms of key performance metrics and merit figure.

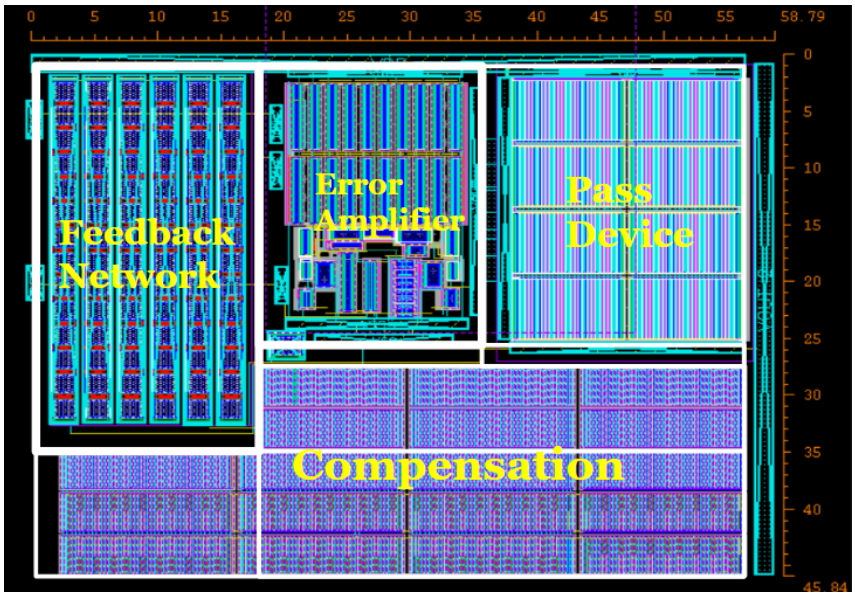

Figure 11. Proposed Layout.

4.5. CONCLUSIONS

This work enabled the design and simulation of a low-dropout (LDO) voltage regulator in 28 nm CMOS technology, successfully achieving the proposed objectives.
The regulator delivers an output voltage of 900 mV, ensuring stability through proper loop compensation and maintaining low power consumption across all PVT variations. Although the study was limited to simulation results, the project represents a practical and methodological reference for future developments, demonstrating how theoretical design principles can be effectively applied to realistic and scalable analog systems.

4.6. FUTURE WORK

Several directions for extending and enriching this project are identified:

- Explore advanced techniques to improve high-frequency rejection and transitory response.

- Include comprehensive DRC and LVS verification as well as post-layout validation.
- Integrate the LDO into the microcontroller, assessing its performance in real application scenarios.

BIBLIOGRAPHY

FENG CHEN, Yasu Lu and PhilipK. T. MOK. “Transfer Function Analysis of the Power Supply Rejection Ratio of Low-Dropout Regulators and the Feed-Forward Ripple Cancellation Scheme”. In: *IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, VOL. 69, NO. 8* (2022) (cit. on p. 20).

FERNANDEZ, L. “Design of a low drop-out volatge regulator for system-on-chip applications in a 130 nm cmos technology”. Thesis. Escuela de Ingenierías Eléctrica, Electrónica y de Telecomunicaciones. Universidad Industrial de Santander, 2017 (cit. on p. 34).

KEIKHOSRAVY, Kamyar and Shahriar MIRABBASI. “A 0.13-μm CMOS Low-Power Capacitor-Less LDO Regulator Using Bulk-Modulation Technique”. In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 61.11 (2014), pp. 3105–3114. DOI: 10.1109/TCSI.2014.2334831 (cit. on p. 11).

LI, Qingyun et al. “A CMOS Low-Noise, Low-Dropout Regulator”. In: *Asia-Pacific Power and Energy Engineering Conference*. 2010 (cit. on pp. 20, 21).

MOHAMMAD AHMADI, Emad Ebrahimi. “A new LDO regulator with adaptive PSR improvement under wide load current range and fast load transient response”. In: *2024 32nd International Conference on Electrical Engineering*. 2024. DOI: 10.1109/ICEE63041.2024.10667855 (cit. on p. 34).

MORITA, Glen. “Understand Low-Dropout Regulator (LDO) Concepts to Achieve Optimal Designs”. In: *Analog Dialogue* 48.4 (2014), pp. 27–31 (cit. on p. 17).

NAGATEJA, T. et al. “A 8-ns Settling Time Fully Integrated LDO with Dynamic Biasing and Bulk Modulation Techniques in 40nm CMOS”. In: *2020 IEEE International Symposium on Circuits and Systems (ISCAS)*. 2020, pp. 1–4. DOI: 10.1109/ISCAS45731.2020.9181197 (cit. on p. 11).

RAZAVI, Behzad. *Design of Analog CMOS Integrated Circuits Second Edition*. McGraw-Hill Education, 2017 (cit. on pp. 21, 22, 28).

RINCON-MORA, Gabriel Alfonso and Phillip E. ALLEN. *Study and Design of Low Drop-Out Regulators*. School of Electrical and Computer Engineering Georgia Institute of Technology Atlanta, (cit. on p. 25).

RINCÓN-MORA, G. "Analog IC Design With Low-Dropout Regulators (LDOs)". In: *Analog IC Design With Low-Dropout Regulators (LDOs)*. McGraw-Hill. 2009. Chap. 1–8 (cit. on pp. 11, 16).

TORRALBA, José María Hinojo Clara Luján Martínez Antonio. *Internally Compensated LDO Regulators for Modern System-on-Chip Design*. `https://doi.org/10.1007/978-3-319-75411-6`. 2018 (cit. on pp. 17, 20, 32).

XUEWEN WANG Fengge Wang, Zhongwei Li. "The Analysis of LDO and the Stability of Loop Compensation". In: *International Conference on Electrical and Control Engineering* (2010), pp. 4369–4371 (cit. on pp. 29, 32).

A. Appendix

A.1. Small-Signal Analysis of the LDO

This annex presents the small-signal analysis of the Low Dropout Regulator (LDO).

A.2. Noise Analysis

This annex presents the noise analysis, including thermal and flicker noise contributions from each stage of the LDO.

A.3. PVT Simulation Results

Figures in this annex summarize the simulation results for loop gain, loop phase, noise, PSR, quiescent current, line regulation, load regulation, and stability.

A.4. Figure of Merit Comparison

This annex presents Figure of Merit (FoM) comparison between the proposed LDO and previously reported designs in different CMOS technologies.