DESIGN OF A CURRENT ACQUISITION CIRCUIT IN 28nm CMOS TECHNOLOGY FOR RESPONSE MEASUREMENT OF ELECTROCHEMICAL SENSORS

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RESUMEN

TÍTULO: DISEÑO DE UN CIRCUITO DE ADQUISICIÓN DE CORRIENTE EN TECNOLOGÍA CMOS DE 28NM PARA MEDIR LA RESPUESTA DE SENSORES ELECTRQUÍMICOS *

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PALABRAS CLAVE: Tecnología CMOS, Transportador de Corriente, Medición Bidireccional de Corriente.

DESCRIPCIÓN:

La medición de concentraciones en fluidos biológicos es fundamental para el monitoreo de salud y aplicaciones en la industria química. Este proyecto presenta el diseño, en tecnología CMOS de 28 nm, de un sistema de medición de corriente capaz de registrar corrientes bidireccionales en el rango de los nanoamperios, como bloque de un potenciostato en chip. El circuito implementa un amplificador de transimpedancia con resistencia de realimentación (R-TIA) y usa la técnica *chopper* para reducir el ruido *flicker*. El sistema logra un ruido máximo integrado de 28 pA en 1 kHz, detecta corrientes de hasta 1 nA y opera en un rango de $-1\ \mu$A a $1\ \mu$A, con linealidad de 0.9999981 y un error máximo de 0.1

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* Trabajo de Grado

** Facultad de Ingenierías Físico-Mecánicas. Escuela de Ingenierías Eléctrica, Electrónica y de Telecomunicaciones. Director: JOSE LUIS HERRERA CELIS

ABSTRACT

TITLE: DESIGN OF A CURRENT ACQUISITION CIRCUIT IN 28nm CMOS TECHNOLOGY FOR RESPONSE MEASUREMENT OF ELECTROCHEMICAL SENSORS *

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KEYWORDS: CMOS Technology, Current Conveyor, Bidirectional Current Measurement.

DESCRIPTION:

The measurement of compound concentrations in biological fluids is essential for health monitoring, spanning from biomedical research to the chemical industry. This project focuses on the design of a current measurement system in CMOS technology, capable of recording minimal bidirectional currents in the nanoampere range, as one of the fundamental blocks of an on-chip integrated potentiostat. The design corresponds to a transimpedance amplifier with a feedback resistor (R-TIA), in which the chopper stabilization technique is employed to reduce flicker noise. The system, implemented in a 28 nm CMOS technology node, achieves a maximum input-referred integrated noise of 28 pA within a 1 kHz bandwidth, with the capability to detect currents as low as 1 nA. Furthermore, it enables measurements over a wide range from -1 μA to 1 μA, maintaining a linearity of 0.9999981 and a maximum error of 0.1%.

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* BSc Thesis

** Facultad de Ingenierías Físico-Mecánicas. Escuela de Ingenierías Eléctrica, Electrónica y de Telecomunicaciones. Director: JOSE LUIS HERRERA CELIS

INTRODUCTION

Electrochemical sensors have become indispensable tools for the detection and quantification of chemical compounds, particularly in biological fluids. Their applications span diverse fields, including biomedical research, clinical diagnostics, and the chemical industry [1]. These sensors are especially critical in health monitoring applications, where the accurate detection of biomarkers at very low concentrations can provide early indications of diseases and enable personalized medical treatments. Consequently, it has been necessary for researchers to explore various techniques and characterization methods for designing electrochemical sensors.

The accurate detection of these very weak signals requires highly sensitive and robust interface readout circuits. Amplifiers, as core building blocks within these circuits, are particularly susceptible to noise and offset issues. Specifically, thermal and flicker (1/f) noise, as well as offset voltages, represent major challenges that can significantly degrade overall sensor performance and limit the precision required for ultra-weak signal detection. In this context, CMOS technology has gained notable prominence, as it not only allows for the integration of sensors and conditioning circuits on the same substrate but also offers higher sensitivity, reliability, and low power consumption [2]. Furthermore, advancements in fabrication technologies over the last few decades have facilitated the development of sensor systems and devices that are not only robust and precise but also highly reliable, laying the groundwork to overcome the inherent

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[1] Chao Yang ANDREW MASON Yue Huang and Jichun ZHANG. "Amperometric Readout and Electrode Array Chip for Bioelectrochemical Sensors". In: *IEEE Sensors Journal* 5.18 (2007), p. 5. DOI: 10.1109/JSEN.2016.2537841.

[2] Serdar TOPRAK, Revna ACAR VURAL, and Okan Zafer BATUR. "High accuracy potentiostat with wide dynamic range and linearity". In: *AEU - International Journal of Electronics and Communications* 142 (2021), p. 154018. DOI: https://doi.org/10.1016/j.aeue.2021.154018.

challenges of noise and offset.

To effectively harness the capabilities of these sensors, the design of a current acquisition circuit is fundamental for enabling bidirectional measurement [3] of currents in the nano-ampere to micro-ampere range. This capability is essential for leveraging the potential of new electrochemical sensors that operate within a lower current pickup range. However, during the design process, it is crucial to consider the limitations and constraints imposed by CMOS technology, such as minimum channel length, intrinsic transistor noise, device mismatch, and the inherent transconductance of n-type and p-type MOS transistors. These intrinsic limitations, particularly the presence of thermal and flicker (1/f) noise, pose significant hurdles for low-noise applications [4]. Techniques like chopper stabilization have emerged as vital strategies to mitigate these effects, demonstrating their importance in achieving high-performance readout circuits. These factors complicate the design of analog circuits, especially when targeting low-noise applications across a wide dynamic range [5].

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[3] Markus HABERLER et al. "A Bidirectional Current-Mirror-Based Potentiostat Using a Slice-Based Class-AB Amplifier". In: *IEEE Solid-State Circuits Letters* 3 (2020), pp. 298–301. DOI: 10.1109/LSSC.2020.3013667.

[4] Min CHEN et al. "A High Dynamic Range CMOS Readout Chip for Electrochemical Sensors". In: *IEEE Sensors Journal* 16.10 (2016), pp. 3504–3513. DOI: 10.1109/JSEN.2016.2537841.

[5] Varsha MOHAN. "Wide Dynamic Range, Highly Accurate, Low Power CMOS Potentiostat for Electrochemical Sensing Applications". Master's Thesis. University of Tennessee, 2019.

OBJECTIVES

0.1. General Objectives

Design a current acquisition circuit in CMOS technology that allows bidirectional measurement of minimal currents ranging from nano amperes to micro amperes for electrochemical sensing.

0.2. Specific Objectives

- To study and define the circuit specifications for the selected current acquisition circuit topology, based on the system requirements for bidirectional measurement of minimal currents in an electrochemical sensor, using 28nm PDK CMOS technology on Synopsys Custom Compiler.
- To design a current acquisition circuit using Synopsys Custom Compiler 28nm CMOS PDK, focusing on noise reduction and a wide measurement range.
- To validate the performance of the current acquisition circuit using different types of simulations, such as Monte Carlo and process, voltage and temperature (PVT) variations.

1. ELECTROCHEMICAL SENSING: FUNDAMENTALS AND PRINCIPLES

Electrochemical analysis is a powerful analytical technique that investigates chemical reactions by measuring electrical properties (current, voltage, impedance) at the interface between an electrode and an electrolyte solution. It is indispensable in various fields, such as biomedical diagnostics, environmental monitoring, and industrial process control, since it enables the detection and quantification of chemical compounds. Measuring extremely low concentrations is essential in these applications, which has driven the development of measurement architectures capable of detecting increasingly weaker signals.

The fundamental principle consists of applying a controlled voltage to a solution in order to monitor the redox (reduction-oxidation) reactions that occur. This process is carried out using two electrodes immersed in the electrochemical solution: the first applies the controlled voltage required to drive the redox reactions, while the second records the electrochemical response at the surface by detecting the currents generated by electron transfer. In this way, the electrodes serve as the interface between the solution and the measurement system, enabling the conversion of chemical reactions into electrical signals that can be analyzed. The resulting electrical signal, typically a current or a voltage, provides direct information about the presence, concentration, and kinetics of the target analytes.[6] The instrument responsible for exciting, controlling, and measuring the response of the electrochemical cell is known as a potentiostat.

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[6] Allen J. BARD and Larry R. FAULKNER. *Electrochemical Methods: Fundamentals and Applications*. 2nd. New York: John Wiley & Sons, 2001.

1.1. ELECTRODE CONFIGURATION

An electrochemical amperometric sensing system can be represented as in Figure 1.1. The electrochemical cell consists of a working electrode (WE), a reference electrode (RE), and a counter electrode (CE). The current acquisition circuit holds the working electrode at a known potential and records the reduction-oxidation (redox) current generated due to the voltage difference between the working and reference electrodes.[6] The working electrode (WE) serves as the active site where the electrochemical reaction of interest occurs. The redox process generates a current at this electrode, while its potential is precisely controlled by the potentiostat relative to the reference electrode. The reference electrode (RE) provides a stable and well-defined potential against which the working electrode is controlled, and to ensure its stability, ideally no current flows through it. Finally, the counter electrode (CE) completes the electrical circuit; the potentiostat drives the required current or potential through this electrode to sustain the reaction at the working electrode and to accurately maintain its target potential.

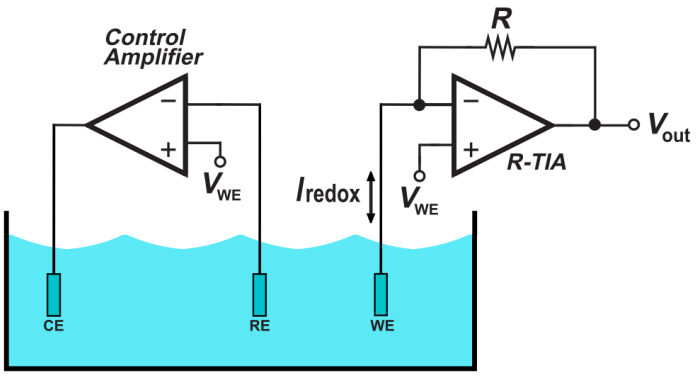

Figure 1.1. Conceptual view of an electrochemical sensory system.

A common representation of the impedance seen in the chemical compound is depicted in Figure 1.2

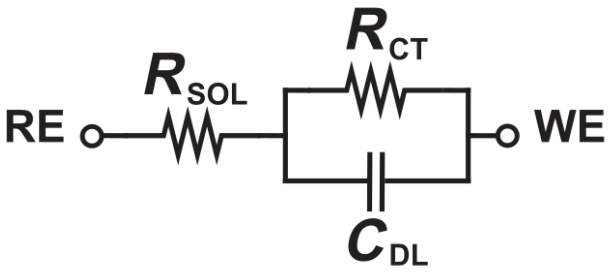

Figure 1.2. Equivalent electrical circuit model (Randles circuit) for the electrochemical interface. It consists of the solution resistance R_{SOL} , the charge transfer resistance R_{CT} , and the double-layer capacitance C_{DL}.

1.2. CHALLENGES IN ELECTROCHEMICAL CURRENT ACQUISITION

The unique characteristics of electrochemical signals, particularly their low magnitude and dynamic nature, present significant challenges for the design of high-performance current acquisition circuits. Below, it is addressed two important issues to consider when designing a current acquisition circuit for this type of application.

Low-level signal detection and dynamic range: The need to measure currents ranging from nanoamperes to microamperes requires circuits with an exceptionally wide dynamic range. Detecting picoampere-level signals is especially challenging, as they are easily obscured by noise.

Linearity and accuracy: Maintaining high linearity and accuracy across the wide dynamic range of electrochemical currents is crucial for reliable quantitative analysis. Many amplifiers used in current acquisition circuits can be prone to output variations, requiring a wide output voltage swing to maintain linearity across the entire sensing range.

2. TOPOLOGIES

As electrochemical currents often range from nanoamperes to microamperes, their sensing and measurement require sophisticated current acquisition circuits, which serve as a critical interface between the electrochemical cell and subsequent signal processing stages. Electrochemical sensors transduce chemical information into electrical currents, which can be either oxidative or reductive, demanding bidirectional measurement capabilities. The challenge is compounded by the often extremely low magnitude of these currents, particularly for biomarker detection at low concentrations, making them highly susceptible to noise and offsets. Therefore, the current acquisition circuit must not only provide accurate current-to-voltage conversion but also offer high gain, wide dynamic range, excellent linearity, and robust noise immunity.

The Transimpedance Amplifier (TIA) is one of the most common used topologies regarding current acquisition circuit topologies. The TIA sets a virtual potential at the working electrode and at the same time generates an output voltage that is proportional to the redox current.This conversion can be achieved through a resistive feedback configuration [13] or a switched-capacitor circuit [14]. However, using resistors on the feedback loop is not efficient, as it adds considerable thermal noise, while increasing chip area.In contrast, TIA configuration of a swiched capacitor is a more common choice [7], where resistors are replaced with capacitors and switches in the feedback loop, which helps to descrease the chip area, while reducing the resistor noise as capacitors exhibit way less noise, and in some cases, capacitors become considered noise-free components. Nevertheless, this configuration can vary its linearity over a wide dynamic range, as the impedance seen on the capacitor is affected by frequency. Another current acquisition circuit is the widely used current conveyor (CC), whose basic principle is to hold the WE to a virtual potential and to convey (as its name indicates)

the current from the WE to a high-impedance output node. After that, the mirror current is converted into a voltage signal. However, the current conveyor topology is very susceptible to noise. Although it isolates the WE from the clock circuitry (reducing the effect of charge injection), and avoids external noise, internal noise creates significant limitations, as it requires additional stages for the conveying of the current.

Since the aim was to obtain a circuit that exhibited minimal noise, while maintaining linearity, the resistive feedback TIA was chosen. This configuration may add undesirable noise to the measurement caused by the resistor, however, this configuration offers other advantages.The final design will feature an external, variable resistor. From this point of view, the user will access to different measurement ranges by modifying the resistance value (this will be discussed in more detail later on). Additionally, a resistive feedback offers better linearity, as the resistor has stablished value at any frequency and over the wide dynamic range.

The design also includes a chopper stabilization circuit, as a modulation technique to reduce flicker noise [7] (this will be analyzed in later sections as well). The R-TIA topology, including the chopper modulators, allong with the representation of an electrochemical cell, is schematically represented in Figure 2.1.

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[7] C. C. ENZ and G. C. TEMES. "Circuit techniques for reducing the effects of op-amp imperfections: autozeroing, correlated double sampling, and chopper stabilization". In: *Proceedings of the IEEE* 84.11 (1996), pp. 1584–1614. DOI: 10.1109/5.542410.

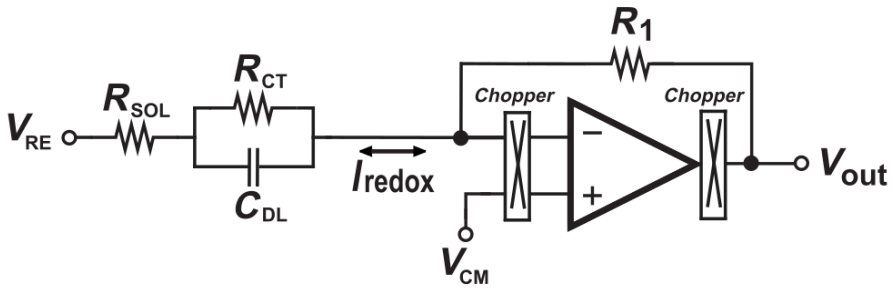

Figure 2.1. General topology of a chopper-stabilized R-TIA connected to an electrochemical interface modeled as an equivalent Randles circuit, consisting of the solution resistance (R_{SOL}), the charge transfer resistance (R_{CT}), and the double-layer capacitance (C_{DL}). Also observed are V_{CM}: common-mode voltage, R_1: feedback resistance, V_{RE}: potential difference in the electrochemical interface, I_{redox}: redox current, and V_{OUT}: output voltage.

The folded cascode OTA (which will be described in subsequent chapters) requieres a biasing circuit that provides neccesary voltages for each device to stay in established opearation point. The proposed topology for the biasing circuit is discussed in appendix B.

2.1. Operational Transimpedance Amplifier (OTA)

As seen in Figure 2.1, the chopper-stabilized R-TIA topology requires the design of an operational transimpedance amplifier (OTA) (converts an input current into a voltage), where the folded cascode topology was selected, due to its high gain, low noise performance, wide output voltage swing and good linearity. The differential folded cascode amplifier used is depicted in Figure 2.2, with a single ended output. The modulation chopper switches are placed at the input of the OTA (gate terminals of $M_{1,2}$), while the demodulation chopper switches are placed after the NMOS current sources (drain terminals of $M_{4,5}$). The design of the OTA will be discussed later on.

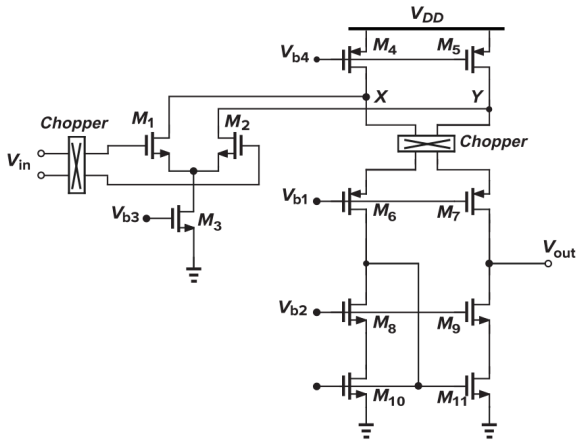

Figure 2.2. Schematic circuit of the folded cascode OTA with modulator/demodulator chopper.

2.2. NMOS chopper switches

The chopper stabilization technique is widely used in sensing applications where flicker noise and offset voltage are the main limiting factors (this will be discussed on noise section later on). It is frequently implemented with 4 NMOS switches, where two of them operate at the phase of the first clock (ϕ) and the others operate at the phase of the second clock (ϕ_1). The proposed topology is shown in figure 2.3.

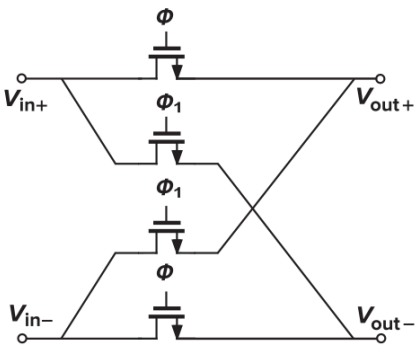

Figure 2.3. Schematic of a chopper circuit based on differential NMOS switches.

3. Design Specifications

Considering the application of this current acquisition circuit in electrochemical sensing, certain specifications were stablish in order to guarantee the circuit performance. These specificacion are detailed on table 3.1. The circuit must operate within a supply voltage range between 1.62 V and 1.98 V, ensuring that the amplifier exhibits a maximum input referred noise integrated in a bandwidth from 0.01 Hz to 1 kHz of 100 pA. Additionally, it must achieve a minimum bandwidth of 1 kHz while offering a linearity of at least 0.999 over a $-1\,\mu$A to $1\,\mu$A dynamic measurement range.

Parameters	**Units**	**Design target**		
		Min	**Typ**	**Max**
VDD	V	1.62	1.8	1.98
Input noise (rms, 0.01Hz–1kHz)	pA	-	-	100
BW in the current measurement range	kHz	1	-	-
Linearity R^2	–	0.999	-	-

Table 3.1. Target design parameters for the current acquisition circuit.

4. Specifications Analysis

As the specifications were stablished and the topology was selected, an in-depth analysis was carried out to determine the main variables that may hinder meeting the stablished requirements. This strategy allowed to identify trade-offs within the circuit, and provides deep understanding of the variables and their functioning. Based on this analysis, the designer may develop a work plan in order to maximize the utilization of the circuit's inherent characteristics.

4.1. Noise

Considering the relevant role of noise in extremely low current sensing applications, and a frequency range between **0.01 Hz and 1 kHz**, the performance of the acquisition system is critically limited by the input-referred current noise of the amplifier. In this context, noise is considered to be an intrinsic phenomenon of electrical components and is caused by various sources that must be taken into account during design. There are two main noise sources to be considered: thermal noise and flicker noise [8].

Thermal noise origins from the thermal agitation of charge carriers in conductors and is linked to both temperature and the random motion of electrons within them. Flicker noise is linked to gradual changes in the device state, like fluctuations in the mobility of charge carriers through the channel [9]. It is distinguished by a power spectral density

[8] Mahdi TARKHAN and Mohamad SAWAN. "A Novel Current Density Based Design Approach of Low-Noise Amplifiers". In: *IEEE Sensors Journal* 12.16 (2022), p. 12. DOI: 10.1109/JSEN.2016.2537841.

[9] Meysam AKBARI and Omid HASHEMIPOUR. "Design and analysis of folded cascode OTAs using Gm/Id methodology based on flicker noise reduction". In: *Analog Integrated Circuits and Signal Processing* 83.3 (2015), pp. 343–352. DOI: 10.1007/s10470-015-0535-x.

that decreases as the frequency rises.

Circuit-wise, thermal and flicker noise in a NMOS transistor can be represented as shown in figure 4.1. For thermal noise, an independent current source is placed in parallel to the transistor; whereas for flicker noise, an independent voltage source is placed at the gate of the MOS transistor.

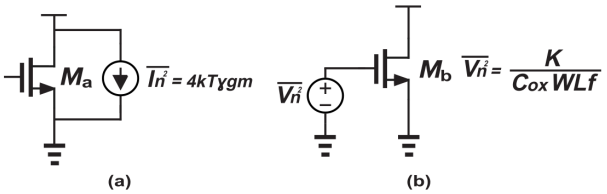

Figure 4.1. (a) Thermal anoise model for a single MOS transistor. (b) Flicker noise model for a single MOS transistor.

4.1.1. Noise analysis in folded cascode OTA

In order to obtain the circuit full noise, it is necessary to take into account the noise contribution on each transistor on the OTA. However, there are specific transistors whose noise contribution is negligible [10], which are the cascode transistors (i.e. $M_{6,7}$ and $M_{8,9}$). When performing thermal noise analysis in these transistors, the noise stays encapsulated in a loop through the transistor itself. Therefore, these transistors will be exluded from the analysis, as seen in Figure 4.2.

[10] Jack OU, Pietro M. FERREIRA, and Jui-Chu LEE. "Experimental Demonstration of gm/ID Based Noise Analysis". In: *Circuits and Systems* 5.4 (2014), March 28.

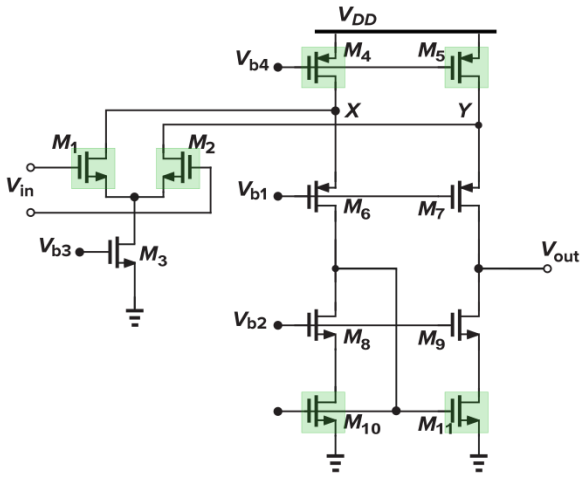

Figure 4.2. Folded cascode OTA noise analysis

First,the thermal noise of each transistor is determined using the previously described current source approximation. An equivalent current in the differential pair is obtained. This current can be referenced to the input as an independent voltage source by dividing it by the squared of the transconductance of the input transistors. Therefore, equation is obtained 1.

$$\overline{Vn^2_{in_T}} = \frac{8KT\gamma}{gm^2_{1,2}} * (gm_{4,5} + gm_{10,11} + gm_{1,2}) \tag{1}$$

Additionally, flicker noise referred to the input can be modeled in a similar way to thermal noise. The voltage source model is used at the gate of the transistors, which can be represented as a current multiplied by the square of the transconductance of each transistor [11]. The currents can be added together as a superposition, then referenced to the input by dividing by the square of the transconductance of the input transistors, where the total flicker noise is given by equation (5)

[11] P.K. CHAN et al. “Designing CMOS folded-cascode operational amplifier with flicker noise minimisation”. In: *Microelectronics Journal* 32 (2001), pp. 69–73. DOI: 10.1016/S0026-2692(00)00105-1.

$$\overline{Vn_{in_f}^2} = \frac{2k}{C_{ox}f} * \left(\frac{1}{WL_{1,2}} + \frac{gm_{4,5}^2}{WL_{4,5}gm_{1,2}^2} + \frac{gm_{10,11}^2}{WL_{10,11}gm_{1,2}^2} \right) \tag{2}$$

4.1.2. Noise in Current Acquisition Circuit

Although every amplifier exhibits both a voltage noise density ($v_{n,in}$) and a current noise density ($i_{n,in}$), the relative importance of each parameter depends directly on the equivalent source impedance (R_s). In systems with low-impedance sources (such as resistive sensors from a few ohms to kilo-ohms), voltage noise is dominant, since the current noise flowing through R_s generates a negligible voltage. However, in electrochemical systems, electrodes and their surrounding medium typically present very high equivalent source impedances, on the order of hundreds of kilo-ohms up to several mega-ohms. Under these conditions, even extremely small input current noise values translate into significant voltage noise contributions, following the relationship:

$$v_{eq}(f) = i_{n,in}(f) \cdot R_i n \tag{3}$$

This value can easily exceed the intrinsic voltage noise of a precision amplifier (typically 5–20 nV/$\sqrt{\text{Hz}}$), making current noise the **true limiting factor** for the system's signal-to-noise ratio (SNR).

4.2. Linearity and error percentage

The design of the current-to-voltage conversion stage focused on ensuring a linear and predictable response across the entire operating. The design strategy was fundamentally guided by the operational characteristics of the amplifier, particularly its linear Output Swing Range (OSR). This parameter defines the voltage window within which the amplifier operates without introducing distortion, thus preserving the integrity of the converted signal.

The key component in this stage is the transimpedance resistor (R_{es}), which functions as the scaling factor between the input current and the output voltage. Its value was strategically selected to map the maximum expected input current (I_{max}) to the limits of the amplifier's linear operating window. This design relationship is expressed as:

$$R_1 = \frac{\text{Useful Voltage Window}}{I_{max}} \tag{4}$$

Here, the "Useful Voltage Window" represents the total voltage excursion available within the amplifier's linear region, ensuring that the conversion always operates under predictable conditions.

By dimensioning the resistor in this manner, a dual objective is achieved. On one hand, the dynamic range of the amplifier is fully exploited, and on the other, the necessary sensitivity is obtained to clearly resolve the smallest current variations. This design ensures that the conversion remains reliable and straightforward, fulfilling the fundamental requirement of the project: accurately measuring currents in the nanoampere range.

Additional specifications analysis were carried out, for more detailed explanation see appendix A.

$$\overline{Vn^2_{in_f}} = \frac{2k}{C_{ox}f} * \left(\frac{1}{WL_{1,2}} + \frac{gm^2_{4,5}L_{1,2}}{WL_{4,5}2I_D\mu_n C_{ox}W_{1,2}} + \frac{gm^2_{10,11}L_{1,2}}{WL_{10,11}2I_D\mu_n C_{ox}W_{1,2}} \right) \tag{5}$$

5. Design Procedure

Once the design specifications were analyzed in the previous section, a design procedure was established, giving priority to certain variables such as the transconductance of the OTA, as well as the various possible trade-offs that could possibly prevent meeting the previously discussed specifications.

5.1. Differential on weak inversion level

As discussed in sections 4.1 and 4.2, the gain and input referred noise of the amplifier are strongly dependent on the trans-conductance of the differential pair, The noise can be reduced using an increased trans-conductance,allowing at the same time to increase the amplifier gain.In order to achieve a high trans-conductance on the differential pair, transistors $M_{1,2}$ were held in weak inversion, as increased trans-conductance can be obtain in this region. Although this design decision results in a power consumption increase as well as toal chip area, these were not among the main design constraints.

5.2. Noise reduction

When designing a low-noise amplifier, increasing the transistor area is a well-established technique to improve noise performance and device matching. Note that this approach can be verified from equation (5), where flicker noise is inversely proportional to the transistor area. However, despite increasing transistor area, flicker noise is still very significant. Additionally, electrochemical sensing applications commonly range between 0.01Hz and 1kHz.

Chopper stabilization is a widely used flicker noise and offset minimization technique in low noise amplifiers [12], [13]. (For better understanding of the chopper modulation principle, please read appendix C). Additionally, this requires the implementation of a low-pass filter, after demodulating the signal (this is discussed in appendix D).

As mentioned on section 2.2.2. the chopper stabilization technique is frequently implemented with NMOS switches, and the proposed architecture was shown in Figure 2.3. The proposed architecture [14], including the chopper circuits is shown in Figure 5.1.

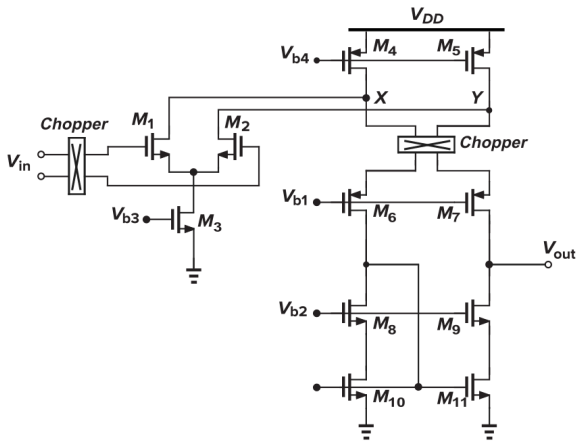

Figure 5.1. Folded cascode OTA with chopper circuit.

The chopper modulator circuit placed at the input of the amplifier is critical to range of nonlinearities and noise, therefore, critical attention was given to its design for better noise and offset minimization. Clock feedthrough and charge injection are the main fac-

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[12] Jiawei XU et al. “Measurement and analysis of input current noise in chopper amplifiers”. In: *2012 Proceedings of the ESSCIRC (ESSCIRC)*. 2012, pp. 81–84. DOI: 10.1109/ESSCIRC.2012.6341261.

[13] Jiawei XU et al. “Measurement and Analysis of Current Noise in Chopper Amplifiers”. In: *IEEE Journal of Solid-State Circuits* 48.7 (2013), pp. 1575–1584. DOI: 10.1109/JSSC.2013.2253217.

[14] Hamed Mazhab JAFARI and Roman GENOV. “Chopper-Stabilized Bidirectional Current Acquisition Circuits for Electrochemical Amperometric Biosensors”. In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 60.5 (2013), pp. 1149–1157. DOI: 10.1109/TCSI.2013.2248771.

tors resulting in nonlinearity in CMOS switches. A MOSFET operating as a switch has all its noise coming from the resistive channel between gate and source.This thermal noise is given by equation (6).

$$i^2{}_n = 4 \cdot \gamma k \cdot T \cdot K'(W/L) \cdot V_{ov} \tag{6}$$

It can be observed that improved noise performance can be achieved by keeping the lenght of the transistor used to the minumum value allowed in the CMOS process technology, whereas the width is adjusted according to the current level flowing through the transistor.By integrating half-sized dummy switches (with drain and source terminals shorted) alongside the primary NMOS switch, dynamic offset noise and charge injection effects during gate voltage transitions toward zero can be significantly reduced [15]. Since the dummy switches have their drain and source connected, their parasitic capacitances match those of the main switch, resulting in cancellation of clock feedthrough during waveform transitions. These dummy switches are driven by the complementary clock phase of the main switch to effectively suppress charge injection.

Clock feedthrough is the direct result of the parasitic gate capacitances, induced between the channel of the CMOS device and the gate metal plate, these capacitancies can be expressed as equations (7) and (8).

$$C_{gs} = \frac{2}{3} \cdot W \cdot L \cdot C_{ox} + W \cdot L_{ov} \cdot C_{ox} \tag{7}$$

$$C_{gd} = W \cdot L_{ov} \cdot C_{ox} \tag{8}$$

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[15] C. EICHENBERGER and W. GUGGENBUHL. “Dummy transistor compensation of analog MOS switches”. In: *IEEE Journal of Solid-State Circuits* 24.4 (1989), pp. 1143–1146. DOI: 10.1109/4.34103.

where, C_{gs} is gate to source capacitance, C_{gd} is drain to source capacitance, L_{ov} is the overlapping length and is and C_{ox} is gate capacitance per unit area.

The differential CMOS chopper circuit with half sized dummy switch incorporation is shown in Figure 5.2.

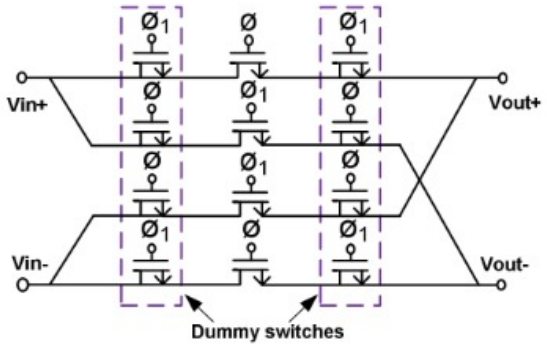

Figure 5.2. Schematic of a differential chopper circuit with dummy switches.

6. RESULTS

In this chapter, final dimensions of all the designed devices are presented, along with simulation results, covering the analysis of input-referred noise, the behavior within the frequency range of interest (0.01 Hz – 1 kHz), the variations across process corners, as well as the statistical evaluation through Monte Carlo simulations. Finally, a comparison with other studies in the state of the art is carried out, highlighting the advantages and limitations of the proposed design.

6.1. Transistor sizing

Table 6.1 lists the dimensions of the transistors that constitute the folded cascode amplifier shown in Figure 5.1. Note that the transistors in the bias branch correspond to the current mirror responsible for establishing the circuit's reference currents. In this case, long-channel transistors were employed in this branch in order to minimize copying errors and avoid the non-ideal effects associated with short-channel devices, which ensures a more stable and accurate operation.

On the other hand, the multipliers column in Table 6.1 indicates the number of transistors connected in parallel, a technique that allows achieving an effective width greater than the maximum permitted by the CMOS process technology. Similarly, the stack column specifies the number of devices connected in series on each branch; this strategy is highly relevant in the design because, it significantly reduces flicker noise.

Table 6.1. Geometric and array parameters of the MOS transistors used in the folded cascode OTA.

	MOS transistor					
Parameter	**M1/M2**	**M3**	**M4/M5**	**M6/M7**	**M8/M9**	**M10/M11**
Width [μm]	1	1	1	1	1	2
Length [μm]	2	2	2	2	2	1
Multipliers	20	10	26	9	8	8
Stack	1	1	8	1	1	4

The dimensioning of the devices on the chopper circuit are shown in table 6.1.

Table 6.2. Geometric and array parameters of the MOS transistors used in the chopper circuit.

	MOS transistor					
Parameter	**Mchp1**	**Mchp2**	**Mchp3**	**Mchp4**	**Mcc1–Mcc4**	**Mcc5–Mcc8**
Width [μm]	5	5	5	5	2.5	2.5
Length [μm]	0.15	0.15	0.15	0.15	0.15	0.15
Multipliers	10	10	10	10	10	10

For this design, a voltage biasing network was developed to ensure the correct operation of the folded cascode amplifier, where the dimensions of each device of this stage is described in appendix E.

6.2. Performance Simulations

Firstly, Figure 6.1 shows the input-referred noise behavior in a typical corner and its evolution after applying the chopping technique, including the current noise spectral density measured for three system configurations: folded-cascode without chopper, folded-cascode with chopper, and the R-TIA system. The red curve corresponding to the standalone folded-cascode exhibits a high noise level at low frequencies, typical of flicker noise. The implementation of the chopper does significantly reduces this low-

frequency noise (see blue curve), resulting in a pronounced drop in spectral density compared to the configuration without the chopper chopper.

The noise behavior of the R-TIA system, which includes all circuit blocks and an external resistor, exhibits an intermediate rms value of noise. In this configuration, the increase in noise level is primarily due to the external resistor, which was modeled considering its own thermal noise. This allows observing how the resistor contributes to the overall system noise. Notwithstanding this contribution, the performance of the R-TIA system remains superior to that of the folded-cascode without chopper at low frequencies.

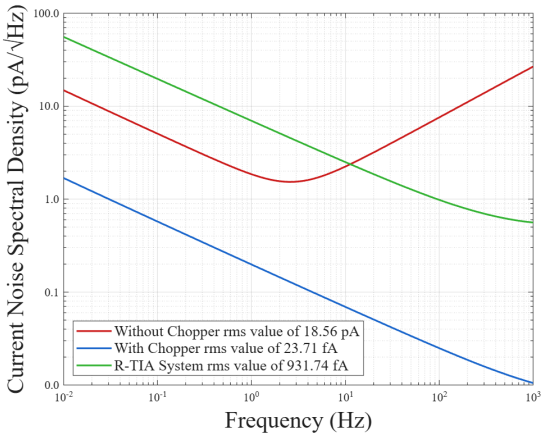

Figure 6.1. Input current noise spectral density for three different configurations of the system.

The primary justification for using an external resistor is to achieve a highly predictable and stable transimpedance gain, which is critical for measurement accuracy. Integrated resistors are subject to significant process, voltage, and temperature (PVT) variations. This introduces a major uncertainty in the amplification factor. By contrast, employing a high-precision external resistor provides the user with a stable and accurately known gain value. Once the system's internal reference voltages are calibrated, this well-defined gain ensures a direct and reliable correlation between the input current and the measured output voltage. This empowers the user to precisely calculate the

analyte's current, confident that the measurement is not being skewed by unpredictable fluctuations in the amplifier's gain.

From the analysis of the 15 worst simulation corners, presented in Table 6.3,it can be observed that the R-TIA system, considering all process, voltage, and temperature (PVT) variations, exhibits an input-referred current noise of 28 pA in the most unfavorable case.. This maximum value lies within the design specifications, validating the robustness of the circuit. Additionally, the histogram in Figure 6.2 provides a statistical analysis of these results, showing that the data present a compact and predictable distribution with a standard deviation of only 0.23 pA.

	corners														
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Temp (°C)	75	50	-50	-50	-50	100	-50	-50	-50	-25	-25	-25	-50	-50	-25
VDD (V)	1.98	1.62	1.62	1.80	1.98	1.98	1.80	1.98	1.62	1.62	1.80	1.98	1.62	1.80	1.62
Process	FS	SF	SF	SF	SF	SS	SS	SS	SS	SF	SF	SF	TT	TT	SS
Noise [pA/$\sqrt{\text{Hz}}$]	28.89	21.86	12.88	12.86	12.79	12.30	10.49	10.46	10.42	10.35	10.29	10.21	8.95	7.42	7.42

Table 6.3. Top 15 Worst-Case Noise Corners Across PVT Variations.

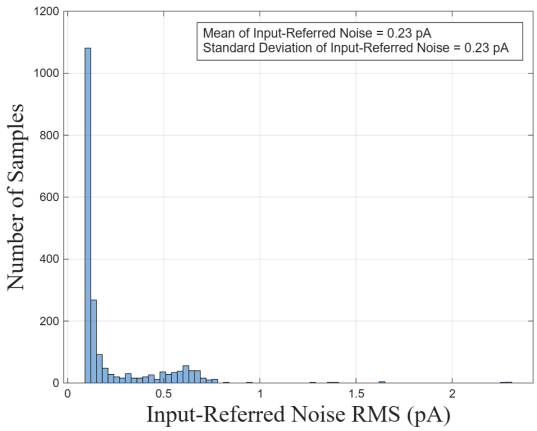

Figure 6.2. histogram of the RMS input-referred noise obtained from Monte Carlo simulations.

6.3. Linearity of the configuration

To quantify the system performance, a linearity analysis was carried out over the entire measurement range, from -1 µA to +1 µA. The circuit response to a current sweep with 100 nA steps is presented in Figure 6.3. The results demonstrate an exceptionally predictable behavior, achieving a linear fit with a correlation coefficient of 0.9999991. For a more rigorous validation, the experimental data were compared with the following ideal theoretical model.

$$V_{\text{out}} = -R_{es} \cdot I_n + 0.9 \tag{9}$$

This model employs the transimpedance resistance of 200 kΩ, which was selected during the design stage to map the input current to the linear output range of the amplifier. Based on this reference, the error at each measurement point was evaluated, as illustrated in Figure 6.3. The error analysis revealed highly precise performance, with a maximum error not exceeding 0.1% across the entire operating range.Taken together, these results quantitatively confirm that the system exhibits a highly linear and consistent response, thus validating the proposed design.

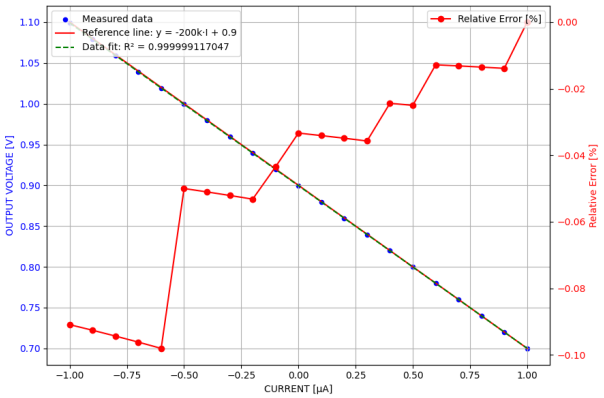

Figure 6.3. Linearity comparison between measured data and the ideal reference line and Relative error per point with respect to the reference line with 100 nA step resolution.

In Figure 6.4, a second linearity analysis is presented, this time considering the measurement range drom -10 nA to 10 nA, with a sweep step of 1 nA. The results show a linear fit with a correlation coefficient of 0.9999981, which demonstrates that even at smaller current scales and with reduced steps, the system preserves its linear behavior. This confirms that linearity is maintained not only over wide operating ranges but also under stricter resolution conditions, thereby reinforcing the reliability of the design, According to information in Figure 6.4, the maximum error in this range is approximately 0.035%, supporting the high accuracy of the system even under low-signal conditions.
Although the comparison with the ideal straight line defined by (Equation 9)
allows evaluating the linearity of the system, this reference is not entirely fair. This is because the value of V_{cm} is subject to variations in the circuit offset. Such variations modify the initial point of the DC response and, consequently, alter the correspondence between the input current and the output voltage. In practice, this effect can shift the measured curve with respect to the ideal line, even when the relative linearity between the samples is preserved.
The impact of this offset is that the user perceives a systematic shift in the measurements, which does not originate from a lack of linearity in the system, but rather from a mismatch in the reference level. To mitigate this issue, the end user can implement an initial calibration process, consisting of recording the system output with a null input current ($I_n = 0$) and using that value as the new reference point. In this way, the effect of the offset is compensated, and subsequent measurements reflect only the true current-voltage relationship of the system.

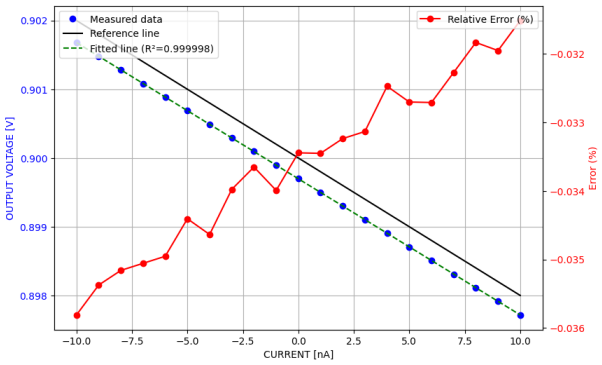

Figure 6.4. Linearity comparison between measured data and the ideal reference line and Relative error per point with respect to the reference line with 1 nA step resolution.

Monte Carlo simulations were carried out to evaluate the robustness of the design against statistical variations of the technological parameters. As shown in Figure 6.5, the ten iterations exhibit an almost complete overlap, producing linear traces with a consistent trend. This behavior demonstrates that the linearity of the amplifier remains unaffected under these conditions, confirming that the circuit performance is not compromised by process-induced variations.

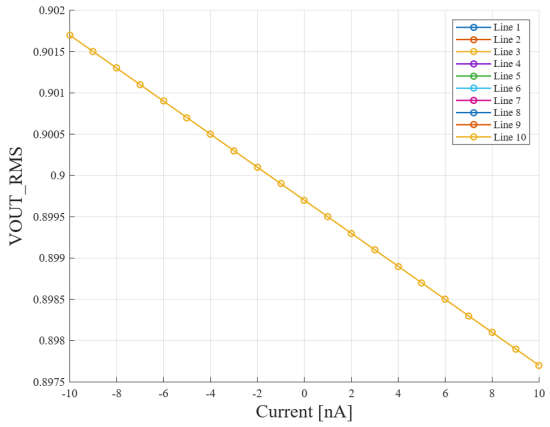

Figure 6.5. Results of 10 Monte Carlo iterations of the R-TIA system

6.4. Comparison

As shown in Table 6.4, the obtained results confirm that the proposed design meets the established targets across all evaluated parameters, including supply voltage, input noise, bandwidth, linearity, and maximum current error rate. In each case, the achieved performance matches or exceeds the specifications of the design target.

Parameter	**Design Target**			**Our Work**			**Judgment**
	Min	**Typ**	**Max**	**Min**	**Typ**	**Max**	
VDD [V]	-	1.8	-	1.62	1.8	1.92	✓
Input noise (rms, 0.01Hz–1kHz) [pA]	-	-	100	0.5	18	28	✓
BW [kHz]	1	-	-	1.24	292.23	613	✓
Linearity R^2	0.999	-	-	0.9999981	-	0.999999	✓
Max. Current Error Rate (%)	-	TDB	-	-	-	0.1	✓

Table 6.4. Performance comparison between design target and the parameters obtained from simulation of the proposed design

Considering the whole results, Table 6.5 presents a comparison with representative works from the state of the art. The parameters taken into account were technology, operating voltage, input noise level, current range, resolution, maximum error rate, power consumption, readout type, and whether the report corresponds to simulation or measurement.It can be observed that the proposed design achieves a significant advantage in terms of low input noise (28 pA) and wide current range coverage ($\pm$1 nA to $\pm$1 μA).

Parameter	**This Work**	[16]	[17]	[18]	[19]	[20]
Technology [µm]	0.028	0.35	0.13	0.18	0.18	0.18
VDD [V]	1.8	3.3	3/1.5	3.3	0.9	1.8
Input noise (rms, 0.01Hz–1kHz) [pA]	28	0.012	–	2.4p	0.024	–
Current Range (A)	± 1 n to ± 1 u	± 24 p to ± 350 n	± 10 n to ± 1 m	±1 n to ±1 m	± 50 n to $\pm 400\,\mu$	100 p to $50\,\mu$
Resolution (A)	1n	-	91.7p	-	1n	14p
Max. Current Error Rate (%)	$<$0.1	$<$5	$<$2	–	1.3	4.27
Power Consumption	126uW	4 μW	3 mW	13.86 mW	60.8 μW	51 μW
Linearity R^2	0.9999981	0.99999993	0.999997	0.9991	0.999999993	0.999999998
Readout Type	R-TIA	Current Conveyor	Current Conveyor	R-TIA and C-TIA	Current Conveyor	Current Mirror
Simulation or Measurement	S	M	M	M	S	M

Table 6.5. Performance comparison between this work (28 nm CMOS) and state-of-the-art references.

7. CONCLUSIONS AND FUTUREWORK

7.1. Conclusions

This work presented the design and validation of a current acquisition system in 28,nm CMOS technology, capable of measuring currents in the range of $\pm$1,nA to $\pm$1,μA with a step of 1,nA, thus meeting the objectives of resolution and accuracy. The system achieved a linearity of 0.9999981, ensuring highly reliable performance across the entire operating range. The implementation of the chopper technique was successful, effectively contributing to noise reduction. The proposed architecture incorporates an external configurable resistor, which allows the measurement range to be adjusted easily and flexibly without modifying the internal circuit design.

The simulations considered the noise of a 200,kΩ resistor, obtaining a maximum RMS noise value of 28,pA integrated between 0.01,Hz and 1,kHz. The substance–electrode–current acquisition interaction was also modeled as a current source at the input. The design was evaluated under process, voltage, and temperature variations, successfully passing all tests.

7.2. Futurework

- As a future line of work, the development of a second-order or higher active low-pass filter with a cutoff frequency close to 1 kHz, fully integrated in CMOS technology, is proposed. This filter would be optimized for low-noise, input-referred current acquisition systems, since an active topology enables the realization of effective resistance and capacitance values that would be impractical in passive implementations, while providing precise control over frequency response and overall system stability.

The design of this block requires the development of operational amplifiers or transconductance (Gm) stages with extremely low intrinsic noise, high linearity, and sufficient phase margin to tolerate process, voltage, and temperature variations. It will also be necessary to evaluate its interaction with the current acquisition stage, considering input impedance, noise coupling, and potential feedback effects. In this context, exploring architectures such as multiple-feedback active filters or Gm-C filters will help identify the most robust solution in terms of stability, post-fabrication tuning, and interference resilience, thereby optimizing system response and enabling the integration of very low-frequency active filters into precision measurement applications.

- The development of a full-custom layout for the proposed circuit will be carried out, ensuring precise transistor placement and optimized routing strategies to minimize parasitic effects. Special attention will be given to matching-critical devices and to the physical symmetry of sensitive nodes in order to preserve the intended electrical performance. Post-layout simulations will be performed to evaluate the impact of parasitics and to validate the circuit's behavior under silicon-like conditions, ensuring that the final implementation meets the design specifications.

- Due to the implementation of the chopper technique in the system, the design and integration of a square-wave generator block operating at the specified switching frequency is required. This block must provide a precise timing reference, with stability in amplitude, duty cycle, and frequency, in order to ensure the correct operation of the modulation and demodulation stages associated with the chopper. The quality of this signal is critical, as any deviation in its parameters could introduce unwanted noise components or distortion, directly affecting the overall performance of the system.

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A. ICMR and OVSR Analysis

A.1. OVSR

The Output Voltage Swing Range (OVSR) is the range of output voltages that an amplifier can produce while maintaining proper operation, linearity, gain and deliver signals without distortion. The output voltage is measured as shown in Figure A.1. It can be observed that the region of interest is where the output voltage has a linear behavior.

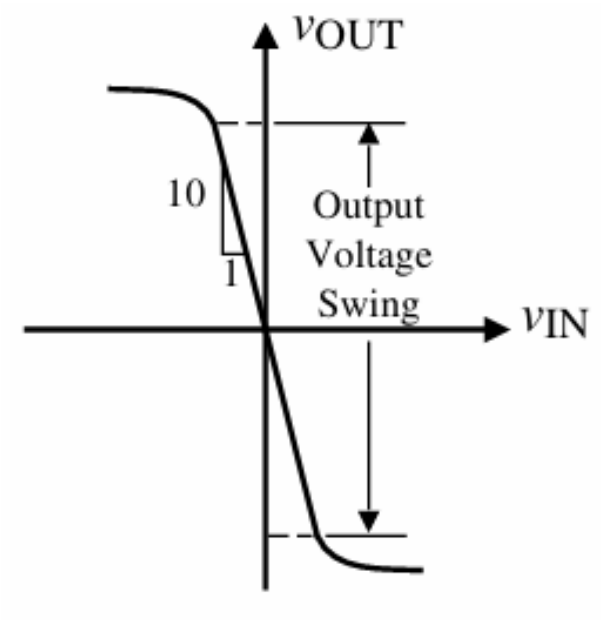

Figure A.1. Represenytative graph of the output voltage swing range.

In electrochemical measurement applications, the sensed signals can vary over several orders of magnitude (from picoamperes to microamperes). When these currents are converted to voltages by the amplifier, the output voltage must accommodate this wide range without saturating. A limited OVSR would distort large signals, reducing measurement accuracy and dynamic range, which makes it crucial to meet the required

OVSR.

In the context of a folded cascode OTA, the OVSR is limited by the maximum and minimum output voltages that the amplifier can deliver while maintaining MOS transistors in the desired operation region (usually in saturation). The maximum output voltage thatthe amplifier can deliver is stablished by the difference between VDD and the overdrive voltages of transistors $M_{4,5}$ and $M_{6,7}$ as can be seen in Figure A.2. the minimum voltage the amplifier can deliver is established by the overdrive voltages of the transistors $M_{8,9}$ and $M_{10,11}$. And the OVSR is then given by equation (10)

$$OVSR = V_{DD} - V_{ov4,5} - V_{ov6,7} - V_{ov8,9} - V_{ov10,11} \tag{10}$$

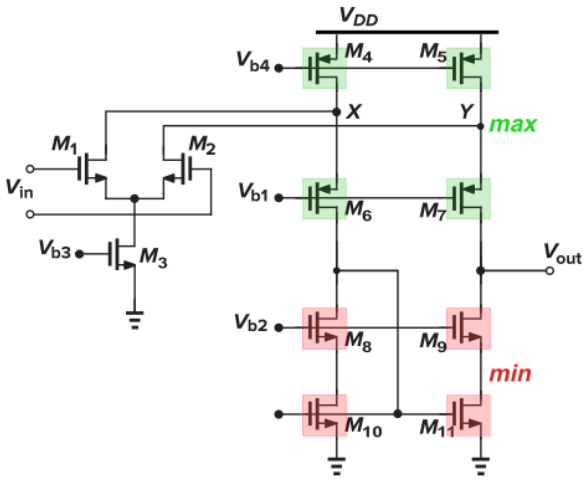

Figure A.2. OVSR analysis of the OTA, specifying the transistors related to the maximum (shaded in green) and the minimum (shaded in red) output voltage.

A.2. ICMR

Input Common Mode Range (ICMR) specifies over what range of input voltages the differential pair continues to sense and amplify the difference input signal with the same gain while maintaining linearity. Figure A.3 shows how the ICMR is measured, where

the linear part of the transfer curve where the slope is unity corresponds to the input common-mode voltage range.

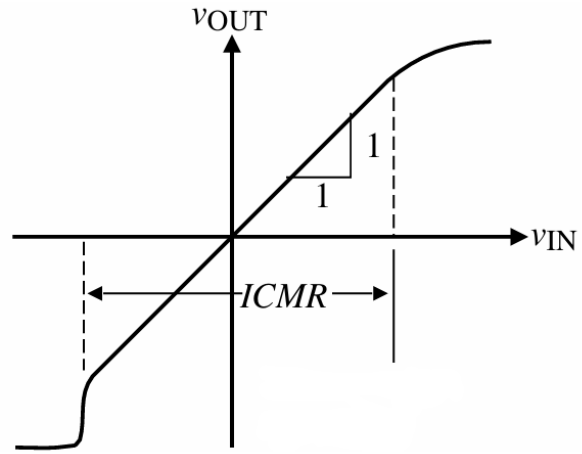

Figure A.3. Representative graph of the common mode range

In a folded cascode OTA, the ICMR is limited by the maximum and minimum input voltages that the amplifier can take at its terminals while maintaining transistors in the desired operation region. The maximum input voltage the amplifier can take is stablished by the sum of bias and source-gate voltage of transistors $M_{6,7}$ (these transistor fix the drain voltages of input transistors), and the threshold voltage of transistors $M_{1,2}$, as can be seen in Figure A.4. Whereas the minimum input voltage the amplifier can take is stablished by the sum of the gate-source voltage of transistors $M_{1,2}$ and the overdrive voltage of transistor M_3. The ICMR is then given by equation 11

$$ICMR = Vb_{6,7} + V_{sg,6,7} + V_{th1,2} - V_{gs1,2} - V_{ov3} \tag{11}$$

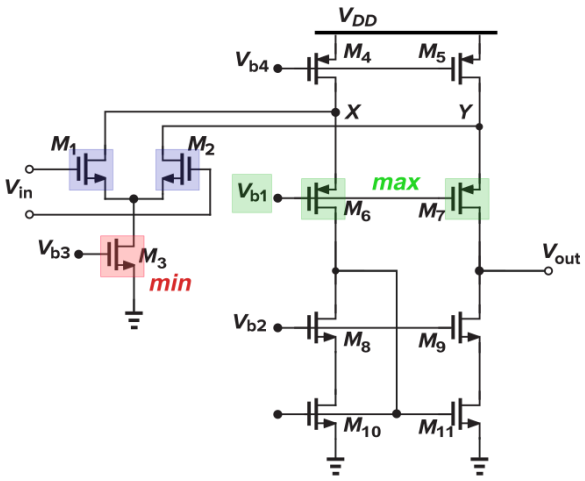

Figure A.4. ICMR analysis on OTA, specifying the transistors associated with the maximum (shaded in green and violet) and the minimum (shaded in red and violet) input common-mode voltage.

B. Supply independent biasing

In order to ensure the correct operation of the system, where the folded cascode is the main stage, a separate power supply circuit is required to provide the necessary voltages to bias the main stage. The proposed independent supply bias circuit topology is shown in Figure B.1. This circuit generates independent constant currents regardless of the supply, allowing the implementation of multiple current mirrors to generate voltage points that satisfy the biasing conditions of the amplifier module.

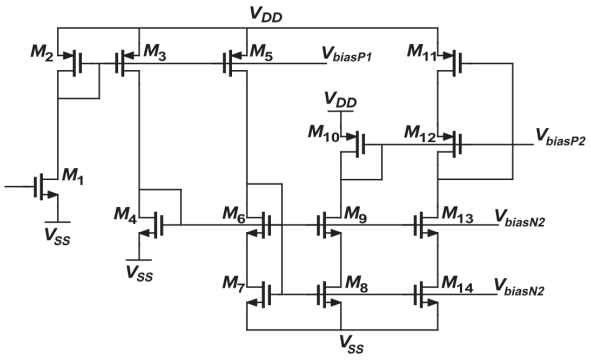

Figure B.1. Schematic circuit for biasing.

C. Chopper Stabilization Principle

Chopper Stabilization works based on modulation and demodulation principles. There is a first chopper circuit is placed at the input of the circuit, where it modulates the sensed input signal to a higher chopping frequency, where there is limited flicker noise. After amplification, second chopper circuit is placed at the output of the circuit which demodulates back the signal to the baseband without affecting noise and offset, which remain at the odd harmonics of the chopping frequency [21].The chopper stabilization principle is ilustrated in Figure C.1.

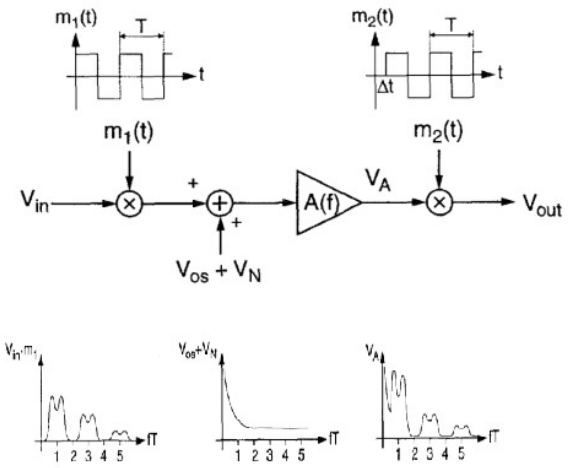

Figure C.1. Diagram showing the chopper stabilization principle. m1(t): modulation signal, Vos: offset voltage.

[21] N. Y. SUTRI et al. “Low-noise, low-offset modulator demodulator circuit for chopper stabilization technique in CMOS-MEMS sensor applications”. In: *2014 5th International Conference on Intelligent and Advanced Systems (ICIAS)*. 2014, pp. 1–5. DOI: 10.1109/ICIAS.2014.6869473.

D. Design of a low-pass filter

Due to the nature of the high frequency square wave modulating signal, the input signal will be shifted not only to the chopping frequency (F_{ch}) but to its odd harmonics as well. The signal is amplified, however, this process introduces some other undesired high frequency artifacts, such as switching transients, residual offset, and the odd harmonics. This makes necessary the design of a low pass filter to supress these high-frequency components. Additionally, due to the inherent limitations of a first-order low-pass filter, the design of a higher-order low-pass filter with a cutoff frequency of 1 kHz is recommended. A first-order filter provides only $-20dB/dec$ attenuation beyond the cutoff frequency, which is insufficient to adequately suppress the higher-order harmonics generated by the chopping process and other non-idealities. As a result, these harmonics can leak into the baseband, degrading the signal integrity. By employing a filter of higher order, the roll-off slope is increased (i.e. $-40dB/dec$ second-order filter, $-60dB/dec$ third order filter, etc), therefore, providing better rejection of unwanted harmonic components while preserving the desired signal. Then, an ideal low-pass filter was incorporated.

E. Device dimensions of biasing stage

The implementation of this biasing network provides robustness against process and temperature variations, guaranteeing reliable and stable performance that maintains the folded cascode properly biased. The dimension of each device can be seen in table E.1.

Table E.1. Geometric and array parameters of the MOS transistors used in the biasing circuit.

MOS transistor							
Parameter	**M1**	**M2/M3**	**M4**	**M5**	**M6/M7**	**M8/M9**	**M10**
Width [μm]	0.41	0.49	0.32	0.28	1.00	0.43	0.70
Length [μm]	2.00	2.00	1.50	2.00	2.00	2.00	2.00
Multipliers	1	1	1	1	1	1	1
Stack	2	1	3	3	1	1	8