

APPENDIX A

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1 Analog Front End

Typically, the continuous-time linear equalizer is only one part of a complete AFE system; therefore, in a larger project it is necessary to give specification to each component. Fig. 0.1 shows the topology normally used for the AFE, which is composed of an impedance coupling circuit, a CTLE and a variable gain amplifier (VGA)¹. In

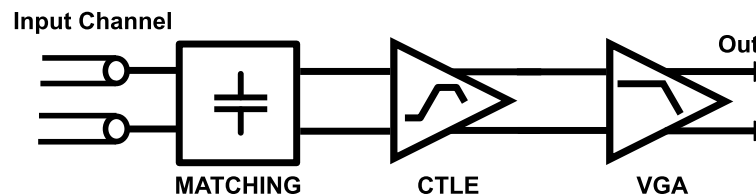


Figure 0.1. Basic AFE.

the architecture proposed by the research group for the RX, after the AFE, a strong arm comparator is expected to be found. Considering that this circuit was previously designed by the Onchip research group ², a proposal was made for the topology and specifications required in the AFE to deliver an adequate signal to the next stage. In the state of the art, some architectures have been observed, such as ³, which proposes

¹ Jiahui ZHENG et al. "A 16gbps programmable ctile design with adjustable gain". In: *2023 3rd International Conference on Electronic Information Engineering and Computer Science (EIECS)*. IEEE. 2023, pp. 220–225.

² Nestor Ivan MATAJIRA ORTIZ DANIEL FELIPE BARRIOS RUEDA. "Design of Energy-Efficient Voltage Comparators for a System-on-Chip Using a CMOS Technology Node of 28nm". Bachelor's thesis. Universidad Industrial de Santander, May 15, 2024.

³ Jonghyuck CHOI et al. "A single-ended nrz receiver with gain-enhanced active-inductive ctile and

an architecture that uses two CTLEs in order to increase the equalization capacity of the system. Based on this information, the architecture shown in Fig. 0.2 is proposed.

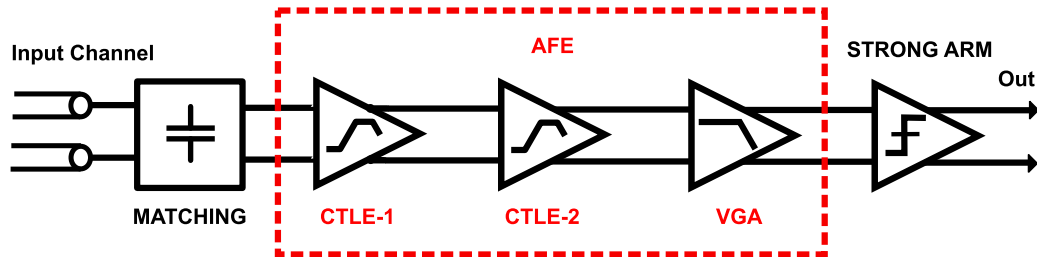


Figure 0.2. Proposed AFE and strong-arm.

Taking as reference the USB 4 gen 3 protocol ⁴ it is established that the AFE output requires a horizontal aperture of $27[ps]$, while the strong arm requires a minimum vertical aperture of $40[mV]$, both data at a BER of 10^{-6} . The VGA should provide a flat-band gain of $2[V/V]$ and the second CTLE should provide a minimum DC gain of 0 dB to avoid vertically decreasing the aperture of the eye-diagram, in addition to the typical high-frequency gain. Based on these considerations, the table 0.1 shows the main specifications for each circuit composing the AFE.

Table 0.1. Design specifications

Circuit	CLTE1	CTLE2*	VGA**
EH [mV]	20	20	40
EW [UI]	0.4	0.54	0.54

* $A_{DC} \geq 0$ [dB], $C_{in} \leq 50$ [fF] ** $A_V \geq 2$ [V/V]

reference-selection dfe for memory interfaces". In: *IEEE Journal of Solid-State Circuits* 59.4 (2024), pp. 1261–1270.

⁴ USB IMPLEMENTERS FORUM. *USB4™ Specification Version 2.0 with Errata and ECN through September 2024 – REDLINE*. <https://www.usb.org/document-library/usb4r-specification-v20>. Accessed: 2025-06-09. 2024.

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