VOLTAGE-TO-FREQUENCY CONVERTER DESIGN FOR SYSTEM-ON-CHIP TESTING IN 0.35 µm CMOS TECHNOLOGY

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RESUMEN

Título DISEÑO DE UN CONVERSOR TENSIÓN A FRECUENCIA PARA PRUEBAS DE SISTEMAS EN CHIP EN TECNOLOGÍA CMOS 0.35 µ m*

Autor Luis Eduardo Chaparro Roa **

Palabras clave ADC, Baja potencia, Baja tensión, Mismatch, VFC, Montecarlo, Offset., System-on-Chip.

DESCRIPCIÓN

Este reporte presenta el diseño de conversor tensión a frecuencia con compensación en temperatura en0.35µm CMOS adecuado para probar sistemas en chip. El diseño propuesto utiliza la arquitectura multi-vibrador y permite una tensión de entrada riel a riel. El conversor tensión frecuencia opera a una tensión de alimentación de 3.3 V ±10% en un rango de temperatura de 0 °C a 60 °C, y la frecuencia de la señal de salida varía entre 73,1 kHz a 1,2 MHz dependiendo de la tensión de entrada. Los resultados de simulación muestran un consumo de energía de 802µW, un error relativo inferior a 1,2%, un error de sensibilidad inferior a 3: 42% y un error de linealidad de 0: 03%. Se utiliza una técnica para reducir el consumo de potencia en los comparadores basándose en el modo de operación y las señales de control, así se reduce un 10% el consumo de potencia de estos circuitos. La técnica de compensación en temperatura utiliza los materiales RPOLYH y RNWELL para la resistencia compensada. Se seleccionan estos materiales ya que presentan mayor resistencia por cuadro y poseen coeficientes de temperatura con signo opuesto, por lo tanto, se obtiene una variación menor al 0.003% para el rango de temperatura de operación. Se incluyen simulaciones de Montecarlo y esquinas para comprobar la confiabilidad del circuito, además se realiza una comparación con trabajos que hacen parte del estado del arte.

* Trabajo de grado

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ABSTRACT

Title VOLTAGE-TO-FREQUENCY CONVERTER DESIGN FOR SYSTEM-ON-CHIP TESTING IN 0.35 MM CMOS TECHNOLOGY*

Author Luis Eduardo Chaparro Roa **

Keywords ADC. low-power, Low-voltage, Mismatch, mixed integrated circuits, Montecarlo, Offset, System-On-Chip, VFC.

DESCRIPTION

This report presents a temperature-compensated voltage-to-frequency converter design in CMOS 0.35µm suitable for system-on-chip testing. The proposed design uses the multi-vibrator architecture and allows a rail-to-rail input voltage. The VFC works with a 3.3V ±10% supply voltage in a temperature range from 0 °C to 60 °C, and its output signal frequency varies between 73.1 kHz to 1.2 MHz depending on the input voltage. Simulation results show a power consumption of 802µW, a relative error below 1.2%, a sensitivity error below 3.42% and a linearity error of 0.03%. A technique is used to reduce the power consumption in the comparators based on the mode of operation and the control signals, thus reducing the power consumption of these circuits by 10%. The temperature compensation technique uses the RPOLYH and RNWELL materials for the compensated resistor. These materials are selected because they present greater resistance per square and have temperature coefficients with opposite sign, therefore a variation lower than 0.003% is obtained for the operating temperature range. Monte Carlo simulations and corners are included to check the reliability of the circuit, in addition, a comparison is made with works that are part of the state of the art.

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INTRODUCTION

Experimental tests need additional circuits which increase the current consumption and area of the chip. These tests need analog-to-digital conversion. A voltage-to-frequency converter (VFC) offers a solution for the analog-to-digital conversion, its area is smaller and its power consumption is lower than an ADC, besides a VFC can be directly interfaced to a microcontroller using a single digital input- output port. It is necessary a frequency-to-code conversion in the microcontroller for getting done the analog-to-digital conversion.

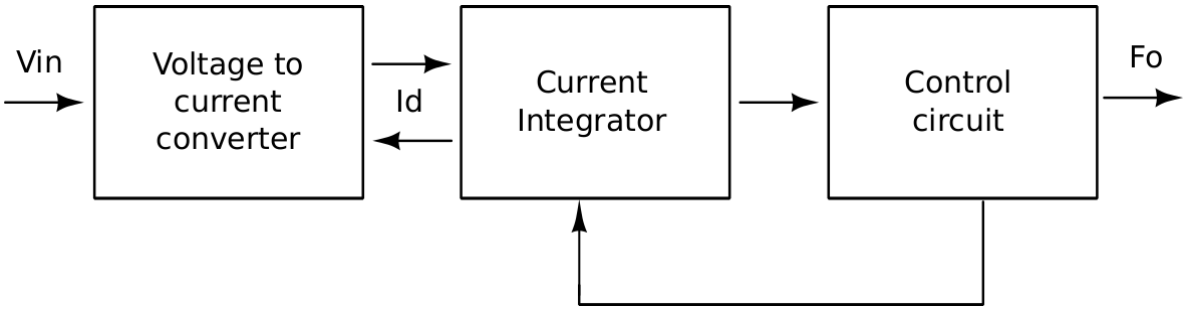
Voltage-to-frequency converters (VFCs) are basically oscillators working at a frequency proportional to the input voltage, that is, F out = KV in. These circuits often are denominated as quasi-digital converters. There are several types of VFCs, such as charge-balance VFCs and multivibrator VFCs. These are mainly based on a voltage-to-current converter (VIC) followed by a current-to-frequency converter (IFC), besides a control circuit. The control circuit allows low power digital conversion.

This report describes the design of a voltage-to-frequency converter for system-on-chip testing in 0.35µm CMOS technology. This design presents low power consumption, high linearity, and a rail-to-rail input voltage. Section II presents briefly the most recent and best performance VFC architectures. Section III explains the architecture used in this work. Section IV describes the VFC design. Finally, the simulation results and conclusions are presented in sections V and VI respectively.

1. VOLTAGE TO FREQUENCY CONVERTERS

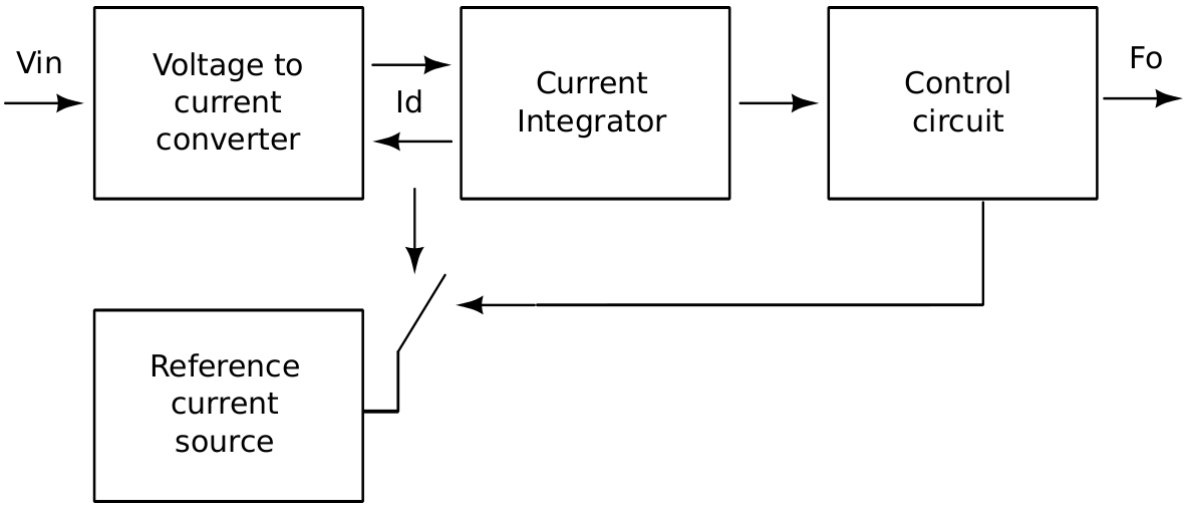
The block diagram of a multivibrator VFC is shown in Fig. 1. This architecture is composed of a voltage-to-current converter (VIC), followed by a current integrator, which is driven by a control circuit.

Figure 1. Block Diagram multivibrator VFC



The operation of this architecture is described next: The VIC converts the input voltage (V in) to current, following this, the VIC output current charges or discharges a capacitor, the block responsible for this task is the current integrator, whose output voltage is a linear triangular wave between two voltage levels VH and VL. VH and VL are voltage references used by the comparators. The control circuit drives the current integrator and establishes a voltage signal whose frequency is F o, where F o is directly proportional to the input voltage (F o = KV in).

Figure 2. Block diagram Charge-balance VFC.



Charge-balance VFC is presented in Fig. 2 [4]. The principle of operation of the charge-balance VFC architecture is similar to multivibrator VFC. Its architecture is composed of a VIC, a current integrator, and a control circuit. The control circuit includes a reference current source as can be noted in the diagram. Therefore, the charge-balance VFC is more complex than the multivibrator VFC and provides better linearity, however, its power consumption is higher.

2. ARCHITECTURE

2.1 VOLTAGE-TO-CURRENT CONVERTER.

Basically, this circuit is based on a negative feedback, it is compound of two operational transconductance amplifier (OTA), M 1 and M 2 transistors and Rs, R1 and R2 resistors. As shown in Fig. 3. The input voltage (V in) is scaled by a factor a = R 2 / (R 1 + R 2) at node Va (Va = aVin).

Figure 3. Schematic of the proposed voltage-to-digital converter.

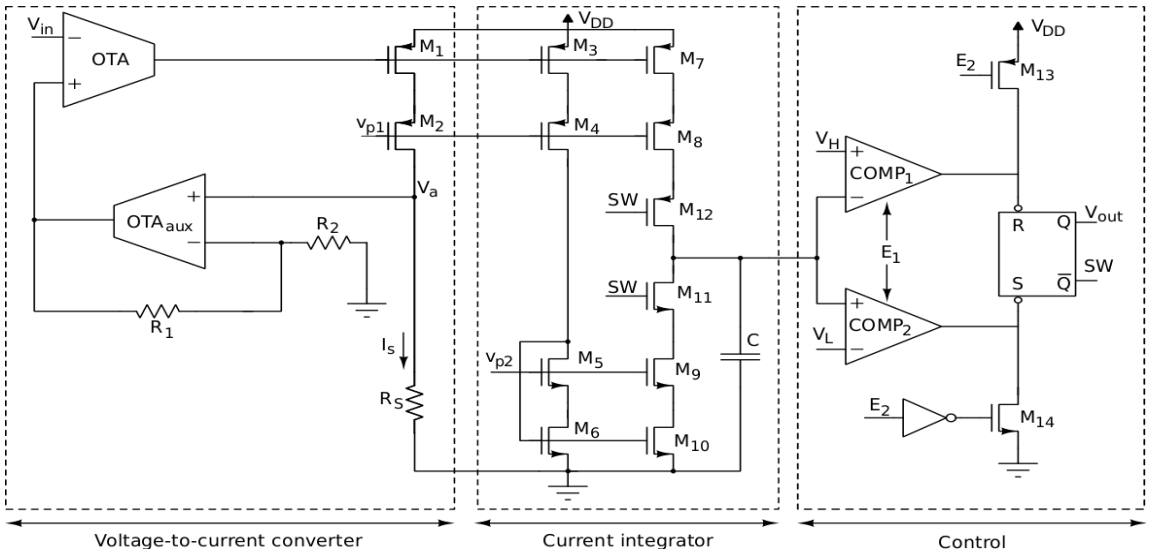


Figure 4. Conventional V-I converter with cascode mirror.

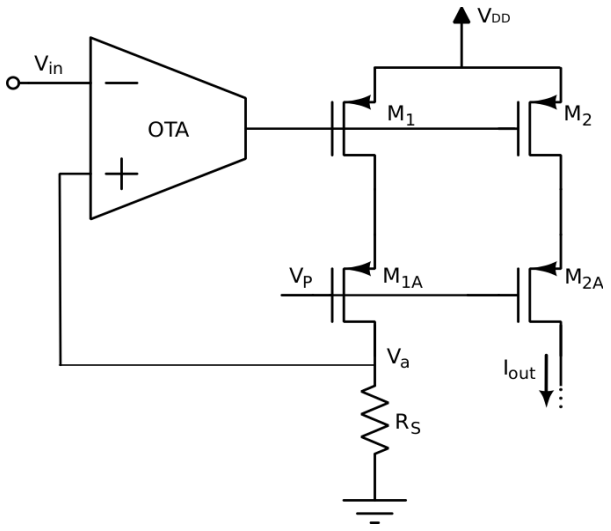


Fig. 4 shows a simpler VIC topology than the topology presented in Fig. 3. Contrasting with the topology shown in Fig. 3, this only is composed by an OTA, M 1 and M 2 transistors and the resistor Rs. This VIC has a less range of excursion. The input V in must be sufficiently low to keep M 1 and M 1A in saturation. The topology shown in Fig. 3 solves this problem because the voltage V a is aVin (a < 1). Therefore, the VIC output current (Is) is V a/Rs. The OTA architecture that receives the input voltage (V in) is shown in Fig. 5. To increase the range of excursion to input an OTA rail-to-rail is used. This OTA is composed of two differential pairs, a PMOS and other NMOS pair. Thus, it achieves a higher common mode input voltage composed of three main operation regions. These regions are function of the input voltage and are shown in table 1. In each region of operation, a significant variation of the circuit characteristics is presented.

Figure 5. Schematic of the VIC OTA.

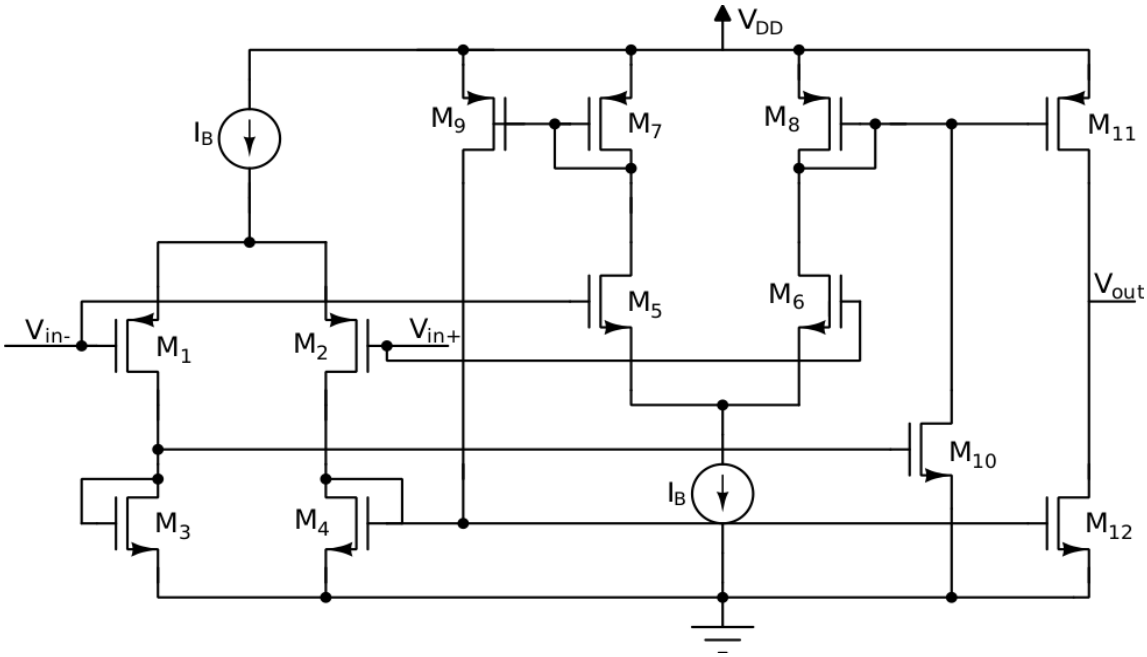


Table 1. Region of operation OTA.

Region	PMOSPair	NMOS Pair
1	ON	OFF
2	ON	ON
3	OFF	ON

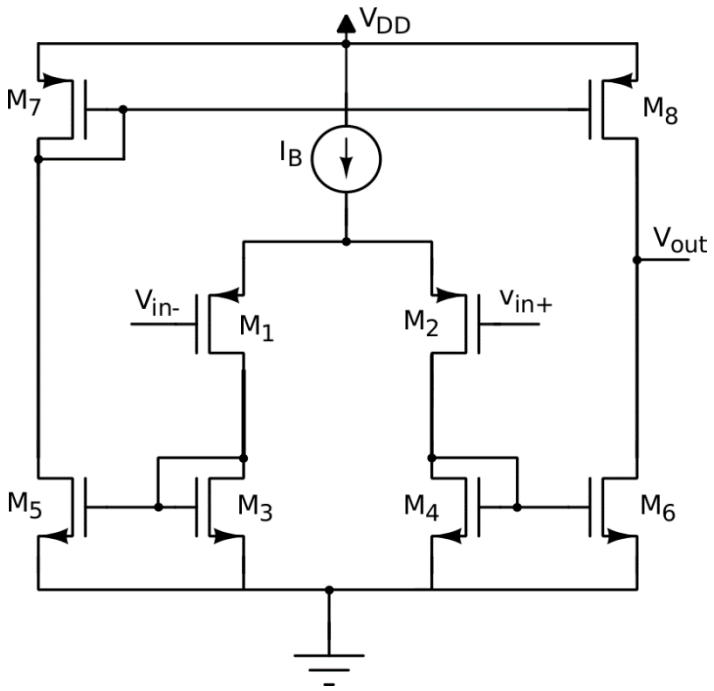
Table 2 shows the transconductance (Gm) and output resistance (R) [4] for the three regions presented in table I. As shown in Fig 3, there is an auxiliary OTA (OTAaux) whose architecture can be seen in Fig. 6. It is a symmetrical OTA with a PMOS input differential pair. A PMOS differential pair was selected because the OTAaux input voltages are low (aV

in). This OTA architecture is more symmetrical than a Miller OTA, therefore, it presents a lower offset voltage.

Table 2. Main parameters of OTA.

Region	Gm	R
1	gm1	1 / IB(λ11 +λ12)
2	gm1 + gm5	1 / 2IB(λ11 +λ12)
3	gm5	1 / IB(λ11 +λ12

Figure 6. OTAaux topology.



2.2 CURRENT INTEGRATOR.

This circuit copies the current established by the VIC using a high-swing cascode mirror, in order to improve the current copy and manage low voltages [6]. The current integrator includes transistors M 11 and M12, these transistors behave like switches for the current flow that controls the charge/discharge of the capacitor. M11 and M12 are enabled by a signal from the control circuit.

2.3 CONTROL CIRCUIT.

The control circuit is made up by two comparators and an RS flip-flop as shown in Fig. 3. This circuit established the signal that enables the M11 and M12 transistors, which charge or discharge the capacitor C. Also, this circuit is responsible for delivering the output signal (V out). The comparator architecture is shown in Fig. 8, which consists of a simple differential pair and an inverting gate. This comparator includes a control system to optimize power consumption, through M5 transistor. Finally, as can be seen in Fig. 3, the control circuit contains an RS flip-flop. This enables/disables the transistors that control the charge and discharge of the capacitor. Fig. 7 shows the main signals of this circuit. The waveform of the voltage capacitor (V cap) is linear triangular between the VH and VL levels.

Figure 7. F out, V CL, V CH and V CAP in the time-domain.

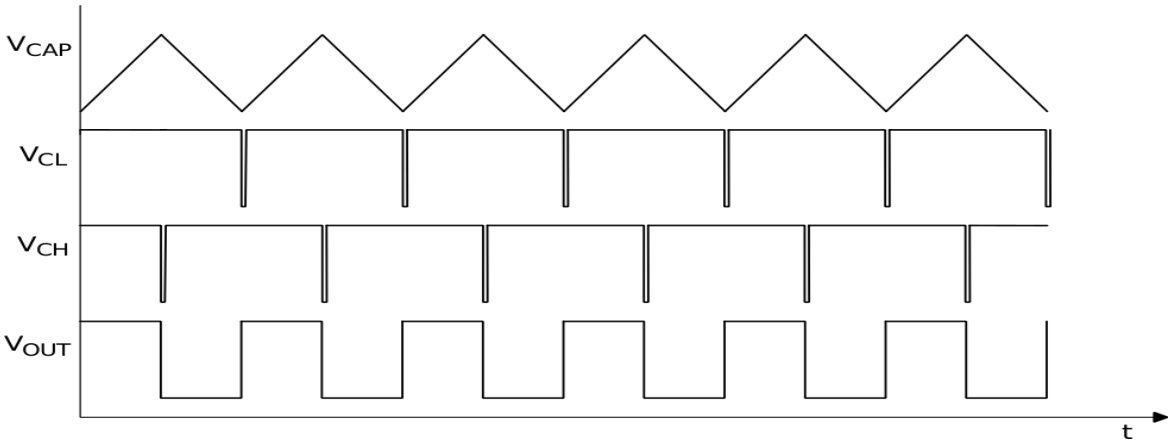
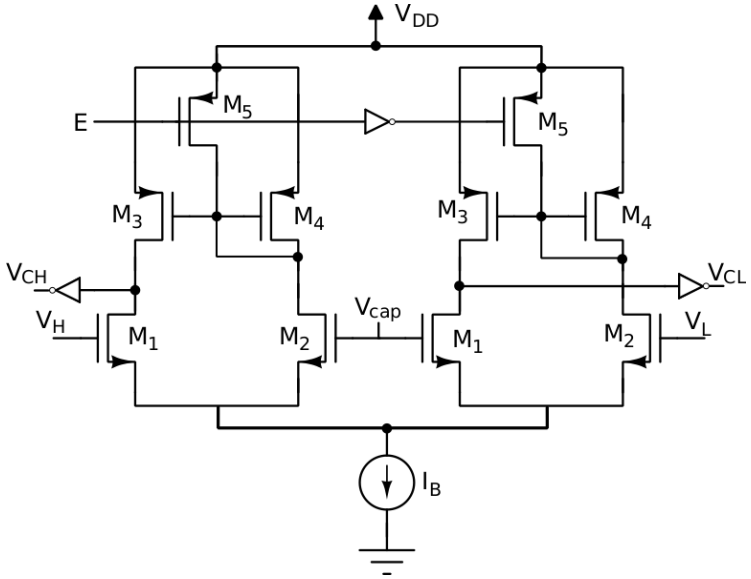


Figure 8. Schematic of the two comparators.



The comparator is only active when the voltage level of the capacitor determines the necessity of operating. Also, can be seen VCH and VCL voltages. These voltages are the output of the comparators that are connected to the R and S inputs of the flip-flop. Table 3 describes the R and S signals and the Q and Q outputs that characterize the RS flip-flop shown in Fig. 3.

Table 3. Description of control system signals.

Vcap	S	R	Q	~ Q
–	0	0	0	0
V cap ≤ V L	0	1	1	0
V cap ≥ V H	1	0	0	1
V L ≤ V cap ≥ V H	1	1	Last Q	Last ~Q

3. CIRCUIT DESING

This work consists of designing a voltage-to-frequency converter (VFC) for system on chip testing in 0.35µm CMOS with low power consumption and high linearity for a rail-to-rail input voltage. The main equation that defines this design is shown below in (1). This equation describes the relationship between the output frequency (F_{out}) and the design parameters of this architecture, where a is the scale factor of the voltage V in, which is defined as $a = R1/(R1 + R2)$, K is the scale factor of the current mirrors, C is the integration capacitor, $\boldsymbol{V_H}$ and V_L are the voltage references and Rs is a resistor that makes part of the current-to-voltage converter.

$$\boldsymbol{F_{out} = \frac{aV_{in}}{2KC(V_H - V_L)R_S}} \quad (1)$$

Transistors M 1 and M 2, shown in Fig. 3, are part of a current mirror, these transistors must remain in saturation to preserve the linearity of the VIC. Therefore, the voltage V a must satisfies (2).

$$\boldsymbol{Va \leq VDD - VDS_{SATM1} - VDS_{SATM2}} \quad (2)$$

For the proposed design R1 = R2, in that way the attenuation factor (a) is 0.5, which help to keep M 1 and M 2 in saturation. Rs is set to 20 kΩ and C in 3.2 pF as a trade-off between current consumption and area. The scale factor K of the current mirrors is set to 8 in order to reduce power consumption. Equation 1 defines an inversely proportional relationship between frequency (F out) and the resistance Rs. Thus, this equation describes a dependence on resistor temperature variations. In order to reduce the impact of temperature variations and optimize area [7], Rs is formed as a series connection between a RPOLYH material resistor ($TC = -0.4x10^{-3}\ K^{-1}$) and other RNWELL resistor ($TC = 6.2x10^{-3}\ K^{-1}$).

M11 and M12 transistors operate like switches in the current integrator, those transistors were designed using the minimum channel length, likewise, the transistors that make part of the RS flip-flop and the comparator. The above setting is done in order to optimize the speed of the transistors transition. In (3) is defined the time of charging or discharging of the capacitor C. Therefore, the capacitor C and V_H and V_L voltages adjustments are made considering the maximum output frequency that can be read by the microcontroller, which is responsible for performing the frequency-to-code conversion.

$$\boldsymbol{t = \frac{C(V_H - V_L)}{I} = \frac{T}{2}} \quad (3)$$

$\boldsymbol{V_H}$ and $\boldsymbol{V_L}$ voltages must have high accuracy, high PSRR and temperature independent. Therefore, these voltages must be established by a bandgap reference with these

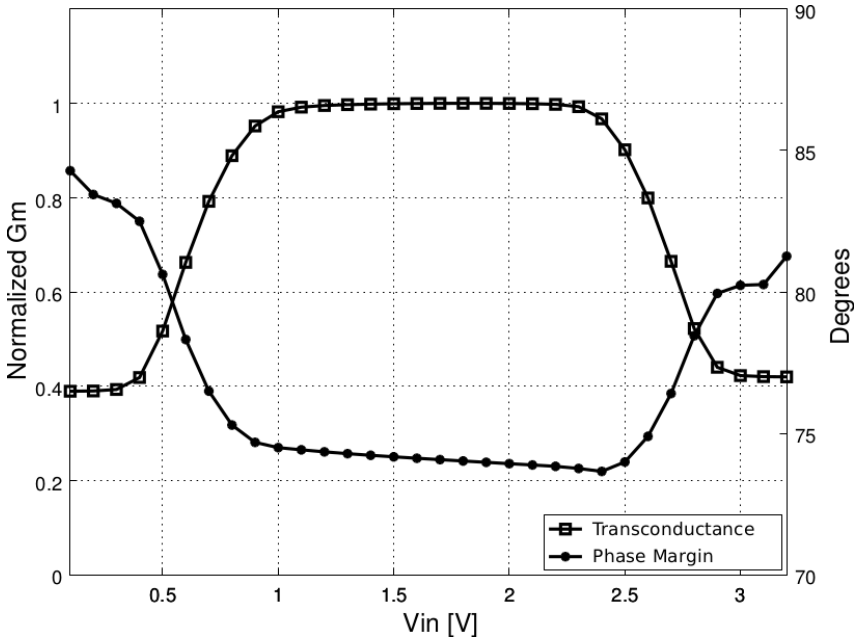
characteristics. The bias voltages (Vp1 and Vp2) are provided by two arrays of diode-connected PMOS and NMOS transistor.

4. SIMULATION RESULTS AND COMPARATIVE STUDY

The VFC proposed in this work is shown in Fig. 3, the VFC is designed with a single supply of 3.3V in low-cost CMOS 0.35µm technology with a power consumption of 802µW.

Since the OTA rail-to-rail is used in the design of VFC, knowing the behavior of its parameters is important to achieved a wide range of excursion. Fig. 9 shows the waveform of the transconductance and the phase margin as a function of range excursion. The transconductance presents a considerable variation in the mentioned domain and this variation influences on the stability of the circuit. Therefore, to improve the phase margin is critical to consider this parameter.

Figure 9. Transconductance and phase margin for the range of input voltages (Vin).



The Fig. 10 shows the behavior of the capacitor charging and discharging and the output voltage for an input of 1.6 V. The waveform of the capacitor voltage presents almost instantaneous changes when intercepts the levels imposed by the comparator due to the minimum channel length was used in M 11 and M 12 transistors. The output voltage oscillates at a frequency of 655.9 kHz. For other values of voltage V in similar results are obtained, the main difference is the frequency of oscillation which is described by (1).

The Fig. 11 shows the variation of resistance for two different materials (Rs=RPOLYH + RNWELL and Rs=RPOLYH). A resistor composed of a series connection of two materials (RPOLYH and RNWELL) was implemented. This resistor presents a variation of 0.003 %

(±62Ω) against a variation of 0.04 % (±871Ω) of RPOLYH material. Thus the percentage of variation is reduced by a factor of 13 for the resistance Rs shown in Fig. 3.

Figure 10. Simulation results of the capacitor voltage and the output voltage.

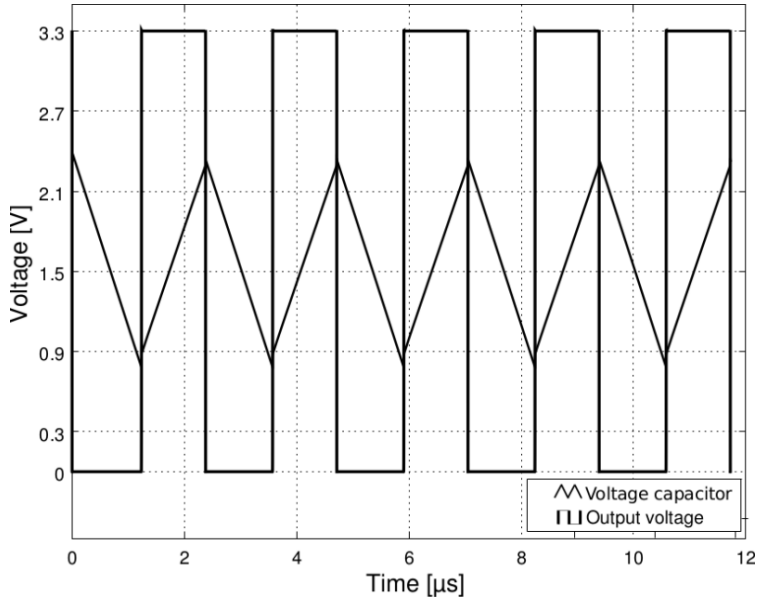
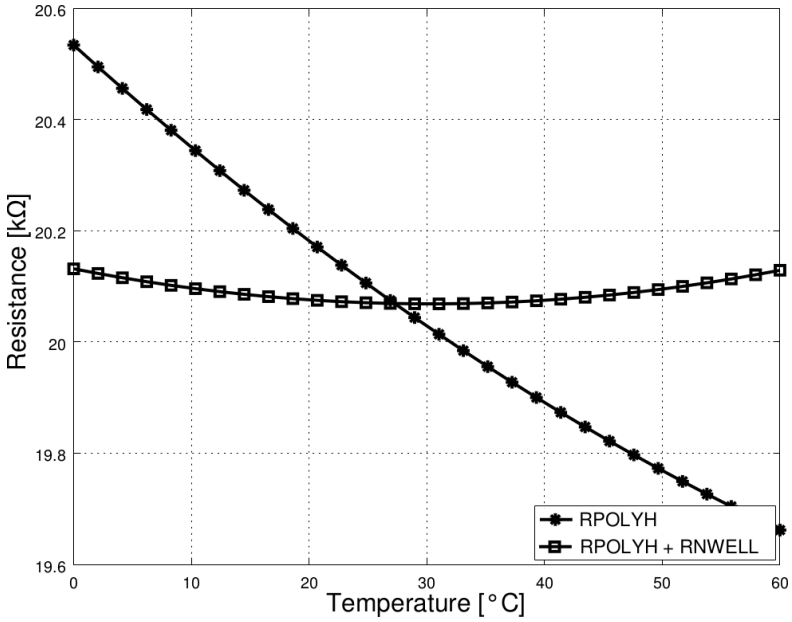


Figure 11. Variation of resistance as a function of temperature.



In order to check the performance of a VFC, precision errors for the output frequency are calculated. There are several equations that define the error for this type of signals, among the most used is the relative error as follows:

$$\%\boldsymbol{Er} = \frac{\boldsymbol{fo_{teo}} - \boldsymbol{fo_{sim}}}{\boldsymbol{fo_{teo}}} \quad (4)$$

Where $\boldsymbol{fo_{teo}}$ is the theoretical frequency value. In order to obtain $\boldsymbol{fo_{teo}}$ calculating the linear regression data is necessary and then to evaluate the input voltages on the calculated regression. $\boldsymbol{fo_{sim}}$ is the frequency obtained in the simulation. This makes it possible to find the relative error. Another error of equal importance is the linearity error. The two most common forms to calculate the linearity error are as follows: as 1 − R 2, where R 2 is the coefficient of determination of the linear regression and the other form most commonly used for the calculation of this error is shown below.

$$\%\boldsymbol{E_L} = \frac{\boldsymbol{fo_{teo}} - \boldsymbol{fo_{sim}}}{\boldsymbol{f_{max}}} \quad (5)$$

where $\boldsymbol{f_{max}}$ is the full range that can take the output frequency and $\boldsymbol{fo_{teo}}$ and $\boldsymbol{fo_{sim}}$ are obtained in the same manner as in the relative error.

Figure 12. Output frequency and linearity error.

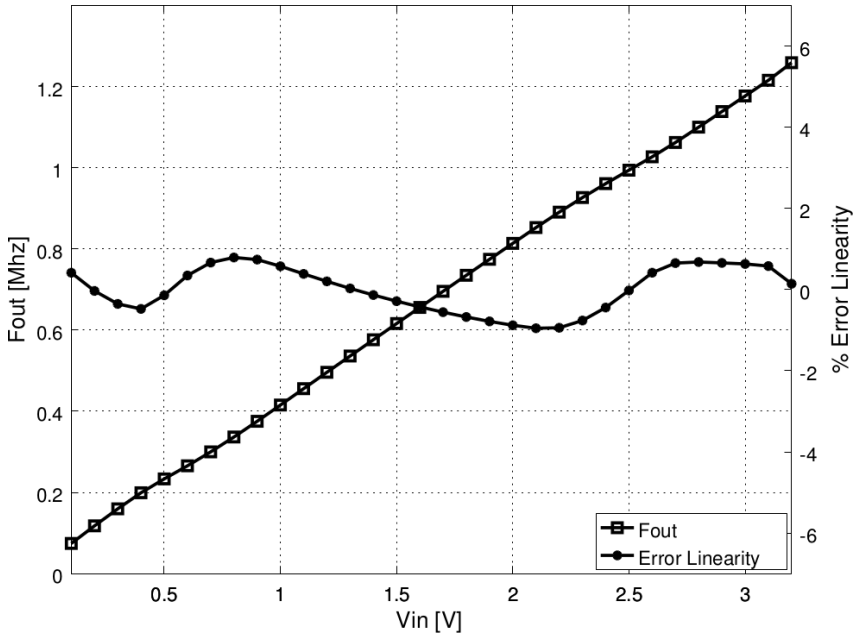


Fig. 12 shows the output frequency with the linearity error as a function of the input voltage, calculated as shown in (5). The maximum linearity error is 0.9 % and a mean error of 0.4 % for typical operating conditions is obtained. Also, in this operating condition the output

frequency has a mean relative error less than 1.2 % and the sensitive error is 3.4 %. The table IV shows the results of simulation in the worst cases presented in corners and table V shows the results of simulation of Monte Carlo analysis. Also in Table 3 VFC performance compared.

Table 4. Summary of VFC performances in corners.

Parameter	Min	Typ	Max
Fmin	43.9 kHz	74.39 kHz	97.8 KHz
Fmax	852.06 kHz	1.2 MHz	1.57 MHz
Frequency span	791 kHz	1.18 MHz	1.49 MHz
Sensitivity	279.3 kHz/V	381.04 kHz/V	527.9 kHz/V
Sensitivity Error	0.002 %	3.41 %	33.8 %
Relative Error Mean	1.04 %	1.2 %	3.2 %
Linearity Error Max	0.81 %	0.9 %	1.8 %
Linearity Error Mean [1]	0.32 %	0.4 %	0.69 %
Linearity Error [2]	0.016 %	0.03 %	0.085 %

Table 5. Summary of VFC performances in Monte Carlo.

Parameter	Mean	Sigma
Fmin	73.1 kHz	8.4 kHz
Fmax	1.2 MHz	0.1 MHz
Frequency span	1.1 MHz	0.1 Mhz
Sensitivity	382.6 kHz/V	36.3 KHz/V
Sensitivity Error	7.1 %	5.4 %
Relative Error Mean	1.2 %	0.07 %
Linearity Error Max	0.9 %	0.04 %
Linearity Error Mean [1]	0.4 %	0.02 %
Linearity Error [2]	0.03 %	0.003 %

Table 6. Comparison of VFC performances.

Parameter	Ref. [8], 2009	Ref. [9],2011	This Work
Technology	0.35 µm	0.18 µm	0.35 µm
Supply Voltage	3.0 V	1.8 V	3.3 V
Sensitivity	1 MHz/V	1.23 MHz/V	381.04 kHz/V
Input Voltage Range	1.0 - 2.0 V	0.1 - 1.6 V	0.1 V - 3.2 V
Fmin	1.2 MHz	0.122 MHz	0.074 MHz
Fmax	2.2 MHz	1.98 MHz	1.25 MHz
Relative Error	< 0.7 %	< 4.8 %	< 1.2%
Linearity Error [2]	–	0.017 %	0.03 %
Power Consumption	1.03 mW	0.423 mW	0.802 mW

[1]Equation 5 [2]1 − R2

5. CONCLUSION

A compact 3.3V 0.35µm CMOS voltage-to-frequency converter with a rail-to-rail input stage and a temperature-compensated technique was designed. Circuit such as a RS flip-flop, comparators, high-swing cascode current mirror, symmetrical OTA and rail-to-rail OTA make out of this VFC. It's output signal frequency range is 74.39 kHz to 1.2 MHz and it presents a low power consumption compared with other works keeping a good performance in the results.

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