Circuit and Architecture Techniques for Clock Generation in Systems-on-a-Chip

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A mi padre, a mi madre y a mi hermana.

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Resumen

Título: Técnicas para Arquitecturas y Circuitos de Generación de Reloj en Sistemas-en-Chip [*]

Autor: Juan Sebastián Moya Baquero [**]

Palabras Clave: Sistemas-en-Chip, Internet de las Cosas, Oscilador en Anillo Diferencial en Avance.

Descripción: Sistemas-en-Chip (SoC) son uno de los circuitos más comunes en el Internet de las cosas (IoT). Las fuentes de reloj aparecen como un circuito necesario en los SoC para la transferencia, procesamiento de datos o la transmisión vía radiofrecuencia [33]. Generalmente, se instancian varias fuentes de reloj en los SoC para cumplir con los protocolos de comunicación incorporados [43]. Con varias fuentes de reloj, el área ocupada, el costo de instanciación, de verificación e integración en un SoC aumentarán, impactando el precio y la accesibilidad [37]. Una opción para reducir el costo del SoC es disminuir el número de fuentes de reloj. Esto nos lleva a querer integrar, en un único chip, una fuente de reloj que satisfaga el mayor número de estándares de comunicación. Sin embargo, se deben contemplar varias consideraciones y características asociadas a estos estándares. La interferencia entre símbolos en las comunicaciones alámbricas y la fluctuación, el ruido de fase o el rango de frecuencia en las fuentes de reloj integradas son las preocupaciones más relevantes. Este trabajo presenta algunas contribuciones para aplicaciones alámbricas de alta velocidad en circuitos de reloj y recuperación de datos y dos análisis sobre la extensión del rango de frecuencia operativo y la evaluación y reducción del ruido de fase en osciladores de anillo diferenciales en avance (FFRO). Finalmente, proponemos utilizar la arquitectura FFRO como generador de pulsos en transmisores UWB no coherentes para abrir la puerta a una nueva área de investigación además de la generación de fuentes de reloj en SoC.

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Abstract

Title: Circuit and Architecture Techniques for Clock Generation in Systems-on-a-Chip [*]

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Keywords: Systems-on-a-Chip, Internet of Things, Feedforward Differential Ring Oscillators.

Description: Systems-on-a-Chip (SoC) are one of the most common circuits in the Internet of Things (IoT) network. Among the blocks composing SoC, clock sources appear as a mandatory circuit for data transfer, data processing, or radio frequency transmission [33]. Usually, several clock generation sources are instantiated in SoC to fulfill the different communication protocols incorporated in the system [43]. With a large number of clock sources, the area occupied will rise, and the cost to instantiate, verify, and integrate an SoC increases, which impacts price and accessibility by the user [37]. A possible option to reduce SoC's cost is to decrease the number of clock sources. This brings us to the possibility of integrating, in a single chip, a unique clock source that satisfies the largest number of communication standards. However, several considerations and characteristics associated with these standards must be contemplated. Intersymbol interference in wireline communication, and jitter, phase noise, or frequency range in on-chip clock sources are some of the most relevant concerns. This work presents some contributions to high-speed wireline applications for clock and data recovery circuits and two analyses regarding the extension of the operating frequency range and the assessment and reduction of phase noise in feedforward differential ring oscillators (FFRO). Finally, we propose a proof-of-a-concept to use the FFRO architecture as a pulse generator in Non-Coherent UWB transmitters to open the door for a new research area and impact other research fields besides clock source generation in SoC.

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Introduction

0.1. Thesis overview

This thesis presents some contributions associated with the generation of clock sources in Systems-on-a-Chip. Clock sources are presented in different voltage and frequency domains and applications associated with the performance of SoC. For instance, clock sources are present during the transmission and reception of data during wireline communications. Another application of clock sources in SoC is the clock that is used in the microcontroller to synchronize all the processes occurring during data processing. Other applications that use clock sources are frequency synthesizers to upconvert or downconvert the wireless signals that are transmitted or received, respectively.

Chapter 2 proposes a fully integrated resistance termination to enhance the reception of information during wireline data transference, for applications such as USB. During the reception of data in wireline applications, the signal clock associated with the transmitter is embedded in the incoming data. Embedding the transmitter clock in the data allows the receiver to extract the information related to the clock and synchronize the clock instantiated in the receiver with the transmitter clock to avoid data losses during the reception, this process is named clock and data recovery [54]. Still, during the transmission, the amplitude of the transmitted signal deteriorates with different undesired effects associated with the transmission channel. Thus, we present a circuit that mitigates these

undesired effects and enhances the reception of the information for later data processing while considering Electro-Static Discharges (ESD) and current density.

Chapter 3 presents a technique applied to ring oscillators known as feed-forward that enhances up to 4 times the maximum operating frequency of a Complementary Metal-Oxide-Semiconductor (CMOS) technology node. A piece-wise model is developed to estimate the oscillation frequency and the oscillation mode based on both the feedforward and cross-coupled strengths, which can be used as control signals. Post-layout simulation results allow the possibility to cover a frequency range from 100kHz to 1.5GHz, which is suitable for several circuits, architectures, and applications used in SoC. The clock architecture was designed using a unique cell, which is a tri-state inverter, that is implemented in standard cell format to allow scaling of this clock source to more recent CMOS technology nodes. Moreover, the standard-cell format allows the possibility to reduce instantiation and verification costs during the design flow.

Chapter 4 complements the work developed in Chapter 3 since a simple model based on multi-loop control system theory to estimate the phase noise of the architecture is implemented. This model is constructed with a reduced number of steps to decrease the time for phase noise estimation while considering both Flicker and Thermal noises, which are the most representative noise sources in phase noise. Compared with the worst corners' post-layout simulation results, the errors obtained are acceptable, indicating that the model is functional. An analysis based on the impulse sensitivity function allows us to determine that small values of the feedforward strength reduce the

phase noise of the clock architecture.

In Chapter 5, a proof of a concept for the feedforward ring oscillator as a pulse generator in non-coherent architectures for ultra-wideband (UWB) applications is presented. This chapter looks to expand the number of circuits, architectures, or applications where the feedforward ring oscillator could be implemented. Initial simulation results are promising for the feedforward ring oscillator due to its wideband frequency range.

Finally, Chapter 6 presents the final conclusions of this thesis, the main contributions, the published works in the different conferences and journals, and the future work that can extend the results obtained so far.

Still, before presenting the main contributions of this thesis, follow a description of the main context that encompasses this work. Furthermore, to give more meaning and understanding to the work developed in this thesis, I describe the path paved by the Onchip Microelectronics Research Group, its evolution, and where my Ph.D. journey starts to make some contributions to clock generation in SoCs.

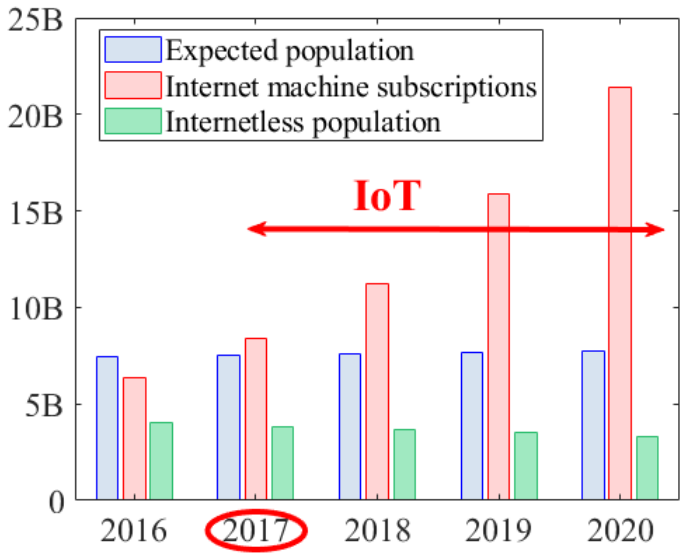
0.2. Internet of Things Era and Systems-on-a-Chip

The Internet of Things or IoT defines a colossal network of sensors and software constantly processing, transmitting, and interchanging information via the Internet, and it is supported by a massive number of data processing servers named the Cloud. The network's elements make

different decisions depending on the processed information to fulfill human needs. In 2017, the number of consumer electronic devices connected to the Internet surpassed the expected world population by approximately 1 billion, [67, 71]. Data trends show that the gap between these two categories has increased even more over the years, as depicted in Figure 1. Meanwhile, the internetless population will decrease slowly, reducing the possibilities of fairness and universal accessibility in the short and middle terms.

Figura 1

During 2017, the number of machines subscribed to the Internet surpassed the expected worldwide population, initiating the IoT era.



As the number of machines extracting information increases, new applications are being developed to fulfill current human needs in different scenarios. For instance, houses incorporate different IoT applications such as sensors capturing information associated with humidity or temperature, proximity devices that work as keys to open or close doors, drawers, or cars, music volume, or light intensity are some of the variables controlled in a house environment according

to household preferences, [48]. Applications in movement or in bigger spaces are also possible as vital sign tracking, landslide monitoring, fire detection, or snow level sensors, [1, 42, 51].

Systems-on-a-Chip (SoC) are the most common devices that compose the IoT network in current applications. SoC are electronic systems that integrate into a single substrate all or the majority of the modules and functions that a device should have to respond to the necessities of the different applications required in the network.

To implement SoC, several requirements should be considered by the engineers. The first requirement consists of developing and designing a data processing center to do the corresponding operations for subsequent decision-making steps. This data processing center is considered the heart of SoC and it is commonly known as a microcontroller. Like the human body, the microcontroller needs arteries, named buses, to exchange information (digital domain) with the different on-chip and off-chip submodules that compose the system. A second requirement for SoC appears when an interaction with the analog world takes place, especially when some information needs to be extracted from the different phenomena that are constantly changing around us. Phenomena such as temperature, humidity, or heat must be monitored in real-time to have a more accurate perception of our surroundings. The requirements above would tend to suggest that SoC must operate 24/7 to fulfill human needs, which raises the question about power consumption and leads us to a third requirement: optimization of the energy in SoC.

For instance, pretend that we would like to monitor several variables in a specific room. To have accurate control, 20 SoC are installed in the physical area and each one of the sensors consumes around 5mW per second. Then at least, all the SoC will consume 100mW per second, and

adding the operation of several consumer electronics, such as personal computers (PC), heating, or TV monitors, the sensed space will not be environmentally friendly. This high level of energy consumption is in strong opposition to the worldwide trend to reduce and preserve energy resources, thus optimization of the power consumption in SoC is imperative.

The microelectronics research group Onchip, located in the Universidad Industrial de Santander, Bucaramanga, Colombia, looks to strengthen the community towards the industry. Onchip explores and incorporates the development of open-source SoC by adopting the requirements mentioned above. The expertise of Onchip is supported by the exploration, research, and development of different VLSI circuits and systems for Computer Architecture, High-Speed circuits, Electronic Design Automation (EDA) algorithms, Machine Learning, and Security Hardware. A brief history of Onchip's contribution to electronics development in the Latin America region follows.

I would like to mention that the following sections associated with Chapter describe the more relevant events that occurred at the Onchip group during the period 2016 - 2022. I describe the path paved by the Onchip research group and its evolution to clarify how my journey started in this group, the different tasks and works that I developed, and how my Ph.D. fits in.

0.3. Turpial: The first worldwide RISC-V silicon-proven microcontroller designed in Colombia

In 1982, the University of California, Berkeley, in the hope of implementing VLSI computers in single chips, developed an architecture set of instructions for academic purposes named Reduced Instruction Set Computer (RISC). It is a well-defined and small set of instructions to optimize the architecture mapping, reduce the layout area, and decrease the operations time [64]. In

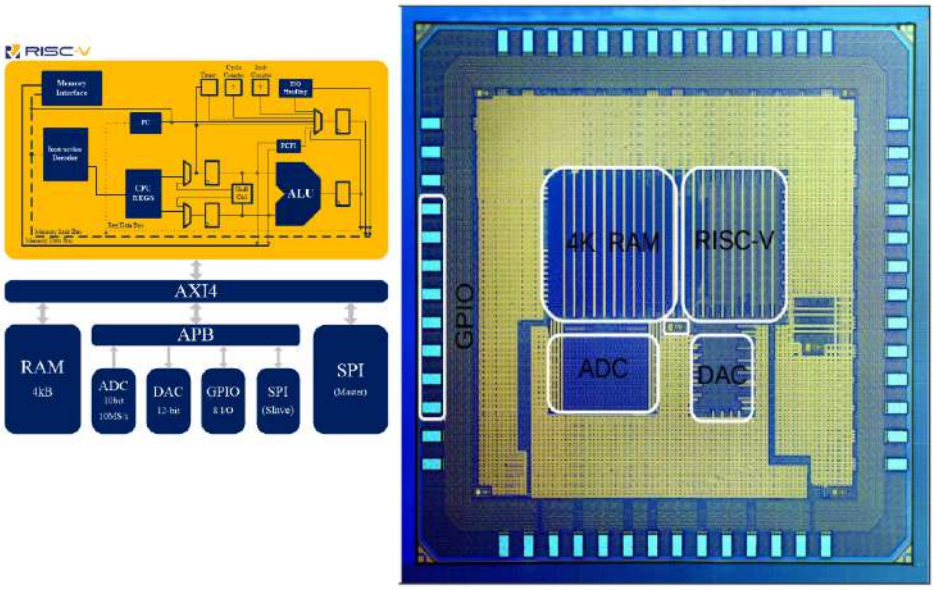
2010 when Berkeley started developing the RISC-V version, both industry, and academia became more interested since it was a free and open-source set of instructions compatible with different microcontroller architectures for small, fast, and low-power applications. These characteristics fit in the development and design of SoC applications, which drew attention and were adopted by the Onchip group.

It is important to mention that before 2015 no RISC-V microcontroller with a performance to substitute commercial microcontrollers was silicon-proven. In 2016, Onchip designed, tested, and presented worldwide the first RISC-V microcontroller. The microcontroller was named Turpial, referring to an endemic bird species of the Santander region in Colombia, and designed with a 130nm CMOS technology [15]. It is a 32-bit microcontroller that occupies a 2.1mm x 2.1mm layout area, and its operation is equivalent to the ARM M0 architecture. Figure 2 presents on the left side the block diagram of Turpial and on the right side the die with the placement of the different circuits.

Besides the RISC-V microcontroller, the other blocks included are:

- AXI4-Lite and APB buses.
- A Serial Peripheral Interface (SPI).
- 8 I/O GPIO modules for the digital interface.
- A SAR 10-bit analog-to-digital converter (ADC).
- A 12-bit digital-to-analog converter (DAC).

Figura 2
Turpial block diagram and die.



As observed in Figure 2, the 32-bit RISC-V architecture uses two buses, a master (AXI4-Lite) and a slave (APB) to communicate with the peripherals (SPI, GPIO, ADC, and DAC). Additionally, a 4kB-external RAM is connected with Turpial for correct operation. Table 1 presents a summary of Turpial performance and main characteristics.

To evidence the scope of Turpial, we used this microcontroller in several applications. Principally, we included Turpial in a development board that took the shape of puzzle pieces for primary and secondary educational purposes, as depicted in Figure 3.

It was a four-part educational agreement between an academic program that engages children in Bogotá named STEM, the Universidad Industrial de Santander (UIS), the Universidad de Los Andes (Bogotá, Colombia), and the Instituto Colombiano de Bienestar Familiar (ICBF). Besides Turpial, the puzzle piece included USB connectors, 2.5V and 1.2V regulators, an SPI interface,

Tabla 1
Turpial Performance

ISA	RV32IM
Process	TSMC 130nm GP
Die Area	2.1mm x 2.1mm
μC core area	0.12 mm^2
Max. Frequency	200MHz
Core Voltage	1.2V
I/O Voltage	2.5V
Core Dynamic Power @100MHz	167 μW/MHz
1.2V Current @2.5MHz	1.8mA

level shifters, and clock generators. The connection between the different puzzle pieces was made through magnets that ensure power continuity and a correct fitting. Depending on the connected side of the puzzle, different applications took place.

I joined Onchip in 2017, thus I could not be part of the design and testing of Turpial. However, in 2019, I led a pilot test for the massive production of Turpial puzzle pieces in the Jorge Ramón Laboratory (the local equipment and testing laboratory at UIS). This test demonstrated the scope and potential of our local laboratory for development board massive production. In December 2020, I presented at the Congreso Multidisciplinario Sistema CEUNI, a summary of the results that we achieved during this pilot test.

After the echo and success of Turpial, it is possible to mention that the first requirement to consider in SoC design was achieved. Furthermore, Onchip attracted the attention of several institutions such as CERN, Cambridge, and SiFive. The latter contacted Onchip in 2017 to start a collaboration to develop a more advanced SoC. In this collaborative work, the core was designed

Figura 3
Puzzle piece developed by Onchip for education purposes using Turpial.

by SiFive and an analog sensing interface was designed by the Onchip members. This collaboration allowed the Onchip group to explore the second requirement for SoC design: an analog interface to sense phenomena in real-time.

0.4. Tucan: A collaborative IC design SoC with SiFive

The collaboration between Onchip and SiFive took place between 2017 and 2018 and was a highly productive one. During the collaboration, the Onchip group was in charge of designing analog circuits for sensing. In total, we developed 10 analog intellectual properties (IPs) intended for low-energy and low-duty cycle sensor nodes. The IPs were designed for the microcontroller Tucan, another name referring to an endemic bird species of the Santander region. The microcontroller occupies a 2.6mm x 3.3mm layout area and the technology used was 180nm with 1.8V and 3.3V core and I/O nominal voltages. The IPs designed were:

- Low Start-Up Energy RC-Based Oscillator (RCO).

- Low-Frequency Crystal Oscillator (LFXO) for real-time counters.
- Power-On Reset (POR) for initial reset on both Always-ON and Core domains.
- Brown-Out Detector (BOD) as a voltage monitor for sleep mode transitions.
- 3.3V to 1.8V linear low-dropout (LDO) regulator for Core domain supply.
- 3.3V bandgap (BGAP) reference for the LDO regulator.
- 1.8V bandgap (BGAP) reference.
- Current references for biasing control.
- A SAR 10-bit analog-to-digital converter (ADC).
- A 12-bit digital-to-analog converter (DAC).

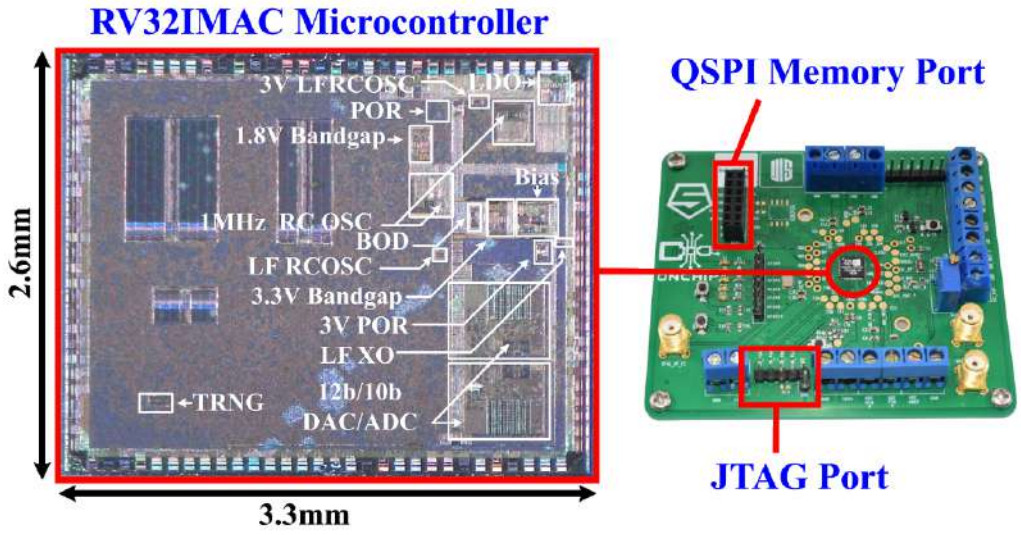
Figure 4 presents on the left side Tucan die with the placement of the blocks mentioned above. On the right side of the figure, it is possible to observe the test board of Tucan. The test board includes different ports, such as QSPI, JTAG, or SMA, to validate the performance of the SoC.

Once the Onchip group executed the testing phase in Tucan and confirmed that the chip functioned correctly, we developed some applications to determine the scope of the SoC. During the 10th Latin American Symposium of Circuit and Systems (LASCAS) in 2019, organized in Armenia, Colombia, by IEEE, the Onchip group presented several demos using Tucan. The demos presented were: A μ neural network, a temperature sensor based on the RC oscillator behavior, a

signal generator using the 12-bit Tucan's DAC, an air quality sensor, and a distance meter application.

Figura 4

Tucan die and test board.



The outcomes regarding Tucan's performance during the testing phase and the demonstrations yielded satisfactory results. With this in mind, it is possible to say that the second requirement to consider during the design phase of SoC was accomplished. Ten analog IPs were designed and tested successfully to include them in the SoC analog interface.

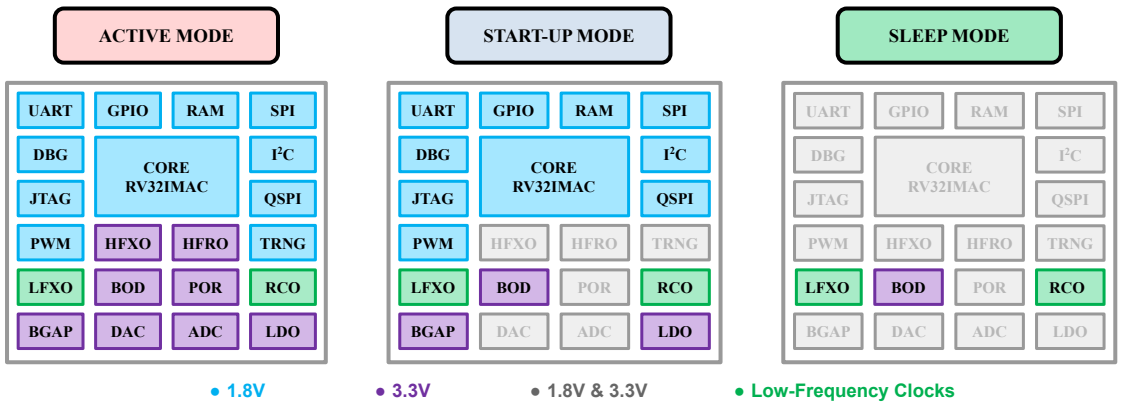
Furthermore, Tucan let us explore an essential research line associated with optimizing energy consumption during the different operating states of the microcontroller. As mentioned, Tucan was designed for low-energy and low-duty cycle sensor nodes. Thus, most of the time, the microcontroller was in a sleepy or lazy state to save energy until it was activated for sensing. Three primary states were identified during the operation of Tucan: 1) Sleeping mode, 2) Starting-up mode, and 3) Active mode.

It is desirable that Tucan stays in the sleeping mode for a large period of time consuming the minimum amount of energy ($\leq 1\mu W$). Therefore, only the essential blocks within Tucan must remain working during this mode. Before sensing, Tucan must start up, turning on the secondary blocks to make sure that the circuits that are going to do the sensing, for instance, temperature, will operate correctly. The time while Tucan operates in the starting-up mode must be small ($\approx$ 1ms) and the power consumption should still remain low ($\approx 10\mu W$). Finally, during the active mode, all the circuits to sense turn-on ($\approx 10mW$) and transmit the information requested. The time associated with this mode should be small ($\approx$ 10ms). The latter results were elaborated in greater detail at the 2020 IEEE Custom Integrated Circuits Conference (CICC)) [14]. Figure 5 depicts the three modes mentioned with the corresponding operating circuits.

During the design and tape-out of Tucan, I was in charge of the BOD and LDO layouts. Through the testing phase, I helped with the characterization of Tucan analog circuits, especially with the BOD block.

Figura 5

Block diagram of the circuits associated with the operation of the three mentioned modes.



In recent years, one of the major concerns in consumer electronics is the extension of battery life, especially with IoT devices. Thus, as mentioned above it is desirable that the SoC could operate in different operating modes to save energy consumption. Still, to optimize even more energy in SoC, it is insufficient to disable the circuits that are not needed during a specific mode, but while operating the circuits should work correctly with the minimum energy possible. Confident in optimizing the power consumption of Tucan's analog blocks, the Onchip group focused its efforts on designing its third SoC: Guerinii.

0.5. Guerinii: A microcontroller for minimum energy consumption to extend the battery life of SoC

Once Tucan was submitted for tape-out (fabrication) at the beginning of 2018, the 10 analog IPs were redesigned to optimize their different characteristics. For instance, the power consumption per analog IP was decreased even more, we lowered the voltage operation of certain IPs, and the layout area of each IP was reduced. These improvements are in complete harmony with the third requirement mentioned at the beginning of this section: optimization of the energy consumption in SoC.

We used a TSMC 180nm Logic technology node with 3.3V and 1.8V for I/O and core, respectively. It is worth mentioning that the technology node used in botch Tucan and Guerinii is the same, avoiding the rescaling of the IPs, which helped reduce the times associated with the redesign.

With the goal to design a second microcontroller 100% made in Colombia, and with the experience acquired during the collaboration with SiFive, the Onchip group developed a second

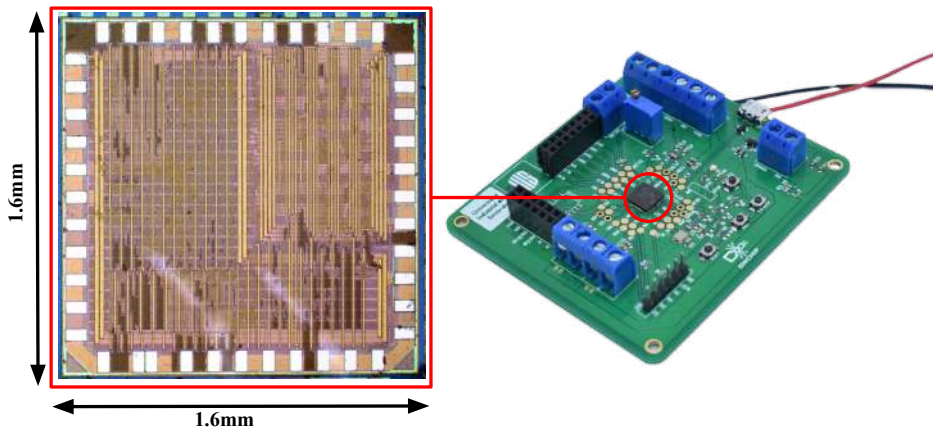
RV32IM microcontroller version, named Olinguito. Besides Olinguito, new circuit blocks were designed to explore new features associated with a nano-Watt always-on domain, debugging, and encryption:

- Multi-Voltage Level-shifters.
- Modular current and nano-Ampere current references
- NVRAM.
- Always-ON (AoN) circuitry for nW consumption.
- JTAG-based debugger platform for behavioral and performance analyses in Olinguito.
- True random number generator (TRNG) for encryption.
- Advanced Encryption Standard (AES) 128-b module.
- Circuits for USB 1.1/2.0 compliance.
- Direct memory access (DMA) module.

With the optimization of the blocks and the instantiation of the Olinguito microcontroller, the Guerinii SoC occupied a 1.6mm x 1.6mm layout area. Figure 6 presents the Guerinii die and its test board.

Similar to Tucan, we also developed and presented some demos using Guerinii in the 2019 10th Latin American Symposium of Circuit and Systems (LASCAS). The presentation of these

Figura 6
Guerinii die and test board.



demos created a positive impression on the conference assistants and demonstrated the know-how and expertise of the Onchip group in SoC design.

In this third microcontroller, I was in charge of optimizing the layout of a few blocks and I was part of the team that characterized Guerinii in the Jorge Ramón Laboratory.

In 2019, there were three key issues that led me to achieve a better understanding of the possible contributions that I could develop during my Ph.D. First of all, I was in charge of the clock tree circuit for the upcoming chips, which let me define and limit my research area. Secondly, during the optimization of the Guerinii IP blocks, one of the goals of the RC oscillator required extending the oscillation range from 33kHz-1MHz to 10kHz-1MHz. The latter frequency range looked to cover more applications, reduce the number of clock source generators in Guerinii, and aim to reduce power consumption and instantiation times. With this in mind, an important question arises regarding the number of clock sources in SoC:

Why not use a unique clock source whose frequency range covers all the applications inside an

SoC?

Finally, the third issue that strengthened my Ph.D. journey occurred in April 2019 during the IEEE Customs Integrated Circuits Conference (CICC) organized in Austin, Texas (US). The Onchip Group presented the work associated with the 10kHz-1MHz RC oscillator architecture with very low start-up energy [23]. During the same conference, Song et al. [68] presented a 2-to-20GHz multi-phase PLL for high-speed wireline applications. The authors covered the extensive tuning range with a PLL composed of two cross-coupled ROs intertwined. Further investigations by Park et al. [53] resulted in the emergence of a technique named feedforward that was implemented in ring oscillators in 2009, which extended the oscillator frequency range by including additional simple and compact structures.

With those three issues in mind, my Ph.D. aimed to explore and implement circuit and architecture techniques to contribute to developing SoC research areas where clock sources are needed, such as clock generation or data transfer front-ends.

We propose the following goals to achieve the above-mentioned:

- To explore and propose a unique clock generator instance covering a wide frequency range for sensor-based Systems-on-Chip (SoC) applications.

The objectives defined for this thesis are:

- To design a voltage-controlled oscillator that can extend its maximum oscillation frequency to cover the kHz-GHz band to fulfill several SoC applications. The basis of the circuit is the

ring oscillator, which covers the widest frequency band among the different oscillators in the literature.

- To model the estimation of the extended oscillation frequency range and the phase noise oscillator.
- To develop additional building blocks to contribute to the development of clock generation in SoC.

The next Onchip tape-out took place at the end of 2019; it was named Amazilia and incorporated several graduate and undergraduate projects. Among the different circuits in Amazilia, I instantiated a clock generator to alleviate the number of clock sources in SoC and an analog front-end for data reception in wireline communication.

In Amazilia, I had several tasks and goals to accomplish that contributed to the evolution of my Ph.D. journey and work. I integrated an analog front-end for data reception in wireline communication applications to reduce the impact of undesired effects, such as InterSymbol Interference (ISI) or Electro-Static Discharges (ESD). I was also in charge of integrating a clock source with a wide frequency range, and I designed and integrated the buffer circuits to test the clock architecture correctly. Follows a brief list of my Ph.D. contributions:

- A fully integrated resistance termination for ESD and current density compliance.
- A piece-wise approach for frequency estimation in feedforward differential ring oscillators.

- A phase noise model based on multi-loop control system theory for feedforward differential ring oscillators.
- Proof of concept of the feedforward differential ring oscillator as a pulse generator in UWB transmitters.

However, it is worth mentioning that the contributions of my Ph.D. are described in detail in Chapters 2, 3, 4, and 5. In Chapter 6, I compile and describe in detail the contributions mentioned above. To appreciate my Ph.D. work and achieve a better understanding of my contributions, I describe straightaway the landmarks of Amazilia that set the main paths I paved to contribute to the development of clock sources in SoC.

As mentioned before, one of the main research lines of the Onchip group in SoC was optimizing energy consumption during the different operation modes. Among the different circuit blocks composing an SoC, we detected that there are several topologies of clock sources designed to cover different frequency ranges and to operate in distinct energy consumption modes. A summary of the different clock sources designed for the three microcontrollers described above is presented in Table 2.

With the results presented in Table 2, it is possible to observe that the range that needs to be covered with the different topologies is 32.768kHz - 72MHz. Thus, it would be desirable to design a clock source that covers at least the kHz-MHz range.

Apart from that and looking forward to contributing to other research areas we designed Amazilia, the next chip focused on developing a high-speed wireline interface with USB com-

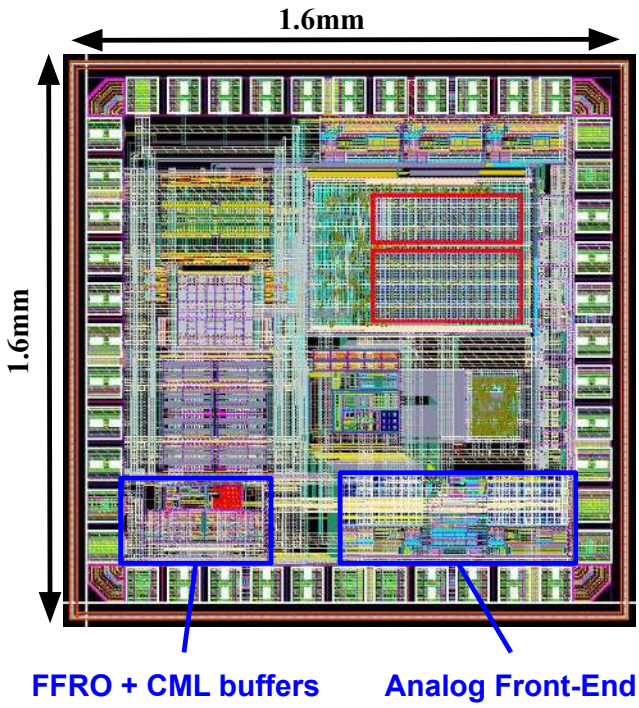
Tabla 2
Clock Source summary

Clock Source	Microcontroller	Frequency Range	Operation Mode
LF XTAL	Turpial	32.768kHz	Active
3V RCO	Tucan	32.768 - 1024kHz	Sleep
1.8V RCO	Tucan	32.768 - 1024kHz	Sleep
LF XTAL	Tucan	32.768kHz	Sleep
HF XTAL	Tucan	30MHz	Active
HF ROSC	Tucan	1.25 - 72MHz	Active
LF XTAL	Guerinii	32.768kHz	Sleep
1.8V RCO	Guerinii	32.768 - 1024kHz	Sleep
HF XTAL	Guerinii	16MHz	Active
HF ROSC	Guerinii	1.25 - 72MHz	Active

pliance. As it is known, the latest USB standards, USB 3.2 (2017) and USB 4.0 (2019) achieve 20Gbps and 40Gbps data rates, respectively. Limited to the same technology node (180nm) used in Tucan and Guerinii, it was not feasible to target either USB 3.2 or USB 4.0. Thus, the Onchip group decided to design a high-speed interface associated with the USB 3.0 (5Gbps) standard to contribute to the research line associated with data transference in SoC. Figure 7 presents the final layout of Amazilia.

Amazilia is comprised of several undergraduate and graduate integrated projects. Among them, it is possible to find two main systems: a clock and data recovery circuit (CDR) and a clock source that overcomes the technology node limit to extend its maximum oscillation frequency. The CDR is part of a wireline interface for data reception in SoC. It is in charge of synchronizing the local clock with the clock embedded in the incoming data to recover the information correctly. Still, before the synchronization occurs, the received information passes through the communication

Figura 7
Amazilia final layout.



channel and an analog front-end that is matched at 50 Ω to maximize the transmitted energy.

As new communication applications demand larger data rates, additional undesired effects appear, such as InterSymbol Interference (ISI) in the communication channel. The latter affects the shape of the vertical transitions of the incoming data, increasing the possibility to generate errors while recovering the information. Another consequence of incrementing the operating frequency is energy reflection since the wavelength associated with the signal becomes comparable to the size of the integrated connections and circuits. Thus, new structures for impedance matching between the transmitter and the receiver should be developed to ensure correct data transference in modern SoC.

An undergraduate project developed by the Onchip member, Luisa Dovale, looked to overcome some of the issues that could occur during the reception of the information in SoC. Professor Elkim Roa, as the co-director, and I, as the director, joined efforts with Luisa to design an analog front-end for the incoming data. Chapter 2 of this thesis presents the design of an impedance matching network considering high-current density and ESD events for correct data reception in SoC.

Once the reception of the data is assured by the analog-front end, it is possible to recover the data and the clock from the incoming signal with the CDR. The latter uses a quadrature technique to alleviate the sampling rate by utilizing four lanes in parallel, reducing the sampling clock from 5Gbps to 1.25Gbps. Once the CDR architecture and the clock sampling rate were defined, it was necessary to design a clock source that operates at 1.25GHz. This clock source increases the predefined kHz-MHz to the kHz-GHz frequency range. Still, the maximum operating frequency that a ring oscillator architecture could reach in a 180nm CMOS technology was approximately 650MHz, which was insufficient for the USB 3.0 application. It is worth mentioning that LC oscillators could reach the 1.25GHz frequency, still, after some tests, we concluded that it was not possible to integrate inductors with an acceptable quality factor in the actual technology (Logic flavor). In 2019, I joined efforts with Julian Arturo Arenas, an Onchip Master student member, to study the feedforward technique mentioned in the section 0.5. Chapters 3 and 4 present the results and contributions of our research associated with the implementation of the feedforward technique in the ring oscillator (FFRO).

In Amazilia, I had several tasks to accomplish, since I had to test the ideas and projects

where I was involved during my Ph.D. I integrated and validated the complete analog front-end, composed of two resistor terminations, two ESD protections, and a differential Continuous Time Linear Equalizer (CTLE). Regarding the clock source architecture, I was in charge of discussing the FFRO design with Julian, I collaborated with the layout implementation, and I designed the common mode logic (CML) buffers for testing and overcoming the 10pF output capacitance associated with the pins. In Figure 7 it is possible to identify the location of the FFRO, the CML buffers, and the analog front-end.

Finally, Chapter 5 proposes a Non-Coherent pulse generator circuit for UWB applications based on the FFRO circuit developed in Chapters 3 and 4 for UWB regulation compliance. Chapter 6 concludes this book and states future work.

1. Goals

1.1. Main Goal

- To explore and propose a unique clock generator instance covering a wide frequency range for sensor-based Systems-on-Chip (SoC) applications.

1.2. Specific Goals

- To design a voltage-controlled oscillator that can extend its maximum oscillation frequency to cover the kHz-GHz band to fulfill several SoC applications. The basis of the circuit is the ring oscillator, which covers the widest frequency band among the different oscillators in the literature.
- To model the estimation of the extended oscillation frequency range and the phase noise oscillator.
- To develop additional building blocks to contribute to the development of clock generation in SoC.

2. A Compact On-the-Fly-Enabled Termination with High-Current Density and ESD Compliance

In Chapter , we presented the different domains and applications where clock sources are used in SoC. Among the applications mentioned, high-speed wireline applications, and especially analog front-end circuits for clock and data recovery appear as an area of interest. It is well known that as integrated circuit scaling advances, transmission data rates increase, and data becomes more susceptible to different undesired effects, such as signal integrity. Thus, several effects and new considerations must be taken into account by the designers to increase the circuit's robustness.

InterSymbol Interference (ISI) may occur in wireline communication systems by termination mismatch at either end of a long channel. Termination resistors, characteristic channel impedance, and connectors may get altered by temperature and supply voltage variations during operation. Another undesirable effect that could affect the performance of a receiver analog front-end is the ElectroStatic Discharge (ESD) event. The latter could momentarily increase the current density in metal connections, impacting negatively the physical structure, and consequently in their performance.

In this chapter, a resistance termination is presented for on-the-fly termination calibration to mitigate ISI during operation. Additionally, we developed a new termination architecture that considers ESD effects and current density. Simulation results of an implemented calibration scheme within a front-end operating at 3.2-Gb/s ensure open data eyes during on-the-fly termination

calibration.

2.1. Fully-integrated resistance termination for on-the-fly calibration

In this section, we developed a resistance termination that considers ISI effects in an analog communication front-end. We introduce a resistance termination calibration scheme that enables fine and coarse steps and considers high-current density effects during ESD events. Moreover, the termination includes a block to compensate for Process-Voltage-Temperature (PVT) variations. A comparison with a conventional scheme illustrates how coarse calibration generates undesired reflected waves, handicapping signal integrity.

2.2. Introduction

The ever-increasing data transmission rate of wireline communication systems generates many challenges for signal integrity. Communication systems must now contend with transistor speed, parasitic elements, and limited channel bandwidth, [31]. This latter limitation causes data transmitted symbols at rates over several Gigabits per second (Gb/s) to spread their energy out over a Unit Interval (UI) of time. This spreading energy might induce data corruption, known as InterSymbol Interference (ISI), due to the mixing of adjacent symbols' information.

Different methods have been proposed to mitigate ISI effects in data transmission, including preemphasis and deemphasis in the transmitter, equalization in the receiver, or both. These methods face the challenge of unreliability due to process and temperature variations, for instance. Another common practice to minimize ISI effects is implementing an impedance-matching network in the system Input or Output (I/O) pads. A T-coil structure compensates for channel capacitive parasitic, [57], whereas a variable differential resistor termination is set to the channel impedance to avoid

signal reflections and maximize power transfer, [74]. However, resistor terminations and channel impedance values might change not only due to process variations but also during data transmission in regard to the supply voltage and temperature variations.

A typical scenario where signal integrity could be severely affected occurs when temperature varies, forcing a mismatch between channel resistance and termination resistors during data transmission. An on-the-fly resistor adjustment could be implemented to overcome this issue, returning to the matched resistor state. However, transitions of the termination resistor value may generate undesired glitches that interrupt data transmission, making a careful selection of the calibration step necessary to avoid possible data loss [32].

Although much progress has been made over the years in high-speed I/O, there is no comprehensive characterization of their termination design. In contrast to the widespread notion that a programmable termination may not present any challenges, high-current density considerations in conjunction with ElectroStatic Discharge (ESD) compliance demand considerable attention during the termination design. Traditional wisdom indicates that implementing a variable resistor should not present any challenge. However, considering that the termination recognizes ESD events as possible and that the adjusting resistor values might be as low as units of Ohms, several challenges are involved. High voltage and high current values generated by ESD events demand wide resistors with values larger than 100Ω. Transistors operated as switches to adjust the resistive network also might not tolerate residual voltage swings when an ESD event occurs. Most of the resistor termination documentation is in patents, reducing the information available for design considerations such as ESD and high-current density compliance. Reported works such as [30, 63, 70] from well-

known consumer electronics companies do not clarify compliance considerations. These works do not study the effect of the calibration step on signal integrity, which might result in on-the-fly data loss or robust specifications for equalization steps. Connector variations due to temperature and supply voltage alterations are also not studied.

This chapter presents a fine step differential resistor termination covering the 130Ω - 70Ω range for wireline communication systems. The fine step avoids data losses whereas offering a small footprint despite ESD and high-current density compliance. This chapter is an extension of a previous work presented in [13] including additional highlighted material, featuring: 1) integration of the resistor termination with part of the back-end circuit of a high-speed receiver; 2) proof of concept by verification of the proposed termination with a simplified model of a wireline link including channel losses and effects of channel discontinuities; 3) analysis of the impact of coarse and fine calibration steps on transmitted data signal during the matching process; 4) comparison with a prior work topology within the proposed link set up to verify how the lack of calibration resolution deteriorates signal integrity.

2.3. Resistive Termination in Long Channel Wireline Interfaces

Transmitted information should reach the receiver without any data losses. However, in high-speed wireline systems, undesired effects such as attenuation, noise, crosstalk, or impedance mismatch may cause signal integrity issues that result in non-recoverable information. This section presents the qualitative effects of having a resistor mismatch between the different elements integrating the communication system.

2.3.1. Wireline Simplified Interface Model

Figura 8

A high-speed link for wireline communication with decoupling capacitors (C_D) instantiated in the receiver input pads. An adaptive resistor termination in the receiver provides the required 100Ω differential mode matching.

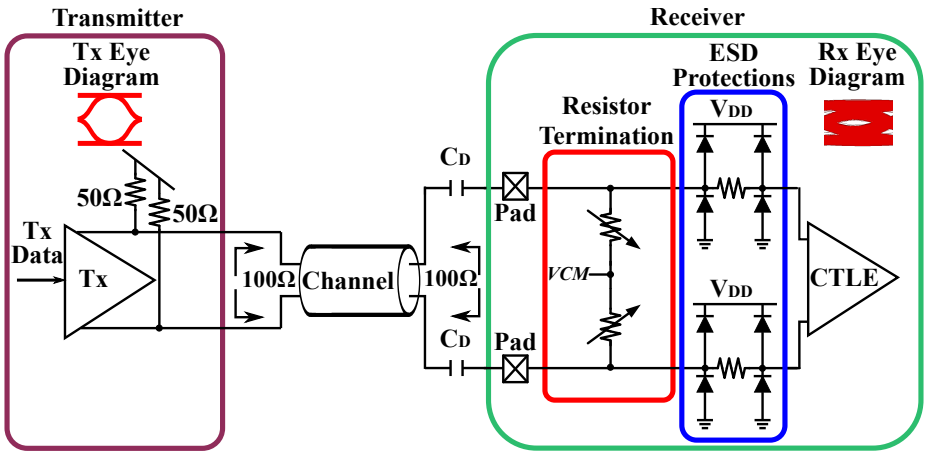
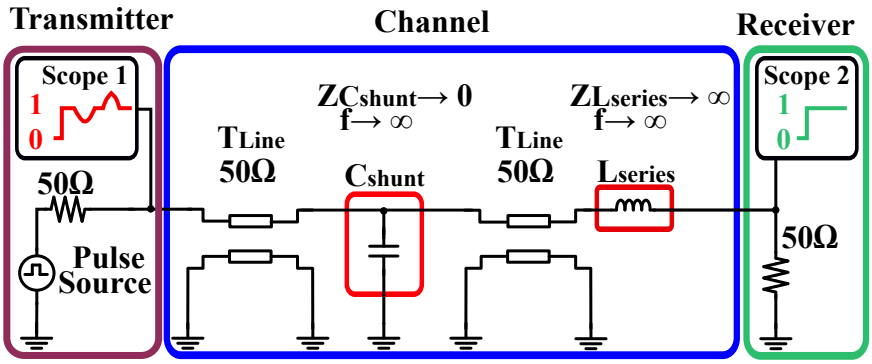


Fig. 8 depicts a block diagram of a differential wireline communication system. Each component in the communication system must offer a resistor matching a differential 100Ω standard value. Matching between the resistors avoids signal reflection and accomplishes maximum power transfer from the transmitter to the receiver. However, the matching condition during operation may be lost due to temperature variation. Non-matched resistors, combined with intrinsic channel power losses, might result in data corruption or information losses.

Receivers usually have a variable resistor termination to ensure matching, regarding the process and temperature variations, along with a Continuous-Time Linear Equalizer (CTLE) to restore the signal amplitude at high frequencies. Receivers also include ESD protection circuits to protect internal circuits against over-voltages in those events. ESD diodes are forward-biased when the input voltage is high enough. Diodes deliver a high current through a power clamp to the

Figura 9

A qualitative single-ended version of a simplified differential link with passive elements included in the channel. Both C_{shunt} and L_{series} elements model channel discontinuities.



ground to reduce the incoming voltage, avoiding potential interconnection damages or transistor oxide ruptures.

2.3.2. ISI Effects on Signal Integrity

In band-limited communication systems, the channel behaves as a low-pass filter for incoming signals from the transmitter. Digital symbols constitute the transmitted information, and each one of those symbols is, in theory, comprised of infinite frequency components. With the channel bandwidth limitations, the output waveform observed at the receiver experiences a reduction of frequency components compared to the ideal input waveform. Thus, the data waveform no longer has vertical transitions, causing the transmitted pulses to start mixing due to their reduced transition slopes. This phenomenon is called InterSymbol Interference (ISI) and affects the process of data detection in the receiver [28]. An event that boosts the ISI effect over transmitted data is channel impedance discontinuities. These discontinuities appear due to undesired effects such as parasitic elements and unmatched impedance/resistor terminations, generating wave reflections that deteriorate the transmitted information.

Figura 10

Relevant prior work from patents of on-die differential 100Ω standard terminations. In a), a core of multiple 120Ω branches in parallel for impedance matching switched by PMOS and NMOS transistor. In b), two 100Ω resistors at the input and the output of signal transmission bus for high-speed transfer mode. In c), an adjustable pull-up resistor network with power consumption compensation to maintain a constant current value through an external resistor.

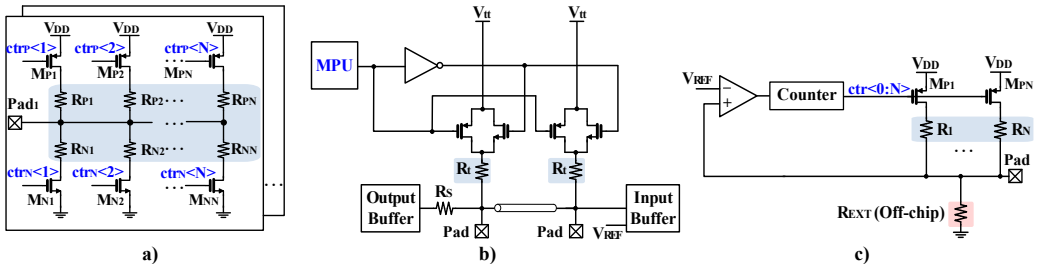


Figura 11

A qualitative illustration of a reflected wave event seen by the source due to capacitor and inductor impedance discontinuities in a high-speed link (blue). These discontinuities can also be observed with the changes in the equivalent impedance in red.

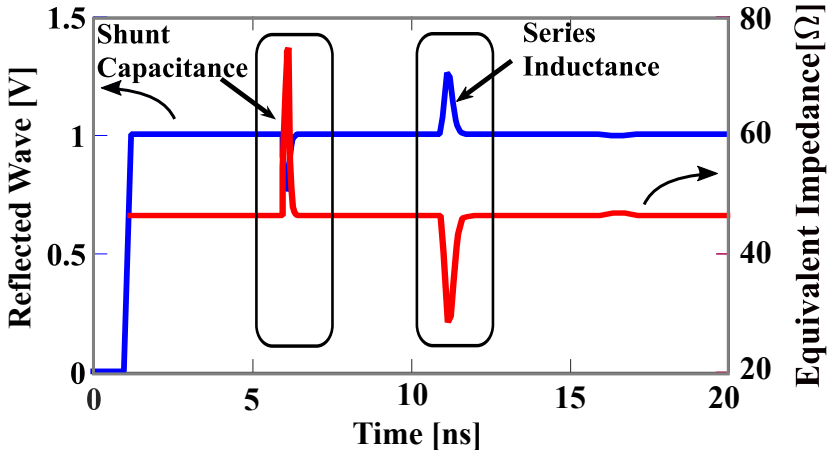


Fig. 11 presents the Time-Domain Reflectometer (TDR) measurement of the simulated wave and the equivalent impedance seen by the transmitter in Fig. 9. The simulation setup implements a 2pF capacitor and an 8nH inductor to illustrate the reflected wave concept when an unmatched impedance condition occurs. Discontinuities due to the shunt capacitance and the series inductor affect the signal integrity of transmitted data causing glitches, as illustrated. A common methodo-

logy for analyzing high-speed digital signals is a data eye diagram. Parts of the signal waveform associated with each bit are folded into a single graph to represent the average statistics of the signal. The result of folding the different parts will resemble an eye, as illustrated in the transmitter or the receiver block in Fig. 8. Impedance discontinuities and attenuation, and noise might close the eye, avoiding the correct data recovery at the receiver side.

2.3.3. Prior Work on Resistor Terminations

Fig. 10 summarizes three different patents of on-die terminations from well-known consumer electronics companies. The work presented by [63] in Fig. 10 a) illustrates a system that obtains multiple impedance values in a communication system with a variable load. The matching core is composed of 120Ω resistor branches switched by PMOS and NMOS transistors. Although fine calibration steps can be achieved using multiple resistor branches in parallel, there is no fixed step. This lack of a fixed step might cause undesired wave reflections during the calibration process when a low number of parallel branches is used.

Taguchi [70] proposes a single-value resistor-matching network controlled by a Microprocessor Unit (MPU). Taguchi et al. only use one 100Ω resistor at the input and the output of a signal transmission bus, as illustrated in Fig. 10b). These two resistors are only activated for high-speed operation, getting turned off for low-speed transfer mode to save power consumption. Nevertheless, process and temperature variations affect the matching condition, which cannot be mitigated due to the resistors' fixed value. Another approach uses a pull-up network, as Fig. 10c) shows. Kim et al. [30] propose a termination that adjusts its value if the user modifies the voltage supply. Instead of maintaining a constant resistor value, Kim et al. offer a termination that maintains a constant

current through an external resistor.

As mentioned in section 2.2, there is little documentation available regarding resistor termination design. The selected references do not present relevant information to make a quantitative comparison. Thus, a qualitative comparison with recent works based on an estimation of the occupied area of the ESD protection, the possibility to vary the resistor value, and the presence or absence of devices to withstand ESD are made to validate the proposed design.

A termination design must include other considerations, such as high-current density and ESD compliance. For instance, ESD and high-current density demand large-area devices that withstand large current values to protect the integrated circuits. The lack of ESD and high-current density considerations prevent the deployability of reported works. Besides, channel discontinuities caused by an unmatched resistor should be mitigated with fine steps (units of Ω) to avoid further signal integrity issues. None of the previous works take into account all the considerations together. Here we introduce a resistor termination design with a novel switching technique for ESD residual voltage mitigation and a differential 1.4Ω fine step feature.

2.4. Proposed Resistor Termination

Achieving a fine calibration step requires a proper control scheme. The proposed resistor matching network is designed for a single-ended range from 35Ω to 65Ω using two different controlling codes for coarse and fine steps. The matching network is comprised of six banks, a 65Ω initial value, B1, B2, B3, and B4 banks for specific values ranges and B_Adjust for process-voltage-temperature (PVT) compensation as Fig. 12 shows. The termination is connected between the receiver input pad (Vin) and a common voltage node (VCM) that sets the bias voltage of the

Figura 12

Control signals to activate all the blocks of the single-ended termination scheme. A calibration bank B_Adjust is included to compensate for Process-Voltage-Temperature (PVT) variations.

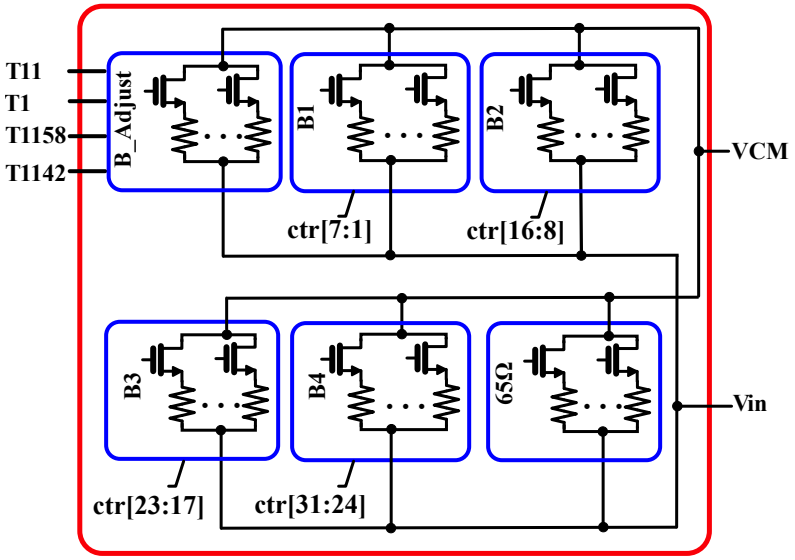
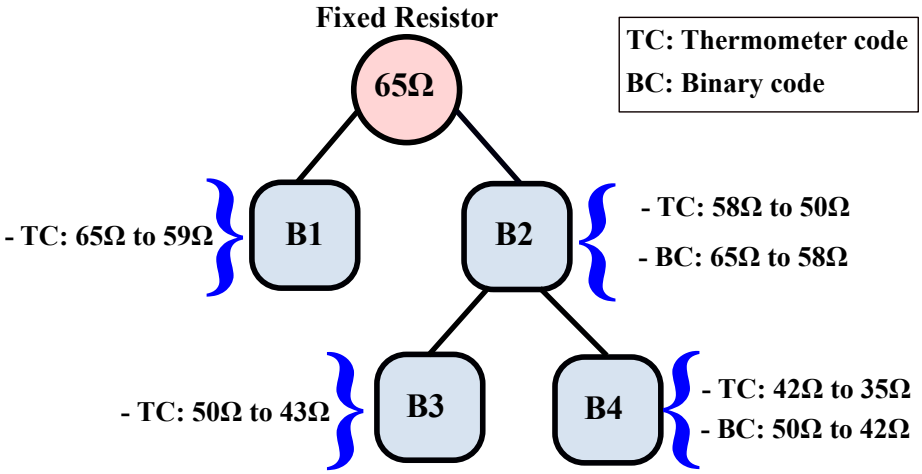


Figura 13

Distribution of Single-ended resistor banks and the operating modes for the 65Ω-35Ω range.



CTLE instantiated in the receiver.

Banks B1 and B3 only operate with a thermometer code from 65Ω to 59Ω and from 50Ω to 43Ω ranges. Both thermometer and binary codes can be applied to banks B2 and B4, as depicted

in Fig. 13. The thermometer code modifies the termination value in ≈0.8Ω-steps during the transmission, whereas the binary code changes the resistance value in 8Ω-steps, mainly at the initial calibration of the termination resistance. The thermometer code on bank B2 is used for fine steps from 58Ω to 50Ω, whereas binary code offers a coarse step to change the resistor value from 65Ω to 58Ω. Bank B4 operates with a thermometer code for fine steps from 42Ω to 35Ω and with binary code for a coarse step from 50Ω to 42Ω. Finally, banks B3 and B4 operate only when bank B2 is active.

Regarding the *B_Ad just* bank, T1 is a control signal to set the 65Ω nominal value, and T11, T1158, and T1142 are control signals to adjust termination values for FFLLL[1] corner variations. T11: adapts the 65Ω value, T1158, and T1142: Adjust the termination value when a binary step is applied to achieve 58Ω and 42Ω, respectively. The proposed design only uses resistors in parallel for area minimization at the expense of precision loss. A combination of series and parallel resistors should be used if precision is one of the main goals. Each resistor bank comprises an array of parallel branches formed by a series connection of a resistor and an NMOS switch. Every switch has an independent control signal to adjust equivalent resistor termination.

During the design phase, the 50Ω resistance was defined as the mean value of the resistance termination. To achieve lower values than 50Ω and to maintain the unitary resistance in all the banks, bank B2 is turned on first to reach the 50Ω value. Then banks B3 and B4 operate independently to achieve the remaining range.

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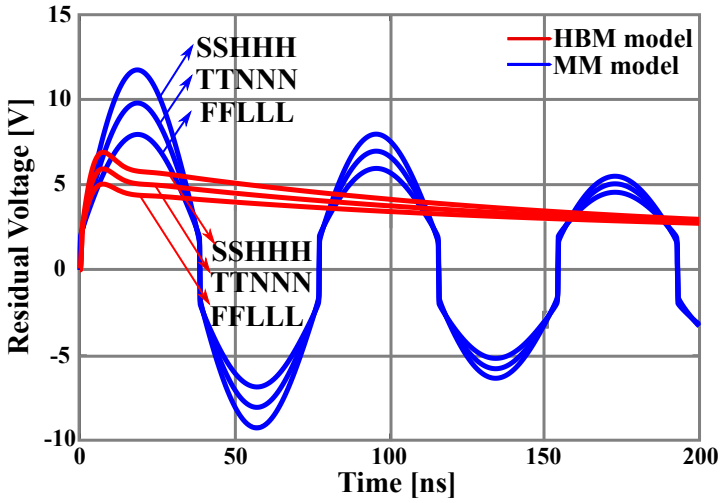
[1] FFLLL indicates Fast - Fast - Low - Low - Low, for instance.

Figura 14
Residual voltage in the input pad for HBM and MM extreme corner discharges.



2.4.1. ESD Considerations

The three most common ESD events modeled in the consumer electronics industry are the Human-Body Model (HBM), the Machine-Machine Model (MM), and Charged-Device Model (CDM). These models describe ESD discharge standards using passive elements (resistors, capacitors, and inductors) with different transient responses, as reported by [24]. The impedance matching network presented in this chapter only considers HBM and MM models. The available power clamp has a time constant in the nanosecond range, which is appropriate for HBM and MM pulse rise time. However, the CDM model requires a power clamp with a time constant of less than 1ns for proper verification. Thus, the CDM model is discarded for the present resistor termination design.

Corner simulation results for HBM and MM electrostatic discharges generated in the input pad are presented in Fig. 14. Residual voltage values are measured for HBM and MM models with

peak values of 7V and 11V. For instance, the residual voltage appears in the MM simulations after the activation of ESD primary diodes. The ESD current deviates from the circuit to be protected by crossing over the bias rails and then passing through the power clamp for its dissipation in the system ground. The diode activation reduces the input voltage from the 200V predicted by the model to a residual voltage of 11V. However, the residual voltage value is higher than the transistor's technology oxide rupture voltage instantiated in the resistor termination. Therefore, the NMOS-resistor structure of each branch in the resistor termination must be redefined to guarantee reliability after an ESD event.

2.4.2. Layout and Residual Voltage Considerations

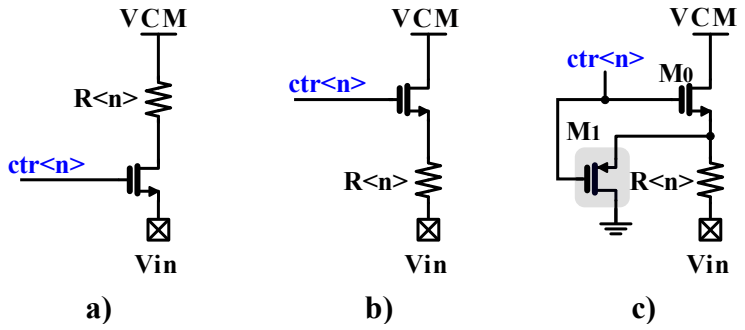
Each of the elements of the matching network must support high current densities caused by ESD events. The selection of the unitary resistor is based on its specific current density and the residual voltage set on the input pad.

A 10kΩ unitary resistor with a 1.5μm width guarantees 1mA of current density for the corresponding 11V MM residual voltage. With these specifications, 153 resistors must be connected in parallel to get the 65Ω resistor, considerably handicapping area availability. Aiming to reduce the area occupied, a width of 19μm is chosen, resulting in an 806Ω unitary resistor. Only 12 parallel resistors are required to achieve the 65Ω value, occupying an area of 0.094mm^2, which is 45.77 % less than the implementation with 1.5μm.

2.4.3. Proposed Topology for Transistor Oxide Protection

Fig. 15 shows two classical switching schemes and the proposed switching scheme. The classical schemes do not consider the residual voltage on ESD events. For example, the transistor's

Figura 15
a) Classical switching scheme, b) modified scheme, and c) the here proposed. An additional PMOS switch is added to prevent over-voltages in any switches' terminals.



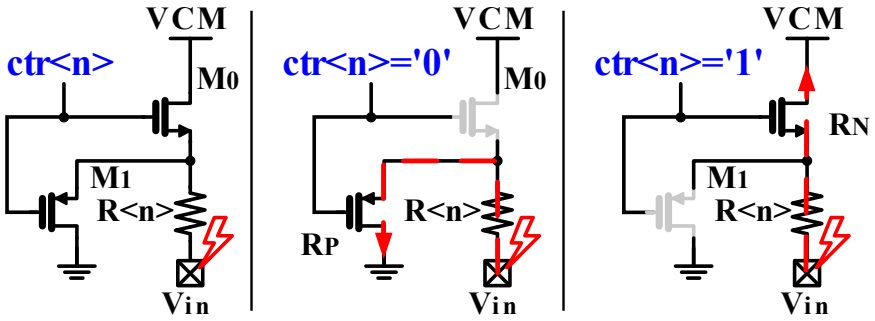
source terminal in Fig. 15 a) experiences a large voltage swing due to the residual voltage in the presence of an ESD event. This issue is avoided by using the scheme in Fig. 15 b) by adding a voltage drop through the series resistor. However, this scheme still experiences a hazardous voltage swing between the drain and source terminals when the control signal is set to zero. This chapter proposes a double switch scheme in Fig. 15 c) to protect the NMOS switches against ESD residual voltages.

The operation of the proposed scheme under ESD events is illustrated in Fig. 16. Maintaining the resistor connection to the pad and adding a PMOS switch, the transistor's source terminal always experiments with a voltage divider due to two possible discharge paths depending on control signal:

- If the ctr is set to 0V (Case 1), the NMOS transistor is off, and all the current flows through the PMOS transistor. To protect and decrease NMOS source voltage, PMOS on resistor value R_{onM1} must be small compared to the resistor branch for voltage division as equation 1 presents. A trade-off between power consumption and PMOS transistor dimensions must be

Figura 16

Illustration of the proposed switch operation in the presence of over-voltage ESD events. The input signal always goes through a resistive divider independent of the control signal.



considered to ensure the proper voltage swing with reduced static consumption.

$$V_{GS_{M0}} = V_{in} \frac{R_{onM1}}{R_{Br} + R_{onM1}} \tag{1}$$

- If ctr is asserted to 3.3V (Case 2), the PMOS transistor is open, and all the current flows through NMOS one, and its V_{GS} voltage is defined by equation 2. The static power consumption of PMOS transistors must be negligible compared to the resistor termination power consumption.

$$V_{GS_{M0}} = V_{ctr} - \frac{V_{in} \cdot R_{onM0} + V_{CM} \cdot R_{Br}}{R_{Br} + R_{onM0}} \tag{2}$$

Fig. 17 shows the simulation results of the proposed and a classical switch to verify the voltage swing reduction. Red waves represent the NMOS source voltage in the topology of Fig. 15

Figura 17

Switching schemes with and without the PMOS transistor instantiation to compensate discharges in extreme corners. The proposed solution guarantees a safe voltage margin in the transistor's source terminal.

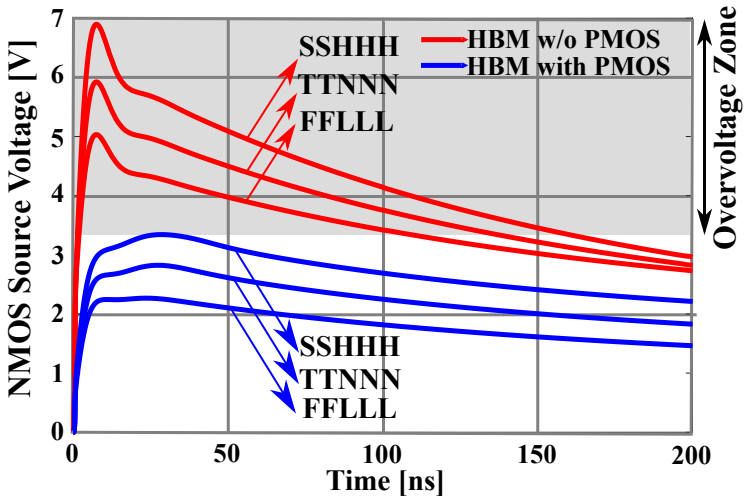
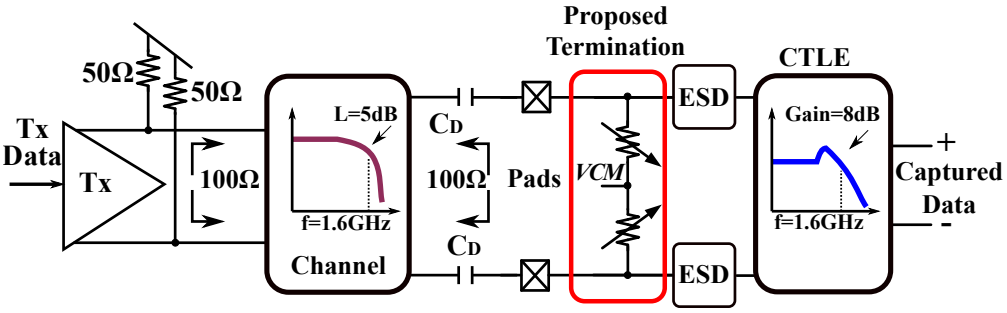


Figura 18

Simulation setup to verify the proposed resistor termination. A PRBS 15 differential source with a 100Ω termination provides the input data, and a two-port network models the channel to include ISI effects.



b), and blue waves correspond to the proposed switching scheme. In the worst-case scenario, the residual voltage is decreased to a safe margin (3.3V), avoiding stress voltages.

2.5. Results

This section presents a verification of the proposed resistor termination in a stand-alone single-ended mode and also with a simplified differential link. Stand-alone verification considers PVT variations and Monte Carlo runs. Also, the layout of part of the back-end circuit of a high-speed receiver (composed of ESD circuits, the proposed termination, and a CTLE) has been extracted and included.

Fig. 18 shows the simplified differential link setup employed to verify the impedance mismatch and the effects on signal integrity. This simulation requires a proper setup to capture the incidence of the reflected wave through the channel. Fig. 18 includes a differential PRBS 15 source and a channel modeled by a two-port network. The channel model considers the associated losses and reflection effects due to mismatch. The channel matches a 100Ω differential mode standard resistor and models 5dB losses (L) at 1.6GHz. Besides the resistor termination, decoupling capacitances (C_D) in the receiver input pads, and ESD circuits used for residual voltage verification are added. The scheme also includes a CTLE to compensate for the channel losses.

2.5.1. Resistor Termination Layout

Fig. 19 presents the single-ended resistor termination layout, occupying an area of $90\mu m$ x $190\mu m$ in a 180nm CMOS standard technology. The NMOS transistors and PMOS transistors are 3.3V I/O nominal devices with dimensions $W_{NMOS} = 10\mu m$, $L_{NMOS} = 350nm$ and $W_{PMOS} = 2\mu m$, $L_{PMOS} = 2\mu m$. The resistor used is a poly resistor and the dimensions of the branch resistors are W = 1,5μm and L = 45,23μm. The dimensions of the fixed resistor of the B1 block are W =

Figura 19
Termination layout in 180nm CMOS standard technology occupying 0.017mm^2.

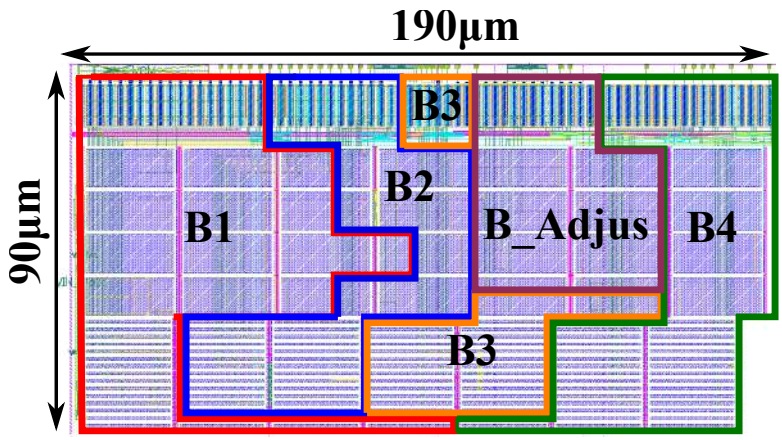
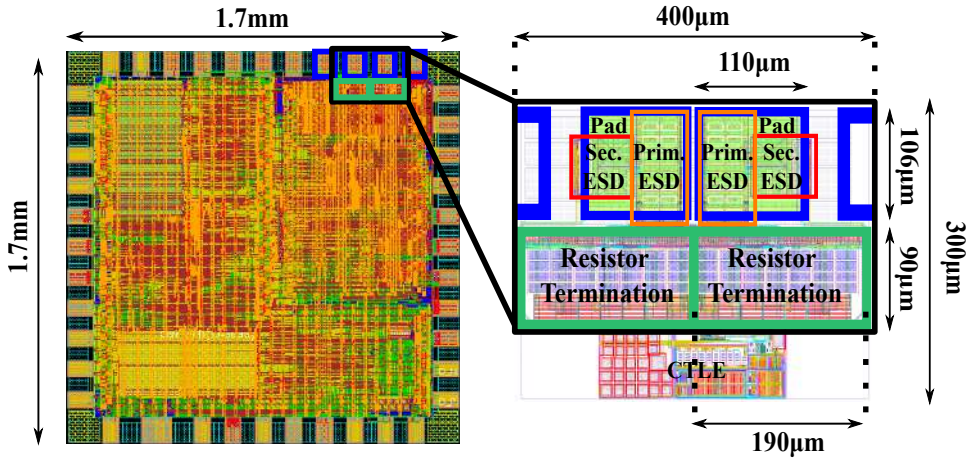


Figura 20
Layout of a differential signal path containing pads, ESD circuits, resistor termination, and CTLE in a standard 180nm CMOS technology. The layout occupies an area of 300µm x 400µm.



20,65μm and L = 47,5μm. The layout design fulfills layout considerations along with the ESD considerations previously mentioned to enhance its reliability. Fig. 19 also depicts the distribution of the five resistor banks.

Fig. 20 illustrates part of the receiver interface layout in a 0,12mm^2 area. Considering the associated differential operation, the layout must be symmetric and compact to avoid unbalanced

signals and power losses. Primary ESD (Prim. ESD) and Secondary ESD (Sec. ESD) are on the Pad ring for direct connection to the power ring. Every layout block is placed as close as possible, maintaining symmetry to guarantee matching conditions with the remaining back-end circuitry that will be integrated next.

2.5.2. Stand-Alone Single-ended Termination Verification

Fig. 21 and Fig. 22 show post-layout results of the single-ended resistor value over PVT variations. Corner nomenclature follows the NMOS process, PMOS process, resistor process, supply voltage, and temperature[2] using the industrial temperature range from -40°C to 125°C and applying a maximum variation of +/- 10% for both voltage supplies. Fig. 21 presents corners with the largest variations for the resistor value as a function of control words ctr[7:1] and ctr[16:8] associated with the banks B1 and B2. The worst-case occurs for 63Ω with a 1.7Ω step in the FFLLL corner.

Fig. 22 depicts corners with the largest variations for the resistor values in the 50Ω - 35Ω range associated with banks B3 and B4. These banks are controlled by the words ctr[23:17] and ctr[31:24], respectively, and they must be activated after banks B1 and B2. The largest error happens in the B3 range with a 1.8Ω for 47Ω value in the FFLLL corner. Fig. 21 and Fig. 22 also illustrate how the whole range can be covered with fine steps of less than 2Ω in the worst case.

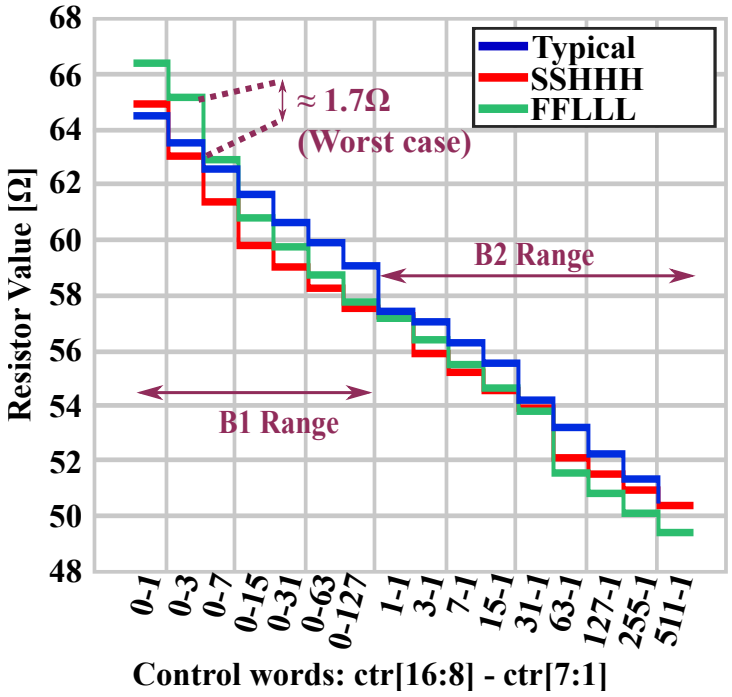
The resistor errors can be reduced by activating the adjustment block integrated into the termination. The adjustment block uses four bits to calibrate corner variations for the 65Ω, 58Ω, 42Ω, and 35Ω reference values, guaranteeing a proper resistor range for the fine calibration step.

---

[2] SSHHH indicates Slow - Slow - High - High - High, for instance.

Figura 21

Worst-case corners for post-layout simulations varying the termination equivalent resistor from 65Ω to 50Ω (B1 and B2 ranges). The whole range can be covered with only fine steps.

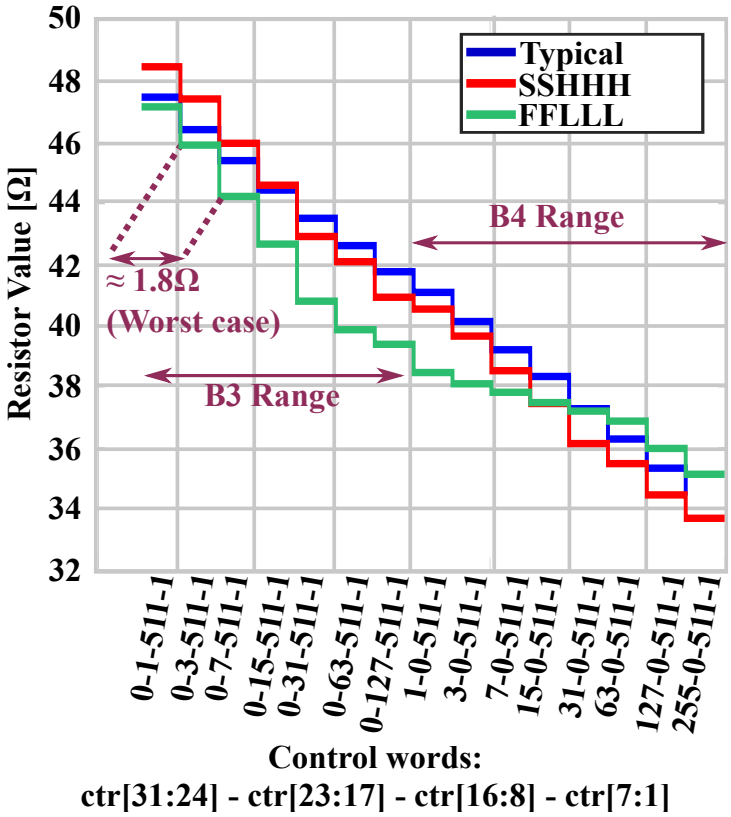


As depicted in Fig. 12, the control word is defined by bits T11, T1, T1158, and T1142. The typical case setup corresponds to a logical one in T1, and the remaining bits in a logical zero value. T1 and T11 activate compensation for variations of the 35Ω (T1=T11='0') and 65Ω (T1=T11='1') reference values. When T1142, T1, and T11 are set to a logical one, the adjustment block corrects the 42Ω value to correct the FFLLL corner case. Otherwise, if T1158, T1, and T11 are set to a logical one, the setup compensates the variations due to the FFLLL corner for the 58Ω resistor value. The previous adjustments for the 42Ω and the 58Ω values are executed to compensate for the variations of the binary mode.

Monte Carlo simulations were obtained for all the banks and their associated resistor values.

Figura 22

Worst-case corners for post-layout simulations varying the termination equivalent resistor from 49Ω to 35Ω (B3 and B4 ranges). The whole range can be covered with only fine steps.



Simulation results with a total of 400 samples demonstrated that the standard deviation is reduced as the number of banks in parallel increases. The maximum standard deviation for B3 and B4 ranges is 17.8mΩ, whereas for the B1 and B2 ranges is 30mΩ. Results indicate a robust performance against random mismatch variations in all cases. Table 3 presents a summary of the worst relative error cases for corners and Monte Carlo results.

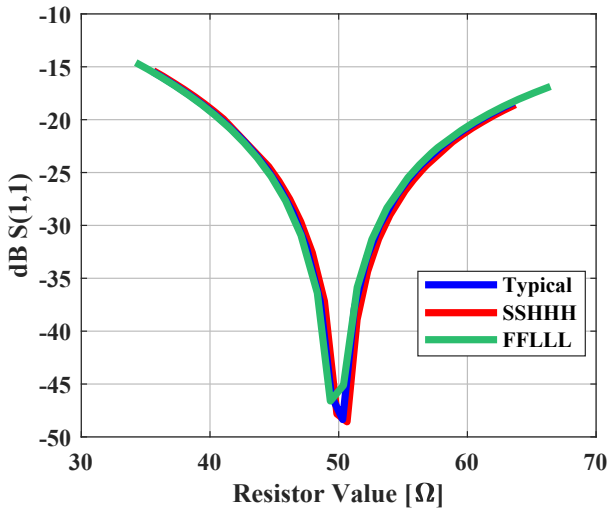
Table 4 presents an area comparison with some prior work terminations. The area of the references is estimated based on compliance with the 2kV HBM ESD model. With this estimation, the proposed termination offers a small footprint with ESD and layout considerations besides

Tabla 3
Worst-Cases Simulation Results Summary

	SSHHH (@35Ω)	FFLLL (@58Ω)	MC (@58Ω)
Max. Relative Error [%]	17,66⋆/ 2.34	13,66⋆ / 0.97	2.94

⋆ without calibration / with calibration

Figura 23
Corner simulations of the S11 parameter for the different resistor values provided by the resistance termination.



featuring a fine step adjustment.

Tabla 4
Comparative Estimated Area of the Resistor Termination Based Upon Compliance with Recent Work Terminations.

	This work	[30]	[63]	[70]
Area [mm^2]	0.2x0.15	0.36x0.36	0.3x0.3	0.16x0.16

⋆ without calibration / with calibration

2.5.3. Reflected Wave Effects on Signal Integrity due to Mismatch Resistor

Resistor matching is mandatory to have maximum power transfer from the transmitter to the receiver. No matching conditions bring impedance discontinuities through the communication link, causing wave reflections. These reflections modify the input signal waveform, resulting in signal integrity issues and possible data corruption or data losses.

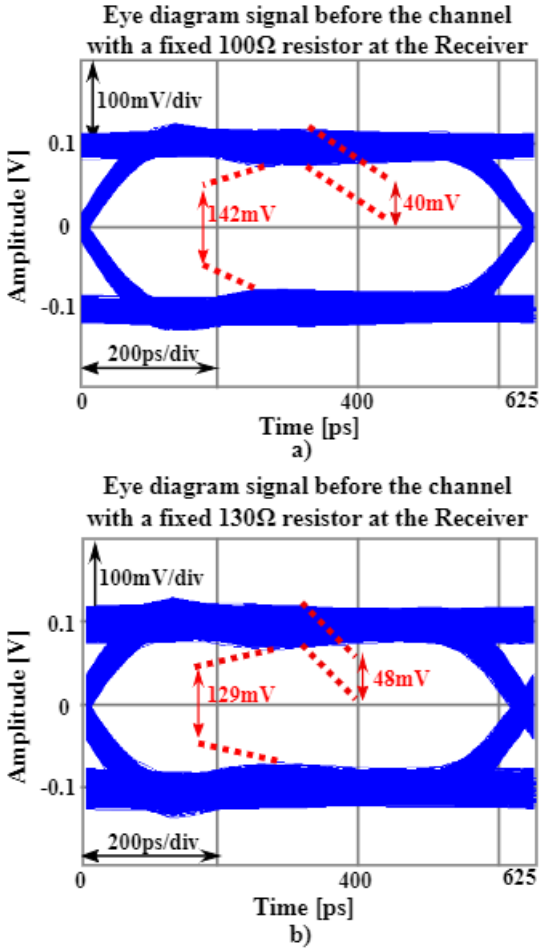
Fig. 23 illustrates the corner (PVT) simulation results for the S11 parameter, modifying the resistor values of the termination resistance. As expected, the minimum value is achieved in the matching condition (a resistance of 50Ω) since the reflected power is minimized.

Then, a simulation is performed during matched and unmatched conditions to illustrate the effects of wave reflections on signal integrity. Fig. 24 shows two eye diagrams of the transmitted signal before the communication channel. In Fig. 24 a), the resistor termination value of the receiver is 100Ω in differential mode, whereas in Fig. 24 b) the receiver equivalent resistor is 130Ω. Simulations are performed using the setup of Fig. 18 at a data rate of 3.2-Gb/s and a differential signal amplitude of 0.2Vp. Both eye diagrams were obtained with a time window of 703.1ns (1125 cycles of the input signal).

The eye diagrams present part of these wave reflections as undershoot voltages, causing an eye height reduction. Fig. 24 a) shows the matched condition where the eye height is 142mV. In contrast, Fig. 24 b) shows the unmatched condition where eye height decreases to 129mV. Additionally, the width of the one-level band for the 100Ω and the 130Ω conditions is 40mV and 48mV, respectively. The latter demonstrates higher ISI in the one-level band for the unmatched

Figura 24

Eye diagrams of the transmitted signal before the channel. Distortion increases and eye height decreases when the communication system is not matched.



situation. These results illustrate the importance of matching conditions due to strong undesired effects that might cause the eye diagram to close at the receiver, preventing data recovery.

2.5.4. Effect of Resistor Termination Adjustment with Coarse and Fine Steps

Resistor mismatch in the communication system generates undesired reflected signals that attain the transmitter and modify the data waveform. It is desirable that the equivalent resistors of the system match at 100Ω. However, the link experiments temperature variations during trans-

mission, leaving the matched condition due to the resistor temperature dependence, for instance. Therefore, the receiver must detect this event and adjust the termination, but this action depends on resistor termination resolution, which is critical for signal integrity considerations.

Two different cases regarding resistor termination variations are explored to identify the effects of coarse or fine steps in the CTLE output eye diagram. The two cases correspond to a modification of the matched resistor, due to temperature variations, for instance, and the effects of the 100Ω calibration mechanism by the resistor termination. Simulations were carried out using the same setup as in section 2.5.3. As mentioned, the setup includes ESD circuits to reduce the residual voltage in the I/O pad and deviate the ESD current through the bias rails. Large-area devices might compose ESD circuits to withstand large current values to protect the integrated circuits. The parasitics associated with these devices limit the bandwidth of the receiver, especially for the CTLE. The latter sets the maximum data rate that the CTLE manages for equalization, which is 3.2-Gb/s.

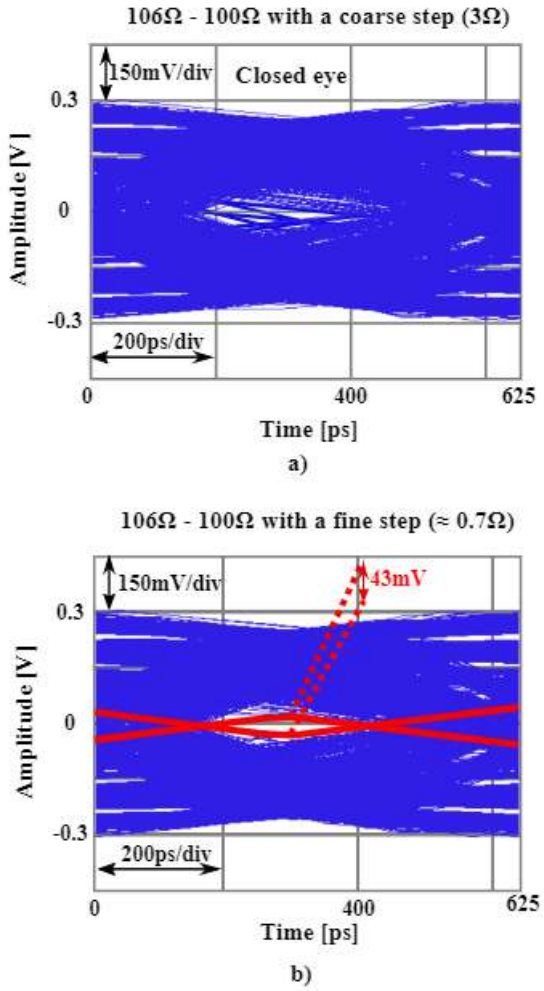
110Ω-100Ω and 106Ω-100Ω transitions were simulated with coarse and fine steps to explore signal integrity. Fig. 25 illustrates eye diagrams for the 106Ω-100Ω scenario with coarse and fine recovery steps.

Fig. 25 a) shows the eye diagram of the CTLE differential output for the coarse step during 3.125μs (5000 cycles). The initial resistor value is 106Ω, and after 2500 cycles, the termination resistor modifies the intermediate resistor values one at a time. Data corruption or data losses might happen due to eye closure with the abrupt resistor transition.

The fine step is then simulated as Fig. 25 b) illustrates. The eye diagram of the CTLE

Figura 25

Eye diagrams for the 106Ω-100Ω resistor transition with a) coarse and b) fine (≈ 1.4Ω) steps. The coarse step completely closes the eye.



differential output is extracted using a transient simulation of 4.69μs (9500 cycles). The initial resistor value is 106Ω, and after 2500 cycles, the termination resistor modifies the intermediate resistor values one at a time. The time used for each resistor transition is 312.5ns (500 cycles). With a ≈1.4Ω fine step, the eye is maintained open during data transmission with a resulting height of 43mV.

Figura 26

Eye diagrams for the 110Ω-100Ω resistor transition with a) coarse and b) fine (≈ 1.4Ω) steps. The coarse step causes glitches that reduce eye height.

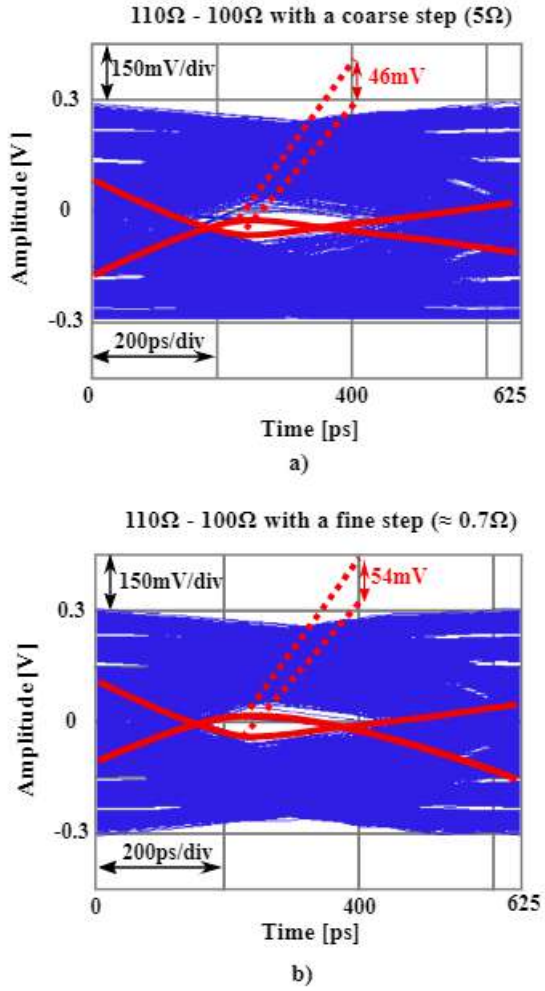


Fig. 26 a) shows the eye diagram of CTLE differential outputs for the coarse step during 3.125μs (5000 cycles). The initial resistor value is 110Ω, and after 2500 cycles, the termination resistor modifies all the control signals simultaneously to achieve the desired 100Ω resistor value. Simulation results demonstrate that the amplitude of the glitches caused by the coarse step reduces the eye height, which might also cause information losses if the resulting amplitude is less than

CTLE sensitivity.

A fine step simulation is also carried out for the same resistor change. Fig. 26 b) illustrates the eye diagram of the CTLE differential output for a time window of 4.69μs (9500 cycles). The initial resistor value is 110Ω, and after 2500 cycles, the termination resistor modifies one at a time the intermediate resistor values. The expected time for each resistor transition is 312.5ns (500 cycles). With a ≈1.4Ω fine step, the eye is maintained open during the transmission with an eye height of 54mV.

To demonstrate the advantages of the proposed resistor termination, a comparison with a prior work termination presented in [63] is carried out. The authors defined the same resistor value for all the branches included in the resistor termination. The resistor value is set to 120Ω, as suggested by the authors in [63]. No ESD considerations nor layout estimation were included to define transistor dimensions. The same setup configuration presented at the beginning of this section is implemented to evaluate the performance of the resistor termination in differential mode. A 3.125μs transient simulation is executed to assess the effect of the resistor step on signal integrity. One branch is activated at the beginning of the simulation to start with a 240Ω differential equivalent resistor in differential mode. After 1.56μs, another branch is activated to reduce the equivalent resistor value to 120Ω. Fig. 27 depicts the eye diagram with glitches reducing both the eye's height and width. Simulation results demonstrate the importance of having a fine step in the resistor termination to avoid ISI during information transmission.

Regarding the algorithm for termination calibration, the USB standard indicates that the transmitter and receiver do a bi-directional time synchronization handshake at low-frequencies to

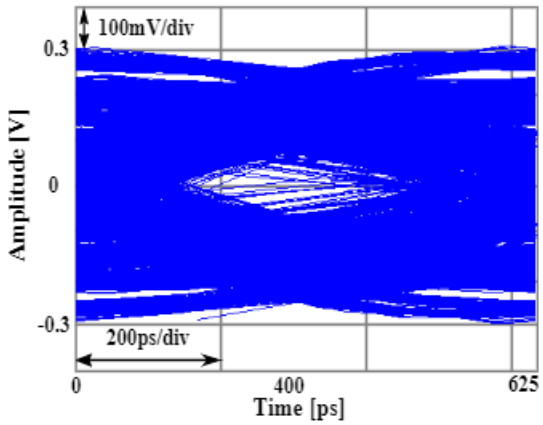
initialize the data transaction. During the synchronization handshake, several measurement and calibration steps occur, such as frequency offset, propagation delay, and time offset. Among those measurements, the USB3 adapter layer indicates to the transport layer if the receiver termination is unmatched (different from 50Ω) to start the calibration. Once the low-frequency calibration occurs, the data transfer frequency increases step-by-step to achieve the frequency defined by the USB standard. For each frequency step, the time synchronization handshake occurs again, enabling maximum power transference.

The calibration algorithm is technology-independent and is beyond this chapter's scope. Thus, a manual approach is adopted to get proof of concept. However, we expect to have the first version of the calibration algorithm after the ongoing tape out. A possible configuration to calibrate the resistor calibration automatically is based on a time-domain reflectometer (TDR) for a similar resistor termination range (35Ω to 75Ω) as presented in [8]. Nevertheless, the TDR technique is not based on the USB standard calibration algorithm, which is desired for high-speed applications. Finally, the chosen calibration range might work in scaled technologies despite the increased variations and let us study the effect of latency and power consumption of the whole system.

Fig. 26 a) shows the eye diagram of CTLE differential outputs for the coarse step during 3.125μs (5000 cycles). The initial resistor value is 110Ω, and after 2500 cycles, the termination resistor modifies all the control signals simultaneously to achieve the desired 100Ω resistor value. Simulation results demonstrate that the amplitude of the glitches caused by the coarse step reduces the eye height, which might also cause information losses if the resulting amplitude is less than

Figura 27

CTLE output eye diagram using the relevant work termination varying the equivalent resistor value from 120Ω to 60Ω.



CTLE sensitivity.

A fine step simulation is also carried out for the same resistor change. Fig. 26 b) illustrates the eye diagram of the CTLE differential output for a time window of 4.69μs (9500 cycles). The initial resistor value is 110Ω, and after 2500 cycles, the termination resistor modifies one at a time the intermediate resistor values. The expected time for each resistor transition is 312.5ns (500 cycles). With a ≈1.4Ω fine step, the eye is maintained open during the transmission with an eye height of 54mV.

2.6. Conclusion

A small footprint differential resistor termination featuring a fine calibration step to mitigate ISI effects due to resistor adjustment has been presented. The use of thermometer control codes enables a fine step of ≈1.4Ω without inducing strong signal integrity issues in a range from 70Ω to 130Ω. A stand-alone termination design considering ESD events, layout considerations, and transistor oxide protection is validated, showing a robust performance against Monte Carlo

mismatch simulations. As expected, PVT effects are strong over resistor value, especially when the temperature varies, but an additional adjustment bank compensates for PVT-induced errors. The proposed termination is also verified by using a simulation setup that includes a PRBS15 differential source as the transmitter, channel losses, ESD circuits, and a CTLE for signal equalization. Considering on-the-fly calibration is desired since impedance matching may change during transmission with temperature variations in the resistor, and on-the-fly adjustment demonstrates the effect of calibration steps. Simulations show how a fine calibration step may reduce ISI effects, relaxing equalization specifications, or even avoiding information losses. The stand-alone single-ended termination occupies an area of $0.2\text{mm}\times0.15\text{mm}$, and it is also integrated into the layout of part of the receiver back-end, including ESD circuits and a CTLE.

2.7. Contributions of this chapter

- A small footprint differential resistor termination ($0.2\text{mm}\times0.15\text{mm}$) considering ESD events, current density, and PVT variations.
- Thermometer and binary control codes to increase versatility for the user.
- Fine step of $\approx1.4\Omega$ without inducing strong signal integrity issues.

3. Analysis and Design Approach of Wideband Digital-Based Feedforward Ring Oscillators

Continuing with the implementation of clock sources in SoC, in this chapter we are going to present some contributions regarding a wide-frequency operating range architecture for clock generation sources. As mentioned before, to reduce the number of clock sources in SoC, it is desirable to implement a unique clock source to cover the largest number of communication protocols. Among the different techniques currently found in the state-of-the-art, the feedforward concept appears as a possible technique to be explored. It is worth mentioning that this concept was presented and developed by Harold S. Black at Bell Laboratories for amplification stabilization in the 1930s, [4]. Although it is true that this concept has been explored during different decades, few works extending the tuning range were reported in the literature, especially in the kHz-GHz range.

This chapter presents an analysis and a design approach of wideband digital-based oscillators utilizing secondary feedforward paths to support most of the data-rate requirements inside systems-on-chips. Here, we present the inclusion of these auxiliary loops as a tuning range enhancement technique to reduce the total number of required clock references. The presented analysis comprises piece-wise functions able to accurately predict a feedforward differential ring oscillator (FDRO oscillation frequency).

3.1. Tuning range enhancement analysis in feedforward differential ring oscillators.

In this section, we developed a piece-wise model based on the work proposed by [68] but we extend the analysis by controlling both core and feedforward delay cells. The FDRO is implemen-

ted in a 12-track standard cell format to reduce instantiation costs and achieve a compact layout. Monotonicity and non-latch-up are guaranteed in a wide frequency range covering a kHz-GHz range with a 180nm CMOS technology node.

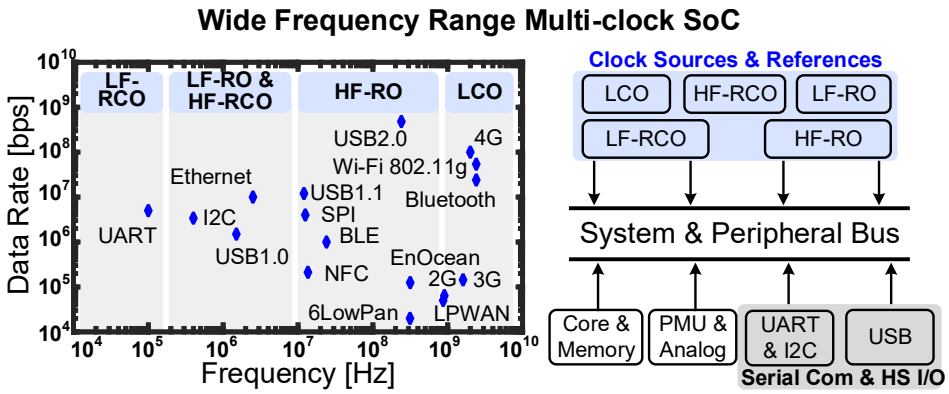
3.2. Introduction

The widespread of multiple communication standards and the constant data-rate enhancement have led frequency references' designs to maximize their oscillation frequency while achieving broader tuning ranges. Systems usually integrate multiple clock sources operating at different oscillation frequencies to support several applications at different data rates. Fig. 28 illustrates a conventional integrated system architecture comprising analog blocks, serial interfaces, peripherals, and multiple clock references. These clock sources might cover different frequency ranges to encompass the majority of applications. High frequency I/Os might operate up to 25GHz [68], while legacy communication protocols and wake-up timer applications must work in the kHz range for low energy consumption [22].

As Fig. 28 shows, systems integrate LC-based oscillators (LCOs) with ring-based oscillators (ROs) to cover most of the frequency requirements. LCOs usually supply high data-rate protocols as they require high-frequency stability and can afford a limited tuning range. In contrast, ROs support legacy protocol applications at lower data rates where frequency stability is not a constraint and a large tuning range is required [68]. Since reported injection and feedback techniques enhance ROs frequency stability while maintaining broad tuning ranges [5, 40, 68], a single RO might fulfill most of the system data-rate requirements and reduce the overall integrated clock references.

Figura 28

In a), the Data rates of different communication applications, with their respective clock sources and frequency bands are presented. In b), a conventional integrated system with several domains, multiple clock references, and different communication interfaces.



The inclusion of auxiliary paths inside the main oscillator chain allowed the increase of the maximum oscillation frequency. In fact, the inclusion of these secondary loops might generate an oscillation on even-stages single-ended ROs [40]. The aspect ratio among the core and secondary delay cells (also named feedforward strength) modifies f_{max} by a controllable factor. Chen et al.[5] proposed a 4-to-16GHz frequency reference by controlling the feedforward inverters while maintaining the core cells constant. In contrast, Song. et al.[68] designed a 2-to-20GHz clock source with fixed feedforward inverters and a controllable main loop. Note that, although these implementations exploit the secondary paths to enhance the maximum frequency, they do not present a tuning range enhancement per se. Fixed feedforward inverters increase the minimum oscillation frequency (f_{min}) while a constant main loop prevents f_{min} reduction [26]. The latter implies that a proper legacy multi-protocol operation using these architectures might employ frequency dividers that increase the overall power consumption and integration costs.

A preferable tuning range enhancement that covers kHz-to-GHz ranges might employ separated controls for core and auxiliary loops. Also, a proper clock source design must ensure a monotonic behavior and avoid possible latch-ups due to auxiliary feedforward paths. To implement the secondary feedforward paths as a proper tuning range enhancement technique, this work illustrates a simulation-based and piece-wise frequency response analysis of digital-based feedforward differential ring oscillators (FDROs). We present a 100kHz-to-1.5GHz FDRO design approach with independent core and feedforward controls by implementing the piece-wise approach. Contrary to conventional implementations [5, 68], the FDRO controls the feedforward strength through variable core and feedforward delay cells. Compared to state-of-the-art works, the proposed FDRO achieves the largest reported tuning range $N_{osc} = f_{max}/f_{min} = 15000$, generating output frequencies on the kHz-to-GHz range. The post-layout performance illustrates a 3.1ps@1.25GHz RMS jitter and a 5mW@1.5GHz total power consumption. The proposed architecture is implemented in a 12-track standard cell format of a 180nm CMOS technology, occupying an area of $0{,}05mm^2$.

This chapter extends the discussion presented in [2]. Here, we extend the feedforward oscillators' mathematical analysis by presenting a piece-wise-based approach to predict the output oscillation frequency. Also, we implement these mathematical results within our 15000 tuning range FDRO design to extract optimum feedforward strength values. For that reason, this paper is organized as follows: Section 3.3 presents latch-up constraints presented in feedforward ring oscillators. To avoid an inappropriate selection of secondary inverters, Section 3.4 presents a frequency response piece-wise analysis for a 4-stage FDRO. Using this piece-wise approach, we can select an optimum feedforward strength to maximize the FDRO tuning range. We also extrapolate our

analysis to 6-, 8-, and 10-stages FDROs. Section 3.5 presents the proposed 4-stages FDRO architecture. The proposed oscillator is implemented in a 12-track standard cell format and it comprises separate current controls for main and auxiliary inverters to maximize the tuning range. Section 3.6 shows the oscillator performance and comparison against previous state-of-the-art clock sources. Finally, Section 3.7 summarizes this work and the proposed oscillator results.

3.3. Limitations in Feedforward Paths: Simulation-based Approach

A feedforward ring oscillator consists of a conventional N-stages oscillator core with auxiliary inverters within the main ring chain. Fig. 29 a) shows a 4-stage differential architecture example, highlighting the feedforward delay cells in *(*red). Note that an arbitrary differential output V_{i+1} now depends on the previous phases V_{i-1} and V_i. In general, we can extract an equivalent differential delay-cell circuit described in Fig. 29 b) [3]. Due to this dependence, feedforward strength α will modify FDRO output frequency and phase difference between delay cells. Although designers exploit feedforward strength to increase oscillation frequency up to four times [5, 62], an inappropriate α value can generate undesirable latch-up states and disrupt the oscillator's monotonicity [26]. This section presents a study of how the feedforward strength α and cross-coupled inverters influence overall phase-shift and oscillation frequency, alongside the possible α values that can generate a non-monotonic behavior. The cross-coupled strength is defined as the aspect ratio between the cross-coupled (*grey*) and core inverter cells [2].

The inclusion of the cross-coupled and feedforward strengths affects the differential ring

---

[3] Core delay-cells comprise core and cross-coupled inverters.

oscillator (DRO) oscillation frequency and phase difference between the delay cells. Regarding the 4-stages FDRO particular scenario, the output frequency might rise with α until the phase between delay-cells change [26]. To determine the effects of α and β on the oscillation frequency, Fig. 30 depicts simulation results for Fig. 29 a) architecture as a function of both strengths. We can control the values of α and β by modifying the internal inverters' aspect ratio. f_{osc} is proportional to α and increases linearly up to four times. Still, the FDRO enters a latch-up state ($f_{osc} = 0$) after a maximum frequency is reached. Also, note that β defines the maximum α bound before a latch-up.

Simulation results in Fig. 30 suggest that undesired values for the feedforward and cross-coupled strength might produce a latch-up and stop the system oscillation. Since secondary loops directly modify the delay cells' phase contributions, a zero oscillation frequency occurs as each of Fig. 29 a) complementary nodes are in phase. Fig. 31 a) and Fig. 31 b) show two possible delay-cell phase contribution ($\theta = -45°, \theta = -270°$) phasor diagrams for a 4-stages FDRO architecture. Fig. 31 a) describes a normal operation where each delay cell contributes $-45°$ of phase. On the other hand, Fig. 31 b) operation reveals that the differential output is canceled despite each single-ended node still oscillating. Although a simulation-based methodology might extract α and β values to achieve a particular f_{osc}, a wide tuning range implementation requires appropriate minimum and maximum bounds for feedforward and cross-coupled strength to avoid latch-up states and monotonicity disruption. To determine α and β suitable ranges, the next section presents a mathematical approach to quantify feedforward and cross-coupled influences in f_{osc} and FDRO phase-difference.

Figura 29

a) Schematic of a conventional 4-stage DRO with additional feedforward delay cells (red). b) Equivalent circuit of a delay cell including the core, feedforward (red), and cross-coupled (grey) inverters.

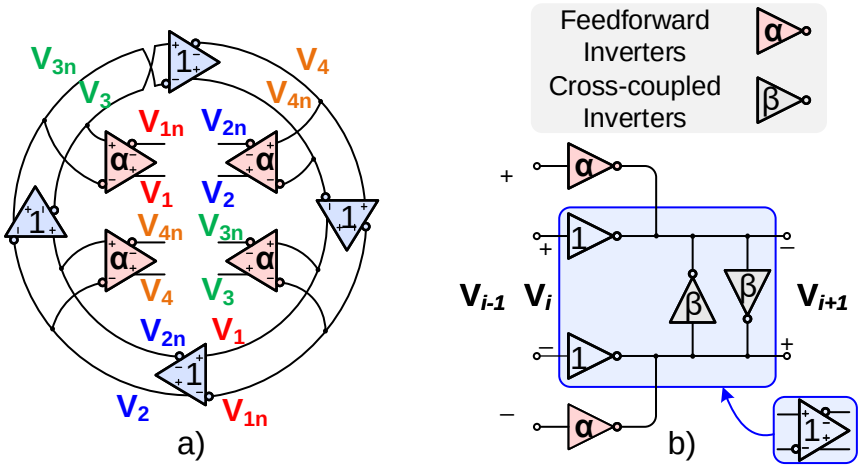
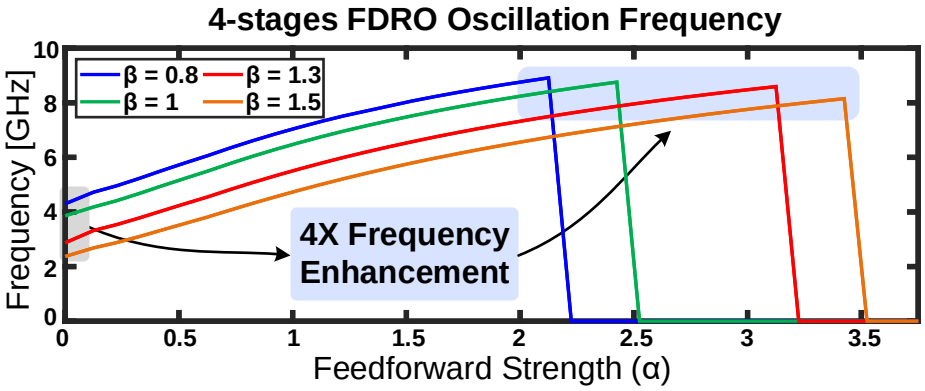


Figura 30

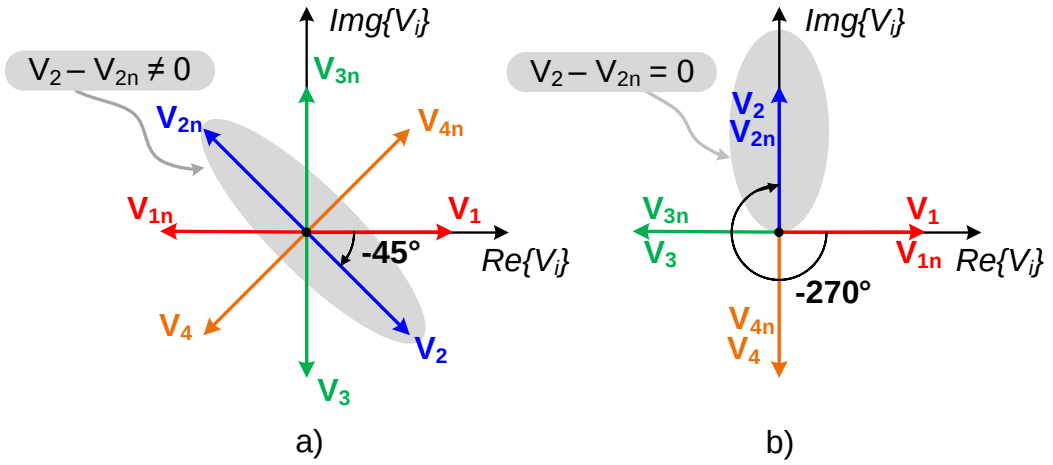
Simulation results for a conventional 4-stages FDRO (see Fig. 29) using regular inverter cells. The main inverter's width is 890nm and L=180nm for all transistors. No PVT variations were considered.



3.4. Analysis and Validation of Feedforward and Cross-coupled Influence

Despite feedforward and cross-coupled strengths modifying the oscillator's output frequency and delay-cells phase contribution, an RO has a fixed number of possible phase shifts, named osci-

Figura 31
4-stages FDRO phasor representations of two possible delay cell's phase contribution: a) -45°, b) -270°.



llation modes, around the loop [53]. In general, an oscillation mode is a delay-cell phase difference that satisfies the -360° total phase shift around the oscillator's main loop. For instance, equation (3) describes all possible oscillation modes for an N-stage DRO. Among those possible modes, the DRO oscillates with a unique phase-shift named dominant mode (DM) [53]. However, some oscillation modes might prevent the DRO from oscillating as illustrated by Fig. 31 b) phasor diagram. In this case, all 4-stages complementary outputs remain in phase, generating a differential latch-up ($f_{osc} = 0$). This section presents a piece-wise frequency response analysis to predict how feedforward and cross-coupled strengths influence all possible oscillation modes.

$$\theta_k = \frac{-360 \cdot k}{2N}; \qquad \{k \in \mathbb{N} \mid k < 2N \;\&\; k \neq N\} \tag{3}$$

3.4.1. Unit Delay-Cell Analysis for a 4-Stages FDRO

As mentioned before, a DRO oscillates at a singular oscillation mode named the dominant mode. Normally, multiple oscillation modes' analysis is not considered as only one phase-shift achieves the oscillation Barkhausen criteria [26]. However, the frequency drop in Fig. 30 suggests a change in the phase shift and so in the DM. In order to determine α and β influence in the DM, we will evaluate the oscillator's frequency response as a function of feedforward and cross-coupled strengths.

Assuming an N-stages FDRO with all delay cells equal, equation (4) represents the half-symmetrical delay-cell transfer function of the Fig. 29 b) circuit [20, 53]. Where G ($G = g_{mn} + g_{mp}$) is the unitary inverter cell transconductance, R is the unitary inverter cell output resistance, C is the equivalent single-ended V_{i+1} node capacitance, ω is the angular frequency, and θ_k is the phase-difference (oscillation mode) between delay cells. Equation (4) reveals that the cell RC product remains constant despite the feedforward and cross-coupled inverters ($R_{eq} = R/(1+\alpha+\beta)$) and $C_{eq} = C \cdot (1+\alpha+\beta)$). Since equation (3) defines the possible delay cell phase-shifts ($\angle H(\alpha,\beta,\omega) = \theta_k$), we can express the transfer function amplitude and oscillation frequency as equations (5) and (6), respectively; where (7) represents the frequency tangent function argument.

$$H(\alpha,\beta,\omega) = \frac{G \cdot R \cdot \left(1 + \alpha e^{-j\theta_k} + \beta e^{j\theta_k}\right)}{(1+\alpha+\beta) \cdot (1 + j\omega RC)} \tag{4}$$

$$|H(\alpha,\beta)| = \frac{G \cdot R}{1+\alpha+\beta} \cdot \sqrt{\frac{1 + (\alpha+\beta)^2 + 2(\alpha+\beta)\cos(\theta_k)}{1 + \tan^2(\phi_k(\alpha,\beta))}} \tag{5}$$

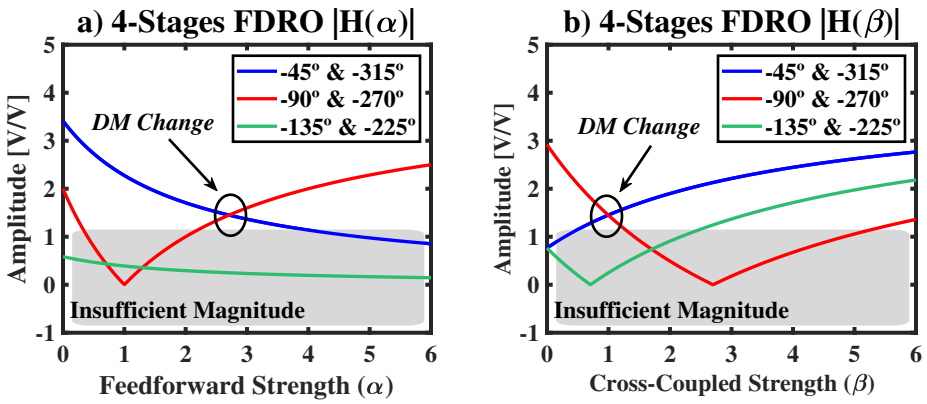
$$f_{osc}(\alpha,\beta) = \frac{\tan(\phi_k(\alpha,\beta))}{2\pi RC} \tag{6}$$

$$\phi_k(\alpha,\beta) = \angle\{1 + \alpha e^{-j\theta_k} + \beta e^{j\theta_k}\} - \theta_k \tag{7}$$

Notice that each oscillation mode will produce its oscillation frequency and transfer function amplitude. Fig. 32 a) illustrates the transfer function amplitude for a 4-stage FDRO, as a function of α. We consider a DC gain of $G = 12dB$, a single pole $1/RC = 1{,}325Grad/s$, and a fixed cross-coupled strength $\beta = 1$. Despite the feedforward strength, *green* oscillation modes do not fulfill Barkhausen criteria for any α value. In contrast, *blue* and *red* phase differences produce amplitudes greater than one. According to the oscillation modes theory, an N-stages oscillator DM sets the highest transfer function amplitude [53].

Fig. 32 a) results reveal a DM change at $\alpha = 2{,}7$. Since some θ_k share the same amplitude plots, amplitude analysis is still insufficient to determine the unique DM as a function of α. However, Section 3.3 simulations provide an insight of $\theta_1 = -45^\circ$ and $\theta_6 = -270^\circ$ as the dominant oscillation modes for $\alpha < 2{,}7$ and $\alpha \geq 2{,}7$, respectively. Regarding the cross-coupled strength effect, Fig. 32 b) shows the 4-stages FDRO transfer function amplitude as a function of β. We keep the same G and $1/RC$ parameters and a fixed $\alpha = 2{,}7$ to determine if β changes the DM switching point. Similar to Fig. 32 a), the DM change occurs when $\alpha = 2{,}7$ and $\beta = 1$. Fig. 32 b) reveals that *red* curve sets the dominant mode for $\beta \leq 1$ whereas *blue* curve defines it for $\beta > 1$. The latter amplitude analysis matches with Fig. 30 simulations as the latch-up point moves to the right as β

Figura 32
a) Delay-cell TF amplitude vs feedforward strength. $\beta = 1$ for all α values. b) Delay-cell TF amplitude vs cross-coupled strength. $\alpha = 2{,}7$ for all β values.

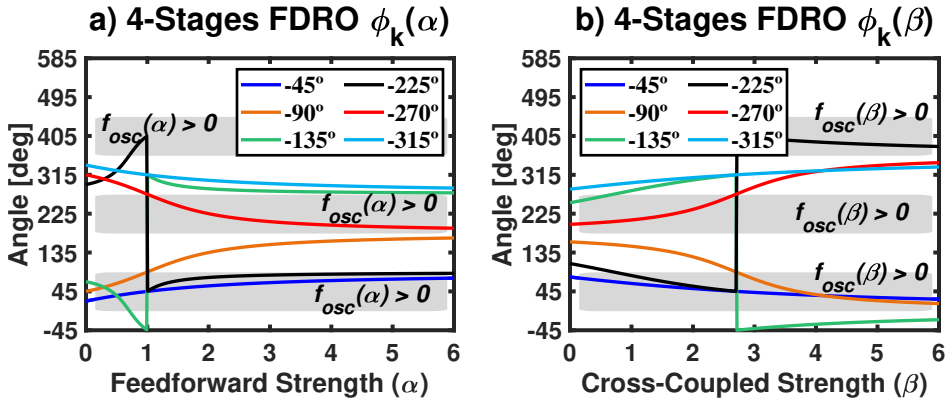


increases.

In Fig. 32, amplitude curves can determine dominant mode changes as functions of α and β. Still, there is no certain dominant mode for every feedforward and cross-coupled strength value. According to equation (6), some oscillation modes can generate negative frequencies depending on ϕ_k values. The dominant mode has to generate a positive oscillation frequency while maintaining $|H(\alpha,\beta)| > 1$. To generate a positive oscillation frequency, ϕ_k must be inside the first or third cartesian plane quadrants. Fig. 33 a) depicts ϕ_k as a function of feedforward strength, maintaining a fixed cross-coupled strength of one. Fig. 33 a) results show that $\theta_1 = -45°$ generates a positive frequency for every α, whereas ϕ_6 is inside the fourth quadrant. From Fig. 32 a) and Fig. 33 a), we can determine that $\theta_1 = -45°$ is the dominant oscillation mode for $\alpha < 2{,}7$. We can apply the same analysis for $\alpha \geq 2{,}7$ interval. For this case, $\theta_6 = -270°$ shows the greatest amplitude value with ϕ_6 always in the third quadrant, resulting in the only DM valid solution.

Fig. 33 b) illustrates the cross-coupled strength influence in ϕ_k. Notice that $\theta_1 = -45°$ and

Figura 33
a) Delay-cell ϕ_k vs feedforward strength. $\beta = 1$ for all α values. b) Delay-cell ϕ_k vs cross-coupled strength. $\alpha = 2{,}7$ for all β values. Grey bands highlight the first and third cartesian plane quadrants.



$\theta_6 = -270°$ generate positive oscillation frequencies for $\beta < 3$. Since Fig. 32 b) reveals a DM change at $\beta = 1$, we can define $\theta_6 = -270°$ and $\theta_1 = -45°$ as the dominant oscillation modes for $\beta < 1$ and $\beta \geq 1$, respectively.

3.4.2. Differential Latch-ups Effects in the Oscillation Frequency

The presented $|H(\alpha,\beta)|$ and $|\phi_k(\alpha,\beta)|$ analyses can estimate the dominant mode for every feedforward and cross-coupled strength value. Fig. 30 simulations match with Fig. 32 and Fig. 33 behavior. Still, equation (6) is not able to properly predict the differential oscillation frequency. As Fig. 31 b) shows, $\theta_5 = 270°$ generates a differential latch-up and stop differential oscillation. In contrast, equation (6) produces a positive oscillation frequency for $\theta_5 = 270°$. Since equation (4) is the half-symmetrical transfer function for the unit delay cell [20], equations (5) and (6) only consider single-ended outputs and despise undesirable complementary outputs effects.

To consider differential latch-up effects, we must evaluate all the oscillation modes where each complementary output pair is in phase. For FDRO on Fig. 29 a), $\theta_3 = -90°$ and $\theta_6 = -270°$

can generate differential latch-ups. In a more general way, a differential latch-up occurs when total phase around half of the loop is $-360°$. Even k values will produce a $-360°$ total phase around half of the loop and a differential latch-up. As a result, we can define equation (8) as the *forbidden* (f_b) oscillation modes associated with unwanted differential latch-ups. Based on equations (3) and (8), we can define a piece-wise approach for differential oscillation frequency as equation (9) shows, including the effects of the forbidden modes.

$$\theta_{f_b} = \frac{-f_b \cdot 360}{N}; \qquad f_b = \{1, 2 \ldots N-1\} \tag{8}$$

$$\begin{cases} f_{osc}(\alpha,\beta) = \frac{\tan(\phi_k(\alpha,\beta))}{2\pi RC} & \{k \neq 2n\ ,\ n \in \mathbb{N}\} \\ \\ f_{osc}(\alpha,\beta) = 0 & \{k = 2n\ ,\ n \in \mathbb{N}\} \end{cases} \tag{9}$$

3.4.3. Piece-Wise Approach Performance

To validate our piece-wise frequency approach, we implemented several differential ring oscillators with a different number of stages in a 180nm CMOS standard technology. We extracted the delay-cell parameters (DC gain and pole frequency) to compare our analysis with simulation results. Similar to the previous section, all transient Spectre simulations were made with a cross-coupled strength $\beta = 1$, a DC gain of 12dB, and a single pole $1/RC$ value of 1.325 $Grad/s$. The dimensions of the selected standard inverter were $W_n = 890nm$ and $W_p = 1{,}76\mu m$ to achieve a

switching point close to half of the supply. The simulation setup considers only nominal conditions with no mismatches between the cells. We controlled α by changing the transistors' width of feedforward inverters.

Fig. 34 a) illustrates the piece-wise oscillation frequency and simulations comparison of a 4-Stages FDRO. For $\beta = 1$, $|H(\alpha,\beta)|$ and $|\phi_k(\alpha,\beta)|$ curves can predict the DM change at $\alpha = 2{,}7$. As Fig. 33 previously predicted, an increase in the cross-coupled strength moves the DM change point to the right. Although the piece-wise frequency, $|H(\alpha,\beta)|$, and $|\phi_k(\alpha,\beta)|$ analyses provide a proper estimation for the oscillation frequency and the dominant mode change, there exist some shape discrepancies between the model and the simulation since equation (4) considers delay cell transistors always in saturation.

We verify our piece-wise oscillation frequency approach for 6-, 8-, and 10-Stages FDROs, as Fig. 34 b) depicts. In terms of the phase shift, the dominant mode for each oscillator is $-30°$, $-22{,}5°$, and $-18°$, respectively. Note that the piece-wise frequency estimation approaches Spectre simulations as the number of stages increases [20]. After a proper understanding and analysis of feedforward and cross-coupled strengths' effects, designers can extract optimum α and β values to maximize the FDRO tuning range and prevent any possible forbidden oscillation mode.

3.5. Proposed 15000 Tuning Range FDRO Architecture and Circuit Implementation

Reported high-tuning range ring oscillators usually employ variable resistors within delay cells to change the RC time constant and enhance their overall frequency range [59]. Although trimming elements can create tuning ranges > 9.5M, these architectures suffer from the rise of the maximum demanded frequency in recent SOC applications (Fig. 28) since the pole associated with

Figura 34

a) Simulation results and piece-wise approach comparison for a 4-Stages FDRO. b) Simulation results and piece-wise approach comparison for 6-,8-, and 10-Stages FDROs.

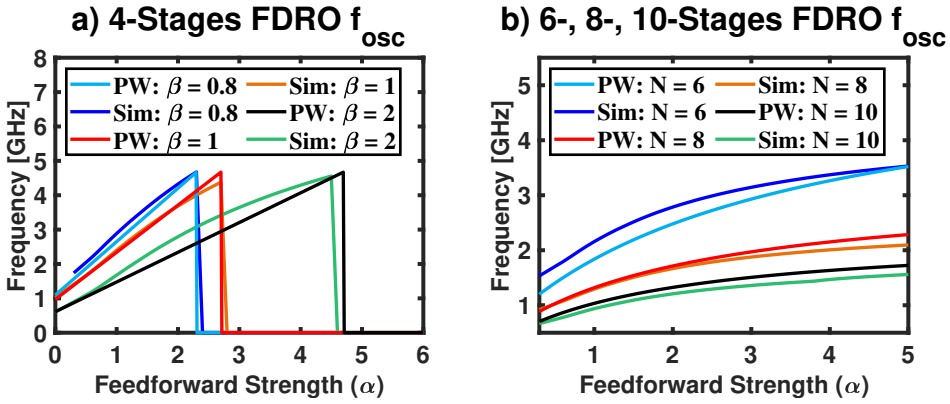
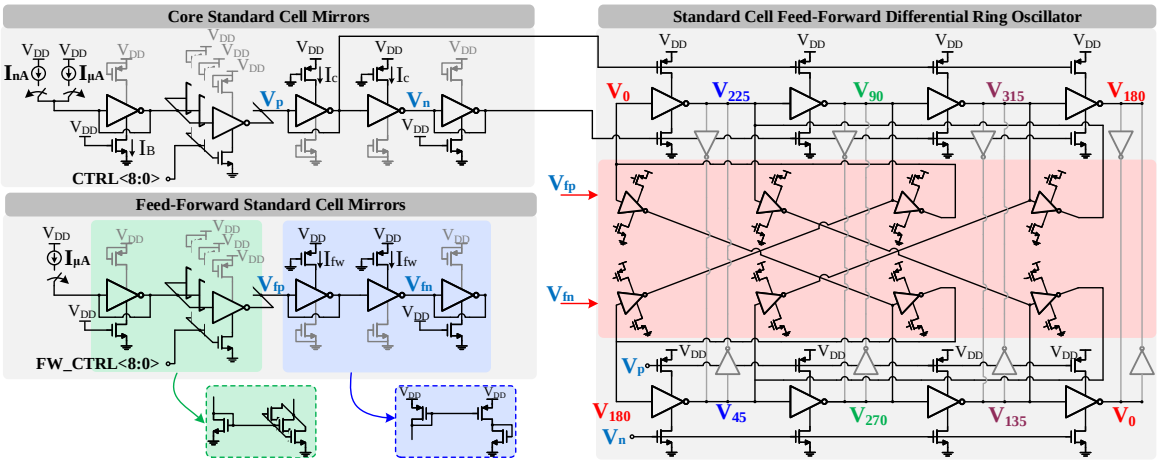


Figura 35

Proposed current-steering differential feedforward ring oscillator. core, Feedforward (red), cross-coupled inverters, and current mirrors were implemented using tri-state inverters. Blue and green dashed boxes highlight the analog equivalent N- and P-type current mirrors, respectively.



the series resistance implicitly enhances the overall time constant. Also, PVT variations among the stages can contribute to additional undesired phase differences in differential ring architectures, while designers might require heavy custom layout techniques to implement desired variable resistances [59]. A standard-cell format implementation, that can avoid using variable resistances,

will guarantee scaling and reproducibility in more recent technology nodes.

The proposed flow to design the FDRO consists of, first of all, designing only the core to oscillate at its maximum operating frequency. In our case, we targeted a 1.25Gbps application (Clock and Data Recovery circuit with 4 lanes for USB 3.0 compliance). Consequently, we designed the core to achieve a maximum oscillation frequency of half of the target frequency, which is 625MHz. Then, we designed the feedforward inverters to achieve the largest operating frequency. In this case, the maximum operating frequency with the feedforward activated was 1.5GHz with an α of 1.5. For $\alpha \geq 1.5$, we observed that the latch-up behavior prevented the FDRO from oscillating, thus, we identified the maximum feedforward strength for the circuit. Finally, for the low-frequency range of the FDRO, we decreased the bias current up to the point where the leakage current was considerable and prevented the circuit from oscillating.

The aim of the proposed oscillator is to exploit the secondary feedforward paths to enhance the total tuning range. Fig. 50 illustrates the proposed standard-cell format differential ring oscillator with the tri-state inverter-based bias current mirrors. As Fig. 50 depicts, our proposed oscillator bases its operation on a current-steered delay cell approach. Each differential stage is comprised of two core, feedforward (*red*), and cross-coupled (*light grey*) tri-state inverters. The implementation of these clamped inverters also allows the design of standard-cell current mirrors and achieves a complete 12-track standard-cell format implementation. Core and feedforward digital words ($CTRL$ and FW_CTRL) control two binary weighted mirrors to define I_c and I_{fw}, respectively. Note that the feedforward strength is now defined as the ratio between the two mirror currents $\alpha = I_{fw}/I_c$. Since modifying the cross-coupled inverters does not enhance the overall RO tuning

range (see Sections 3.3 and 3.4), our proposed design comprises a fixed cross-coupled strength of $\beta = 0{,}2$.

3.5.1. Current Steering Feedforward Paths

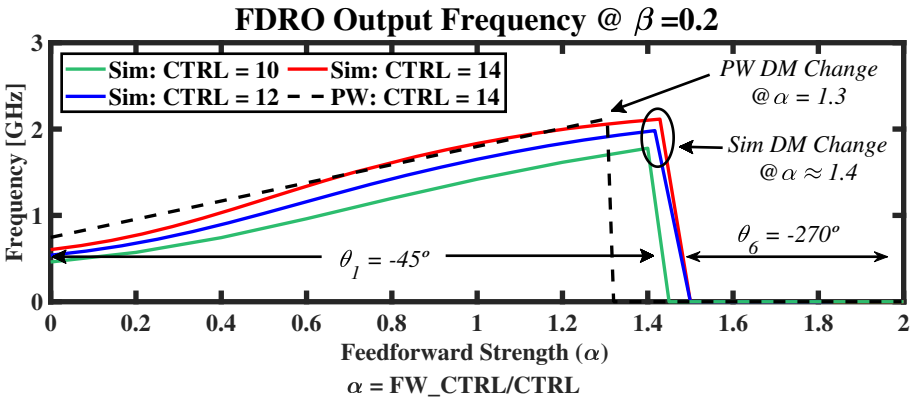
As previously presented, conventional FDROs usually implement either fixed feedforward paths or fixed core inverters [5, 68, 40]. Unlike regular implementations, our proposed approach allows independent calibration of core inverters and auxiliary cells to enhance the overall resolution for legacy protocol support. Still, arbitrary changes in the feedforward strength might cause a phase-shift change and generate a non-monotonic behavior (see Sections 3.3 and 3.4). For a 4-stage DRO case, a high feedforward strength value will generate phase-shift change from $\theta_1 = -45^\circ$ to $\theta_6 = -270^\circ$, causing a latch-up state and disrupting monotonicity. A proper upper bound for the feedforward strength must be determined to maximize the oscillation frequency, and consequently, the tuning range.

The main advantage of having separate controls for main and feedforward inverters is to properly control delay-cell frequency response. Since $CTRL$ word only affects core strength, it modifies equation (4)'s transconductance and RC product. On the other hand, $FW\_CTRL/CTRL$ relation defines the feedforward strength and so ϕ_k. According to the piece-wise frequency analysis, the maximum feedforward strength value only depends on the cross-coupled strength. For $\beta = 0{,}2$ particular case, Fig. 36 piece-wise results predict a constant 45° phase-shift for $\alpha \leq 1{,}3$.

To determine α bounds, Fig. 36 illustrates simulations for the proposed oscillator's output frequency. These simulations consider the proposed FDRO with ideal current mirrors and typical conditions. Notice that independent controls for main and secondary inverters generate a

Figura 36

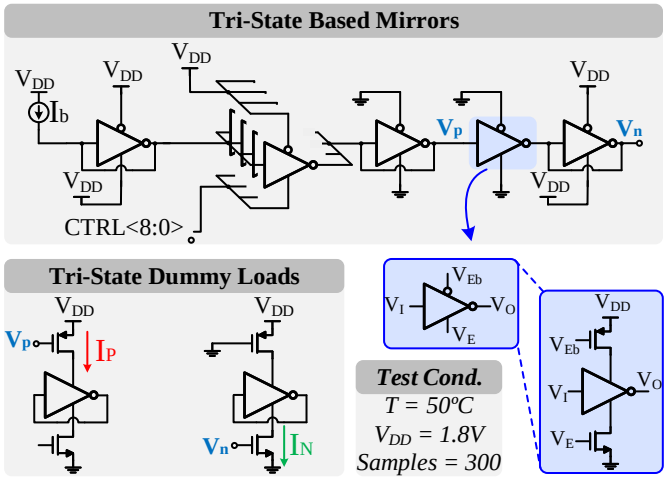
Proposed FDRO simulations for different CTRL and FW_CTRL values. For all simulations, cross-coupled strength remains at 0.2. The three simulations reveal a DM change at $\alpha \approx 1{,}4$.



4X frequency enhancement with no compromises in the oscillator's tuning range. Similar to the piece-wise approach, FDRO simulations reveal that the dominant mode-changing point is almost independent of the feedforward strength. For the three cases, the FDRO enters into a forbidden oscillation mode at $\alpha \approx 1{,}4$. Oscillation mode change discrepancies between piece-wise and simulation results are due to second-order effects presented in tri-state buffers. Still, the piece-wise analysis and the simulation results can give a maximum feedforward strength value of $\alpha_{max} = 1{,}3$.

Comparisons between piece-wise analysis and Fig. 36 simulations reveal that the proposed FDRO achieves a 45° oscillation mode for $\alpha \leq 1{,}3$. We set an $\alpha_{max} = 1$ by enabling the feedforward inverters only while *CTRL* reaches its maximum value. By avoiding a higher feedforward strength, the FDRO can enhance its tuning range and oscillation frequency up to 3X with a constant 45° oscillation mode. Although the FDRO is not able to generate a 4X frequency enhancement due to the selected α_{max}, this maximum feedforward strength gives enough margin to sustain a monotonic operation over the wide tuning range and avoid any oscillation mode change in the circuit.

Figura 37
Standard-cell format tri-state based current mirror test bench. Blue boxes highlight the tri-state inverter gate and schematic equivalents.



3.5.2. Standard-Cell Format Tri-State Based Current Mirrors

The proposed oscillator utilizes two bias sources to supply Fig. 50 standard-cell format current mirrors. It comprises an external $I_{\mu A} = 1\mu A$ and an integrated $I_{nA} = 10nA$ Scaled-Alike Currents Subtraction Source (SACSS) [61]. To maintain the standard-cell format implementations, FDRO current mirrors are designed using the same core and feedforward inverters' cells. We implement the current mirrors using tri-state buffers as Fig. 50 illustrates and validate them using Fig. 37 test-bench. We perform DC simulations to verify the current mirrors' monotonicity and avoid unwanted latch-up states. We used tri-state inverters as dummy loads to emulate an FDRO delay cell. The DC validation considered both $1\mu A$ external source and the 10nA SACSS to evaluate the I_b effect in the mirror's linearity.

To determine the current mirror monotonicity, we evaluate Fig. 37 I_P source and I_N sink

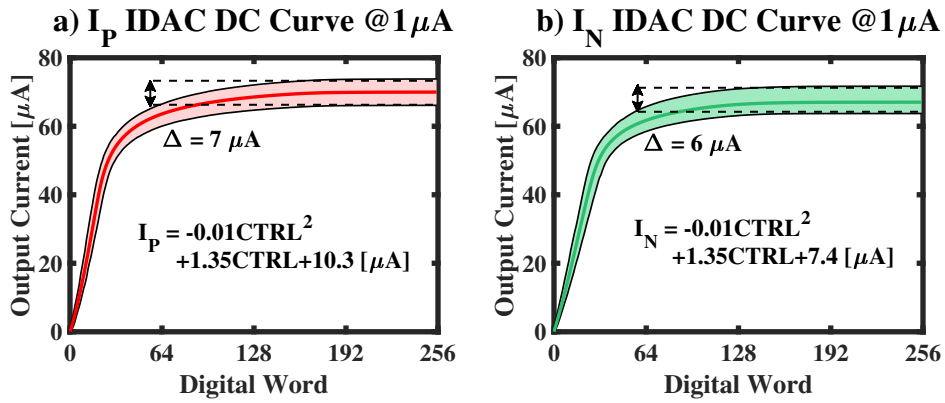
output currents DC transfer curves. Fig. 38 a) and Fig. 38 b) show $I_b = 1\mu A$ simulated DC transfer curve for source and sink outputs, respectively. The tri-state-based approach achieves a linear behavior for lower digital words. For $CTRL \geq 50$, second-order effects start to dominate as tri-state transistors enter into the triode region. Additionally, Fig. 37 *blue* inverter adds a $3\mu A$ systematic leakage error between I_P and I_N. Still, FDRO post-layout simulations reveal that the $3\mu A$ current difference effect in the oscillator's duty cycle is negligible.

Fig. 38 flat regions directly influence the FDRO maximum oscillation frequency. To generate higher output currents, the linear region might be extended by increasing the length of internal transistors. Still, redesigning standard cell layouts might constrain standard-cell format implementation and limit circuit integration. Although current mirrors set a maximum frequency, auxiliary inverters can generate a 3X frequency enhancement. Since main and feedforward current mirrors have the same sizes, $\alpha = I_{fw}/I_c$ relation is not affected by the flattened mirror's curves.

Despite current mirrors being able to control FDRO oscillation frequency, the bias current intrinsically limits the minimum oscillation frequency f_{min} and so the overall tuning range. To decrease the lower bound and maximize the tuning range, the proposed differential ring oscillator splits the operation into three different frequency ranges: 1) Low-frequency range (100kHz $< f_{osc} \leq 4MHz$), where $I_b = I_{nA}$ and the feedforward paths are off. 2) Mid-frequency range (4MHz $< f_{osc} \leq 500MHz$), where the feedforward paths remain off while $I_b = I_{\mu A}$. 3) High-frequency range (500MHz $< f_{osc} \leq 1{,}5GHz$), where the feedforward paths are activated and can boost the maximum frequency up to three times.

The current mirror's random variations set a lower bound for the bias current I_b as output

Figura 38
DC transfer curve of the tri-state based current mirrors using a $1\mu A$ *bias current. a)* I_P *source current. red shaded area highlights DC transfer curve Montecarlo variations over 300 samples. b)* I_N *sink current. green shaded area highlights DC transfer curve Montecarlo variations over 300 samples.*



currents' mismatch might disrupt the oscillator's monotonicity [20]. Fig. 39 a) and Fig.39 b) show $I_b = 10nA$ simulated DC transfer curves for source and sink outputs, respectively. We simulate for $CTRL \leq 100_d$ [4] to keep monotonicity with the $1\mu A$ bias source. These simulations also include SACSS mismatch contributions. As expected, current mirrors mismatch increases compared to Fig. 38 simulations, achieving a maximum variation of $700nA$. Although these variations might disrupt monotonicity, the proposed FDRO is able to generate a monotonic behavior regardless of the maximum current variation.

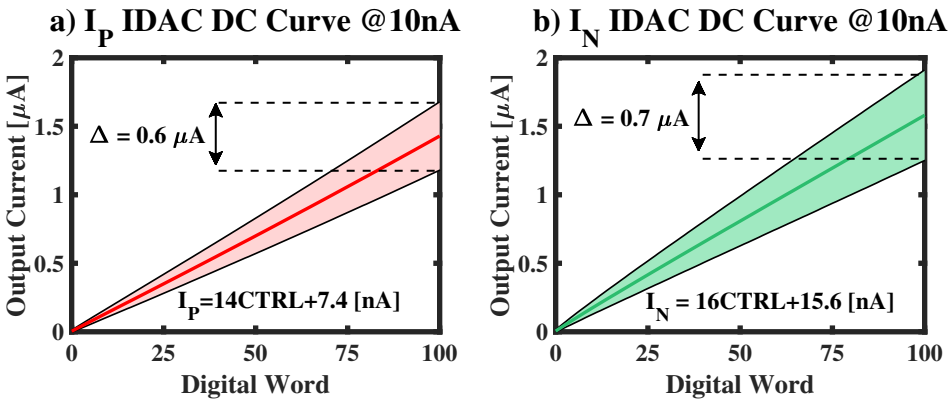
3.6. 15000 Tuning Range FDRO Performance

The proposed 15000 tuning range FDRO was designed in a 12-track 180nm CMOS standard cell format, occupying a 200μm X 180μm area as Fig. 40 layout shows. To improve FDRO

[4] Subscript *d* refers to decimal notation.

Figura 39

DC transfer curve of the tri-state based current mirrors using a 10*nA bias current. a)* I_P *source current. red shaded area highlights DC transfer curve Montecarlo variations over 300 samples. b)* I_N *sink current. green shaded area highlights DC transfer curve Montecarlo variations over 300 samples.*



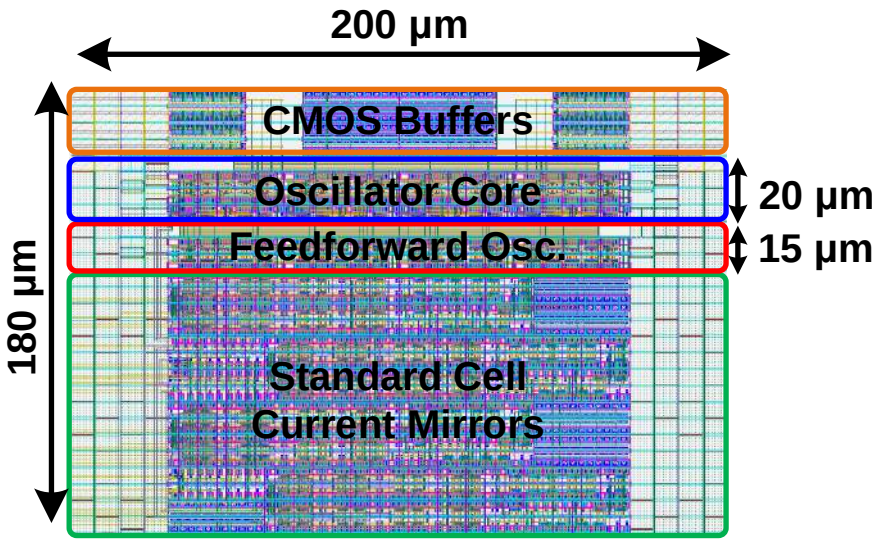
heating reliability, we reduce supply current density by implementing power rails on both sides. We isolate the oscillator core from load effects by an additional CMOS buffer chain. This section presents post-layout simulations over the PVT-bound corners [5] to verify the proposed oscillator performance. All further simulations occur while the FDRO drives a 300fF load to reproduce a CML driver input capacitance.

To evaluate the proposed FDRO tuning range performance, Fig. 41 a) illustrates the post-layout simulations for the low and middle oscillation frequency ranges versus the *CTRL* digital word. We fixed the feedforward strength to 0 while biasing the core current mirrors with I_{nA} and $I_{\mu A}$ depending on the frequency range. When selecting I_{nA} as the bias current, the fastest scenario

---

[5] SSLH corner indicates Slow NMOS – Slow PMOS – Low Supply – High Temperature (worst case). TTNN corner subscript indicates Typical NMOS – Typical PMOS – Nominal Supply – Nominal Temperature (typical case). FFHL corner shows Fast NMOS – Fast PMOS – High Supply – Low Temperature (best case).

Figura 40
Layout of the proposed current-steering FDRO.

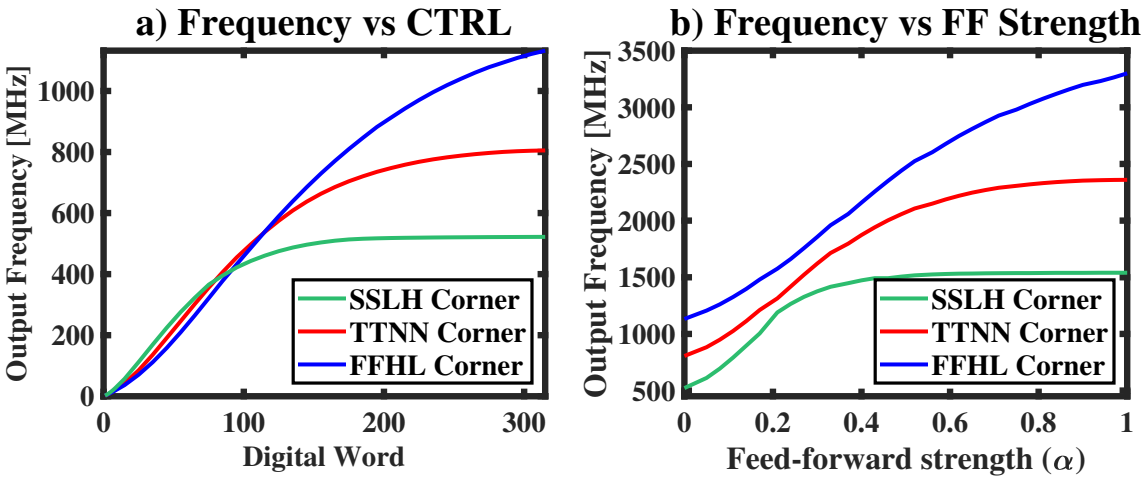


(FFHL corner) achieves a 100kHz minimum frequency. After 4MHz, we change the mirror's bias current and allow the FDRO frequency to rise linearly ($CTRL \leq 100_d$) with a 3MHz/μA resolution. After $I_c \geq 100\mu A$, Fig. 41 a) SSLH curve starts to flatten due to current mirrors' second-order effects. For this slowest scenario, the FDRO acquires a maximum oscillation frequency of 530MHz.

Fig. 41 a) curves expose an asymptotic nature as the core standard-cell mirrors enter the triode region. To overcome these second-order effects, we enable the auxiliary feedforward loops described in Fig. 50 *(red)* while maintaining $CTRL = 300_d$. This setup sets a maximum feedforward strength of 1 to avoid any oscillation mode shifts and a -45° phase difference for all α values. Fig. 41 b) shows the effect of the secondary loops in the oscillation frequency as a function of $\alpha = FW\_CTRL/CTRL$. The feedforward paths boost by 3X the maximum oscillation frequency up to 1.5GHz@SSLH corner. Notice that the Fig. 41 a) asymptotic behavior also occurs in Fig.

Figura 41

a) Proposed FDRO output frequency vs CTRL word over the slowest (SSLH), typical (TTNN), and fastest (FFHL) corners. b) Proposed FDRO output frequency vs the feedforward strength over the slowest (SSLH), typical (TTNN), and fastest (FFHL) corners.



41 b) post-layout results as the feedforward inverters are also biased with standard-cell format current mirrors. After $\alpha = 0{,}27$, the SSLH corner curve starts to flatten. The latter suggests that analog current mirrors, avoiding the standard-cell format constraints, might implement custom-sized transistors to improve the current mirror's linearity and enhance the maximum FDRO output frequency.

To evaluate possible layout mismatches presented in the standard-cell format implementation, Fig. 42 shows the 1.5GHz transient simulations at steady-state operation. Simulation results reveal the worst phase error of 1.4° between $(V45 - V225)$ and $(V90 - V270)$. Note that the phase difference between the cells remains constant as the $\alpha_{max} \leq 1$ prevents any oscillation mode change and maintains Fig. 31 a) operation. Fig. 43 a) and Fig. 43 b) illustrate 200 samples of Montecarlo post-layout simulations for 100kHz and 1.5GHz free-running operation, respectively. As expected, a broader output frequency scattering occurs at the low-frequency operation as most SACSS

Tabla 5
Post-Layout Design Performance Summary and State-of-the-art Comparison.

	Chen et. al[5]	Seong et. al[62]	Sun et. al[69]	Chen et. al[6]	Kim et. al[39]	S. Nagam et. al[47]	Gui and Green[25]	**This Work** †
Technology	7nm FinFet	65nm	65nm	180nm	65nm	65nm	180nm	**180nm**
Oscillator Architecture	FDRO	RO	FDRO	FDRO	RVCO	FDRO	CML RO	**FDRO**
Frequency Range	4GHz to 16GHz	2.3GHz to 2.55GHz	2.68GHz to 3.56GHz	1.77GHz to 1.92GHz	485.7MHz to 1.0116GHz	1.97GHz to 2.75GHz	2.2GHz to 2.7GHz	**100kHz to 1.5GHz**
N_{osc}	4	1.11	1.33	1.085	2.08	1.4	1.22	**15000**
PN [dB] ($\Delta f = 10MHz$)	-120.00	-125.10	-120.00	-123.4	-110.8 @1MHz	-124.00	-92.83 @1MHz	**-90.00**
RMS Jitter [ps]	0.15@16GHz (100kHz - 1GHz)	0.32@2.55GHz (1kHz - 100MHz)	N.A	N.A	N.A	0.63@2.75GHz (1kHz - 100MHz)	8@ 16GHz (10kHz - 10MHz)	**110@1.25GHz (100Hz - 100MHz)**
Area [mm^2]	0.105	0.055	0.0017	0.0024	0.022	0.022	N.A	**0.05**
Supply Voltage [V]	0.8 to 1.2	1.2	1	1.8	1	0.935	1.8	**1.6 to 2**
Power [mW]	48	6	3.23	13	10	5.86	10.1	**5***
FOM [dB]$^{\boxtimes}$	167.27 @16GHz	164.92 @2.4GHz	164.7 @3.11GHz	157.22 @1.77GHz	157 @900MHz	165.08 @2.75GHz	129.63 @2.5GHz	**120.87 @1.25GHz**

†Simulated worst PVT-corner ; *Not considering the buffer chain

$^{\boxtimes}$ FOM $= |PN| + 20\log_{10}\left(\frac{f_o}{\Delta f}\right) - 10\log_{10}\left(\frac{P_{dc}}{1\text{mW}}\right)$; $\Delta f = 10$MHz

transistors operate in weak inversion [61]. Note that the proposed FDRO achieves a $\sigma_R = 0{,}12$ relative standard deviation at 100kHz, whereas the high-frequency range reaches a $\sigma_R = 0{,}02$ relative standard deviation.

Fig. 44 illustrates the post-layout simulations for the phase noise performance over the boundary corners while running at 1.25GHz. For all the bound cases, the FDRO achieves a ¡-110dBc/Hz @FFHL plain lap. We obtained a maximum RMS jitter of 41ps@FFHL over the 100Hz-100MHz interval.

Table 5 compares the post-layout results of our proposed 15000 tuning range oscillator with recent works. We focus our comparison on the frequency range and in the relation $N_{osc} = f_{max}/f_{min}$. As described before, the proposed oscillator achieves an N_{osc} of 15000 with a frequency range of

Figura 42

1.5GHz transient response for a) TTNN, b) SSLH, and c) FFHL during the steady-state operation. Red, Blue, Green, and Orange curves represent $V0-V180$, $V45-V225$, $V90-V270$, *and* $V135-V315$ *outputs, respectively.*

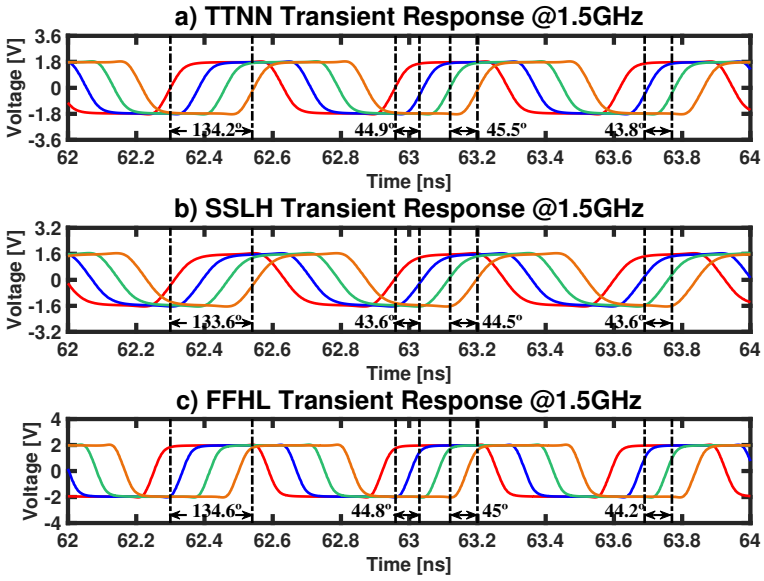
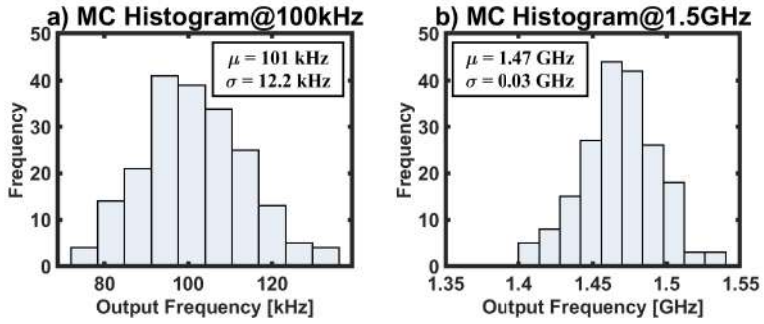


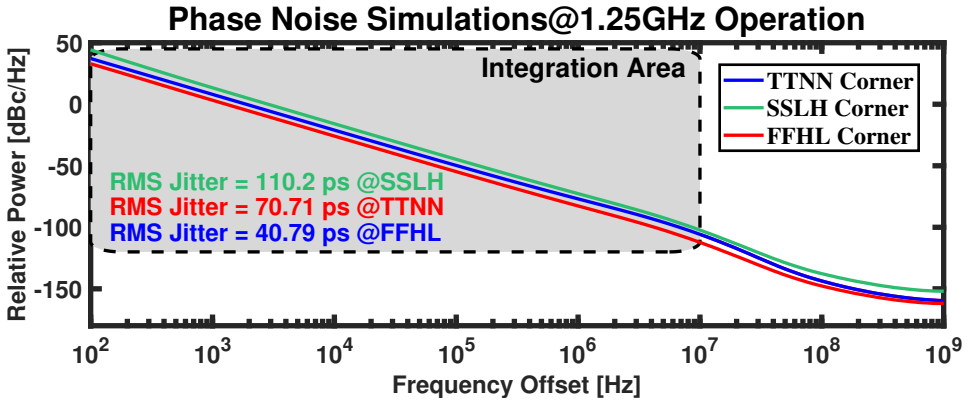
Figura 43

200 Samples Montecarlo post-layout simulations@TTNN corner for a) 100kHz operation and b)1.5GHz operation.



100kHz to 1.5GHz while consuming a 5mW@1.5GHz power consumption. Also, the oscillator achieves a low power operation at 100kHz and consumes 0.12mW. Regarding the area of our proposed approach, note that the auxiliary paths comprise only 8% of the total oscillator while allowing a 3X overall frequency and tuning range enhancement. Therefore, by adding these se-

Figura 44
Phase noise simulations @1.25GHz. Simulations were performed up to 12.5GHz to include the 10 first harmonics.



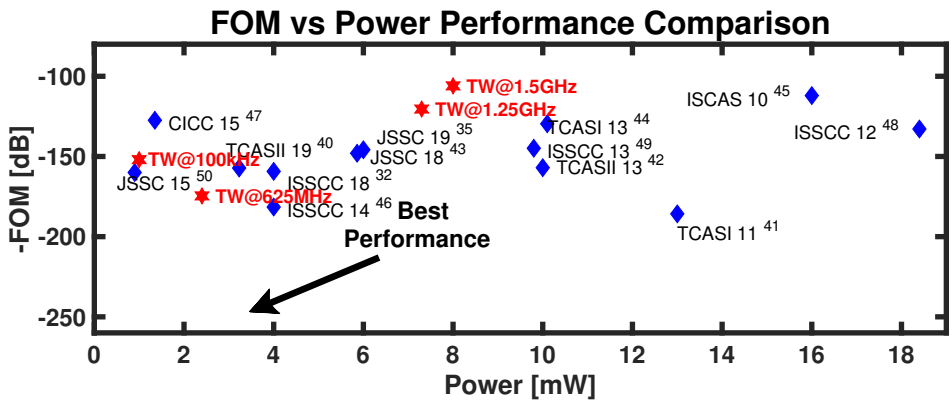
condary feedforward paths with separate and independent current mirrors, our proposed approach achieves the highest reported frequency range with minor area detriments.

Table 5 and Figure 45 present the traditional figure of merit (FOM) based on both phase noise and power consumption. We limit our discussion to ring oscillator architectures and discard LC oscillators for adequate comparison. Figure 45 presents the results of the FoM against power consumption for different works [5, 6, 7, 10, 17, 39, 46, 47, 60, 62, 69, 73]. Among the results, we identify that our work achieves two of the best FoMs at 625MHz and 100kHz while achieving a good compromise for power consumption with the results at 1.25GHz and 1.5GHz operation.

3.7. Summary

This work presents a 100kHz-to-1.5GHz 15000 tuning range scalable FDRO capable of covering legacy multi-protocol support applications. By offering independent controls for main and secondary delay cells, the proposed oscillator can enhance by 3X the maximum oscillation frequency while reaching an $f_{min} = 100kHz$@FFHL corner. Optimum feedforward strength values

Figura 45
FOM Comparison against state-of-the-art clock sources.



and possible constraints are presented by a piece-wise frequency response analysis. Although we utilize the piece-wise results to perform a design, we extrapolate and validate our model results to conventional 4-, 6-, 8-, and 10-stage differential ring oscillator architectures. The proposed FDRO architecture was designed and implemented in a 12-tack standard cell format 180nm CMOS technology. The post-layout performance reveals a $f_{max} = 1{,}5GHz$@worst case (SSLH corner) while consuming a 5mW corner overall power consumption. The transient simulations illustrate a rail-to-rail output for all bound corners with a 1.4°@1.5GHz maximum phase error. Our proposed architecture reports a 41ps@1.25GHz RMS jitter over the 100Hz-100MHz offset frequency with a -121dB@1.25GHz FOM. Compared to the conventional VCO and divider circuit, the topology presented extends the maximum oscillation frequency of a CMOS technology node up to four times without breaking the standard cell format.

3.8. Contributions of this chapter

- A study and modeling of the feed-forward strength and cross-coupled strength to estimate both oscillation frequency and modes.

- 100kHz-to-1.5GHz (N=15000) tuning range to cover several communication protocols.
- Extrapolation of the model to 4-, 6-, 8-, and 10-stage differential ring oscillator architectures.
- Architecture is designed in a 12-tack standard cell format 180nm CMOS technology for scaling in more recent CMOS technology nodes and reduction of instantiation and verification times.

4. A Phase Noise Model Based on Multi-Loop Control System Theory Applied to Feedforward Ring Oscillators

Previously, we described a piecewise model in a feedforward differential ring oscillator to increase the tuning range in SoC. Based on the results presented, the feedforward technique appears as a suitable technique to extend the operating frequency range of clock sources, while maintaining monotonicity and layout compactness. Moreover, the kHz-GHz frequency range achieved by the feedforward ring oscillator (FFRO) or FDRO might enable us to reduce the number of clock generation sources in SoC.

However, the wideband frequency range is not the only characteristic desirable in SoC clock sources. Another common feature in clock sources is phase noise, which corresponds to the representation in the frequency domain of the ratio between the noise power along the frequency range measured and the carrier power.

Phase noise is one of the main designers' concerns in getting the possibility to reduce the number of clock sources in SoC. Thus, it is highly desirable to model phase noise in FFRO to establish noise limits in SoC and determine the number of legacy support applications that can be fulfilled. In state-of-the-art works, linear and frequency-domain models are developed but considerable mathematical work is a must.

In this chapter, we developed a phase noise approach based on the multi-loop control system theory applied to FFRO. Besides showing a good match between the proposed model and

Spice simulations, the model gives qualitative insights to adjust the extended frequency range with awareness of the phase noise performance.

4.1. A simple approach for phase noise estimation in FFRO

This section describes the phase noise model applied to FFRO using multi-loop control system theory and complemented by the estimation of noise sources in the ring oscillator and the impulse sensitivity function (ISF). The model achieves good accuracy compared to the Spice simulations in a reduced number of steps. Additionally, we identify an ideal region for the FFRO that lets designers achieve a smaller phase noise value compared to the normal operation, where the core is only activated.

4.2. Introduction

Current transceiver architectures satisfy the demand for different communication protocols over a large frequency band to fulfill legacy support applications. As the number of protocols and standards supported by a single system increases, the number of clock sources to accomplish the requirements augments since it is unlikely that one single clock source fulfills several standards' specifications. The latter considerably impacts the area occupied by the frequency synthesizers and raises the time associated with the placement and routing of circuits and system verification. In addition, concerns regarding oscillation frequency, data transfer rates, energy-performance ratio, and noise appear in communication protocols in the frequency operation bands, [58].

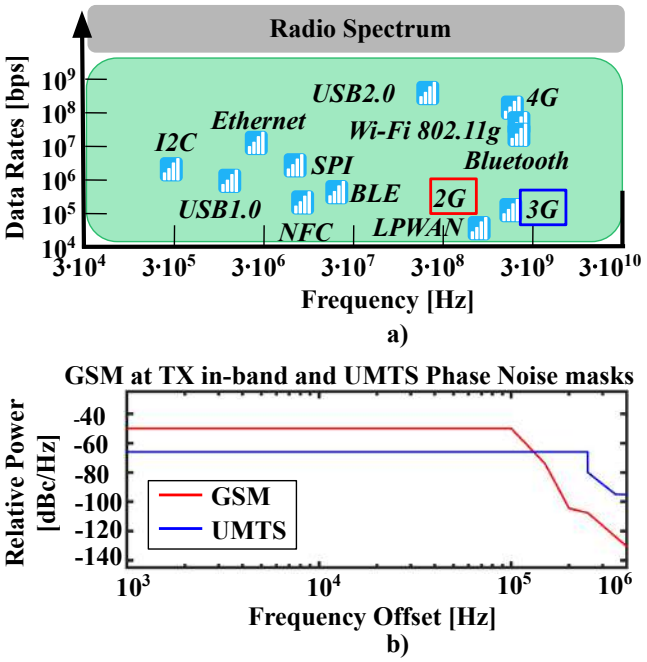
One of the most important constraints in communication protocols is phase noise, which can be represented by communication standards' transmitter and receiver masks, [58]. For example, Fig. 46a) illustrates different communication protocols and technologies associated with the

Radio Spectrum frequency band over a 7-decade frequency range. Among the possible protocols and technologies in the Radio Spectrum, 2G (red) or 3G (blue) are some of the usual communication technologies that could be implemented in a custom transceiver architecture. Fig. 46b) shows the phase noise masks of transmitter in-band GSM and UMTS standards associated with the mentioned 2G and 3G, respectively. It is possible to identify that both standards define different relative powers as the frequency offset increases. The latter confirms the large number of phase noise masks that a single transceiver implementing several protocols might need to satisfy. This leads to the implementation of several clock sources and a consequent increment in design and manufacturing costs. It is worth mentioning that all of the applications associated with the different bands might not work simultaneously, but some bands could operate together. Therefore, the necessity of a clock source that could cluster together several band applications to increase design compactness and efficiency appears.

With the development of new techniques, such as feedforward in ring oscillators, [2, 5, 40, 68], the possibility of a unique clock source operating in a wide frequency band and satisfying several communication standards becomes feasible. Still, a unique frequency reference operating in a wide frequency range might be more susceptible to noise design constraints. This is a serious concern because actual phase noise models imply elaborate calculations adding to the design complexity in both frequency and time domains, [26], and as a consequence, delaying designers' insight. This chapter presents an FFRO model approach based on the multi-loop control system theory for phase noise estimation with a reduced number of steps, as well as the impact of the feedforward strength (α) in phase noise.

Figura 46

In a), we illustrate several technologies and communication protocols with their corresponding data rates in the Radio Spectrum band. In b), we present the GSM at the transmitter (TX) in-band and UMTS phase noise masks associated with 2G and 3G technologies, respectively.



4.3. FFRO Architecture and Noise Performance

As previously mentioned, actual communications systems, for instance, System-on-Chip (SoC), incorporate several frequency synthesizers to fulfill the demand in legacy support applications. Fig. 47a) presents a simplified block diagram of an SoC composed of analog and digital domains, system and peripheral buses for data transferring, and several clock sources. We illustrate a large number of frequency synthesizers (grey) to satisfy the requirements associated with the different communication standard protocols of the SoC. Among the different clock sources, it is possible to identify low-frequency (LF), high-frequency (HF), wide-band (RO), low-energy (RCO), and low-phase noise (LCO) oscillators. To reduce the system's design, verification, and

manufacturing costs, it is desirable to have a unique clock source that might satisfy the demand of all the applications. One possible frequency synthesizer implementation to fulfill the applications' demands might contain an FFRO due to its wide operating frequency range.

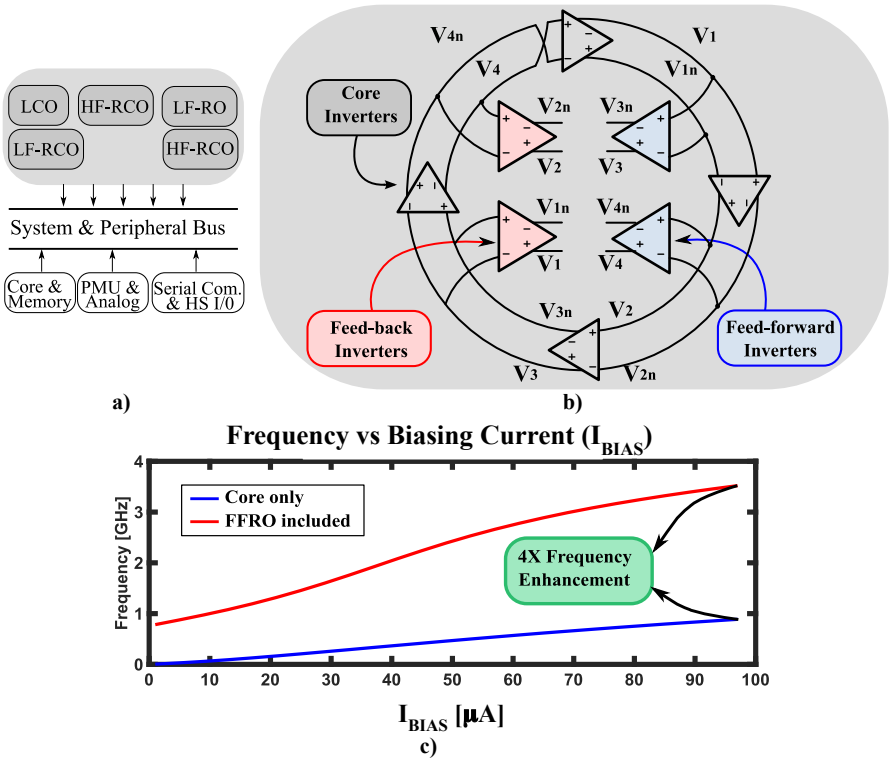
A feedforward ring oscillator consists of a conventional N-stages oscillator core with auxiliary inverters within the main ring chain. Designers adopt the concept of feedforward loops and incorporate the auxiliary inverters to increase the oscillation frequency up to four times, [5, 62]. Fig. 47b) shows a 4-stage differential architecture example with eight differential inverters, each composed of two main tri-state inverter-cells and two additional cross-coupled tri-state inverter-cells, [2].

In Fig. 47c), we present simulation results of the FFRO oscillation frequency described in Fig. 47b) while varying the biasing current I_{BIAS}. Results demonstrate a 4X frequency span enhancement with the inclusion of the FFRO paths to the core. We observe a monotonic behavior for a large digital control word range in both cases.

Yet, there is still a concern regarding phase noise in FFRO. In most state-of-the-art works, FFRO models allow designers to understand the effect of secondary paths on the oscillation frequency. Still, most of these approaches neglect their effect on the oscillator's phase noise [2, 53]. Hafez et al.[26] develop a model based on a modified linear analysis using mathematical and optimization approaches to determine an expression that identifies the main factors to set the oscillation frequency and establish the phase noise values. In spite of the accurate phase noise expression obtained, the proposed algorithm needs considerable mathematical work to set the problem and achieve the solution, thus, implying a time-consuming task. Therefore, the development of a sim-

Figura 47

In a), we illustrate a general SoC block diagram with the different voltage domains, the data transfer buses, and several clock sources. In b), we present a block diagram of a differential 4-stages FFRO with the core and feedforward inverters. In c) simulation results demonstrate a 4X frequency enhancement when we include the feedforward circuit.



ple phase noise model to achieve a correct insight is desirable in FFRO architectures.

4.4. Feedforward Oscillators as Multi-Loop Systems and Noise Model

We developed a phase noise model based on multi-loop control systems theory, [12], which uses simple mathematical expressions to obtain transfer functions from different nodes to the output. For circuit analysis in Fig. 47b), we define phases V_4-V_{4n} as the reference outputs for this chapter. Therefore, it is possible to designate the two inverter cells in *blue* as the feedforward delay cells since the node pair V_3-V_{3n} now depends on the previous V_2-V_{2n} and V_1-V_{1n}, while V_3-V_{3n} and

V_2-V_{2n} condition the phases in V_4-V_{4n}.

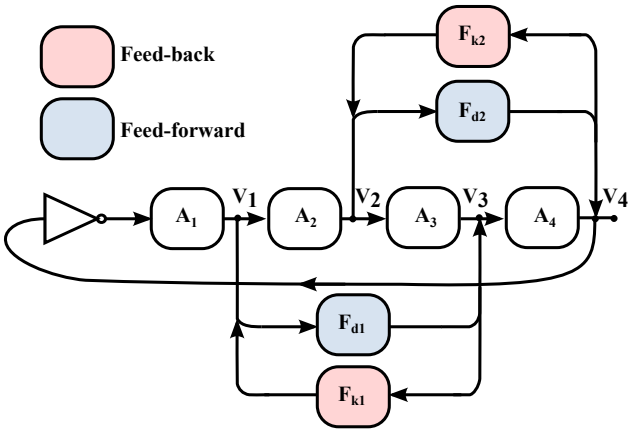
Once V_4-V_{4n} defines the oscillator's main differential output, it is possible to specify the auxiliary inverters in *red* as feedback inverters since their signals' direction opposes the main oscillator's one. Note that the definition of feedback and feedforward cells strictly depends on the reference output.

Fig. 48 illustrates a simplified single-ended block diagram of the feedforward differential ring oscillator schematic in Fig. 47. We set $A_{1\rightarrow4}$, $F_{d1,d2}$, and $F_{k1,k2}$ as the gains of the core, feedforward, and feedback blocks, respectively. Moreover, as mentioned by Arenas et al.[2], the factor α corresponds to the feedforward strength that modifies the FFRO output frequency and phase difference between the core delay cells. We can control α by modifying the auxiliary and core inverters' aspect ratio. The output frequency might rise with α until the phase between delay-cells changes, causing a latch-up state ($f_{osc} = 0$) [26]. For instance, the condition for latch-up was $1{,}3 < \alpha$ in [2].

Fig. 48 lets the authors identify different paths or loops in the diagram from V_1 to V_4 and provides the possibility to implement the multi-loop systems theory for the phase noise calculation.

The proposed flow to estimate the phase noise in an FFRO consists of obtaining the transfer functions from each node to the output node. Then, identify the different noise sources in the unitary delay cell and reference the noises to the output node. Finally, apply the expressions presented by the authors in [19].

Figura 48
presents a simplified block diagram of the feedforward differential ring oscillator with both feed-forward (blue) and feedback (red) blocks. We define the feedforward strength α as the aspect ratio between the feedforward (or feedback) cells and the core cells. An ideal inverter is included before A_1 to represent Fig.47 twisted polarity.



4.4.1. Multi-loop transfer function extraction

As mentioned in section 4.3, we divided the 4-stages differential architecture depicted in Fig. 48 into three main parts: 1) four differential inverter-cells associated with the core, 2) two differential inverter-cells connected in a feedforward configuration, and 3) two differential inverter-cells combined as feedback blocks. Five different loops stand out in the analysis: one main loop associated with the core, two with the feedforward blocks, and two connected through the feedback components.

With the latter, we can implement the multi-loop systems theory reported in [12] to estimate the noise components in each of the delay-cells outputs and consequently reference all the noises to V_4. Mason's signal-flow gain formula presented in (10) determines the transfer function between any two nodes x_i and x_j in a multi-loop control system.

$$T_{ij} = \frac{\sum_k P_{ijk}\Delta_{ijk}}{\Delta} \tag{10}$$

Where P_{ijk} is the gain of the kth path from node x_i to node x_j, Δ_{ijk} corresponds to the co-factor of the path P_{ijk} and Δ represents the determinant of the diagram.

To simplify and reduce (10), we adopt the following considerations: 1) the Δ_{ijk} co-factor is one (1) since all the five loops mentioned above connect in at least one node. 2) We assume that all the component noise sources are uncorrelated. 3) Since all the delay inverter cells are identical, we assume that all the equivalent output noises of the cells are equal. 4) The gain A of all the stages is the same. 5) We used a single-ended block diagram instead of a differential architecture.

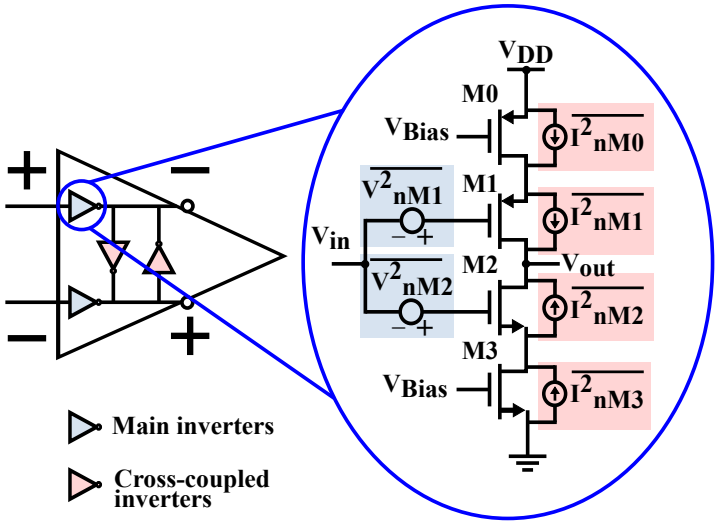
After the previous simplifications, we adopt the multi-loop control system theory to Fig. 48 block diagram. We assume that each one of the eight blocks has an equivalent output noise $N_{i=1\rightarrow 8}$ in their respective output nodes. Consequently, we reference the equivalent output noise sources on the different oscillator nodes to V_4 and obtain an expression for the total output noise. In (11), we present the transfer function between the output V_4 and the power spectrum densities N_i. As expected, the transfer function depends only on A and α, giving a desirable insight for designers.

$$\frac{V_4}{N_i} = \frac{2\{A^3 + A^2[2\alpha+1] + A[\alpha+1] + 1\}}{1 + A^4 + 2\alpha A^2[2A+\alpha]}_4 \tag{11}$$

---

[4] Note that the gain A can be obtained as a function of the current mirrors set up through Spice simulations.

Figura 49
Differential delay cell with two main and two cross-coupled inverters. For each of those inverters, we considered the flicker noise sources (blue) and the thermal noise sources (red) for noise and phase noise analysis.



4.4.2. Derivation of the noise sources and phase noise model

Once the multi-loop control theory presented in section 4.4.1 obtains a transfer function between any node and the FFRO output, we present a noise analysis and subsequently determine the output phase noise of the architecture.

The main sources that we considered in the noise analysis are the channel thermal noise and the flicker noise of the input transistors. Then, we reference the noise sources to the output of each differential cell and consequently transfer all the noise sources to the main oscillator output V_4, as presented in (11), for later calculation of phase noise spectrum, [19]. It is important to mention that we multiply the flicker and thermal noise expressions by the square of the transfer function in (11) to obtain the corresponding phase noise expressions.

We present the thermal noise (12) and flicker noise (13) expressions for both NMOS and PMOS transistors.

$$\left(\frac{i_n^2}{\Delta f}\right)_{th} = 4kT\gamma_N g_{dsN} + 4kT\gamma_P g_{dsP} \tag{12}$$

$$\left(\frac{i_n^2}{\Delta f}\right)_{F} = \frac{K_P g_{mP}^2}{C_{OX} W_P L_P f} + \frac{K_N g_{mN}^2}{C_{OX} W_N L_N f} \tag{13}$$

Once we identify the main noise sources in Fig. 49, we convert the noise to phase noise spectrum using (14), [19].

$$S_{\phi_f} = (\frac{c_n f_0}{f})^2 \cdot S_n(f) \tag{14}$$

Where $S_n(f)$ is (12) or (13), depending on the noise to evaluate and c_n takes different expressions for thermal (15) and flicker noise (16), [44].

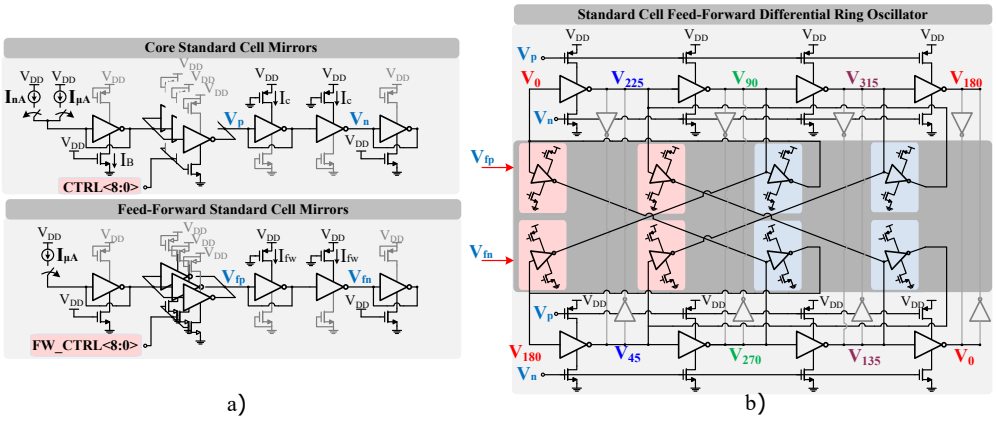
$$c_W = \sqrt{\frac{1}{T_0}\int_0^{T_0} \Gamma^2(\tau) \cdot d\tau} \tag{15}$$

$$c_F = \frac{1}{T_0}\int_0^{T_0} \Gamma(\tau) \cdot d\tau \tag{16}$$

Regarding the cross-coupled inverters, they are commonly placed to guarantee a proper counter phase between their differential outputs. Their size ratio and influence can be modeled

Figura 50

Proposed current-steering differential feedforward ring oscillator. The core, feedforward (blue), feedback (red), cross-coupled inverters, and current mirrors were implemented using tri-state inverters.



using the same methodology as α (named cross-coupled strength). Still, as their effect is much lower compared to α, this paper mostly focuses on the influence of the conventional feed-forward strength.

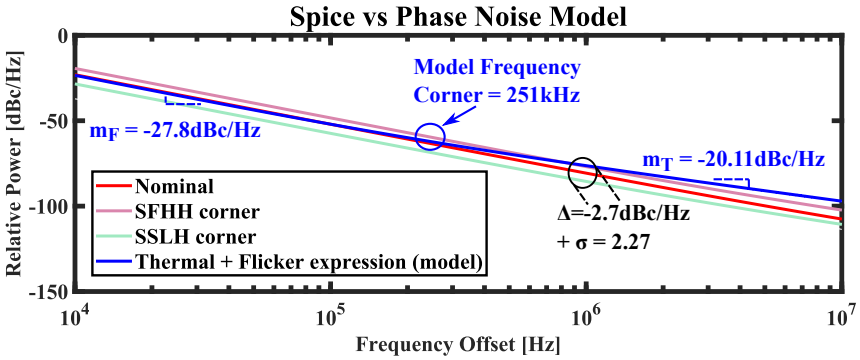
4.5. Simulation Results

Fig. 50a) and Fig. 50b) present the biasing and FFRO architectures to validate the multi-loop control system approach, respectively. They consist of a bias circuit for both core and auxiliary inverter-cells (a) and the differential oscillator (b), tri-state inverters compose both circuits. In Fig. 50a), the digital words $CTRL$ and FW_CTRL in the core and feed-forward biasing circuits, respectively, control the feed-forward strength α ($FW\_CTRL/CTRL$).

Fig. 51 presents the nominal and best and worst corners (SSLH and SFHH) phase noise simulation results of a $200\mu s$ Spice commercial model for a 180nm CMOS technology node, and the model described in Section 4.4.2. The setup consists of a 1.25GHz beat frequency, 20

Figura 51

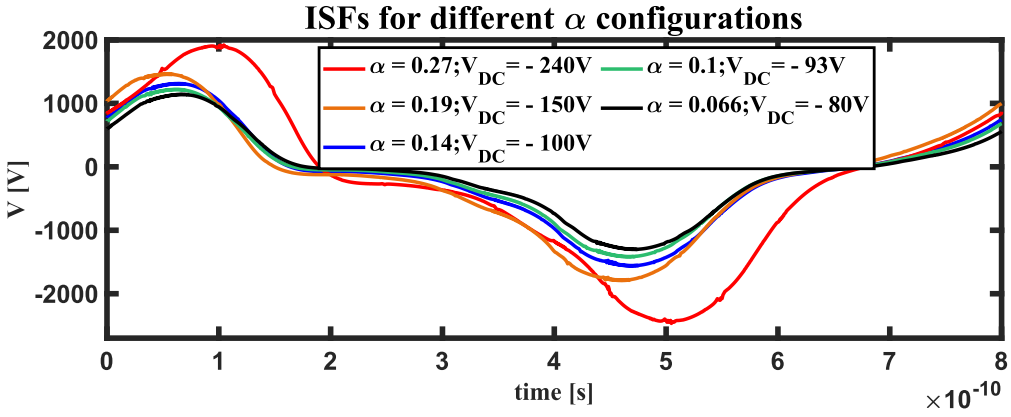
Comparison of phase noise model (thermal + flicker) with nominal and Spice best and worst corners results for f_{osc} = 1.25GHz and α = 0.14.



output harmonics, a gear2 integration method parameter, the maximum sideband is 36, and the relative harmonic is 1 for pss and pnoise analyses. We observe the results for the nominal Spice simulation and the phase noise model expression in red and blue, respectively. The slopes of Spice, thermal noise, and flicker phase noise model are -25.16dBc/Hz, m_T = -20.11dBc/Hz, and m_F =-27.8dBc/Hz, respectively. Note that the slopes differ from the theoretical -20dBc/Hz (thermal) and -30dBc/Hz (flicker) slopes. Regarding the frequency corner (f_{1/f^3}), simulation results show a value of 265kHz compared to the 251kHz model result. The outcome above shows that the proposed model results approach Spice simulations results in both $1/f^2$ and $1/f^3$ regions, indicating the model is functional for design. For the $1/f^2$, we have, at 1MHz, an error of -2.7dBc/Hz with a standard deviation σ=2.27, obtained from the Spice corners' simulation. Note that the model uses constant K_P and K_N for simplification, which is an approximation since the coefficients vary with the bias applied in the transistors' gate, explaining the difference in the results between Spice and our proposed model.

Regarding α, a parameter that confirms the relation between voltage deviation and injected

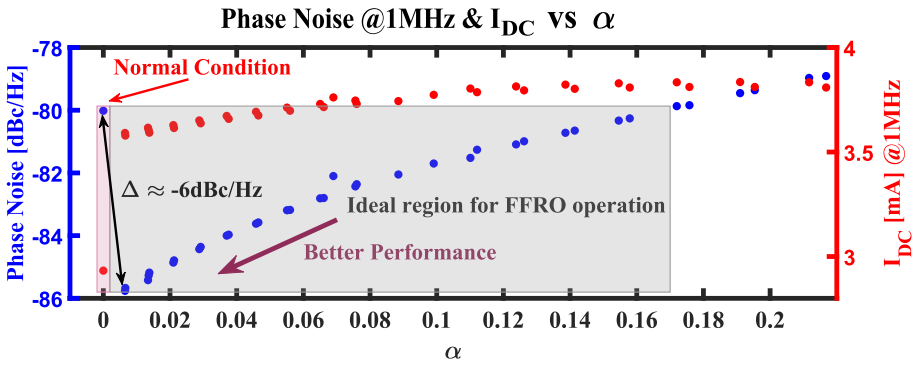
Figura 52
ISF nominal simulation results maintaining f_{osc} = 1.25GHz for all the different α configurations. The DC value of the ISF decreases with α.



charge in a node is the Impulse Sensitivity Function (ISF) defined for oscillators in [27] and depicted in Fig. 52. As the injected charge in a node increases (higher α), the voltage variations rise too, and since the voltage variations are random, the ISF DC value will distance the 0V. This gives us an insight that smaller α values generate lower ISF DC offsets. It is worth mentioning that to reduce the effect of flicker noise in the phase noise spectrum, we decrease the DC value associated with the ISF [21]. The more symmetrical the ISF function is, the more we reduce the flicker noise effect. Note that the ISF non-zero DC value occurs due to the standard cell's difference between rise and fall times ($t_r \approx 0{,}9t_f$). Thus, more minor phase noise values imply more symmetric standard-cell waveforms.

Finally, in Fig. 53, we present phase noise and DC current results @1MHz for different α values, maintaining the oscillation frequency f_{osc}=1.25GHz. We observe that turning on only the core limits the oscillator's phase noise (red area). In contrast, the FFRO enables the possibility to work in a range (grey area) where phase noise values are smaller. As a result, we achieve ≈

Figura 53
Phase Noise @1MHz and DC current for different α configurations maintaining the oscillation frequency f_{osc} = 1.25GHz in all the cases.



-6dBc/Hz improvement with α = 0.0065 in a layout area of 0.05mm^2 and a raise in DC current of 26%.

4.6. Concluding Remarks

This chapter presents a simple phase noise model of a differential FFRO that could be extended for single-ended architectures based on multi-loop control system theory. We complement the control theory with an estimation of noise sources in the current-starved inverter cell and ISF results to achieve an error of -2.7dBc/Hz with σ=2.27 at 1MHz in a 180nm CMOS technology node. Compared to reported frequency and time-domain models, we estimate the phase noise with a reduced number of calculation steps. Furthermore, we identify that the normal operation condition limits the application's overall phase noise. Still, while activating the feedforward circuit, it is possible to find a region associated with small α values that achieves less phase noise values, as long as designers consider the trade-off and impact in the layout area and DC current.

4.7. Contributions of this chapter

- Validation of the simple model for phase noise estimation in FFRO.

- A study of the impact of the feed-forward strength in the phase noise.

- Determination of an ideal region for the FFRO operation based on the feed-forward strength.

5. A pulse generator based on a feedforward ring oscillator for UWB regulations compliance

In Chapters 3 and 4, we developed a piece-wise approach and a phase noise model for feed-forward ring oscillators. We achieved an estimation of the frequency enhancement and a reduction in 6dBm/Hz of the phase noise, originally set by the core, by controlling the $\alpha - \beta$ values. The latter results pave the path to continue exploring the advantages of the FFRO to reduce the number of clock sources in SoC and consequently decrease the times and costs associated with design, validation, and instantiation.

Still, with the results obtained in the last two chapters, we believe that besides to the clock source generation area in SoC, the FFRO could open up new doors to explore and impact other research areas. Among the different topics developed nowadays, we identify several areas where FFRO could be used to complement recent solutions. We consider that enhancement of the frequency range, small layout area, and scalability could be suitable for different research fields. We believe that FFRO is convenient to be used in several applications such as Ultra Wide-Band (UWB) for object detection [9, 52], UWB for sensing in medicine, biohacking, biosensors for body parameters real-time monitoring, cancer breast detection, or multi-band transmission information as a security protocol.

In this last chapter, we decided to focus on UWB for data transmission and object detection, which is completely in line with IoT. We explore the possibility of including the FFRO in actual UWB architectures to better exploit its wide frequency range.

5.1. Feedforward Ring Oscillator as a pulse generator in Non-Coherent transmitter architectures

This section presents a review of the main transmitter and receiver topologies and their characteristics in actual UWB architectures. We identify that it does not exist a unique UWB regulation adopted by all the countries and regions around the world. The lack of a unique regulation reduces the possibility of having a transceiver solution in compliance with all the regulations. Among the different transmitter and receiver circuits, we explore the Non-Coherent transmitter since it is a low-power topology that uses simple circuits to transmit the UWB signal. Most actual Non-Coherent solutions use LC oscillators for pulse generation, allowing them to reach higher operating frequencies. Still, as it was mentioned before, LC oscillators do not cover large frequency ranges, limiting the possibility of positioning in several and specific ranges. Pulse generators based on ring oscillators are also explored in state-of-the-art works, but could not reach higher operation frequency values. We propose the FFRO as a pulse generation circuit for UWB Non-Coherent transmitters to solve the issues mentioned. It is worth mentioning that the available 180nm CMOS technology used to develop the proposed circuit limits the results obtained since the maximum operating frequency of the technology could not cover the UWB range where most of the applications work. Nevertheless, the concept that we explore is discussed and verified in the chapter.

5.2. Introduction

In recent years, the number of efforts associated with exploring and developing Ultra-Wide-Band (UWB) technology has increased due to the emergence of new applications. Modern devices

for personal area networks (PAN), radio-frequency identification (RFID), radar and localization, or biological applications [75] are more commonly encountered in daily situations [38]. Compared to traditional technologies such as infrared or ultrasonic, UWB offers several advantages. For instance, the power spectral density (PSD) of UWB signals is considerably low, -41.3dBm, enabling the compatibility to share the same frequency spectrum with other technologies. High and low-data rate sensors can operate simultaneously, which increases the versatility of the network. In indoor applications, UWB penetrates adequately objects since the signal expands over a large frequency range, and the material penetration losses are low. Additionally, shadows in indoor spaces do not affect UWB signals, allowing the possibility to increase accuracy during the transmission-reception process [50]. The latter confirms the use of UWB as a suitable solution for different scenarios that are nowadays being explored.

It is important to mention that not all UWB applications are allocated in the same frequency range. Three main types of UWB devices could be found in consumer electronics products: 1) imaging systems, 2) vehicular radar systems, and 3) communication measurement systems [9]. For instance, ground penetrating radar systems (GPRs) must operate below 960MHz or between the 3.1-10.6GHz frequency range. Surveillance systems work between the 1.99GHz and 10.6GHz frequencies, whereas vehicular radar systems use the frequency band 22-29GHz. Among the three different types of UWB devices, the majority of GPRs, and communication and measurement systems are allocated in the 3.1GHz and 10.6GHz frequency range, as defined by the Federal Communications Commission (FCC) [9]. Nevertheless, several characteristics and requirements should be accomplished to consider a technology appropriate for UWB applications.

Figura 54

Power spectral densities of some UWB regulations for different countries and regions. In blue and red, are UWB regulations for indoor and outdoor applications in the USA, respectively. In green the UWB regulation for indoor applications in Europe. In violet, the UWB regulation for indoor applications in Japan.

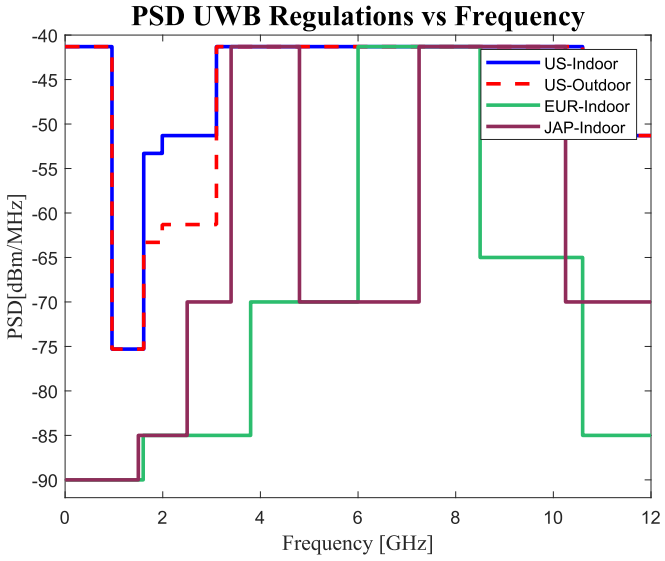
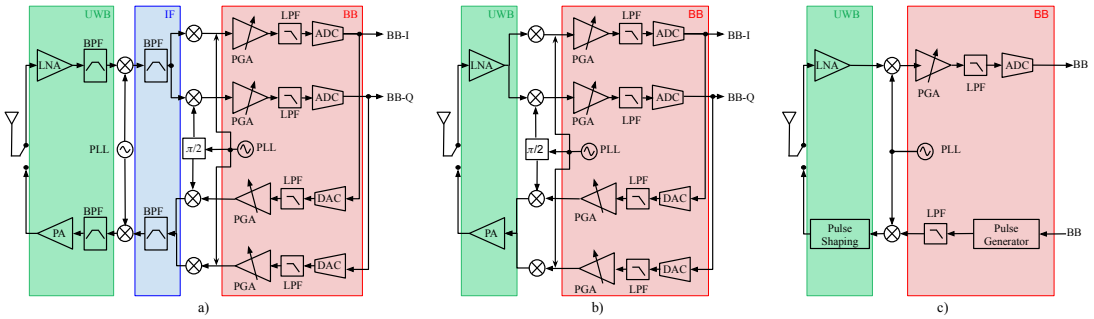


Figura 55

Transceiver architectures for UWB applications. In a), we present the superheterodyne architecture, in b) we depict the Direct Conversion topology, and in c) we illustrate the Direct Sequence main block diagram.



A signal can be classified as UWB by the FCC if it satisfies the following requirements [52]:

1) $\beta_f \geq 0{,}2$, with = $\beta_f = 2 * \frac{f_H - f_L}{f_H + f_L}$, 2) BW $\geq$ 500MHz, and f_H and f_L are the higher and lower -10dB bandwidths. Thus far, a unique regulation adopted worldwide for UWB signals does not

exist, in spite of one attempt in 2003, [49, 50]. The only characteristic common to all regulations is the -41.3 dBm/Hz maximum mean equivalent isotropic radiated power (EIRP). Figure 54 illustrates several power spectral densities (PSDs) associated with different UWB regulations adopted by some countries or regions. The blue and red-dashed plots correspond with the PSDs for United States (US) indoor and outdoor scenarios. We observe that for both regulations, the peak of -41.3dBm is maintained along the 3.1-10.6GHz range. Regarding the indoor scenario for the region of Europe (EUR), the maximum PSD value of -41.3dm is allowed only in the narrow band of 6-8.5GHz. In contrast, the Japan indoor regulation has two bands for the -41.3dBm value, the 3.4-4.8GHz, and 7.25-10.25GHz frequency ranges.

Based on the above, the only available band common to all regulations is the 7.25-8.5GHz. Up until this point, the authors have not identified a state-of-the-art work that covers, operates, and is compatible with several of the regulations mentioned above. Therefore, it is desirable to explore and develop an architecture that could be adapted to all the regulations defined by the different countries and regions. Especially covering a large frequency range and controlling its shape to fit in the different UWB signal bands. One architecture that presents favorable results regarding the coverage of a wide frequency range is the feedforward ring oscillator (FFRO) [2], which could be implemented for UWB regulations compliance.

This current work is organized as follows: Section 5.3 presents the characteristics of the main UWB categories in state-of-the-art works. Section 5.4 describes the Impulse Radio (IR) transmitter, a simple and low-power architecture commonly used in sensing and data communication applications. Section 5.5 presents the feed-forward technique to extend and estimate the

frequency operation range in ring oscillators and its main characteristics. Then, Section 5.6 proposes the FFRO as an alternative circuit to be instantiated and included in the IR transmitter chain to be compatible with FCC requirements. Finally, Section 5.7 details the concluding remarks of this work.

5.3. Review of UWB architectures

Two topologies are commonly used in UWB communication state-of-the-art works: continuous and discrete signal-modulated. The continuous-modulated topology is named multi-band orthogonal frequency-division multiplexing (MB-OFDM) and uses a mixer to generate a carrier to send the information. Two subcategories are associated with the MB-OFDM architecture, superheterodyne and Direct Conversion [72]. Among the discrete signal-modulated topologies, two categories are commonly used: Discrete Sequence (DS) and Impulse Radio (IR). The DS architecture uses a mixer for downconversion; thus, it uses a carrier, whereas the IR system is carrier-less. Figure 55 depicts the three carrier-signal architectures: superheterodyne, Direct Conversion, and the DS topologies.

In Figure 55a), the superheterodyne architecture operates with two PLLs to transform the signal between base-band (BB) and UWB through an intermediary frequency range (IF). Multiple non-overlapping frequency bands divide the UWB frequency spectrum to achieve correct multiple access capabilities. The latter allows the possibility of attaining higher robustness against multipath and achieving larger data rates [3]. Nevertheless, the superheterodyne topology has several drawbacks; for instance, it requires a higher signal-to-noise ratio (SNR) to achieve the same bit-error-rate (BER) compared to simple architectures [50] and consumes larger amounts of power.

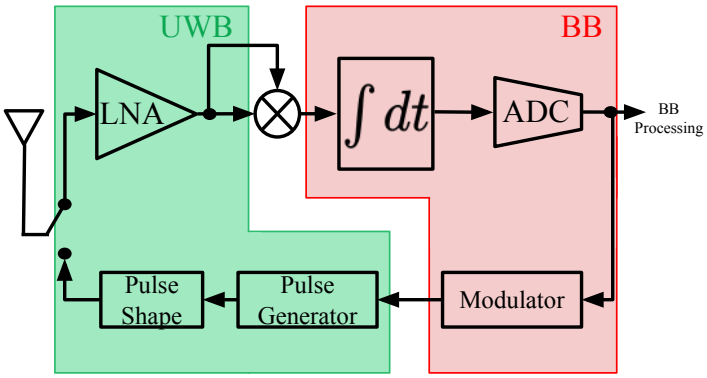
Figure 55b) illustrates the Direct Conversion topology. Unlike the superheterodyne category, Direct Conversion avoids operating in the intermediary frequency range. This frequency jump reduces power consumption and avoids the image-frequency problem originating in the IF band. The main concern in Direct Conversion systems is the DC offset created by mixing the base-band frequency leakage with the UWB frequency.

Regarding the DS architecture, Figure 55c) presents the main block diagram. The architecture is simpler than the previous two since there are no orthogonal (I and Q) signals in the receiver path. A unique lane transforms the signal from UWB to BB. A low-noise amplifier (LNA), a mixer controlled by a local PLL, a programmable gain amplifier (PGA), a low pass filter (LPF), and an analog-to-digital converter (ADC) compose the receiver lane. Unlike the MB-OFDM transmitter, which transmits continuous signals, the DS transmitter uses discrete short pulses to send the information. The BB signal creates short pulses by triggering a pulse generator, then the signal passes through an LPF; consequently, a mixer upconverts the pulse to the UWB range. A final circuit shapes the UWB signal to satisfy the UWB requirements.

As observed in Figure 55, all three architectures use a local PLL for converting the signal from BB to UWB or vice versa, impacting the power consumption. Moreover, the three receivers require adequate synchronization between the local clock and UWB signal in the mixer to avoid data conversion errors, which is not an easy task. When UWB requirements and signal-to-noise-ratio (SNR) are more relaxed, an alternative architecture that could be used for UWB applications is the IR topology, which is a carrier-less modulated system.

There are three categories in the IR receiver: Coherent, Non-Coherent, and Downsampling

Figura 56
The Non-Coherent transceiver main block diagram without local oscillator to downconvert or upconvert the information between UWB frequency and base-band.



[72]. In the Coherent receiver, the designers have complete knowledge of the channel degradation and response, thus all the blocks are optimized to achieve ideal performance. On the contrary, in the Non-Coherent topology, the channel information is not considered and the design aims toward low-power and low-cost requirements [45]. Finally, the Downsampling receiver avoids using a mixer and connects the LNA directly to an ADC, which resembles a software-designed radio application. Based on the above, we consider that it is not always possible to know the channel information, especially for outdoor applications, and that connecting the LNA to the ADC involves working with a sampling rate in the GHz range due to the Nyquist theorem, which impacts negatively the power consumed. Thus, in Section 5.4 we explore, in more detail, the Non-Coherent architecture.

5.4. Characteristics of the Non-Coherent architecture

As mentioned in Section 5.3, the Non-Coherent category is a simple architecture used in low-power UWB transceivers when channel information is not fully available. Figure 56 presents the block diagram of a Non-Coherent architecture. Regarding the receiver, a characteristic that

stands out is the lack of a local oscillator for downconversion, which reduces the power consumption and complexity of the radio technology [3]. The incoming signal is correlated with itself to transform the UWB information to BB. With the lack of a local oscillator, the receiver circuit chain commonly incorporates an antenna, an LNA, a VGA, and a bit decision circuit (integrator and threshold comparator) before baseband signal processing occurs. A bandpass filter before the LNA [66], or placing an analog-to-digital converter (ADC) in between the integrator and baseband [55] are some variants of the Non-Coherent receiver.

Regarding the transmitter of the Non-Coherent topology, the architecture depends on the targetted application. For instance, if the transmitter communicates with other transceivers and exchanges information, the block diagram used is similar to Figure 56 depicts. A modulator triggers the pulse generator with a specific data rate to fulfill the communication standard. On the contrary, if no communication between different transceivers occurs, the application aims to track or determine the position of objects in unknown scenarios.

Figure 57 illustrates the main blocks of the Non-Coherent transmitter with their respective output waveforms for a data transmission application. Since Non-Coherent systems are low-complexity architectures, bi-Phase [41] or On-Off keying [3, 16, 56] usually modulate the BB data. The modulated signal is then multiplied by the programmable time delay block to fulfill at least the 500MHz (t$\leq$2ns) UWB requirement. However, a constant delay between the different pulses generates spikes in the output frequency spectrum that could overpass the maximum values of the UWB regulation. The latter is solved by breaking up the constant pulse train by utilizing a pseudo-random code generator that modifies the time between the transmitted pulses [52], T_{d1} and T_{d2} in

Figura 57
Block diagram of the Non-Coherent transmitter for data transmission applications.

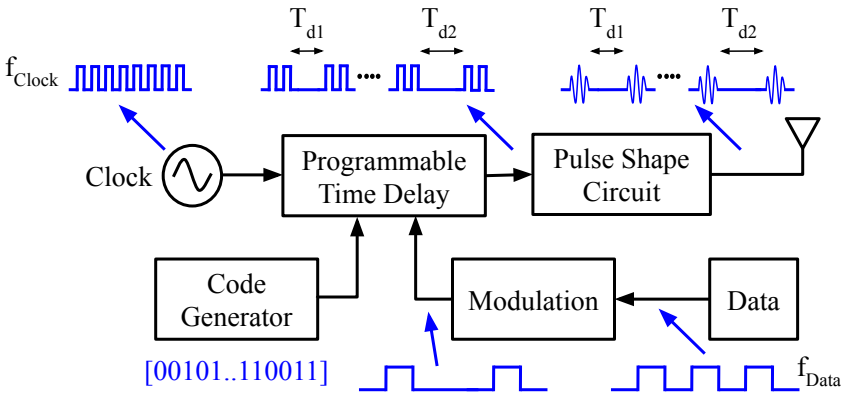


Figure 57. Finally, a pulse shape block fits the programmable time delay block output to the UWB requirements, to fulfill the communication standard.

In state-of-the-art works, several topologies of pulse-shape circuits are used to fit the power spectral density into the UWB regulation. Among the different topologies found in the literature, three specific circuits stand out: Gaussian, return-to-zero, and triangular. The most common topology is the Gaussian pulse, which fits adequately into the UWB mask, and it is the circuit that better exploits the available spectrum of the UWB regulation [11]. A consequence of occupying a wider spectrum is that the Gaussian pulse circuit is suitable for higher data rate applications [41]. Still, Gaussian pulse circuits are less power efficient and occupy a considerable layout area [11]. Sheng[65] demonstrated that for indoor applications, a 4th-order Gaussian pulse is needed, whereas, for outdoor applications, the order of the circuit should increase at least to seven to fit in the FCC regulation. Therefore, as the order of the Gaussian pulse increases, the number of components rises, which impacts the occupied area. More simple topologies could be found in the literature as

return-to-zero and triangular [11, 18, 55]; however, the efficiency of the used spectrum decreases, which limits the data rate.

Regarding the pulse generator, an upconverting technique is usually applied for the latter modulation with a specific data rate. As mentioned above, it is desirable to design a transmitter for several UWB regulations compliance. To achieve this goal, it is preferable to have both coarse and fine controls in a single architecture for frequency covering along the UWB spectrum. We believe that a feedforward ring oscillator (FFRO) could satisfy the characteristics mentioned above since it has a controlled and monotonic behavior along a wide frequency range [2] . Section 5.5 describes the main characteristics of the FFRO.

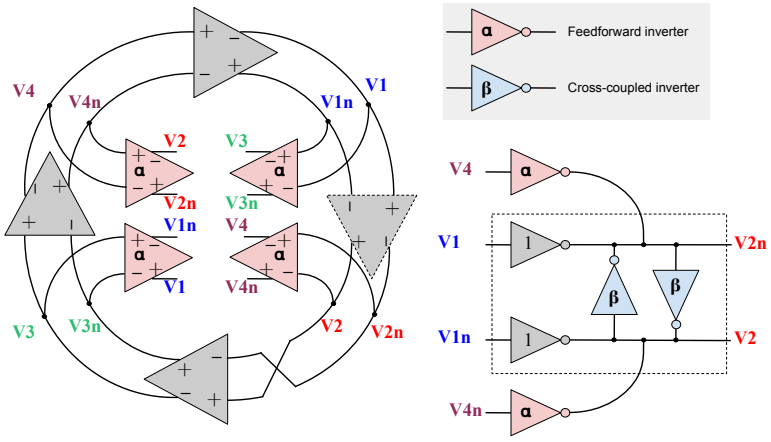
5.5. The feedforward technique in ring oscillators to extend the operating frequency range

Harold Black developed at the Bell Laboratories in the 1930s the concept of feedforward to stabilize amplifiers [4]. Since then, the concept has been explored and used in different areas as a control technique for stabilization. In the last decades, several works implemented the concept of feedforward in ring oscillators to extend the oscillation frequency range [2, 26, 53].

Along with the well-known N interconnected inverters associated with the core, the feedforward ring oscillator uses auxiliary inverters connected to the internal nodes. For instance, in the 4-stage differential ring oscillator depicted in Figure 58a), the signals in nodes $V_1 - V_{1n}$ depend on the information that comes from both nodes pairs $V_3 - V_{3n}$ and $V_4 - V_{4n}$. This double dependency allows the extension of the oscillation frequency range and modifies the phase difference between the nodes of the inverters. With this in mind, it is possible to derive from the FFRO circuit an equivalent delay cell circuit for a suitable analysis of the feedforward effect, as depicted in Figure 58b).

Figura 58

a) Schematic of a conventional 4-stage DRO with additional feedforward delay cells (red). b) Equivalent circuit of a delay cell including the core, feedforward (red), and cross-coupled (grey) inverters.



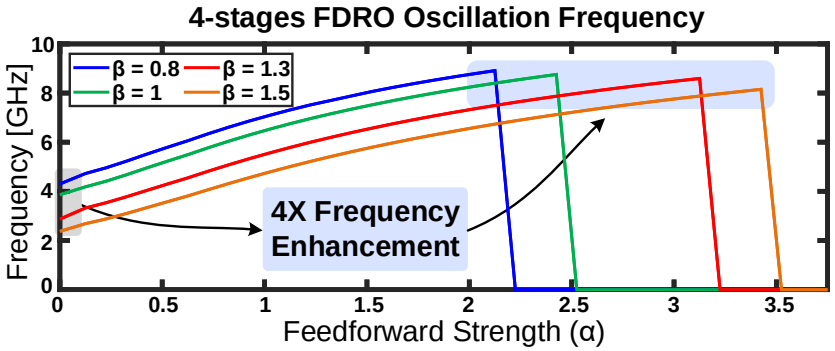
Considering the aspect ratio of the core inverters as a reference, two possible factors or strengths appear to control the extension of the operating frequency range in the FFRO. The aspect ratios between the feedforward inverters (red) and the core inverters and the aspect ratios between the cross-coupled inverters (grey) and the core inverters are known as feedforward strength (α) and cross-coupled strength (β), respectively.

A piece-wise approach developed in detail in [2], demonstrates the effect of α and β in estimating the oscillation frequency. The obtained expressions for the transfer function amplitude and the oscillation frequency of the delay cell are presented in 58b) are derived in (17) and (18), respectively.

$$|H(\alpha,\beta)| = \frac{G \cdot R}{1+\alpha+\beta} \cdot \sqrt{\frac{1+(\alpha+\beta)^2+2(\alpha+\beta)\cos(\theta_k)}{1+\tan^2(\phi_k(\alpha,\beta))}} \tag{17}$$

Figura 59

Simulation results for a conventional 4-stages FDRO (see Fig. 58) using regular inverter cells. The main inverter's width is 890nm, and L=180nm for all transistors. No PVT variations were considered.



$$f_{osc}(\alpha,\beta) = \frac{\tan(\phi_k(\alpha,\beta))}{2\pi RC} \tag{18}$$

Where G ($G = g_{mn} + g_{mp}$) is the inverter cell transconductance, R is the output resistance of the inverter cell, C is the equivalent single-ended node capacitance, and θ_k is the phase-difference (oscillation mode) between two consecutive delay cells. Equation 19, defines the $\phi_k(\alpha,\beta)$, the frequency tangent function argument.

$$\phi_k(\alpha,\beta) = \angle\{1 + \alpha e^{-j\theta_k} + \beta e^{j\theta_k}\} - \theta_k \tag{19}$$

The latter results allow the designers to estimate the operating frequency of the FFRO while controlling α and β. Figure 59 illustrates the 4-stage FFRO simulation results for the operating frequency in a 180nm CMOS technology node.

A 4X frequency enhancement is possible with the correct values for α and β. Nevertheless,

it is possible to observe that some (α - β) values null the operating frequency. In this case, a latch-up state occurs in the oscillator, preventing the FFRO from working correctly. Thus, it is essential to detect latch-up states during the design of the FFRO to avoid undesired conditions. We set a maximum α value of 1, as mentioned in Chapter 3 to consider Process-Voltage-Temperature (PVT) effects in post-layout simulation. With $\alpha = 1$, the frequency enhancement is reduced to three times.

Once we described the effects of the feedforward technique in the ring oscillator operating frequency, and determine α and β as control variables to estimate the frequency, we propose in Section 5.6 the FFRO as a pulse generator for Non-Coherent UWB transmitters.

5.6. FFRO as a pulse generator for UWB transmission

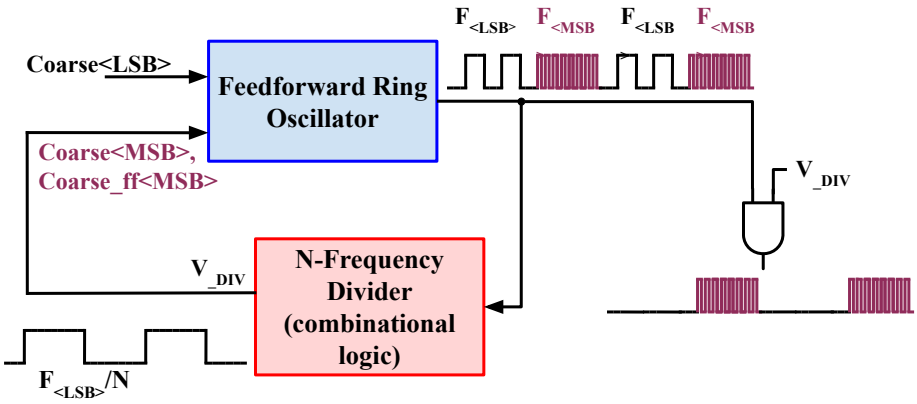
As presented in Section 5.5, the FFRO uses the feedforward technique to extend its operating frequency range up to 3 times the size of its normal range. Therefore, it would be convenient to explore the possibility of instantiating the FFRO in the IR transmitter architecture since it has several advantages compared to the LC oscillator. For instance, the FFRO occupies a smaller area than the LC oscillator due to the larger area of the integrated inductor. Additionally, the FFRO covers a larger frequency range than the LC oscillator, which gives the designer the possibility to sweep all the frequency slots in the UWB regulation.

In Figure 60 we present the proposed block diagram of the Non-Coherent transmitter with the inclusion of the Feedforward Ring Oscillator as a pulse generator. Before the generation of the high-frequency pulses, the FFRO operates at a low-frequency F_{LSB} set by the control word *Coarse_LSB*. Then, the FFRO output frequency enters an N-Frequency divider implemented with

combinational logic to generate in its output $V_{\_DIV}$ a waveform with a frequency equal to F_{LSB}/N. The $V_{\_DIV}$ waveform controls the most significant bits of the core (*Coarse_MSB*) and the feedforward (*Coarse_ff_MSB*) circuits to achieve a higher frequency (F_{MSB}) with the FFRO. Finally, an and-operation between the output of the FFRO and the N-Frequency divider occurs to eliminate the low-frequency signal and consequently obtain the correct shape of the pulses. It is worth mentioning that to generate high-frequency pulses, the FFRO starts in a low-frequency oscillation state since we detected during the simulation results that the FFRO cannot reach the oscillation when both control words *Coarse_MSB* and *Coarse_ff_MSB* activate the FFRO at the same time. We identify that the feedforward signals strive with the core signal to set the oscillation frequency, which prevents the FFRO from achieving a final oscillation value. A different situation occurs when the core of the FFRO has already set an oscillation, and then the feedforward circuit turns on to boost the oscillation frequency. The latter situation corresponds to the normal operation of the FFRO reported in Chapters 3 and 4. A possibility that allows starting the FFRO from a non-oscillation condition is to delay the control signals of the feedforward circuit with respect to the core signals. In this case, an intermediary oscillation frequency associated with the control signal *Coarse_MSB* occurs before achieving the desired high-frequency pulse. A study in the FFRO associated with start-up energy should be implemented to determine which of the two techniques mentioned above is the more convenient, especially for IoT applications when low power consumption is a necessary requirement.

Figure 61 presents three output voltage waveforms for three different control words. We observe in Figure 61a), Figure 61b), and Figure 61c) the output voltages for the frequencies 179MHz,

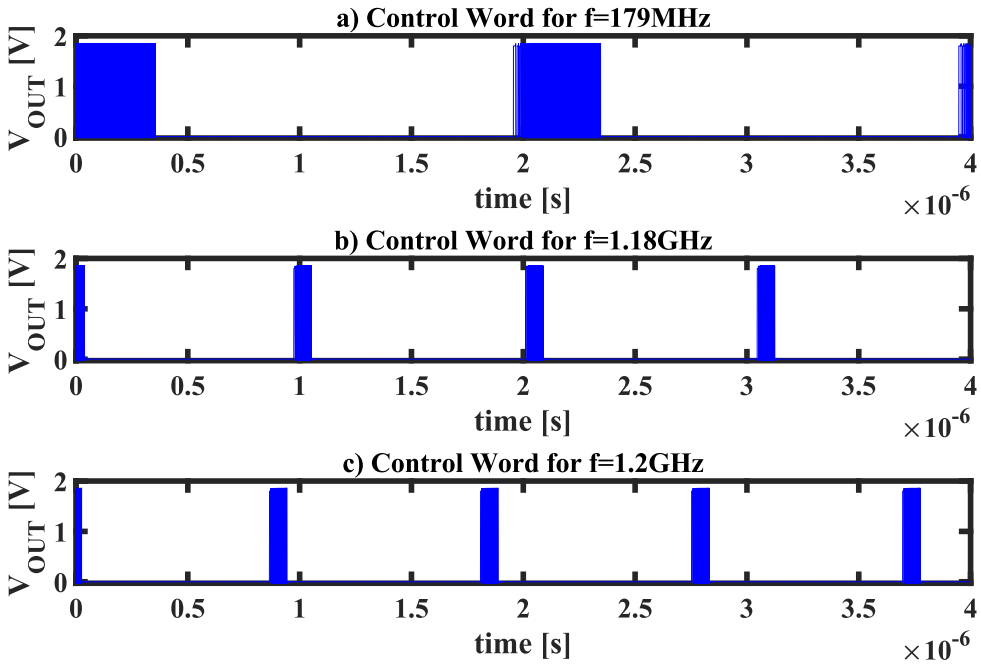
Figura 60
Proposed architecture for the Non-Coherent transmitter based on the FFRO circuit.



1.18GHz, and 1.2GHz, respectively. As expected, smaller oscillation frequencies generate pulses with larger time widths, since the frequency of the N-divider output is smaller. Thus it is necessary to have an accurate control to fit the pulse width in the UWB requirements (BW $\geq$ 500MHz or equivalent to $\approx$ 2ns). As mentioned in Chapter 3, the maximum post-layout oscillation frequency generated with the FFRO is 1.5GHz, which does not fit in the 3.1GHz-10.6GHz UWB frequency range. The latter frequency band could be achieved with a more recent technology node since the available 180nm CMOS node is limited to reaching this frequency band with the FFRO circuit.

As observed in Figure 61, it is possible to achieve a large range of frequency values, depending on the control word set in the FFRO. With both coarse and fine steps, it is possible to cover specific frequency bands defined for UWB applications. Moreover, the FFRO circuit avoids the use of a circuit that upconverts the BB signal to UWB, which reduces power consumption and keeps the Non-Coherent transmitter architecture. Finally, it is important to mention that the output signal of the pulse generator should pass through a circuit that shapes the waveform to fit in the power

Figura 61
Pulse generator outputs for different control words. a), b), and c) are pulses with oscillation frequencies 179MHz, 1.18GHz, and 1.2GHz, respectively.



spectral mask defined by UWB regulation.

5.7. Concluding Remarks

This work presented a review of the different architectures commonly used in UWB applications. We presented several UWB regulations associated with different countries or regions and we detected that there is not a worldwide consensus regarding the frequency of UWB requirements. Among the different frequency bands affiliated with UWB, the 3.1GHz - 10.6GHz is the actual band that operates the larger number of applications and there is only a small frequency band between 7.25GHz and 8.5GHz which is common to all countries and regions. Large differences between UWB regulations exist regarding the extension of the band associated with the peak value

of the power spectral density or the number of bands with this peak value. Due to the several disparities and discontinuities between the UWB power spectral densities, we propose the feedforward ring oscillator as a pulse generator for UWB regulation. With both coarse and fine frequency steps the FFRO could cover large and well-defined frequency ranges. Moreover, the FFRO avoids the use of upconversion circuits that increase design complexity and rise power consumption. Future works suggest that the FFRO should be scaled to a more recent technology node to verify the results in the 3.1GHz - 10.6GHz range.

5.8. Contributions of this chapter

- Proof-of-a-concept validated of the FFRO as a pulse generator for Non-coherent transmitter UWB architectures.
- Proposal of the FFRO as a possible solution to reduce disparities and discontinuities between the UWB power spectral densities in different countries.

6. Summary and Conclusions

This chapter presents the contributions that we explored, analyzed, and developed concerning clock circuits in systems-on-a-chip.

We proposed and validated some ideas regarding the reception of data in wireline communication applications and the extension of the frequency range in clock circuits to reduce the number of clock sources in SoC. The main problems regarding SoC were defined in the introduction of this book associated with *reception of data in wireline systems*, *wide operating frequency range*, *phase noise modeling*, and *phase noise reduction* in clock generation sources. The solutions involve different techniques and analyses described in chapters 2, 3, 4, and 5, which are addressed as the contributions of this dissertation. This final chapter compiles all the main contributions and ideas developed in this work to offer a broad perspective for the reader.

6.1. Compiled list of contributions and highlighted results

The key contributions of this dissertation are as follows.

- *An on-the-fly-enabled resistance termination for ESD effects and high-current density compliance.* We developed a resistor bank that uses two codes: a thermometer and a binary, to adjust the equivalent resistance while receiving real-time information. Coarse and fine steps mitigate ISI effects along the channel and maintain signal integrity during the reception. The resistor termination was validated with two ESD models: HBM and MM, commonly occurring during fabrication or testing, and impact integrated circuits yielding. Finally, the

circuitry is concentrated in a small footprint of 0.2mmx0.15mm, facilitating its integration.

- *A piecewise approach for operating frequency and dominant mode estimation in feedforward differential ring oscillators*. We analyzed, developed, and proposed a piecewise approach to the architecture considering both feedforward (α) and crosscoupled (β) strength to extend the maximum operating frequency of a low-cost CMOS technology node oscillator. We identify prohibited α-β values since the oscillator operates in a latch-up state. We achieved a 15000 tuning range implementation after post-layout results, covering the desired kHz-GHz range for SoC applications. The design was implemented in a 12-track standard cell format to reduce instantiation, placement, and routing times, which enhances scalability, and, consequently, decreases implementation costs.

- *A phase noise model based on multi-loop control systems theory* was developed for the feedforward differential ring oscillator. We considered the main transistor's noise sources, Flicker and Thermal, to achieve correct and accurate results with a reduced number of steps and a small number of mathematical calculations, aiming for the reduction of times associated with design and validation. Moreover, we identify that the core configuration limits the output phase noise since it is possible to reduce it by changing the feedforward strength value.

- *A proof of concept of the feedforward ring oscillator as a pulse generator in Non-coherent transmitter architectures for UWB applications.* Due to the wide operating frequency range (kHz-GHz), the monotonicity along the frequency range of interest, and the possibility of

controlling the oscillation frequency with coarse and fine steps, we propose the FFRO architecture as a possible solution for UWB regulation compliance. With this in mind, we expect that we will enable new applications for FFRO.

6.2. Conclusions

SoC is a relevant technology for both actual and next-generation applications due to its capacity to sense real-time phenomena, consume reduced amounts of energy to operate, and transmit large amounts of data. We identified that clock sources are a relevant area in SoC since clocks are commonly used in different domains (digital, analog, mixed-signal, radio frequency), distinct energy modes (active, start-up, and sleep), and must cover a large frequency range (kHz-GHz). Contributions regarding the reception of data in wireline communication applications and a wide frequency range clock architecture to reduce the number of clock source generators in SoC are presented in this thesis.

With the contributions presented above, we enable the possibility to enhance robustness during the reception of data in wireline applications. With the on-the-fly calibration, the input termination could be adjusted for maximum power transfer and to avoid data losses. We developed a fully integrated compact resistance termination with on-the-fly calibration. The design presents considerations for ESD and high-current density compliance, and it is complemented by a sub-circuit that compensates for Process-Voltage-Temperature variations. Post-layout simulation results demonstrate a fine step of $\approx 1.4\Omega$ in a range from 70Ω to 130Ω. The calibration scheme demonstrates a reduction of the maximum relative error from 17.66 % to 2.34 %. Compared to the selected state-of-the-art works, the area occupied by the resistance termination developed in

this work is one of the smallest. Still, it is important to mention that our design considers ESD, high-current density effects, and PVT compensation.

We also enable the possibility of using the feedforward ring oscillator as a source generator in SoC. We developed a simple piece-wise model for oscillation frequency and oscillation mode estimation along the 100kHz-1.5GHz range, which is the largest range among the state-of-the-art works. The N = 15000 allows covering a wide frequency range, which was extended by 3 times the maximum oscillation frequency of the CMOS technology node with the feed-forward technique, to try to satisfy several communication standard requirements. We identify that our work achieves the best FoM at 625MHz while obtaining competitive results at 100kHz, 1.25GHz, and 1.5GHz operation. The model was validated for 4-, 6-, 8-, and 10-stage differential feed-forward ring oscillator architecture, showing correct results, and demonstrating that the model is functional. The 12-track standard cell format facilitates scaling of the architecture to more recent technology nodes and reduces instantiation and validation costs.

Once the estimation of the oscillation frequency and oscillation mode by the piece-wise model were verified by the post-layout simulation results, we decided to explore even more the FFRO architecture by developing a phase noise model, which is another important characteristic of oscillators. A wide frequency range and techniques for phase noise reduction allow the possibility of fulfilling different communication standards with the FFRO. Thus, a model based on the multi-loop control system theory for phase noise estimation was implemented. The model consists of obtaining the transfer function from each node to the output node, identifying the noise sources in each unitary delay cell, and referencing the noises to the output node. Finally, we obtain the

ISF coefficients and apply them to the phase noise expressions for both thermal and flicker noises. Post layout results show a frequency corner f_{1/f^3} of 265kHz, which is close to the obtained by the model developed (251kHz). For the $1/f^2$ region, we have at 1MHz, an error of -2.7dBc/Hz with a standard deviation σ=2.27, obtained from the Spice corners' simulation. The model can be more accurate by considering the constants K_P and K_N dependent on the transistor's gate voltage and also include the dependency of the gain of each delay cell stage on the bias point of each transistor. Still, by considering the two dependencies mentioned above, the model increases in complexity, and simulation time could increase considerably, which is not desirable. Moreover, the presented results demonstrate the importance of the feed-forward strength as a control parameter to reduce the phase noise of the architecture.

Finally, in Chapter 5 we present a review of the main transmitter and receiver topologies for UWB architectures. We identify that there are several power spectral densities of UWB regulations for different countries and regions, which delay and disallow the possibility of developing UWB architectures that are compatible with all the regions in the 3.1 - 10.6GHz frequency range. We identify that the most suitable system to implement the FFRO is the Non-Coherent UWB transmitter architecture. The FFRO could be used as a pulse generator to cover the frequency range of interest Simulation results validate the idea that the FFRO could be used in UWB applications and avoids the use of additional circuits to upconvert the digital base signal. Thus, we believe that Chapter 5 opens a new door in UWB applications since the FFRO could be used in the different worldwide UWB regulations looking to achieve compatibility with all the worldwide UWB regulations.

6.3. Future work

Most of the ideas presented in this dissertation made it to the post-layout simulation phase. Due to the pandemic and semiconductors crisis between 2020 and 2021, the works developed and presented above were relegated by the manufacturing company, since commercial chips were the priority. The latter implied several drawbacks that prevented all the ideas described from being silicon-proven.

Thus, one of the main future works is to resubmit the different projects in new tape-outs for testing and make sure that the ideas work correctly. Following this line, the different circuits developed in this dissertation might be instantiated in complete systems to target actual applications for IoT and wireline communications.

Regarding the feedforward differential ring oscillator, since it was implemented in a standard cell format, it would be suitable to implement it in more recent technology nodes. This will ensure the possibility of increasing the maximum operating frequency of the circuit and consequently cover more communication standards. Additionally, it is expected that by using more recent technology nodes, the circuit's power consumption will decrease, making these architectures more suitable for IoT and low-power applications. Due to the different tape-out inconveniences with Amazilia, there was insufficient time to close the loop and include the FFRO in a frequency synthesizer architecture. Therefore, it is desirable to close the loop to reduce even more the phase noise of the clock source and to target several communication standards. Additionally, new analyses could be developed with a closed-loop architecture regarding α and its influence on the

bandwidth, jitter, and stabilization time, among other parameters.

To improve the UWB test, first of all, it is necessary to use a recent node since the technology used in this dissertation achieves a maximum operating frequency (1.5GHz) less than the UWB frequency range of interest (3.1GHz - 10.5GHz). Then, it is desirable to design a frequency filter that shapes the output frequency response of the pulse generator incorporating the FFRO, to satisfy the power spectral density along the frequency band of interest. Finally, a transmission-reception test of the UWB signal would be necessary to identify the impact of the communication channel in the received signal and the adjustment in the transmission for UWB regulation compliance.

Sensing in medicine, biohacking, biosensors for body parameters real-time monitoring, cancer breast detection, or multi-band transmission information as a security protocol are some areas where I believe FFRO could be used to impact positively. Thus, new doors open up to explore new solutions in biomedical and biosensor applications. For instance, due to the small power values used by the UWB technology, human body tissue could not be damaged and consequently, several non-invasive measurements could be done. Permittivity or remote motion of some organs could be identified by UWB signals as mentioned in [29].

Since 2022, I have been working with some undergraduate students at the Onchip Group and we have developed some material and some ideas regarding chip design with Open Source tools, aiming to be part of the global trend to democratize integrated circuits. we have been working with the open source process design kit (PDK) Skywater SKY130 released by Google in 2020. As a result of this work, two undergraduate projects are being developed to explore and contribute to

the open-source research line. One project concerns the design and layout implementation of an RFID fully integrated for object tracking. The second project consists of two sub-projects: 1)the design and layout implementation of a PAD cell considering the trade-off between occupied area, current density and bandwidth, and 2) the design and layout implementation of a library for some digital cells based on a 12-track standard format, targetting a symmetry of the waveform with both rise time and fall time equal. I am also exploring with some undergraduate students another open source PDK, named GF180 released by Global Foundries in 2022. A 5-bits multiplier was accepted for the shuttle GFMPW-0, and we expect to test it during 2023.

Finally during my internship at Universidad de Los Andes (10/2022 - 07/2023), I have been developing some material associated with microelectronics and SKY130 to democratize IC design in other universities. Also, I have been given the chance to teach a graduate class at the Universidad de Los Andes, named Diseño de Circuitos Integratos, during the first semester of 2023.

Contribution List

6.4. Conference papers

1. **J. S. Moya**, J. Arenas, and E. Roa. *A Phase Noise Model Based on Multi-Loop Control System Theory Applied to Feed-Forward Ring Oscillators*, 2023 IEEE International Symposium on Circuits and Systems (ISCAS), 2023, pp. 1-4, 10.1109/ISCAS46773.2023.10181894.

2. J. Arenas, **J. S. Moya** and E. Roa. *A 15000 Tuning Range Scalable Feed-Forward Oscillator with 0.05mm2 Area in CMOS Standard-Cell Format*, 2021 IEEE International Symposium on Circuits and Systems (ISCAS)), 2021, pp. 1-4, 10.1109/ISCAS51556.2021.9401776.

3. C. Duran, **J. S. Moya B** et al.. *An Energy-Efficient RISC-V RV32IMAC Microcontroller for Periodical-Driven Sensing Applications*, 2020 IEEE Custom Integrated Circuits Conference (CICC), 2020, pp. 1-4, 10.1109/CICC48029.2020.9075877.

4. L. E. Rueda G., **J. S. Moya B** and E. Roa. *A Compact Industrial-Grade Multi-Threshold Brown-Out Detector*, 2019 26th IEEE International Conference on Electronics, Circuits and Systems (ICECS), 2019, pp. 923-926, 10.1109/ICECS46596.2019.8964634.

5. L. Dovale, **J. S. Moya** and E. Roa. *A Programmable and Low-Area On-Die Termination for High-Speed Interfaces*, 2019 IEEE 10th Latin American Symposium on Circuits and Systems (LASCAS), 2019, pp. 173-176, 10.1109/LASCAS.2019.8667552.

6.5. Journal Papers

1. **Juan Sebastian Moya**, Luisa Fernanda Dovale, Hector Gomez and E. Roa, *Compact on-the-fly-enabled termination with high-current density and ESD compliance*, in IET Circuits, Devices and Systems, vol. 14, issue 6, pp. 788-795, September 2020, doi: 10.1049/iet-cds.2020.0017.

2. Julian Arenas, **Juan Sebastian Moya**, and E. Roa. *Analysis and Design Approach of Wideband Digital-Based Feedforward Ring Oscillators*, Accepted for publication in International Journal of Circuit Theory and Applications, July 2023, doi: 10.1002/cta.3721.

6.6. Patents

1. Elkim Felipe Roa Fuentes, Luis Eduardo Rueda Guerrero y **Juan Sebastián Moya Baquero**, *Dispositivos de detección para caídas de tensión*, given by La Superintendencia de Industria y Comercio - Gobierno de Colombia.

6.7. Directed undergraduate works

1. Luisa Fernanda Dovale Vargas, Director: **Juan Sebastián Moya Baquero**, Co-director: Elkim Felipe Roa Fuentes. *Impedance matching circuit for high-speed applications*. Tesis (Ingeniera Electrónica) - UIS. Escuela de Ingenieria Electrica, Electronica y Telecomunicaciones, 2018.

2. Antony Brayan Sanabria Calderón y Karla Julieth Camacho Mercado. Director: **Juan Sebastián Moya Baquero**, Co-director: Ernesto Aguilera Bermúdez. *Diseño de bloques para una*

etiqueta RFID integrada en un nodo tecnológico de acceso libre - UIS. Escuela de Ingeniería Electrica, Electronica y Telecomunicaciones, 2023-1.

3. Jhon Steven Pinto Hernández y Nelson José Rodríguez Sierra. Director: **Juan Sebastián Moya Baquero**, Co-director: Jaime Guillermo Barrero Pérez. *Diseño de Celdas estándar y celdas I/O para código abierto* - UIS. Escuela de Ingeniería Electrica, Electronica y Telecomunicaciones, 2023-1.

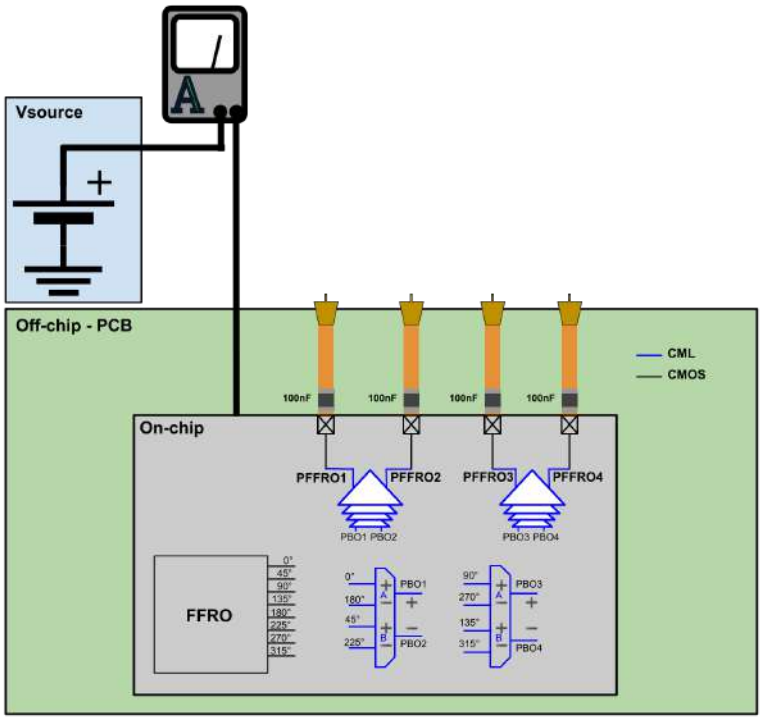
7. Annex

7.1. Test plan of the Feed-forward Ring Oscillator for DC and transient experimental results

This section provides the main information regarding the possible test plan of the FFRO for DC and transient experimental results. The steps to characterize experimentally the FFRO are:

- Power measurements
- Characterization of the FFRO in the 4MHz - 500MHz frequency range with the feed-forward circuits deactivated.
- Characterization of the FFRO in the 100kHz - 4MHz frequency range with the feed-forward circuits deactivated and using the nA current sources mentioned in Chapter 3.
- Characterization of the FFRO in the 500MHz - 1.6GHz frequency range with the feed-forward circuits activated.

Figura 62
Measurement setup for current consumption of the FFRO.



7.1.1. Power measurements

Figure 62 presents the test bench for the power measurements.

The ammeter will measure both FFRO and CML buffer currents, so it is important that both circuits have power-downs separated.

The analog input values for the measurement are:

- VDDA = 1.8V ± 10% for VCO and CML chain.
- VDD3A = 3.3V ± 10% for the bias circuit and the BG.

The digital input values for the measurement are:

- I_coarse [5:1] $\longleftrightarrow$ 0 - 31. Activation and deactivation of all the branches associated with the coarse step for the core. The nominal value for the coarse step is $10\mu A$.

- I_fine [5:1] $\longleftrightarrow$ 0 - 31. Activation and deactivation of all the branches associated with the fine step for the core. The nominal value for the fine step is $1\mu A$.

- IFW_coarse [5:1] $\longleftrightarrow$ 0. Deactivation of all the branches associated with the coarse step for the feed-forward circuit. The nominal value for the coarse step is $10\mu A$.

- IFW_fine [5:1] $\longleftrightarrow$ 0. Deactivation of all the branches associated with the fine step for the feed-forward circuit. The nominal value for the fine step is $1\mu A$.

- $trim\_LF \longleftrightarrow 0$. Selection of the μA current source (designed for Tucan) to bias the circuit.

- $dis\_FW \longleftrightarrow 0$. Deactivate the feed-forward circuit.

- $nA\_select \longleftrightarrow 0$. Deactivate the integrated nA current circuit.

- $CLOCK\_MUX\_FFRO \longleftrightarrow 0$. Deactivate the CML muxes to avoid including the current consumption.

The steps to measure the current and consequently the DC power are:

- Enable the power-down of the FFRO (disable the FFRO circuit) and measure CML current consumption. It is important to mention that the CML current consumption could be considered static (constant).

- Measure the FFRO + CML buffer current consumption.

Figura 63
Truevolt DMM-34460A Multimeter used for FFRO current measurement.

- Subtract the CML buffer current consumption from the ammeter results
- Obtain the plot average current vs frequency range.

The ammeter used is the *Truevolt DMM-34460A Multimeter* [36] and is depicted in Figure 63.

7.1.2. Characterization of the FFRO in the 4MHz - 500MHz frequency range with the feed-forward circuits deactivated.

Figure 64 presents the test bench for the 4MHz - 500MHz frequency range measurements.

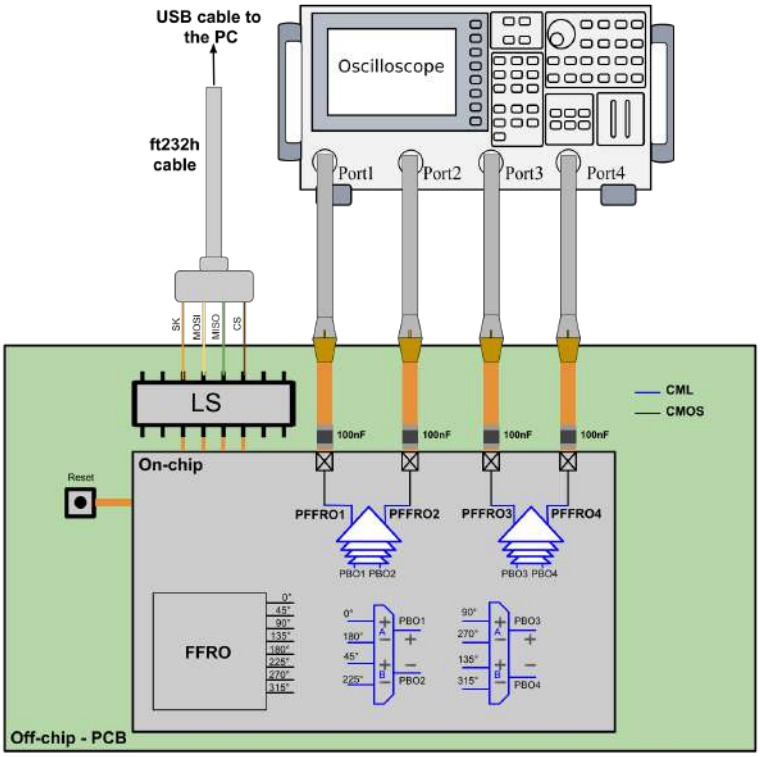
The analog input values for the measurement are:

- VDDA = 1.8V $\pm$ 10 % for VCO and CML chain.
- VDD3A = 3.3V $\pm$ 10 % for the bias circuit and the BG.

The digital input values for the measurement are:

- I_coarse [5:1] $\longleftrightarrow$ 0 - 31. Activation and deactivation of all the branches associated with the coarse step for the core. The nominal value for the coarse step is $10\mu A$.

Figura 64
Measurement setup for the 100kHz - 4MHz, 4MHz - 500MHz, and 500MHz - 1.5GHz frequency ranges.



- I_fine [5:1] $\longleftrightarrow$ 0 - 31. Activation and deactivation of all the branches associated with the fine step for the core. The nominal value for the fine step is $1\mu A$.

- IFW_coarse [5:1] $\longleftrightarrow$ 0. Deactivation of all the branches associated with the coarse step for the feed-forward circuit. The nominal value for the coarse step is $10\mu A$.

- IFW_fine [5:1] $\longleftrightarrow$ 0. Deactivation of all the branches associated with the fine step for the feed-forward circuit. The nominal value for the fine step is $1\mu A$.

- $trim\_LF \longleftrightarrow 0$. Selection of the μA current source (designed for Tucan) to bias the circuit.

- $dis\_FW \longleftrightarrow 0$. Deactivate the feed-forward circuit.
- $nA\_select \longleftrightarrow 0$. Deactivate the integrated nA current circuit.
- $CLOCK\_MUX\_FFRO \longleftrightarrow 0$ - 1. Activate or deactivate the CML muxes to measure different phases.

The outputs measured are:

- PFFRO1 - PFFRO2 are the outputs for 0°-180° and 90°-270°.
- PFFRO3 - PFFRO4 are the outputs for 45°-225° and 135°-315°.

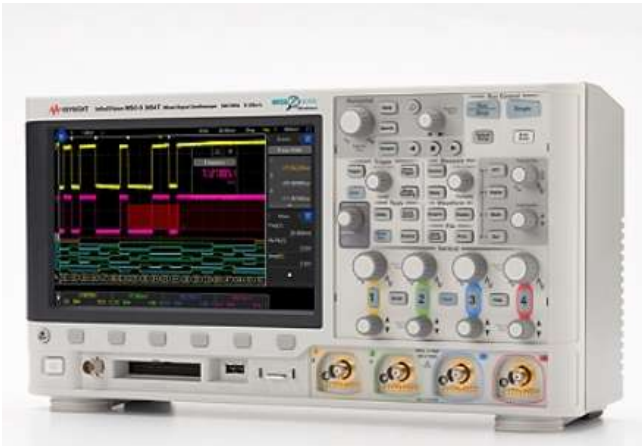
Finally, a jumper will be placed in the PCB to short-circuit the decoupling output capacitor (100nF) in case it is desirable to avoid the effect of this capacitor. All the reported data results will be presented by considering the decoupling capacitor.

Since the range to do measurements is 4MHz-500MHz, we decided to use a common oscilloscope. This oscilloscope is the *InfiniiVision 3000T X-Series* [34] and it is displayed in Figure 65.

Some additional information for the test is provided:

- Input Impedance of the *InfiniiVision 3000T X-Series*: 50Ω - 1MΩ.
- Maximum frequency of the *InfiniiVision 3000T X-Series*: 1GHz.
- We need two probes to measure the oscillation frequency (differential).
- We need two probes to measure the phase error (single-ended).

Figura 65
InfiniiVision 3000T X-Series for the measurement in the 100kHz - 4MHz and 4MHz - 500MHz frequency ranges.



- We need four probes to measure the phase error (differential).
- We will use this oscilloscope for the low-frequency range ($\leq$600MHz)

7.1.3. Characterization of the FFRO in the 100kHz - 4MHz frequency range with the feed-forward circuits deactivated and using the nA current sources.

Figure 64 presents the test bench for the 100kHz - 4MHz frequency range measurements.

The analog input values for the measurement are:

- VDDA = 1.8V $\pm$ 10 % for VCO and CML chain.
- VDD3A = 3.3V $\pm$ 10 % for the bias circuit and the BG.

The digital input values for the measurement are:

- I_coarse [5:1] $\longleftrightarrow$ 0. Deactivation of all the branches associated with the coarse step for the core. The nominal value for the coarse step is $10\mu A$.

- I_fine [5:1] $\longleftrightarrow$ 0 - 9. Activation and deactivation of all the branches associated with the fine step for the core. The nominal value for the fine step is $1\mu A$.

- IFW_coarse [5:1] $\longleftrightarrow$ 0. Deactivation of all the branches associated with the coarse step for the feed-forward circuit. The nominal value for the coarse step is $10\mu A$.

- IFW_fine [5:1] $\longleftrightarrow$ 0. Deactivation of all the branches associated with the fine step for the feed-forward circuit. The nominal value for the fine step is $1\mu A$.

- $trim\_LF \longleftrightarrow$ 1. Selection of the nA current source (designed for Guerinii) to bias the circuit.

- $dis\_FW \longleftrightarrow$ 0. Deactivate the feed-forward circuit.

- $nA\_select \longleftrightarrow$ 1. Activate the integrated nA current circuit.

- $CLOCK\_MUX\_FFRO \longleftrightarrow$ 0 - 1. Activate or deactivate the CML muxes to measure different phases.

The outputs measured are:

- PFFRO1 - PFFRO2 are the outputs for 0°-180° and 90°-270°.

- PFFRO3 - PFFRO4 are the outputs for 45°-225° and 135°-315°.

Finally, a jumper will be placed in the PCB to short-circuit the decoupling output capacitor (100nF) in case it is desirable to avoid the effect of this capacitor. All the reported data results will be presented by considering the decoupling capacitor.

Since the range to do measurements is 100kHz-4MHz, we decided to use a common oscilloscope. This oscilloscope is the *InfiniiVision 3000T X-Series* [34] and it is displayed in Figure 65.

7.1.4. Characterization of the FFRO in the 500MHz - 1.5GHz frequency range with the feed-forward circuits activated.

Figure 64 presents the test bench for the 500MHz - 1.5GHz frequency range measurements.

The analog input values for the measurement are:

- VDDA = 1.8V $\pm$ 10% for VCO and CML chain.
- VDD3A = 3.3V $\pm$ 10% for the bias circuit and the BG.

The digital input values for the measurement are:

- I_coarse [5:1] $\longleftrightarrow$ 31. Activation of all the branches associated with the coarse step for the core. The nominal value for the coarse step is $10\mu A$.
- I_fine [5:1] $\longleftrightarrow$ 9. Activation of all the branches associated with the fine step for the core. The nominal value for the fine step is $1\mu A$.
- IFW_coarse [5:1] $\longleftrightarrow$ 0 - 31. Activation and deactivation of all the branches associated with the coarse step for the feed-forward circuit. The nominal value for the coarse step is $10\mu A$.
- IFW_fine [5:1] $\longleftrightarrow$ 0 - 9. Activation and deactivation of all the branches associated with the fine step for the feed-forward circuit. The nominal value for the fine step is $1\mu A$.

- $trim\_LF \longleftrightarrow 1$. Selection of the μA current source (designed for Tucan) to bias the circuit.
- $dis\_FW \longleftrightarrow 1$. Activate the feed-forward circuit.
- $nA\_select \longleftrightarrow 0$. Deactivate the integrated nA current circuit.
- $CLOCK\_MUX\_FFRO \longleftrightarrow 0$ - 1. Activate or deactivate the CML muxes to measure different phases.

The outputs measured are:

- PFFRO1 - PFFRO2 are the outputs for 0°-180° and 90°-270°.
- PFFRO3 - PFFRO4 are the outputs for 45°-225° and 135°-315°.

Finally, a jumper will be placed in the PCB to short-circuit the decoupling output capacitor (100nF) in case it is desirable to avoid the effect of this capacitor. All the reported data results will be presented by considering the decoupling capacitor.

Since the range to do measurements is 500MHz-1.5GHz, we decided to use a high-frequency oscilloscope. This oscilloscope is the *DSAZ254A Infiniium Oscilloscope: 25 GHz* [35] and it is displayed in Figure 66.

Some additional information for the test is provided:

- Input Impedance of the *DSAZ254A Infiniium Oscilloscope: 25 GHz*: 50Ω.
- Maximum frequency of the *DSAZ254A Infiniium Oscilloscope: 25 GHz*: 25GHz.
- This oscilloscope only supports active probes.

Figura 66
DSAZ254A Infiniium Oscilloscope: 25 GHz for the measurement in the 500MHz - 1.5GHz frequency range.

- We will use two channels to measure the oscillation frequency, and single-ended phase error.
- We will use this oscilloscope for the high-frequency range (600MHz $\leq$ f $\leq$ 1.5GHz)

7.2. Test plan of the Feed-forward Ring Oscillator for phase noise experimental results

This section provides the main information regarding the possible test plan of the FFRO for phase noise experimental results.

Figure 67 presents the test bench for the phase noise measurements.

The analog input values for the measurement are:

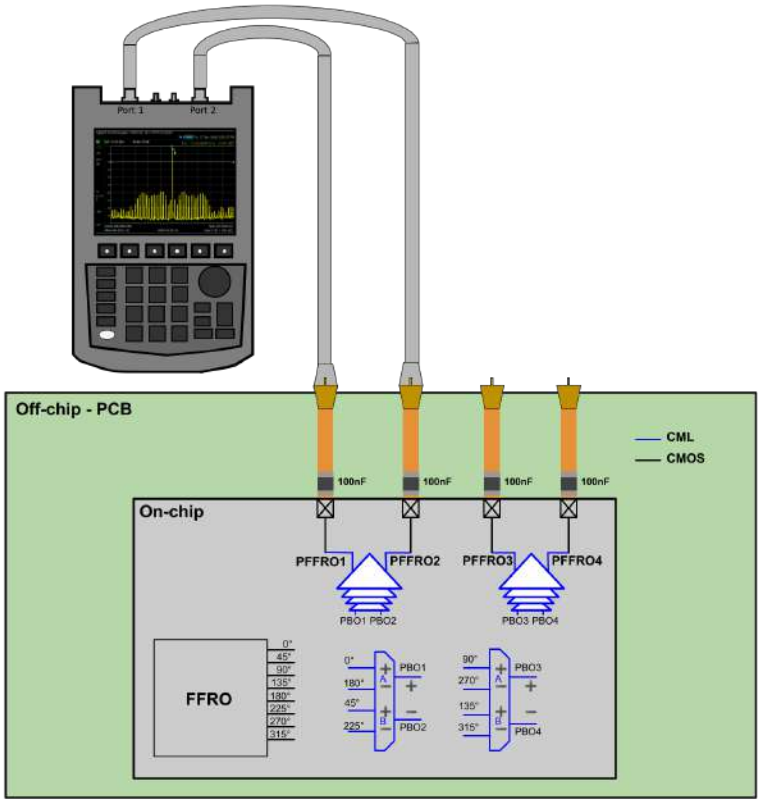
- VDDA = 1.8V $\pm$ 10 % for VCO and CML chain.
- VDD3A = 3.3V $\pm$ 10 % for the bias circuit and the BG.

The digital input values for the measurement are:

- Se registers to oscillate at 100kHz, 1MHz, 240MHz, 625MHz, 1.5GHz, fmax.

Figura 67

Measurement setup for the phase noise.



The outputs measured are:

- PFFRO1 - PFFRO2 are the outputs for 0°-180° and 90°-270°.
- PFFRO3 - PFFRO4 are the outputs for 45°-225° and 135°-315°.

Finally, a jumper will be placed in the PCB to short-circuit the decoupling output capacitor (100nF) in case it is desirable to avoid the effect of this capacitor. All the reported data results will be presented by considering the decoupling capacitor.

Some additional information for the test is provided:

- To get a more realistic phase noise measurement, it is desirable that the pads of the die that are used for the phase noise measurement are separated from the power ring to avoid the noise coupled to the ring.

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