Crystal Oscillator Design for Energy-Constrained Systems in Standard CMOS 28nm Technology

Sergio Andres Leal Capacho

Undergraduate work for the degree of electronic Engineer

Advisor

Javier Ferney Ardila Ochoa

PhD Electronic Engineering

Co Advisor

Elkim Felipe Roa Fuentes

PhD Electronic Engineering

Universidad Industrial de Santander

School of Engineering Physicomechanics

School of Electrical, Electronic and Telecommunications Engineering

Bucaramanga

2022

Dedication

This work is especially dedicated to my mom who since I was in school dreamed of seeing me get my professional degree, she was always there when I needed support, even in the moments when I doubted my abilities she always encouraged me to believe in me and reminded me that no matter what kind of obstacle came my way, I would always achieve my goals.

Acknowledgments

I thank my family who supported me at all times during my time at university, for the light they represented to illuminate my path, their voices of encouragement and prayers; thanks to my friends and colleagues for all this time and shared experiences full of unforgettable memories, and to those people who will remain in my mind and heart, thanks for always wanting me to be a better version of myself, who at all times showed me their affection in many ways and that they sought in an admirable way that I will be aware of how wonderful life is when decisions are made to be better.

An important acknowledgment and thanks to my degree work director, a person whom I greatly admire and respect, not only for his discipline, intelligence, and professional integrity but also for the quality of human being that he showed me to be, especially a few days of lift, at which point I needed a little push and I received it from him at the most opportune moment.

Índice general

Introduction **11**

1 Objectives **13**

1.1 General Objective 13

1.2 Specific Objectives 13

2 Crystal circuit modeling **14**

3 Mathematical analysis **16**

4 Graphical analysis **20**

5 Survey, Topology Review and Selection **23**

5.1 Short Topology Survey 23

5.1.1 Pierce Oscillator 23

5.1.2 Colpitts Oscillator 24

5.1.3 Santos Oscillator 24

5.2 Topology Used 25

5.2.1 Bias 26

5.2.2 Core 26

5.2.3 Start-Up 26

5.2.4 Amplification 28

5.2.5 Boost 28

6 Test bench 28

7 Performance and Results 29

8 Conclusion 34

Bibliography 35

List of Figures

Figure 1 Circuit modeling of the crystal employing its RLC series equivalent and the parallel capacitance C_p. 14

Figure 2 Behavioral graph of the equivalent impedance of the crystal as a function of the frequency. 15

Figure 3 Configuration for thevenin equivalent of the circuit with a single transistor where the negative resistance is extracted with currents and voltages depicted. 18

Figure 4 Simplified Thevenin equivalent assuming crystal modeling as inductance and series resistance. 20

Figure 5 Equivalent circuit taking into account that the capacitance C_3 is the parallel between the capacitances C_p and C_{gd}. 21

Figure 6 Locus diagram used in the graphical analysis for the crystal oscillation condition. 22

Figure 7 Proposed topology for a XO where each of the modules of which it is composed can be seen integrated. 25

Figure 8 Test bench used to carry out tests where using circuit elements the on-chip, wire-bond and external environment is simulated, on which the behavior of the driver designed in a real environment will depend. 29

Figure 9 Start-Up time measure PWD vs VDD (b) with amplification and (a) without amplification. 30

Figure 10 Transitory response from Start-Up time zoom measure PWD vs VDD. 31

Figure 11 Phase noise for the designed XO, where the measurements for 1KHz, 10KHz, and 100KHz are shown. 32

List of Tables

Table 1 Performance summary and comparison whit the state of the art. 25

Table 2 Design parameters and performance summary 33

RESUMEN

Título: Diseño de un Oscilador de Cristal para sitemas de energía limitada en una tecnología estandar CMOS de 28nm [*]

Autor: Sergio Andres Leal Capacho [**]

Palabras Clave: Oscilador de Cristal, Energía de encendido, Tiempo de endendido, Eficiencia energética, Power-Down

Descripción: Para sistemas de alta velocidad donde la precisión de la frecuencia es significativa y la principal limitación, los osciladores de cristal destacan por su frecuencia de error del 0,1 %. Este trabajo presenta un diseño de un oscilador de cristal (XO) en una tecnología CMOS de 28nm con una frecuencia de operación de 32.74KHz y un error de frecuencia de 854ppm, lo que significa menos del 1 % a pesar de tener el mayor tiempo de puesta en marcha. Asimismo, la medida de puesta en marcha se realizó de dos formas. El primero fue cuando la señal de PWD está activa y el otro cuando la señal PWD está inactiva y se cambia el estado de VDD. En el primer caso, los nodos ya están cargados, pero en el segundo los nodos necesitan tiempo para cargarse, mostrando una diferencia de tiempo considerable en la medida.

---

[*] Trabajo de grado

[**] Facultad de Ingenierías Físico-Mecánicas. Escuela de Ingenierías Eléctrica, Electrónica y telecomunicaciones. Director: Javier Ferney Ardila Ochoa, Doctorado en Ingeniería Informática y Automática.

ABSTRACT

Title: Crystal Oscillator Design for Energy-Constrained Systems in Standard CMOS 28nm Technology [*]

Author: Sergio Andres Leal Capacho [**]

Keywords: Crystal Oscillator (XO), Start-Up Energy, Start-Up Time, Energy-Efficient, Power-Down (PWD).

Description: For high-speed systems where frequency precision is significant and the main limitation, crystal oscillators stand out by their 0.1 % error frequency. This work presents a crystal oscillator (XO) design in 28nm CMOS technology with an operation frequency of 32.74KHz and a frequency error of 854ppm, which means less than 1 %. Despite having the biggest start-up time. Also, start-up measure was done in two ways. The first one was when PWD is asserted and the other one when the PWD signal is deserted and switching VDD. In the first case, nodes are already charged, but in the second nodes need time to charge, showing a considerable time difference in the measure.

---

[*] Bachelor Thesis

[**] Facultad de Ingenierías Físico-Mecánicas. Escuela de Ingenierías Eléctrica, Electrónica y telecomunicaciones. Director: Javier Ferney Ardila Ochoa, Doctorado en Ingeniería Electrónica.

Introduction

A crystal oscillator is an electronic oscillator circuit that works based on a mechanical resonance of a vibrating crystal of piezoelectric material. It creates an electrical signal with a given frequency which is commonly used to keep track of time. Crystal oscillators are widely used in many systems such as industrial applications, computers, digital systems, telecommunications, sensors, and also in disk drives. For example, wristwatches are used in digital integrated circuits to provide a stable clock signal and to stabilize frequencies for radio transmitters and receivers. The start-up time of the crystal oscillators represents a challenge since it takes a long time to start properly in the oscillation regimen. That implies a high-power consumption in the system during the process, which is not proper for energy-constrained systems like bluetooth low energy (BLE) applications or internet-of-things (Esmaeelzadeh y Pamarti, 2019).

An oscillator is a type of feedback amplifier. The feedback signal is what the amplifier requires to sustain oscillation. This paper will discuss three types of oscillators: RC oscillators, ring oscillators, and crystal oscillators. Ring oscillators represent the lowest area. The nonlinearities force them to have robust and complex calibrations systems along with low precision frequency. Furthermore, RC oscillators are easy to adjust their frequency because they only depend on a time constant (τ) that is easy to handle through resistance and capacitor values. Nevertheless, for high-speed systems where frequency precision is very significant, the nonlinearities in the resistive and capacitive elements generate frequency variations. In consequence, crystal oscillators stand out

because of their 0.1 % error frequency.

The main drawback of crystal oscillators is their high start-up time and subsequent high Start-Up energy. In Megawer *et al.* (2019) authors report start-up energy of 133nJ while in Gomez *et al.* (2019) they report energy of $3 \cdot 10^{10}$ times better. Nevertheless, these start-up energy measures are important when the oscillator is operating in a switching on-off state.

Given these observations, this work presents a design methodology applied to a crystal oscillator design in 28nm CMOS technology; the oscillator can reach a 32.74KHz frequency with a frequency error of 854ppm. In spite to have the longest start-up time, this design is suitable for real-time clock (RTC) applications, and applications that have a constantly-on oscillator.

1. Objectives

1.1. General Objective

To study and design a crystal oscillator driver suitable for energy-efficient circuits.

1.2. Specific Objectives

To design a crystal oscillator driver in 28nm CMOS standard process regarding low power requirements.

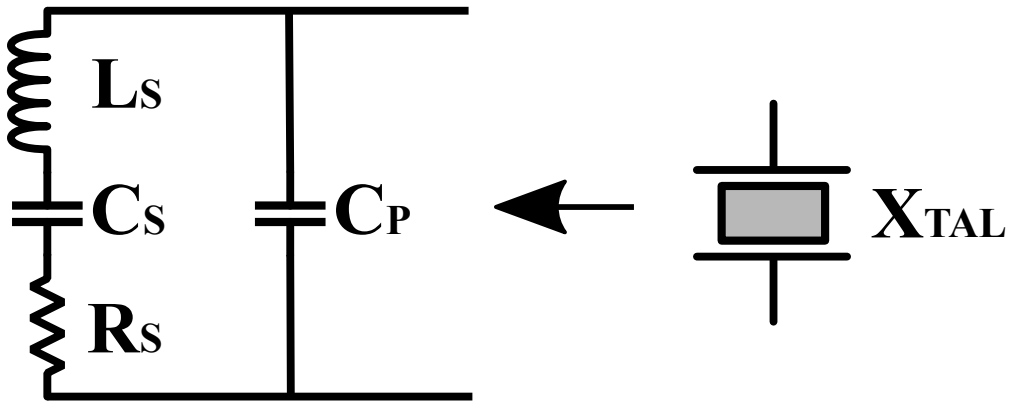
To validate the design performance using Monte Carlo and process, voltage, and temperature (PVT) corners simulations.

2. Crystal circuit modeling

XO uses a crystal usually made of quartz, if mechanical stress is applied along a specific direction or axis, a voltage is generated in a perpendicular direction in response to this stimulus. If an AC voltage is applied to the crystal, it changes its physical form, producing mechanical vibrations. This phenomenon between mechanical and electrical effects is called the piezoelectric effect. Applying a signal whose frequency is equal to the mechanical resonance frequency of the crystal will vibrate and just small voltages will be required to maintain these oscillations.

A quartz crystal resonator may be represented by its electrical equivalent circuit shown in Figure 1. Based on its resonant frequency the crystal can be represented as a series resonant RLC circuit where the motional inductance L_s is proportional to the mass of the mechanical resonator, the motional capacitance C_s is proportional to the inverse of its stiffness and the motional resistance

Figure 1.
Circuit modeling of the crystal employing its RLC series equivalent and the parallel capacitance C_p.

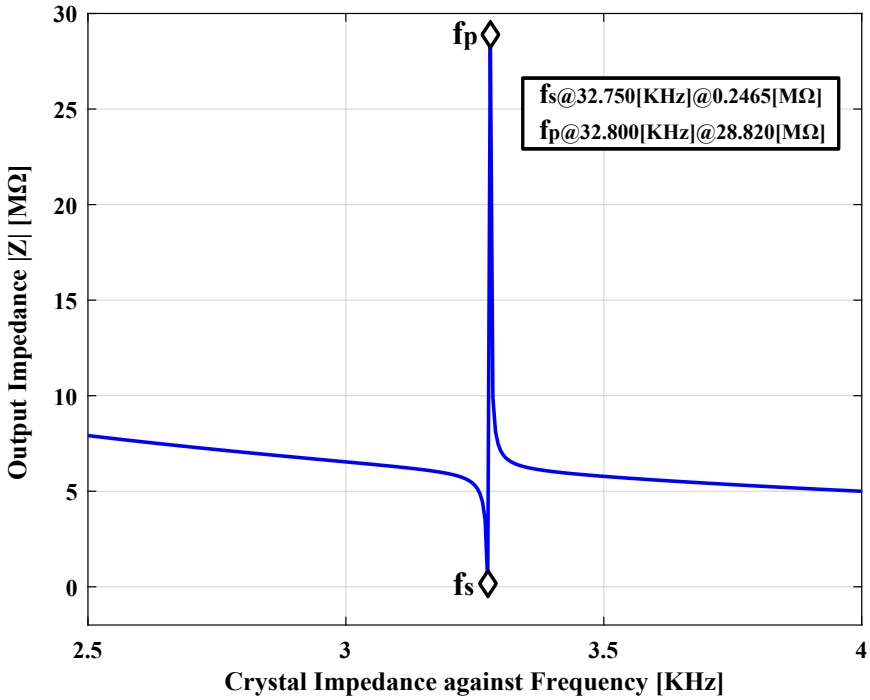


R_s represents the mechanical losses (Structures, xxxx). The resonant frequency f_s is damped by the series resistor R_s, which causes the quality factor Q to be finite. Note that at resonance the reactance of the inductor is equal to the reactance of the capacitor C_s. Actually, at resonance the series RLC circuit is just R_s, itself, the inductor L_s and capacitor C_s cancel each other.

In addition to this series RLC circuit, which represents the electro-mechanical operation of the crystal, a plate capacitance C_p has to be added. It is the capacitance between the two plates used to contact the crystal, with the dielectric constant of quartz (Sansen, 2007).

Taking into account the behavior of the equivalent impedance that the crystal has, for a

Figure 2.
Behavioral graph of the equivalent impedance of the crystal as a function of the frequency.



given frequency the interaction between the series capacitor C_s and the inductor L_s creates a series resonant circuit reducing the crystal impedance to a minimum value which corresponds to R_s. This point is called the series resonance frequency f_s and for frequencies before this point, the behavior of the impedance is capacitive. As the frequency increases above the f_s the impedance begins to have an inductive behavior until it reaches a point called the parallel resonance frequency f_p. At which point the inductor L_s and the capacitor C_p create a parallel LC tank and the impedance seen through the crystal reaches its maximum value. According to the above, depending on the characteristics of the circuit, the crystal may be operating at a series or parallel frequency, which Figure 2 demonstrates, showing the crystal impedance as a function of frequency. Equation 1 also show the dependence of the crystal parameters to obtain crystal impedance.

$$Z(s) = \frac{s^2 L_s C_s + s R_s C_s + 1}{s(C_s + C_p)(s^2 \frac{L_s C_s C_p}{C_s + C_p} + s \frac{R_s C_s C_p}{C_s + C_p} + 1)} \tag{1}$$

3. Mathematical analysis

For the design of the values that model the XO, the following equations are used, where equation 2 is the resonance frequency given by the LC tank.

$$f_s = \frac{1}{2\pi\sqrt{L_s C_s}} \tag{2}$$

and by its quality factor is given by equation 3

$$Q = \frac{1}{2\pi f_s C_s R_s} \tag{3}$$

Since the crystal modeling is based on an RLC series circuit, from the crystal datasheet, some data is taken. Through the equations, the values for L_s and C_s are calculated, and C_p and R_s are extracted from datasheet. Using the quality factor equation, the capacitor C_s in equation 4 can be calculated as a function of the frequency, the resistance R_s and the quality factor.

$$C_s = \frac{1}{2\pi f_s R_s Q} \tag{4}$$

Then for the inductance value, we have the equation 5 where the quality factor intervenes, the series resistance, and the nominal frequency of the crystal.

$$L_s = \frac{QR_s}{2\pi f_s} \tag{5}$$

A resonator composed of an LC tank would oscillate indefinitely over time. However, this is physically impossible since the inductors and capacitors commonly have an associated resistance which causes the decreased response of the resonator, which means that the oscillations over a specific time will stabilize at zero.

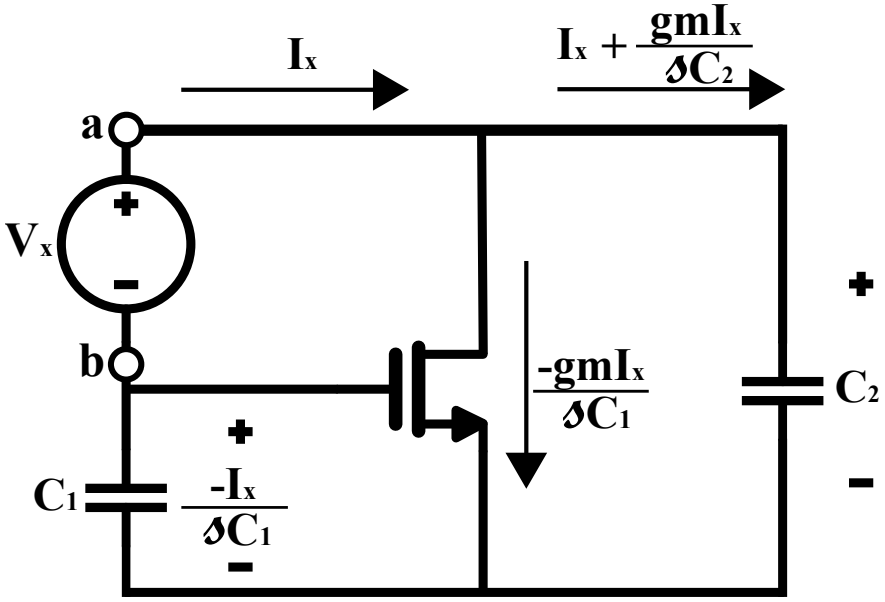
In resonance, the inductor impedance is equal in magnitude to the capacitor impedance, in

consequence, the equivalent of the crystal is resistive. According to the Barkhausen criterion, the impedance of the circuit must be equal to the impedance that the crystal represents to maintain oscillations. Therefore the only way to cancel the resistance of the crystal in resonance is obtaining a negative resistance which requires the use of active devices.

In Figure 3 there is a configuration of a common source with two capacitors C_1 and C_2 wherein the indicated terminals a and b, the equivalent of thevenin is applied to find the equivalent resistance provided by the circuit of the crystal driver.

$$V_x = I_x(1 + \frac{gm}{sC_1})\frac{1}{sC_2} + I_x\frac{1}{sC_1} \tag{6}$$

Figure 3.
Configuration for thevenin equivalent of the circuit with a single transistor where the negative resistance is extracted with currents and voltages depicted.



$$\frac{V_x}{I_x} = Z_{Th} = \frac{1}{sC_1} + \frac{1}{sC_2} + \frac{gm}{s^2 C_1 C_2} \tag{7}$$

Applying an LVK in the circuit depicted in Figure 3 we obtain equation 6, which represents the equivalent resistance of the circuit. As shown in equation 7, it is composed of three impedances, which represent each of the capacitors and the one provided by the transistor. Finally making an equivalent of the two capacitors we have the equation 8 and solving we have equation 9.

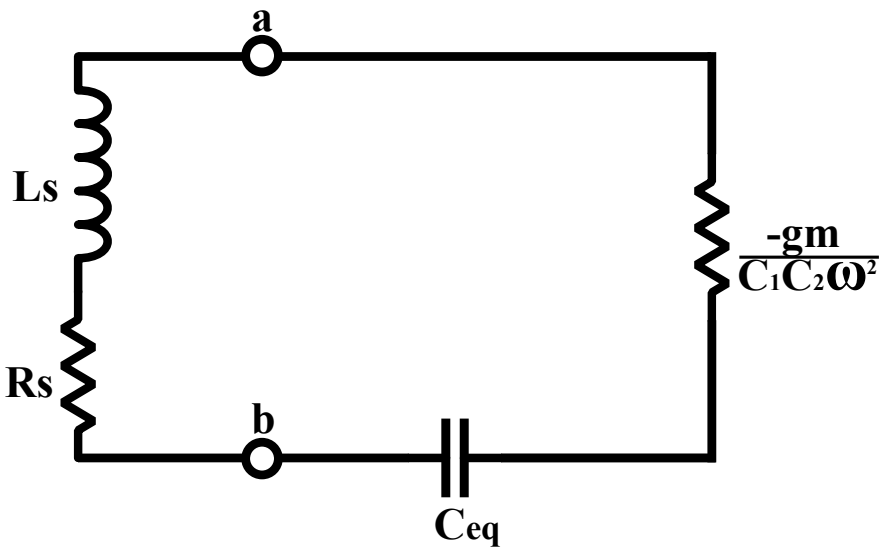
$$C_{eq} = \frac{C_1 C_2}{C_1 + C_2} \tag{8}$$

$$Z_{Th} = C_{eq} - \frac{gm}{C_1 C_2 \omega^2} \tag{9}$$

When the circuit in Figure 3 is operating under resonance conditions, its equivalent impedance is inductive, and connecting that to the Z_{Th} provided by equation 9 we have Figure 4. This indicates that the inductor reactance together with the reactance of the equivalent capacitor is canceled. Then the value of the series resistance must be equal to the resistance value obtained from the equivalent but with the opposite sign. This would ensure that the oscillations are maintained.

$$R_s = \frac{gm}{C_1 C_2 \omega^2} \tag{10}$$

Figure 4.
Simplified Thevenin equivalent assuming crystal modeling as inductance and series resistance.



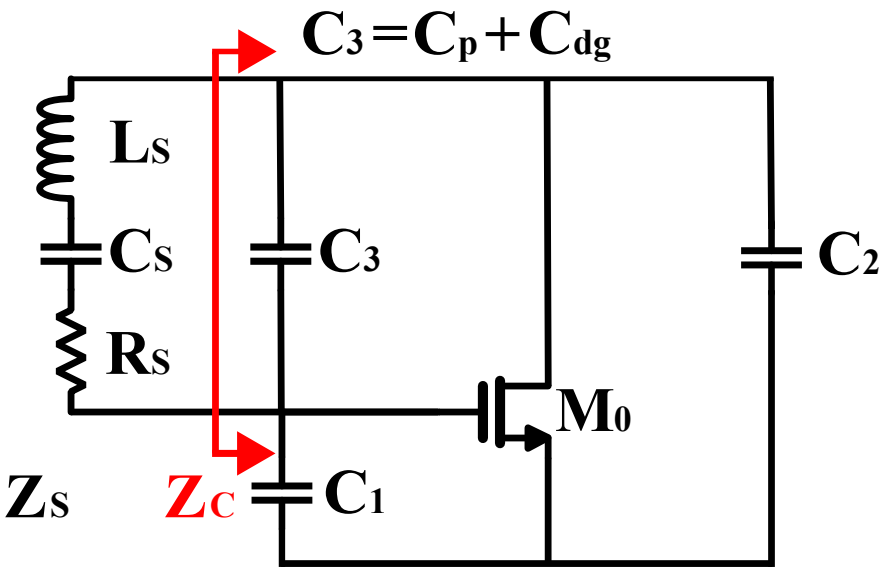
The equation 10 indicates that the value of the resistance R_s must be equal to the absolute value of the resistance extracted from the circuit in question. However, since R_s is already predefined by crystal datasheet, the parameter available to design is g_m which will be called critical gm (gm_{crit}) because it is the exact value that generates the oscillations. Then solving equation 10 we have equation 11.

$$gm_{crit} = R_s \omega^2 C_1 C_2 \tag{11}$$

4. Graphical analysis

Figure 5 is an equivalent circuit for the pierce configuration, where we will denote C_3 as the equivalent parallel capacitor between the crystal capacitance C_p and transistor parasitic capacitance

Figure 5.
Equivalent circuit taking into account that the capacitance C_3 is the parallel between the capacitances C_p and C_{gd}.

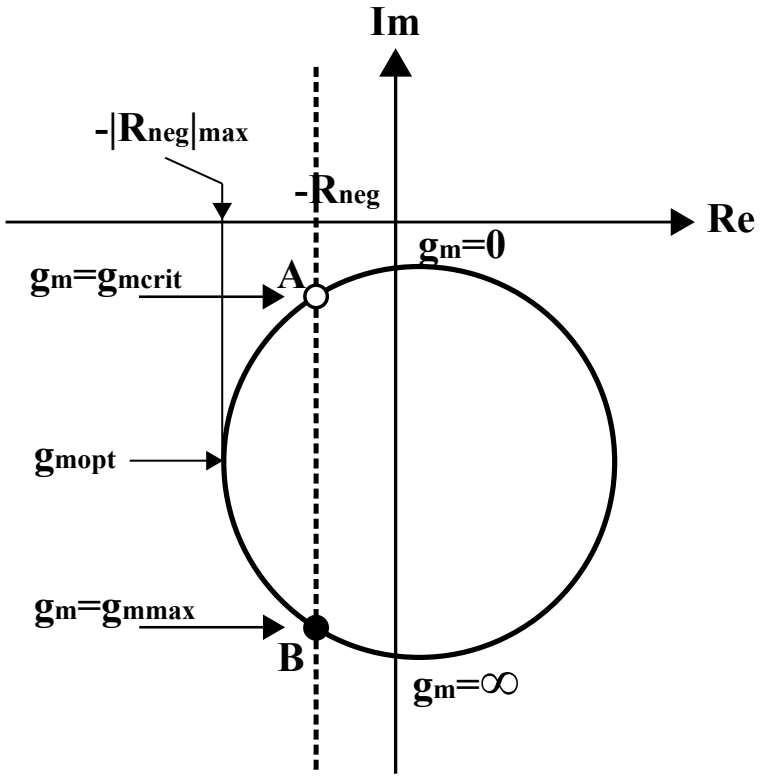


C_{gd}. In the graphical analysis method, the equivalent impedance represented by the circuit is plotted on a polar diagram in Figure 6. The representation is made in a semicircle that begins on the imaginary axis for a *gm* equal to zero and ends on the same axis for an infinite *gm*, where this semicircle intersects a vertical line that corresponds to the value of the negative resistance R_{neg}. The first condition to maintain the oscillations according to the Barkhausen criterion is fulfilled at point A, where the circuit presents a negative resistance R_{neg} that is exactly compensated by the crystal resistance R_s. On the other hand, the second condition tells us that at point A, the imaginary part gives us the pulling factor and therefore the current frequency (Sansen, 2007). Stable oscillations are reached for a well-defined point A and the circle must be large which now requires a small C_3. For a small pulling factor p, it is necessary to have large capacitors C_1 and C_2, both are usually taken of the same value, but large values for these capacitors imply a large current, therefore a

trade-off that must be taken into account, the pulling factor is given by.

$$p = \frac{C_s}{2(C_3 + \frac{C_1 C_2}{C_1 + C_2})} \tag{12}$$

Figure 6.
Locus diagram used in the graphical analysis for the crystal oscillation condition.



The pulling factor is a dimensionless parameter that indicates how far the current operating frequency is from the series resonance frequency. In this case, the operating frequency is 32.768KHz then the pulling factor is calculated employing the equation 12.

For the case shown in Figure 6 we can see point A and point B, however, this second point is unstable because it does not fulfill the conditions for phase stability, the only stable solution is the

intersection at A. For a specific value g_{mcrit} of g_m called çritical transconductance for oscillations". If g_m increases beyond g_{mcrit}, the oscillation will start to grow exponentially with a time constant τ_0 given by equation 13.

$$\tau_0 = \frac{-2L_m}{R_s + R_{neg}} = -\frac{2}{\omega^2 C_s} \cdot \frac{1}{R_{neg} + R_s} \tag{13}$$

A maximum value of the negative resistance is obtained for $g_m = g_{mopt}$, corresponding to a minimum value of the time constant τ_0. If g_m increases beyond g_{mcrit}, τ_0 starts to increase again until it becomes infinity at point B, for a $g_m = g_{mmax}$.

5. Survey, Topology Review and Selection

5.1. Short Topology Survey

To make a correct choice of the topology to be used for the XO, we start with a single transistor oscillator 3. However, taking into account that a transistor has three possible terminals, omitting the connection of the body, three possible connections can be obtained for the crystal. Configurations are analyzed in the following order: pierce, colpitts, and santos oscillator configuration.

5.1.1. Pierce Oscillator

In this configuration common source is used, in resonance, the crystal behaves like a very small resistor. Then the voltage at both the drain and the gate of the transistor are identical, the

output therefore can be either the drain or the gate of the transistor.

5.1.2. Colpitts Oscillator

In this type of oscillator, the gate of the transistor is grounded and the crystal is also grounded in one of its terminals. In this case, a single pin of the oscillator is connected to the drain of the transistor, then the configuration looks like a voltage follower and the output can only be taken from the source. The drain only carries a very small signal as it is connected to the ground by the crystal, which behaves like a small resistor.

5.1.3. Santos Oscillator

In this third type of oscillator, the drain is grounded, there is only one pin of the crystal connected to the transistor, in this case, the gate. Now the transistor looks like a cascode and the output can only be taken from the source again, the gate of the transistor is connected to the ground through the crystal which behaves like a small resistor.

The last two oscillator types are single-pin oscillators, which means that the crystal is grounded. This may add more parasitic capacitance in parallel to the crystal than the pierce oscillator. This is why pierce is often preferred even though it requires two pins for the crystal (Sansen, 2007).

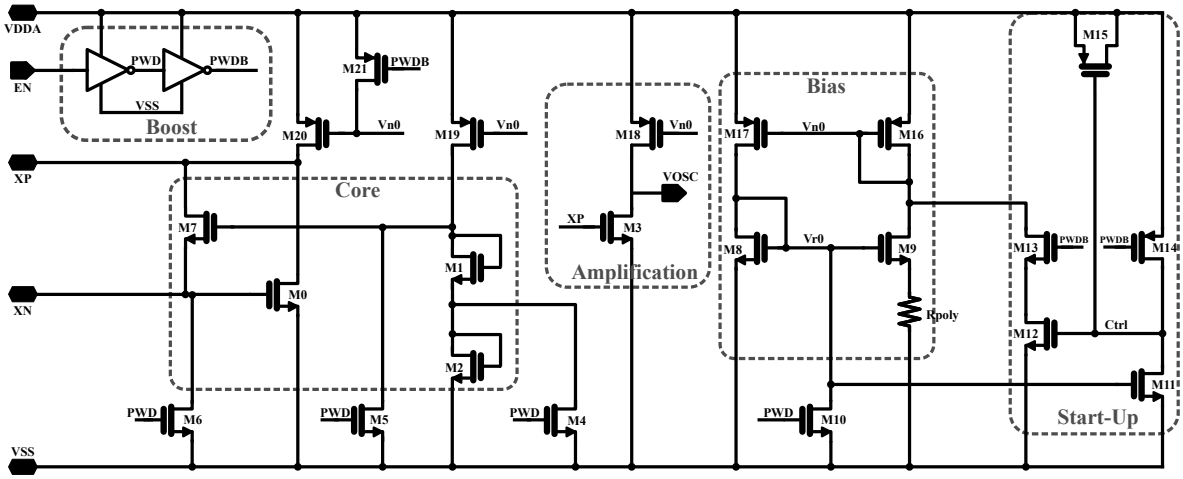
Table 1
Performance summary and comparison whit the state of the art.

	D. Yoon et. all. JSSC	M. Siniscalchi et. all. TCASI	A. Shrivastava et. all. JSCC	H. Esmaeelzadeh et. all. JSSC	K.-M. Kim et. all. JSSC	Y. Zeng et. all. VLSI	L. Xu et. all. ISSCC	This Work
Technology $[nm]$	180	130	130	65	55	55	40	28
Supply voltage $[V]$	0.94	0.06	0.94	0.5	0.3	0.4	0.45	1
Frequency $[KHz]$	32.767	32.763	32.76783	32.760	32.790	-	32.788	32.74
Load Capacitance$[pF]$	10 to 20	3	6	-	0.93	-	1.9	3.7
Steady state power$[nW]$	5,58	2,26	1,5	0,55	0,74	1,7	0,51	$1536{\cdot}10^3$
Temperature range $[°C]$	-20 to 80	25 to 62	0 to 80	-20 to 80	-20 to 80	-20 to 80	-25 to 85	-40 to 125
Resonance mode	Parallel	Parallel	Parallel	Series	Parallel	Parallel	Parallel	Series
Start-Up time$[ms]$	-	-	-	-	-	-	-	200
Start-Up Energy$[nJ]$	-	-	-	-	-	-	-	26.48
PN **1**$[KHz]$	-	-	-	-	-	-	-	-92.9
[dBc/Hz] **10**$[KHz]$	-	-	-	-	-	-	-	-98.53

5.2. Topology Used

For better understanding of the topology used, all the system is divided as follows: bias, core, start-up, amplification and boost modules which can be seen in Figure 7.

Figure 7.
Proposed topology for a XO where each of the modules of which it is composed can be seen integrated.



5.2.1. Bias

For polarization circuits, it is common to establish a DC reference, either a voltage or a current. These references must not be very susceptible or dependent on variations in voltage, process, and temperature, in consequence, a supply-independent biasing is used. This supply generates a reference current and an output current independent of the power supply where the output current is k times greater than the reference current (Razavi, 2001). In addition, a polysilicon resistor is used which fulfills two functions, one of them is to redefine the currents making the relation between the reference current and the output current be 1:1. The other function is that due to its material it keeps the nodes Vn0 and Vr0 stable against temperature changes. In addition, generate the reference current to the amplification stage and the core of the circuit.

5.2.2. Core

A single transistor pierce oscillator topology is applied with some changes. The feedback resistance is represented by M7 which must be polarized such that its value is larger. M0 must be polarized to generate a critical *gm* that together with the resistance of M7 fulfill the design conditions necessary to maintain the oscillations. Then, to guarantee the polarization of M7 we have the pair M1 and M2 which are polarized by a current mirror and ensure the high value of M7.

5.2.3. Start-Up

It uses a circuit with a power-down signal (PWD), this signal is used to keep the bias circuit in idle or reset mode. When the power down signal is asserted, nodes Vn0 and Vr0 are pulled to

VDD and VSS respectively, and hence no current flows into the reference circuit. The circuit should return to its normal operation when the PWD signal is de-asserted. This circuit is needed to either charge the node Vr0 or discharge the node Vn0, which initiates a current into the reference circuit until the circuit settles to its normal operating point.

Considering the circuit in Figure 7, the startup circuit comprises PMOS M14 and NMOS M13, M12, M11. When the PWD signal is asserted, M13 is off and M14 pulls node CTRL to VDD, which turns on M12. Since M12 is in series with M13, the startup current (Istart) that across M13 will be zero. The nodes Vn0 and Vr0 will be at VDD and VSS respectively. There will be no current in the reference circuit and M11 will be off. Now when the PWD signal is de-asserted, M14 is turned off and M13 is turned on. Since Vr0 is at VSS, M11 will remain off, and node CTRL will remain at VDD. This will cause M12 to remain on. A small capacitor of a few femto farads can also be added at node CTRL to avoid the possibility of getting it discharged due to any leakage current. Now both M13 and M12 are on and the current Istart starts flowing from the node Vn0, which will start discharging the node Vn0 from VDD towards VSS. This initiates a flow of current in M16 and M17. The flow of current in M17 will start charging the node Vr0 from VSS towards VDD causing a current flow in M9 and M8. As the voltage Vr0 reaches a value greater than V_{TH}(M11), M11 is turned on and pull node CTRL to VSS, hence turning off M12, which shuts off Istart. The value of the Istart depends upon the size of M12, which can be adjusted according to the required startup time (Khan *et al.*, 2003).

5.2.4. Amplification

XP signal is taken from the drain of M0, however, the excursion range of the signal is not large enough. For this reason, an amplification stage with a common source is used which takes XP and converts it into a rail to rail signal.

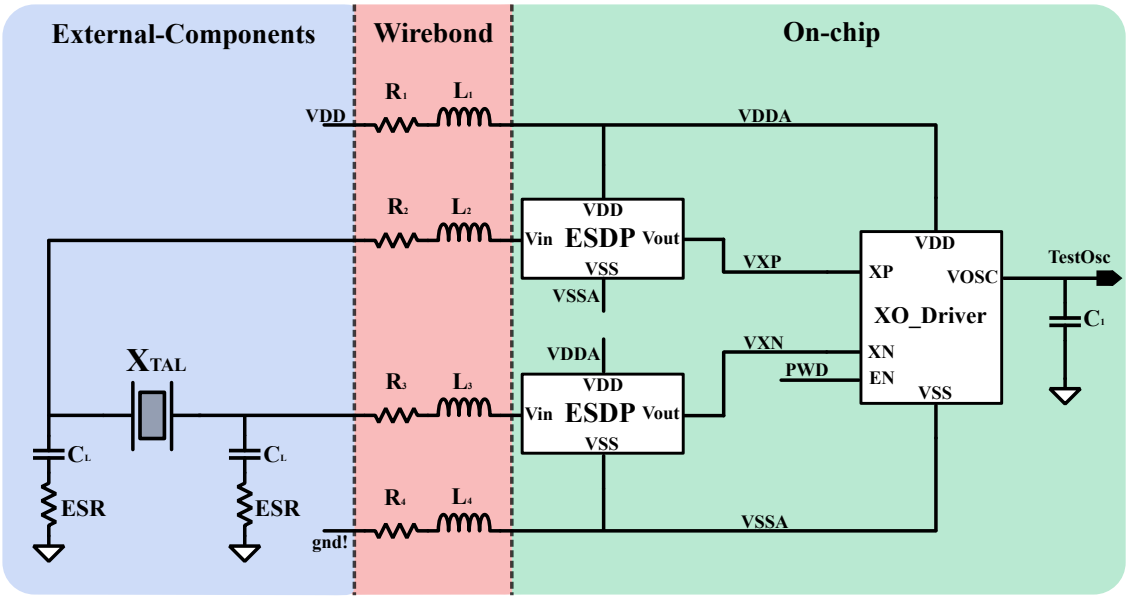
5.2.5. Boost

Two inverters are used which are in charge of giving strength to the power down signal coming from outside the circuit. This force provided to the inverters translates into reducing the rise and fall time of the signal from both PWD and PWDB.

6. Test bench

In the external components, we have C_L and ESR which are necessary for the datasheet specifications. Crystals typically require load capacitance C_L of a specific value to achieve frequency accuracy. If C_L is too low, the actual frequency will be higher than the target frequency, and vice versa. The equivalent series resistance ESR is the resistance that the crystal exhibits at the series resonant frequency f_s. It should not be confused with motional resistance R_s. ESR is typically specified as a maximum resistance value (in ohms) in the datasheet crystal. The RL components that model wirebond connections between the outside and inside part of the chip simulate the losses that these connections can generate. Moreover, the wirebond can be considered like a transmission line which represents the losses for high-frequency values(Tian *et al.*, 2019). In the On-chip area, we have electrostatic discharge protection (ESDP), these structures protect the input, output,

Figure 8.
Test bench used to carry out tests where using circuit elements the on-chip, wire-bond and external environment is simulated, on which the behavior of the driver designed in a real environment will depend.

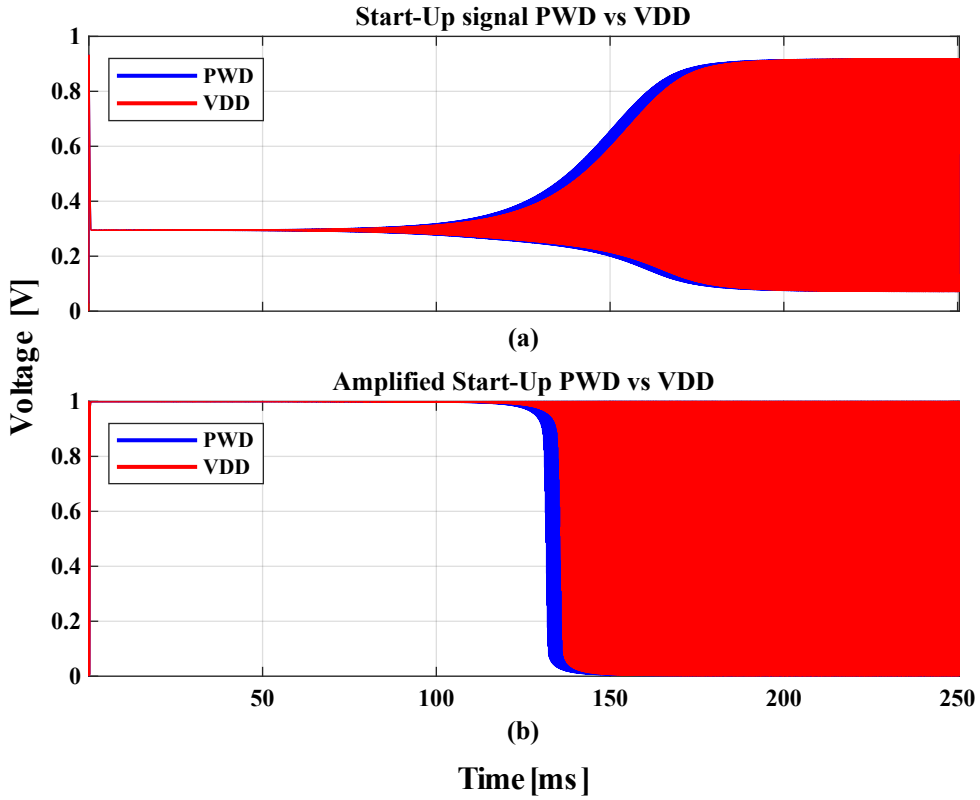


and power supply pins of the core circuit by providing a safe ESD discharge path to the ground bus/rail. These protection elements remain passive during regular operation of the protected device and activate only in the presence of an ESD pulse by detecting the rise time and the overvoltage. When an ESD pulse is detected, the protection circuitry will provide a safe discharge path for the ESD current.

7. Performance and Results

This XO was designed in a 28nm TSMC CMOS technology, the transistors used were standard transistors of the technology, and polysilicon resistance was used, whose function is described in section 5.2.1. Even though this design does not have a layout (due to the scopes of the project)

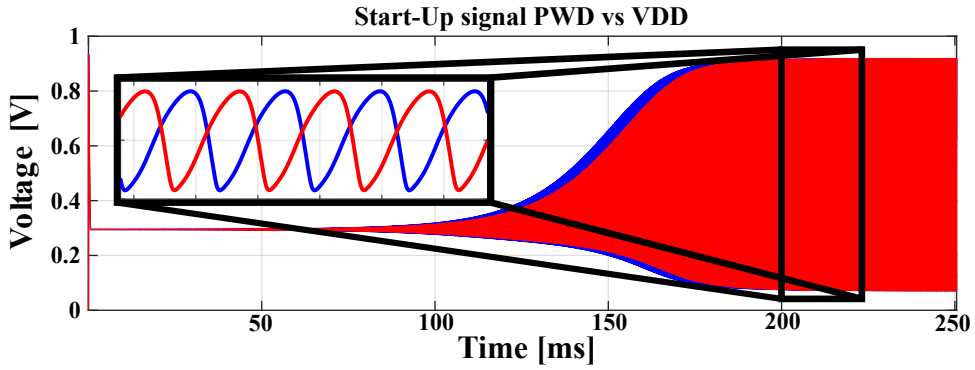
Figure 9.
Start-Up time measure PWD vs VDD (b) with amplification and (a) without amplification.



we have an estimated area of 16.7μm x 12μm, and a comparison with some designs in the state of the art is made in Table 1.

Regarding operating frequency, the XO reports 32.74KHz nominal against corners and 32.66KHz and 32.75KHz as maximum and minimum operating frequencies respectively, against monte carlo simulations. It reports an average of 32.51KHz and a standard deviation of 2.2584KHz, about the duty cycle of the oscillations against corners shows 38.66 % and in monte carlo simulations it shows an average of 45.98 % with a standard deviation of 8.45 %. Table 2 also shows the

Figure 10.
Transitory response from Start-Up time zoom measure PWD vs VDD.



summary results and Figure 10 shows a zoom of the transitory response of the oscillations.

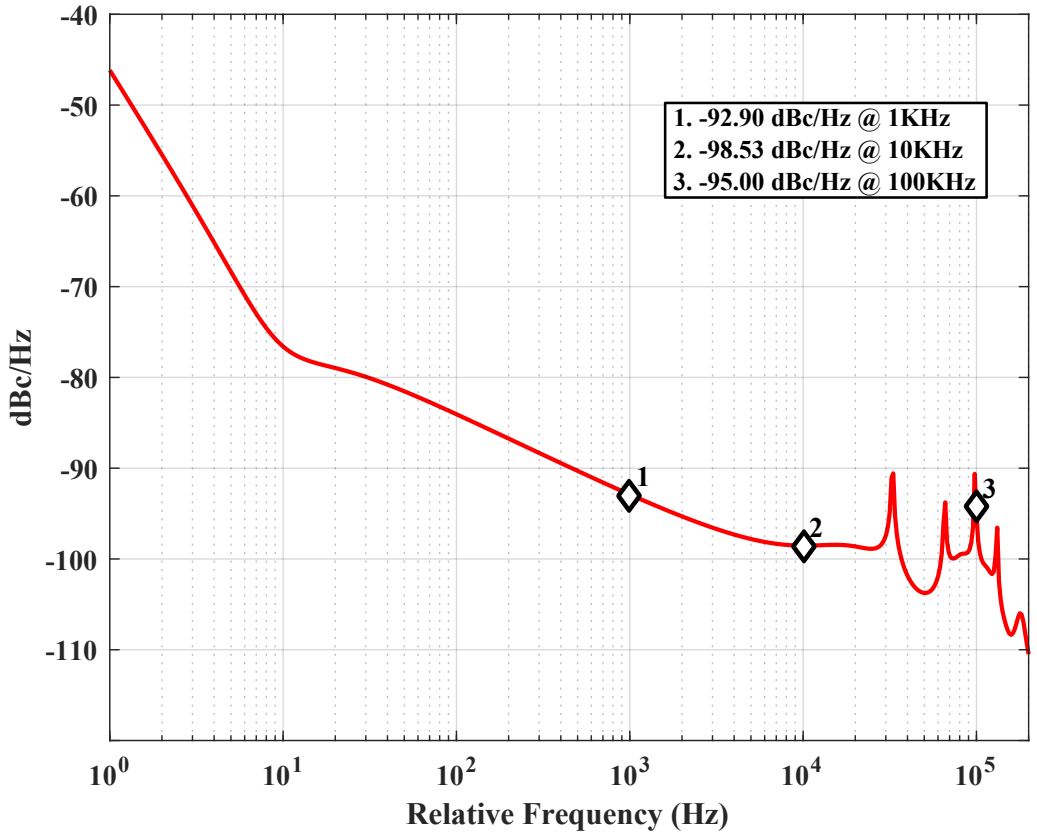
Despite reporting a very large start-up time, a significant decrease is seen in terms of the power dissipated by the XO in a steady-state, the trade-off that is present between these two variables is notable.

In the state of the art, it is found that the time to report for the start-up is the one seen in Figure 9 (a) which corresponds to the unamplified signal and its start-up is 200ms. However, in (b) it can be seen how the final signal that comes out of the amplified driver has a setting of 150ms.

In addition, when the simulation is done to measure the start-up time, the measurement is carried out in two different ways, one is by having PWD enabled, that is, the circuit is inactive, PWD is disabled and the time in which the crystal reaches rail to rail oscillations is measured in steady-state. The other way is to have PWD disabled but switching the power supply, that is, the supply goes from 0 to VDD and the result that is observed is that in Figure 9. When it is measured

by PWD the simulation decreases the time to enter steady-state and have oscillations, that if the simulation is carried out by switching VDD. This is because when it is done by PWD the nodes are already preloaded and ready to operate at the moment in which PWD is disabled, however when it is switched by VDD there is an additional time in which the nodes must wait to load and then operate normally. It is noteworthy that the start-up measurement made using the PWD or VDD activation differs by a time of 50ms, which can be observed in 9 (b).

Figure 11.
Phase noise for the designed XO, where the measurements for 1KHz, 10KHz, and 100KHz are shown.



A phase noise measurement was obtained in Figure 11 where the graph shows a measure in

Table 2
Design parameters and performance summary

CMOS process [nm]		28				
Oscillation frequency Target: 32.768[KHz]		**PVT**			**MC**	
		Typ	**Min**	**Max**	μ	σ
		32.74	32.72	32.76	32.74	5.505
Duty Cycle		38.21	35.32	48.64	40.94	10.49
gm Target: >3.3[μS]		8.383	6.367	10.68	8.346	2.155
Negative Resistance Target: >15[MΩ]		28.86	15.08	309.6	45.85	55.96
Supply Voltage [V]		1				
Steady state power [μW]		1.536				
Temperature Range [°C]		-40 to 125				
Start-Up time [ms]		200				
Start-Up Energy [nJ]		26.48				
CL [pF]		3.7				
PN [dBc/Hz]	**1[KHz]**	-92.9				
	10[KHz]	-98.53				
	100[KHz]	-95				

1KHz, 10KHz, and 100KHz and that compared to the state of the art in table 1 is high. To explain this (Megawer *et al.*, 2019) mentions two reasons. The first is that for oscillation amplitudes less than 200mV there is a degradation of the phase noise, however, this is not the case since the amplitude of the oscillations reaches 850mV of amplitude before the signal passes through the amplification stage; the second reason is that when it is working with short channel devices this can degrade the signal. Although we may be able to use long channel devices to mitigate these second-order effects this would impact the area of the design.

8. Conclusion

In this work, a modularized XO was presented and designed in TSCM 28nm CMOS technology obtaining an operating frequency of 32.74KHz. With this frequency, an error of 854ppm was obtained which translates to an error lower than 1 %.

The fact that this crystal oscillator is designed to be a system-on-chip that never turns off, We focused on power consumption due to the start-up time of the crystal oscillator does not impact the steady-state power consumption. Nevertheless, indeed, the RL series component that simulates wirebond is not fundamental in the test bench because this crystal is about low power consumption, and the current that we extract from the supply is small; therefore the oscillations produced by these components are not so large.

An observation is made regarding the relationship that exists between the start-up and the core modules. As mentioned in the start-up section, M12 is dimensioned in such a way that start-up time can manipulate the response of the circuit. Therefore adjusting this transistor implies a mismatch in the core against corners. Because it takes M7 out of their operating point and causes it not to be fulfilled in all corners. Therefore as M7 represents the feedback resistance whose value is a design condition to sustain the oscillations, the design of this transistor was thorough to avoid that process, voltage and temperature changes did not affect the system behavior.

Bibliografía

Esmaeelzadeh, H. & Pamarti, S. (2019). 18.4 a 0.55nw/0.5v 32khz crystal oscillator based on a dc-only sustaining amplifier for iot. En *2019 IEEE International Solid- State Circuits Conference - (ISSCC)*, pp. 300–301.

Gomez, H., Arenas, J., Rojas, C., Reyes, D., Mantilla, A., & Roa, E. (2019). Oscillator with 72 / 6pJ Start-up Energy. *2019 IEEE Custom Integrated Circuits Conference (CICC)*, pp. 1–4.

Khan, Q. A., Wadhwa, S. K., & Misri, K. (2003). Low power startup circuits for voltage and current reference with zero steady state current. En *Proceedings of the 2003 International Symposium on Low Power Electronics and Design, 2003. ISLPED'03.*, pp. 184–188. IEEE. https://doi.org/10.1109/LPE.2003.1231859.

Megawer, K. M., Pal, N., Elkholy, A., Ahmed, M. G., Khashaba, A., Griffith, D., & Hanumolu, P. K. (2019). Reduction Using 2-Step Injection in 65nm CMOS. *2019 IEEE International Solid-State Circuits Conference - (ISSCC)*, 64(5):2018–2020.

Razavi, B. (2001). *Design of Analog CMOS Integrated Circuits*. Tsinghua University Press Co.

Sansen, W. M. (2007). *Analog design essentials*, volumen 859. Springer Science & Business Media.

Structures, M. B. (xxxx). *Foundations of Oscillator Circuit Design*. yyyyy.

Tian, W., Cui, H., & Yu, W. (2019). Analysis and experimental test of electrical characteristics on bonding wire. *Electronics (Switzerland)*, 8(3). https://doi.org/10.3390/electronics8030365.