DESIGN OF AN ANALOG TO DIGITAL CONVERTER (ADC) IN A 28 NM CMOS PROCESS

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Degree work presented as a requirement to qualify for the title of Electronic Engineer

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Dedicated to our families and friends.

And to our team, with whom we started and finished this amazing journey.

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I would like to thank the people who have contributed significantly to this project. First of all, my family for their unconditional support and important teachings, especially my mother, who helped me discover my vocation and the value of university in my life.

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- Jorge Eduardo Angarita Pérez

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Finally, I want to thank my entire family, especially my parents, who always stood by my side, supporting me every step of the way and are the reason I am obtaining this university degree today.

- Nicolás Orcasitas García

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RESUMEN

TÍTULO: DISEÑO DE UN CONVERSOR ANÁLOGICO A DIGITAL (ADC) EN UN PROCESO CMOS DE 28 NM [*]

AUTORES: JORGE EDUARDO ANGARITA PÉREZ
NICOLÁS ORCASITAS GARCÍA [**]

PALABRAS CLAVE: ADC, SAR, ENOB, SINAD, Monotonic Switching.

DESCRIPCIÓN:

El grupo de investigación Onchip de la Universidad Industrial de Santander (UIS) ha diseñado en los últimos cinco años tres generaciones diferentes de sistemas en chip (SoC) en un proceso CMOS de 180 nm. Recientemente, se ha empezado el desarrollo de una nueva familia de microcontroladores, la cual se implementará en un nodo tecnológico de 28 nm. Esto cambio trae consigo nuevos desafíos en la implementación de los diferentes bloques constitutivos de este sistema, que se ven reflejados en las especificaciones del circuito, en la metodología de diseño, y el conexionado (layout) de los mismos.

En este trabajo se trabaja con un conversor analógico a digital (ADC), que como su nombre lo indica, es un componente fundamental para la comunicación entre el mundo exterior (señales analógicas) y el sistema integrado (información digital). Debido a lo anterior, para el diseño de este circuito se priorizaron las métricas asociadas a la velocidad de operación, a la precisión de la información transmitida, la linealidad y al consumo, siendo estas respectivamente la frecuencia de muestreo, la cantidad efectiva de bits (ENOB), no-linealidad integral (INL) y diferencial (DNL), además de la potencia promedio.

Finalmente, el diseño propuesto es validado mediante el monitoreo de las especificaciones a través de simulaciones de corners de proceso, voltaje de alimentación y temperatura (PVT), de variaciones estadísticas utilizando el método de *Monte Carlo* y de efectos parásitos post-layout.

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[*] Trabajo de Grado

[**] Facultad de Ingenierías Físico-Mecánicas. Escuela de Ingenierías Eléctrica, Electrónica y de Telecomunicaciones. Director: HUGO DANIEL HERNÁNDEZ HERRERA

ABSTRACT

TITLE: DESIGN OF AN ANALOG TO DIGITAL CONVERTER (ADC) IN A 28 NM CMOS PROCESS [*]

AUTHORS: JORGE EDUARDO ANGARITA PÉREZ
NICOLÁS ORCASITAS GARCÍA [**]

KEYWORDS: ADC, SAR, ENOB, SINAD, Monotonic Switching.

DESCRIPTION:

The Onchip research group at the Industrial University of Santander (UIS) has designed three different generations of System-on-Chip (SoC) over the last five years in a 180 nm CMOS process. Recently, the development of a new family of microcontrollers has started, to be implemented in a 28 nm technological node. This change brings along new challenges in implementing the various constituent blocks of this system, which are reflected in the circuit specifications, design methodology, and their layout.

This work involves working with an analog-to-digital converter (ADC), which, as its name suggests, is a fundamental component for communication between the outside world (analog signals) and the integrated system (digital information). Due to this, the design of this circuit prioritized metrics associated with operating speed, accuracy of transmitted information, linearity, and consumption, respectively: sampling frequency, effective number of bits (ENOB), integral and differential non-linearity (INL and DNL), as well as average power.

Finally, the proposed design is validated by monitoring the specifications through simulations of corner process variations, power supply voltage, and temperature (PVT), statistical alterations usign the *Monte Carlo* method, and post-layout parasitic effects.

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[*] BSc Thesis

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INTRODUCTION

Nowadays, a significant portion of signal processing tasks are performed in the digital domain, which has historically demonstrated greater simplicity in the implementation of the various computational processes required for this purpose. However, the use of a different information domain poses several challenges, since the real world is still fundamentally analog, and the signals it contains are continuous, so intermediate processes are needed to facilitate the bidirectional flow of information.

In this context, circuits known as data converters arise, whose function is to transform information, represented as electrical variables such as voltage or current, between the aforementioned domains. Because of this, two distinct devices are identified: ADCs, responsible for the transformation of analog to digital signals, crucial for various sensing systems and/or reception of external signals; and DACs, which perform the reverse process and are commonly used for trimming or process control tasks.

With this in mind, the OnChip research group at the Universidad Industrial de Santander is currently working on the design of a new microcontroller to be implemented in a system-on-chip (SoC) with 28 nm CMOS technology. This project consists of several essential components, including a power management unit (PMU) responsible for managing the system's energy resources, the processor that acts as the central processing unit, and the peripherals that facilitate the processor's interaction with external components. Among these peripherals are the aforementioned analog-to-digital converters (ADC) and digital-to-analog converters (DAC).

In this project, it will be mainly focused on the design of the ADC, which is the focus of this paper. To do so, it will start with initial specifications that include the ADC resolution, which determines the number of bits used to digitally represent each signal;

the sampling frequency, which indicates the converter's operating speed; the effective number of bits (ENOB), which quantifies how much bits of information the converter actually handle; the differential and integral nonlinearity, which evaluates to what extent the ADC's behavior deviates from the ideal case; and finally, the power, which represents the consumption required by this component.

Once the project requirements have been defined, it is necessary to establish a suitable architecture capable of satisfying them. For this purpose, an initial literature review will be carried out to compare the performance of different architectures. Subsequently, the implementation of all the blocks that make up the chosen topology will be carried out, taking into account different design considerations to meet the specifications of the entire system. This will be followed by an initial validation in simulation to verify that the specifications have been met.

Finally, when this steps have been completed, the physical connection scheme of the different layers of the ADC, known as the circuit layout, will be presented. From this layout, an improved model of the converter will be generated, taking into account various parasitic effects introduced due to the interconnections. After confirming its performance through a round of post-layout simulation verification, the design process will be completed, allowing the fabrication of this circuit.

OBJECTIVES

0.1. General Objectives

- To design an Analog to Digital converter (ADC) using SAR topology for a System-on-Chip (SoC) in a 28nm standard CMOS process.

0.2. Specific Objectives

- To study and define the circuit specifications for the selected ADC topology based on the system requirements for a SoC in a standard TSMC 28nm CMOS process design kit.
- To design every block required for the construction of an ADC for a SoC using a 28nm CMOS standard process.
- To validate the performance of the design of each block used for the entire ADC system using different types of simulations such as Monte Carlo, post-layout and process, voltage, and temperature (PVT) variation corners.

1. ANALOG TO DIGITAL CONVERSION

An analog-to-digital converter (ADC) is a circuit that transforms continuous voltage or current signals into a binary code proportional to the sampled input, thus allowing a digital circuit to process this data later. The performance of this process is defined by different parameters related mainly to its speed and the quality of the information transmitted, which are crucial in the design process. These metrics will be explained below. Starting from its definition based on an ideal ADC and subsequently including some effects that influence the conversion process in a real implementation.

1.1. Ideal ADC

An ADC transfer function is depicted in Figure **1.1**, illustrating the behavior of the V_{out} vs. V_{in} function plotted for $N = 3$ Bits. This function is defined only between $V_{in,max}$ and $V_{in,min}$, and its difference is known as the *Full-scale range* (FSR) of the converter [1]. Additionally, its staircase shape reveals one of the primary limitations in A/D conversion, involving the unavoidable loss of information when collapsing a real value into a discrete variable. Consequently, the parameter of the Least Significant Bit (LSB or sometimes simply Δ) is defined as the width of each step in the transfer function [1]:

$$LSB = \frac{V_{in,max} - V_{in,min}}{2^N} \tag{1}$$

With this value, measured in volts $[V]$, it is determined that the ideal ADC output will always be an integer multiple of one LSB. Consequently, the maximum possible quan-

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[1] Walt KESTER. "Chapter 2: Fundamental of Sampled Data Systems". In: *Data Conversion Handbook*. Ed. by Walt KESTER. Burlington: Newnes, 2005, pp. 57–143. DOI: https://doi.org/10.1016/B978-075067841-4/50010-5.

tization error between the obtained output and the real value is $0.5LSB$.

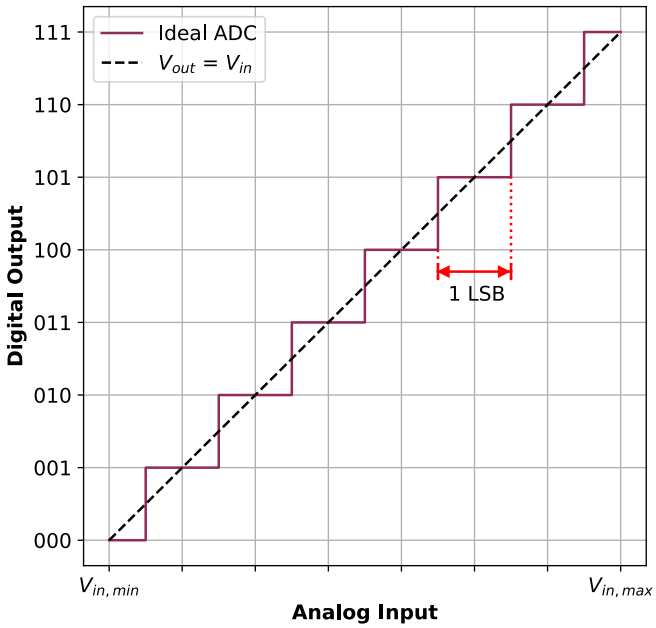

Figure 1.1. ADC ideal transfer function.

Starting from the LSB idea, the concept of quantization noise is also defined from the subtraction between the ideal $V_{out} = V_{in}$ curve and the transfer function in **1.1**, resulting in a triangular signal with an amplitude between $\pm 0.5LSB$. This signal can be used to determine the total quantization noise power with its mean square error [2]:

$$P_{noise} = \frac{1}{T}\int_{0}^{T} e^2(t)\,dt = \frac{LSB^2}{12} \tag{2}$$

Additionally, if the input is a sinusoidal signal with an amplitude equal to the ADC's full-scale range, meaning it is equal to $0.5(V_{in,max} - V_{in,min})$, the power of the AC component

[2] TEXAS INSTRUMENTS. *Understanding Data Converters*. Application Report. Published in Mixed-Signal Products. Texas Instruments, 1995.

will be equal to the following expression:

$$P_{signal} = \frac{(V_{in,max} - V_{in,min})^2}{8} \tag{3}$$

Then, the signal to quantization noise ratio is defined as the value in decibels of the quotient between (2) and (3). This can be approximated as the following expression:[2]

$$SQNR = 10log(\frac{P_{signal}}{P_{noise}}) \approx 6.02N + 1.76 \tag{4}$$

1.2. Non-Linearities in A/D Conversion

During the physical implementation of an ADC, several effects arise that cause its behavior to deviate in various ways from the ideal case [3]. Primarily, these phenomena affect the system's linearity, resulting in distortion in the output signal, as observed in its spectral representation such as in Figure **1.2**, where a portion of the power of its fundamental harmonic is distributed among different higher-frequency components.

Because of this, two new metrics are defined based on the signal-to-noise ratio. The first one is the *Spurious Free Dynamic Range* (SFDR)[3], which essentially measures the ratio between the signal power and the highest unwanted component (spur), whether it's a harmonic or noise. It is also measured in dB and can be graphically determined, as shown in the Figure **1.2**.

The second one is the *Signal to Noise and Distortion Ratio* (SNDR or SINAD) [4], which represents the quotient between the signal power and the sum of the noise power and

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[3] Bonnie BAKER. *A Glossary of Analog-to-Digital Specifications and Performance Characteristics*. Application Report. Published in Data Acquisition Products. Texas Instruments, Oct. 2011.

[4] Eduardo BARTOLOME. "Understanding and Comparing Datasheets for High-Speed ADCs". In: *Analog Applications Journal* (2006). High-Speed ADC Systems and Applications Manager.

any additional harmonic components.

$$SNDR = 10log(\frac{P_{signal}}{P_{noise} + P_{distorsion}}) \tag{5}$$

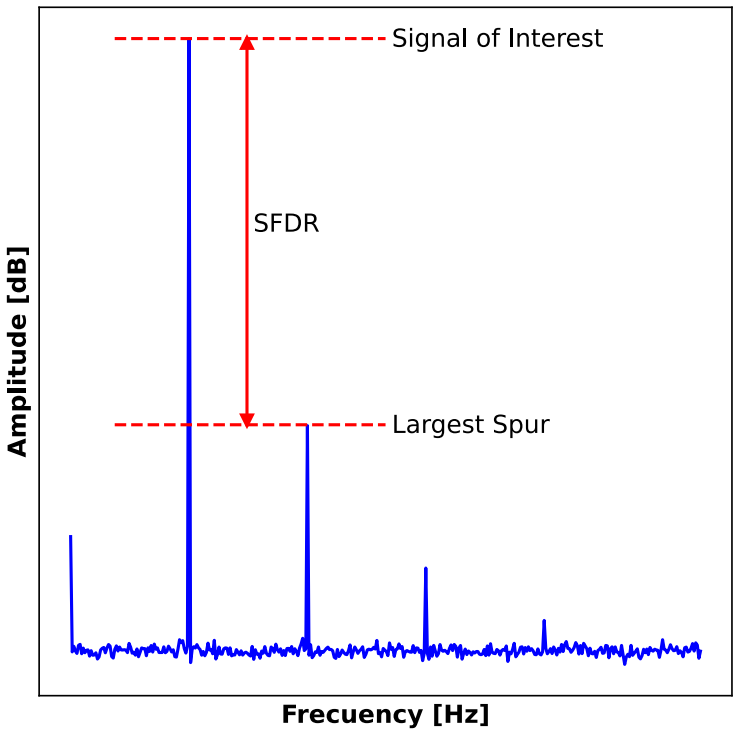

Figure 1.2. Distortion in the ADC output spectrum.

Making a comparison with the equation in (4), it can be observed that the SNDR will always be less than the SQNR. This can be interpreted as if the system's bits were fewer than they actually are. Because of this, a new specification is defined, called the *effective number of Bits* (ENOB)[3], which by this logic is given by:

$$ENOB = \frac{SNDR - 1.76}{6.02} \tag{6}$$

In addition to frequency effects, non-linearity also affects the transfer function seen before in the Figure **1.1**, causing the length of each step to not be the same[2], and differ from 1 LSB , as can be seen in Figure **1.3**.

From this phenomenon arise two additional metrics too, the first of them is the *Differential Non-Linearity* (DNL)[2], for the k-th step is defined as its width minus 1 LSB, in this case it will be:

$$DNL_k = \widetilde{X}_{k+1} - \widetilde{X}_k - LSB \tag{7}$$

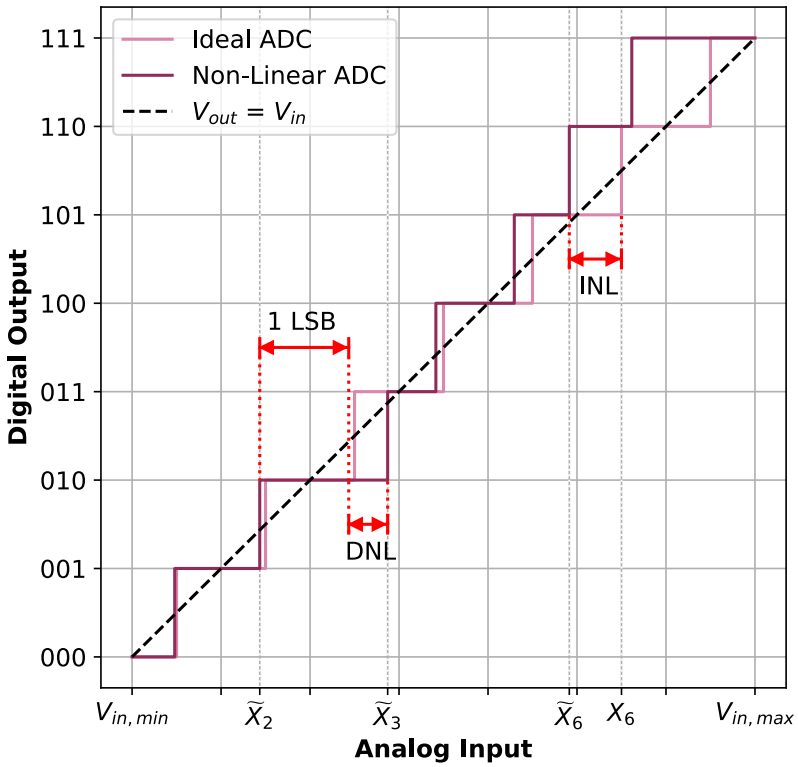

Figure 1.3. Non-linearities in the ADC transfer function.

On the other hand, the *Integral Non-Linearity* (INL) [2] of the k-th step is defined as the difference between the real ($\widetilde{X}$) and ideal (X) transition. Then:

$$INL_k = \widetilde{X}_k - X_k \tag{8}$$

It's worth noting that both specifications are measured in terms of LSB, and during their measurement, they are plotted against all possible output codes of the converter.

1.3. Nyquist Sampling Theorem

As mentioned initially, the A/D conversion process always results in a loss of information from the continuous input due to the finite number of values at the output. A similar phenomenon occurs in time because regardless of the architecture used, the circuit will take a certain amount of time to deliver the final bit sequence. Hence, the ADC will have to *sample* the input, leading to discretization in this domain as well.[1]

The interval between two consecutive samples is referred to as the *sampling period* (T_s), while its multiplicative inverse is known as the *sampling frequency* (F_s). This value imposes limits on the bandwidth of the input signal. Specifically, according to the Nyquist sampling theorem[1], the maximum allowed input frequency f_{in} cannot exceed the limit specified in equation (9).

$$\frac{f_s}{2} \geq f_{in} \tag{9}$$

If the above conditions are not met, the input signal will suffer from overlapping in its spectral components, causing its higher frequency components to become indistinguishable from those of lower frequency in a process known as *aliasing*, resulting in the loss of this information at the output. [1]

1.4. Power Considerations

One of the most crucial parameters in ADC design is its energy efficiency. Despite it is not directly associated with the conversion quality, it holds vital significance from the perspective of the overall integrated circuit, as its power consumption usually represents a significant percentage of all the blocks of an SoC [5] significantly impacting this metric, especially in portable systems. In such cases, the ADC typically accounts for

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[5] Hui WANG et al. “A Battery-Powered Wireless Ion Sensing System Consuming 5.5 nW of Average Power”. In: *IEEE Journal of Solid-State Circuits* 53.7 (2018), pp. 2043–2053. DOI: 10.1109/JSSC.2018.2815657.

the majority of power cost. [6]

According to circuit theory, the instantaneous power of any circuit component can be determined as the product of its voltage $v(t)$ and its current intensity $i(t)$.

$$p(t) = v(t)i(t) \tag{10}$$

However, since this value changes over time, it is preferred to work with two associated metrics: the arithmetic mean (AVG) and the root mean square (RMS)[7]. These are defined as follows:

$$P_{AVG} = \frac{1}{T}\int_0^T p(t)\,dt \tag{11}$$

$$P_{RMS} = \sqrt{\frac{1}{T}\int_0^T p^2(t)\,dt} \tag{12}$$

Where T represents the temporal period of the power function. As inferred from the previous section, it is equivalent to the ADC sampling frequency or a multiple of it, allowing for the analysis of this variable's evolution over multiple cycles.

Finally, the energy per conversion parameter is introduced, measured in pJ, and commonly used to compare the energy consumption of different types of ADCs [8]. This parameter represents the ratio between average power and sampling frequency.

$$E_{Conv} = P_{AVG}/F_s \tag{13}$$

---

[6] Wilmar CARVAJAL OSSA. "Configurable Analog-to-Digital Converter Design Integrated in CMOS Technology". Degree work. Universidad Industrial de Santander (UIS), 2007.

[7] Doug ITO. "RAQ Issue 177: RMS Power vs. Average Power". In: *Analog Dialogue* 54.2 (May 2020).

[8] Boris MURMANN. *ADC Performance Survey 1997-2023*. [Online]. Available: `https://github.com/bmurmann/ADC-survey`.

The upcoming chapters will outline the progression of the project. Chapter two will show the chosen architecture, reveiwing its operational principles and the necessary subcircuits for its implementation. Chapter three will provide an overview of the design process for each constituent block, clarifying all design considerations and schematics. Chapter four will consolidate all achieved results, comparing them to other ADCs presented in the literature, and will present the final layout along with its dimensions. Lastly, chapter five will present conclusions and future work.

2. ADC TOPOLOGY AND SPECIFICATIONS

2.1. Typical Architectures

When it comes to implementing an ADC, there are various types of architectures to consider, each with its own set of advantages and disadvantages. As a result, the selection of the topology becomes highly dependent on the required specifications.

In Figure **2.1**, a graph comparing various ADC designs from the literature[8] is depicted. This graph correlates the SNDR (as a measure of system linearity) with the conversion energy mentioned in (13), highlighting the type of topology used with different colors.

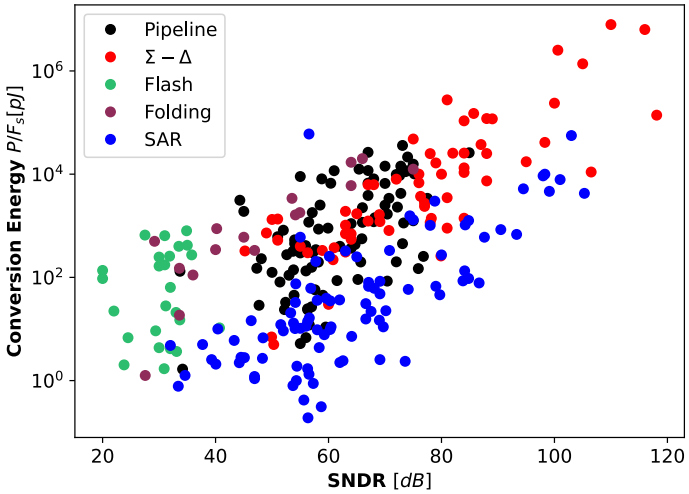

Figure 2.1. ADC linearity and energy comparison.[9]

Analyzing the trends between the different architectures, it is observed that the *flash* topology presents moderate to low power consumption. However, it maintains a low SNDR, leading to a lower effective number of bits (ENOB). In contrast, the ADCs *Sigma-Delta* and *Pipeline* achieve high linearity, but at the expense of higher power consumption. Finally, *Folding* and *Successive Approximation Register (SAR) ADC* fall between the two metrics, with the latter demonstrating better overall energy efficiency.

2.2. Design Specifications

The design specifications for the proposed ADC are shown in Table 2.1, detailing the minimum, maximum, or the typical expected value, as appropriate, for the each metric:

Table 2.1. Design specifications

Parameter	Min	Typ	Max
V_{DD} [V]	1.62	1.8	1.98
F_s [MHz]	-	-	10
Resolution [bits]	-	10	-
ENOB [bits] @$F_{in} = F_s/10$	9	-	-
DNL [LSB]	-	-	0.7
INL [LSB]	-	-	0.8
P_{AVG} [mW]	-	-	1

2.2.1. Selected Architecture From the specifications summarized in Table **2.1**, the SNDR can be calculated using Equation (6), resulting in approximately $56[dB]$. In addition, the energy consumption of the proposed ADC, calculated using Equation (13), is $100[pJ]$. Plotting these values in Figure **2.1**, positions this design in a ”transition” region between the *SAR* and *pipeline* converters. However, since the ADC is applied to a general-purpose system-on-chip, where power resources are shared, the *SAR* topology emerges as a superior choice. This is shown in the graph, as the different SAR designs tend to reduce the conversion energy while maintaining the same linearity.

2.3. SAR ADC Topology

A Successive Approximation Register (SAR) ADC is a type of converter that utilizes the binary search algorithm to identify the optimal code corresponding to an unknown analog value within its full-scale range, in this case, $\pm V_{Ref,P}$. Its operational principle is illustrated in the in the simplified diagram of the Figure 2.2.

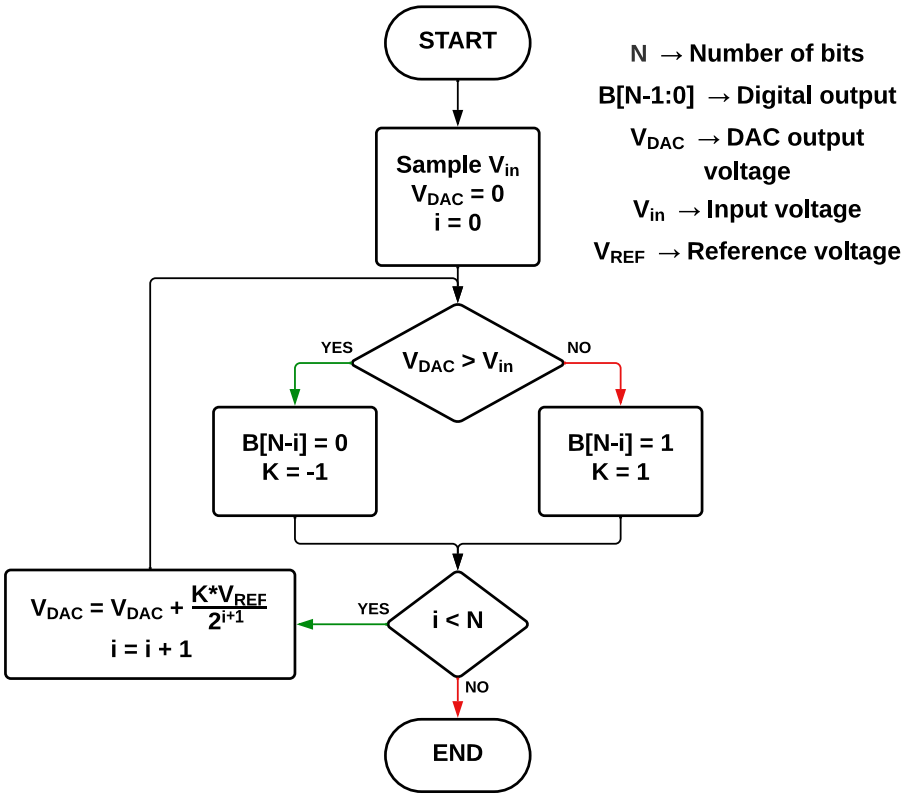

Figure 2.2. SAR ADC Binary Search Algorithm.[10]

Initially, the input voltage V_{in} undergoes sampling and comparison with V_{DAC}, set to half of the entire range, being equal to $0[V]$. This determination establishes the first bit value that encodes the input polarity. Subsequently, the process involves halving the search interval (either positive or negative based on the comparison result), recalculating V_{DAC} by employing the mid-value of this updated range. This iterative procedure repeats for N cycles,[11] eventually converging to a V_{DAC} value with an absolute error from V_{in} that is less than or equal to $0.5LSB$.

[11] David Alejandro REYES GONZALEZ. “Projeto de um Conversor Analógico-Digital para um Receptor UWB Aplicado na Detecção de Câncer de Mama em Tecnologia CMOS”. Tesis de Maestría. São Paulo: Escola Politécnica da Universidade de São Paulo., 2021.

2.3.1. SAR ADC Implementation For the realization of the previous algorithm are necessary four fundamental components[11], as shown in the simplified diagram of the Figure **2.3**:

- **Sample & Hold Circuit**: This block samples the input signal (in this case the difference between V_{iP} and V_{iN}) at the start of every conversion, holding it for the rest of the process.
- **Capacitive DACs (CDACs)**: This block serves two functions: firstly, it operates as a capacitive load required for the *Sample & Hold*, and secondly, it generates V_{DAC} through charge redistribution using $V_{REFP,N}$ voltages.
- **Comparator**: As its name suggests, this block monitors the voltages V_{DAC} and V_{in}, providing a 1-bit digital output.
- **Digital Logic Unit**: It is responsible for determining the output bits ($B[N-1:0]$) based on the comparison signal. Furthermore, it continuously modifies the CDAC voltage to proceed with the next comparison cycle.

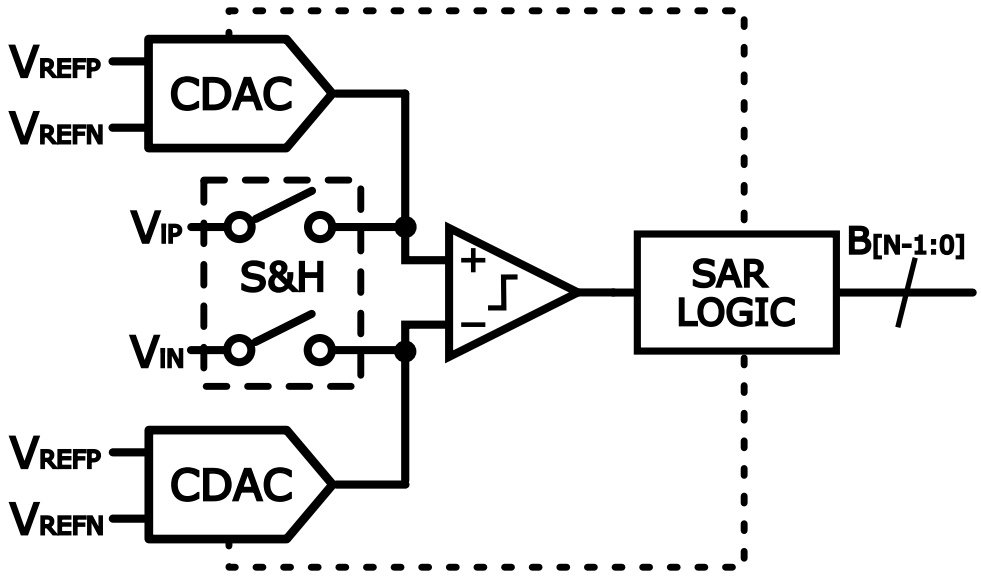

Figure 2.3. Simplified diagram of the SAR ADC topology.

3. ADC DESIGN PROCESS

In this chapter, the examination will focus on each of the blocks depicted in Figure **2.3**, providing a thorough understanding. It will include a presentation of the circuit architecture at the transistor level, along with an exploration of the design equations and essential features that must be considered during the design phase.

3.1. Sample and Hold (S/H)

The basic idea of a sample and hold is shown in Figure **3.1a**, where it consists of a switch connected between the input and a capacitive load[12] [13]. The mode of operation of this circuit is controlled by a digital signal called in this case *Samp*, when active the switch will close and the output will ideally be equal to the input, while if it is ”off” the output sampled voltage will be stored in the capacitor.

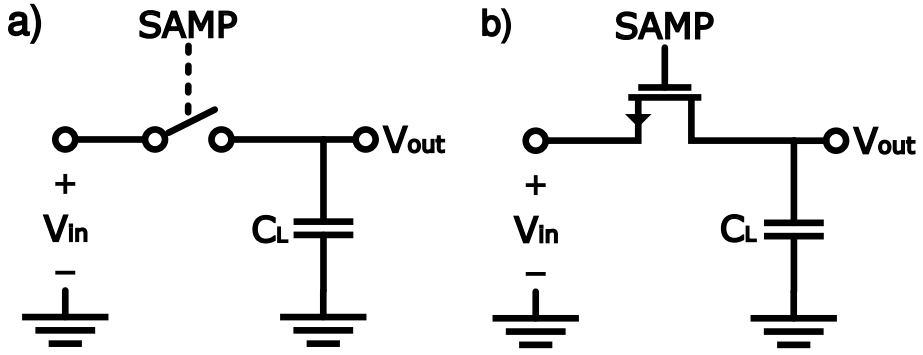

Figure 3.1. Sample and Hold Circuit: Functional and Real implementations

The physical implementation of the switch is usually done using a MOS transistor in deep triode region as seen in Figure **3.1**, however, this causes several effects to arise

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[12] Behzad RAZAVI. “The Bootstrapped Switch [A Circuit for All Seasons]”. In: *IEEE Solid-State Circuits Magazine* 7.3 (2015), pp. 12–15. DOI: 10.1109/MSSC.2015.2449714.

[13] Behzad RAZAVI. “The Design of a Bootstrapped Sampling Circuit [The Analog Mind]”. In: *IEEE Solid-State Circuits Magazine* 13.1 (2021), pp. 7–12. DOI: 10.1109/MSSC.2020.3036143.

that affect the output. The most important one is related to the turn-on resistance of this device[14], this generates the circuit to behave as a low-pass RC filter, facing then band limitations for the input signal.

On the other hand, distortion can also occur if this value changes, creating harmonic distortion[13] just as seen in Figure **1.2**, this value can be obtained using the quadratic MOSFET model[15], which shows this resistance can be approximated as follows:

$$R_{ON} = \frac{1}{\mu C'_{ox}(\frac{W}{L})(V_{GS} - V_{TH})} \tag{14}$$

Where μ is the carrier mobility, C_{ox} the MOS oxide capacitance, while $\frac{W}{L}$ is its width to length ratio, V_{GS} is the gate-to-source voltages and V_{TH} is the threshold voltage.

Then, if the input changes, it will be necessary to modify the gate voltage V_G in the same proportion to maintain the same turn-on resistance. This can be done by a *bootstrapping* technique[13], generating a constant and preferably large V_{GS} to decrease R_{ON}. The topology and details of this will be explained below.

3.1.1. Bootstrap S/H The idea behind the S/H bootstrap is depicted in the Figure **3.2**, where a capacitor can be found that can be charged/discharged depending on which set of switches are closed [12]. In the *Hold* mode the capacitor will be charged up to the supply voltage V_{DD} ($M_{0,5,6}$ are ON), while in the *Sample* mode this component is connected through the gate and the main switch source ($M_{3,8}$ are ON).

Figure **3.3** shows the MOS implementation[12] [13], where each switch has a corresponding transistor, however new transistors are required for different purposes. Firstly M_9

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[14] Fei YUAN. "Bootstrapping Techniques for Energy-Efficient SAR ADCs : A State-of-the-Art Review". In: *2021 IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*. 2021, pp. 575–578. DOI: 10.1109/MWSCAS47672.2021.9531736.

[15] Behzad RAZAVI. *Design of Analog CMOS Integrated Circuits*. 2nd. McGraw-Hill Education, 2017.

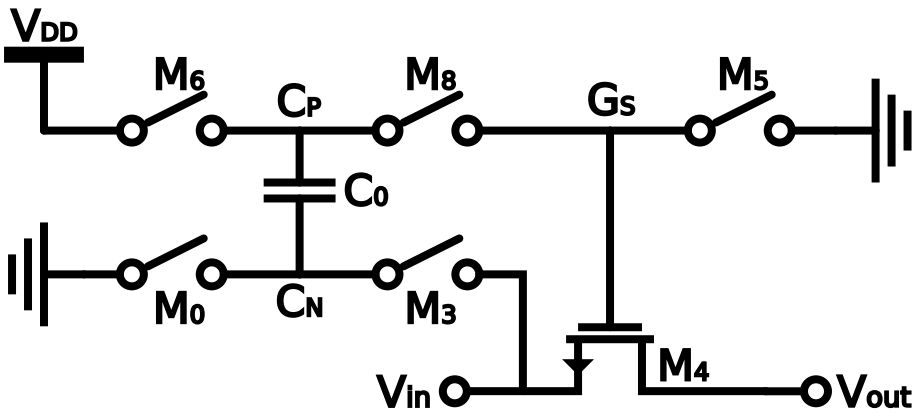

Figure 3.2. Bootstrap Circuit: Functional Schematic

is employed to decrease the device stress on M_5 since this could have a V_{DS} equal to V_{DD} during the sampling phase. Meanwhile, $M_{1,2,7}$ are utilized to properly enable/disable M_8 in each mode. Finally, it is important to note that the bulk terminals of $M_{6,7}$ are not connected to V_{DD}, since V_{CP} may exceed this value during input bootstrapping and turn on the parasitic bulk-source diode.

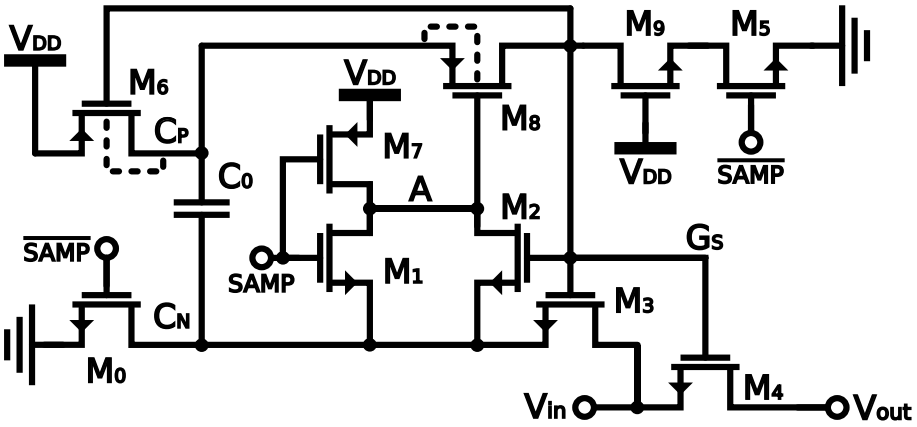

Figure 3.3. Implementation of the Bootstrap Circuit

3.1.2. Design Considerations Like the ADC, the main performance metric of the S/H circuit is its linearity, again measured using the SNDR and ENOB[13]. However, its specifications must exceed those of the ADC by some margin [13], as several additional sources of nonlinearity appear for the entire system. In this case, the target will be an ENOB of 12 Bits or a SNDR of 74 dB.

It can be concluded from the above analysis, that the main transistor in the circuit is M_4, since it is the only one directly connected in the signal path. By (14) it is suggested to increase width-length ratio to decrease R_{ON}[13], however, this also increases the parasitic capacitance, this effect being especially undesirable for C_{ds} since it couples the input and output even in *Hold* mode, affecting the sampled value.

Additionally, it is necessary to take into account another effect, this is the charge injection[12], which occurs when a MOS is turned off, injecting its channel charge Q_{Ch} to nearby components, this also increases with larger dimensions and is given by:

$$Q_{Ch} = WLC_{ox}(V_{GS} - V_{TH}) \tag{15}$$

For M_4 this creates a small error in the output, then a moderate W should be used. however, this can also be seen in transistors connected to C_0, decreasing their charge and thus making their voltage lower than V_{DD} affecting the boostrapping effect [13]. But for them, decreasing their dimensions is desirable, since it reduces the parasitic capacitance, decreasing the voltage drop, moreover, their R_{ON} is not critical for linearity.

3.1.3. Simulations For the circuit simulation, the ENOB was measured using the *Spectrum* in the *Cadence Virtuoso* environment. In its test bench, a V_{sine} source between 5% and 95% was used. Its input frequency was chosen considering a coherent sampling for an FFT[16], for example, with 1024 samples, 103 cycles and an F_s of 10MHz. With these values F_{in} is equal to $1005859.375[Hz]$ following this equation[16]:

$$F_{in} = F_s \frac{N_{cycles}}{N_s} \tag{16}$$

In this example, the ENOB obtained was 12.43 bits for a typical corner simulation.

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[16] *Coherent Sampling vs. Window Sampling*. A/D and D/A Conversion/Sampling Circuits. Maxim Integrated Products - Analog Devices, Mar. 2002.

3.2. Digital Logic

After selecting the architecture, the next necessary step is to select the DAC switching scheme. In this process, both its topology and the digital logic control are defined. For this thesis, monotonic switching is proposed. This is characterized by the fact that the digital output increases with the analog input. In this case this means that $-V_{DD}$ will have a code equivalent to $10'd0$ [17], while for a $+V_{DD}$ it has the final code, $10'd1023$.

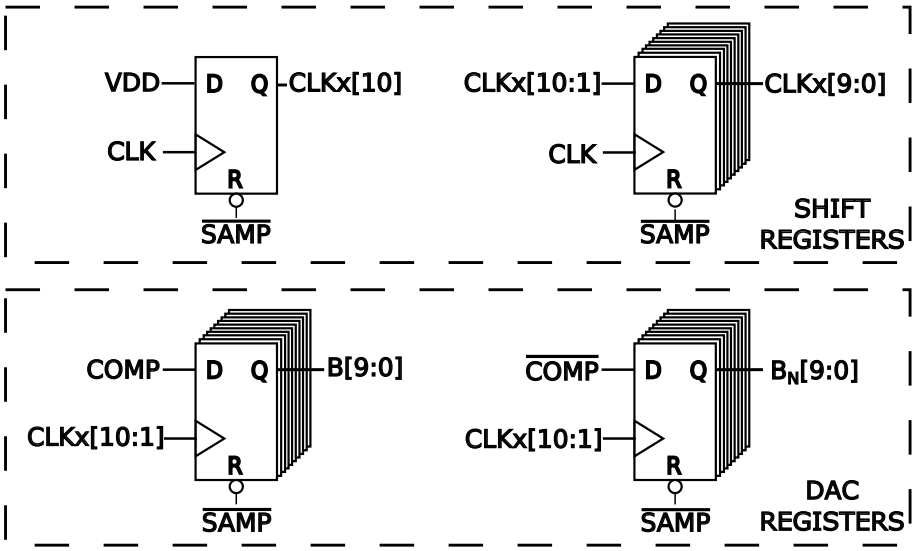

Figure 3.4. SAR Logic Implementation

3.2.1. SAR Logic With this consideration, the SAR logic scheme [18] is represented in the Figure **3.4**, where it consists of two different groups of flip-flops: DAC registers, connected in parallel, which determine each bit and its logical negation given the comparison signal (**COMP**), controlling the current state of the DAC; and shift registers, connected in series, which sequentially activates each DAC register and uses the $CLK_x[0]$ node as the end-of-conversion (EOC) signal when the comparison is com-

[17] $10'd0$ represents the number 0 in a 10-bit binary representation.

[18] Yuxiao LU et al. "A single-channel 10-bit 160 MS/s SAR ADC in 65 nm CMOS". in: *Journal of Semiconductors* 35.4 (2014). DOI: 10.1088/1674-4926/35/4/045009.

pleted. The latter are triggered by the falling edge of the same clock signal, which, as will be seen in the next section, controls the comparator.

The flip-flops will use static logic with a negated, asynchronous reset signal. The gate-level schematic of this circuit is shown in Figure **3.5**.

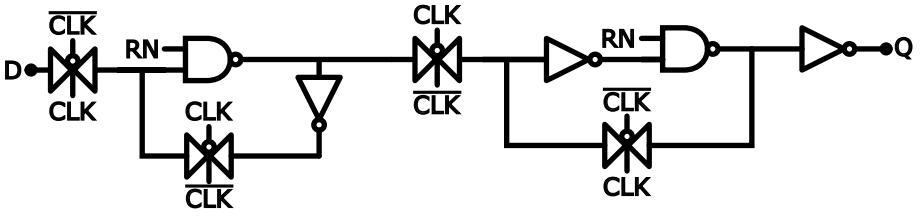

Figure 3.5. Static Flip Flop

The logic implementation also requires buffers at the inputs to ensure correct signal propagation[19], however for the design of this gates and the flip flop it is required to first analyze the basic inverter and then apply its results to the following circuits.

3.2.2. Inverter Analysis The inverter is the circuit that implements the NOT function, its schematic is shown in the Figure **3.6a**. It is usually modeled as **3.6b** or **3.6c** for a high or low input respectively [19]. Where C_x is an equivalent capacitance at the output node as a result of MOS parasitics. Meanwhile, $R_{EQN,P}$ is the equivalent resistance of the N- or P-type transistor during a transition from one state to the other. Even if, this variable is different from that of (14), it retains some similar characteristics [19], such as inverse proportionality with the $\mu C_{ox} W/L$ product.

Using this scheme, the inverter behaves as an RC network, so the output will have an associated constant τ given by $R_{EQN,P} C_x$. In this case, symmetrical transient behavior was desired, so both transistors were required to have the same equivalent resistance. Due to reduced hole mobility, R_{EQP} is larger than R_{EQN}, so it is necessary to scale the PMOS W/L ratio by some factor to compensate for this effect. To find this relationship,

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[19] Jan M. RABAEY, Borivoje NIKOLIC, and Anantha P. CHANDRAKASAN. *Digital Integrated Circuits: A Design Perspective*. Prentice Hall, 1995.

a transient simulation was performed with a square pulse signal, using a chain of three inverters, and measuring the input-output delay in the second device, this using the minimum MOS length of a 28nm TSMC 1.8 [V] transistor ($0.15[um]$).

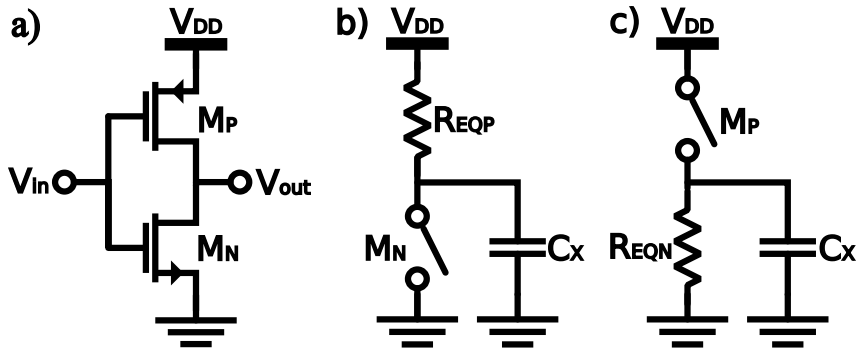

Figure 3.6. CMOS Inverter

It was found that this proportion varies with transistor width, while $(W/L)_P$ should be about 1.8 times larger than $(W/L)_N$ if $W \geq 0.5[\mu m]$, for smaller widths a ratio of 2 gives better results. In most of the ADC digital circuits the first ratio was preferred. For the SAR logic implementation $W_N = 0.5[\mu m]$ and $W_P = 0.9[\mu m]$ were used.

However, in some cases, as in the SAMP inverter or in the buffers, an increase in the W of their transistors was required, dividing their extension with fingers, so that the width of these would also be of the size mentioned above and thus facilitate the layout connections. This increase was necessary since these devices handle the capacitance of several flip-flops, thus generating a higher delay. The result was six times wider for the SAMP inverter and two and six times wider for the buffer, where the width of the second inverter was increased three times to decrease chain propagation[19].

3.3. Capacitive Digital to Analog Converter (CDAC)

A digital to analog converter (DAC) is a circuit that generates an analog output value given a digital input. In this case, it will make the V_{DAC} reference seen in Figure **2.2** that is used for V_{in} quantization into bits. However, given the connections in **2.3**, its output

won't be directly this voltage, but a function of it. Furthermore, since the ADC input is differential, this value will depend on the difference of the actual reference voltages given by the DACs of the corresponding comparator's positive and negative inputs.

3.3.1. DAC operating principle The implemented DAC is based on charge redistribution. The Figure **3.7** shows a pair of 3-bit DACs [11], each consisting of an array of $N = 3$ capacitors that increase exponentially based on a unit value used in the two least significant bits, whose top plates are connected to the DAC output. Meanwhile, each of its bottom plates are next to a switch that selects between $V_{REF,N}$ and $V_{REF,P}$ voltages, being in this case equal to GND and V_{DD} respectively. These switches are implemented as inverters whose input is the corresponding bit.

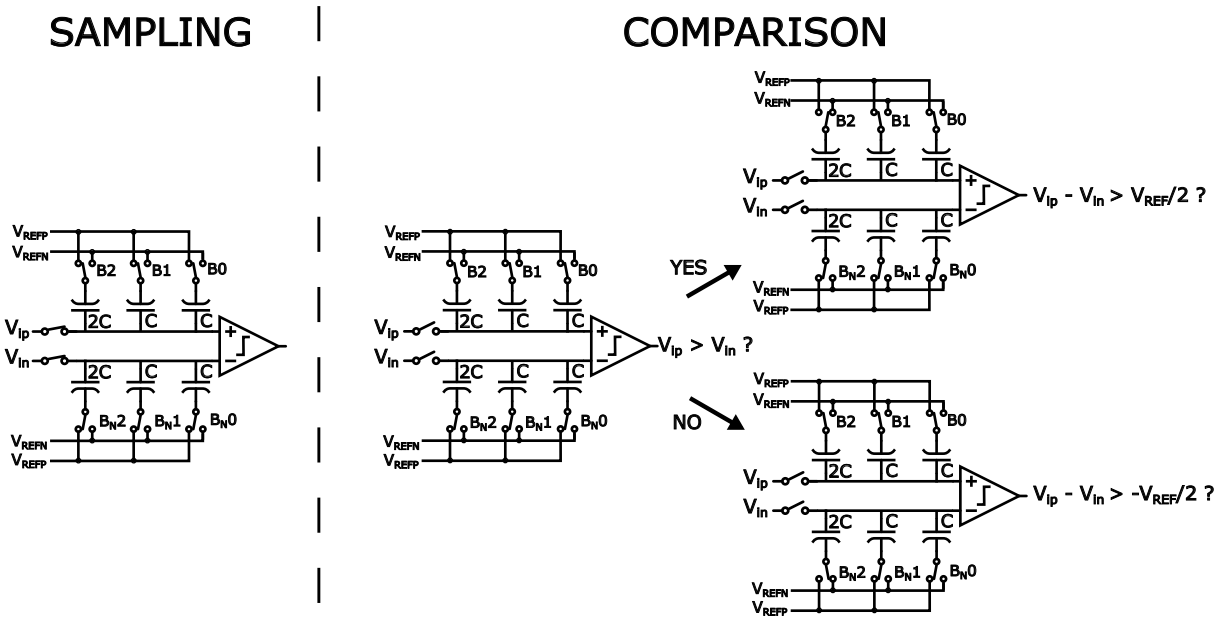

Figure 3.7. 3-Bit DAC operating principle

During the *Hold* phase, each signal B and B_N are set to 0, as each of their flip-flops are in reset mode. Then the lower plate voltage of each capacitor is equal to V_{DD}, and the top plate differential output voltage $V_{DAC,D}$ is equal to the differential input $V_{in,D}$. Then, for the first clock cycle in *Comparison*, the SH is turned off and the most significant bit (MSB) is obtained as seen in Figure **2.2**, this will cause $B[2]$ or $B_N[2]$ to be set to V_{DD},

grounding its corresponding capacitor and then changing its DAC output, but since the charge is conserved the voltage at "X" device can be obtained as follows:

$$Q_0 = Q_1 \tag{17}$$

$$\text{Where:} \quad Q_0 = 4C_u(V_{DD} - V_{inX}) \quad / \quad Q_1 = 2C_u(V_{DD} - V_{DACX}) - 2C_u V_{DACX} \tag{18}$$

Finally obtaining $V_{DACX} = V_{inX} - V_{DD}/2$ independent of the value of the unit capacitance C_u. This result means that the differential output will change by $V_{DD}/2$, since the other DAC has not been switched. In fact, the above analysis can be generalized, obtaining that for the i-th iteration the new differential voltage will be as shown in equation (19), where $K = sgn(V_{DAC,D(i-1)})$ [20] has the same meaning that in Figure **2.2**.

$$V_{DAC,D(i)} = V_{DAC,D(i-1)} + K\frac{V_{REF,P} - V_{REF,N}}{2^i} \tag{19}$$

In addition, it is important to analyze the output common mode $V_{DAC,CM}$. This voltage is defined as the arithmetic mean of both DAC output voltages, and doing a similar analysis can be obtained with the following formula for the i-th iteration:

$$V_{DAC,CM(i)} = V_{DAC,CM(i-1)} - \frac{V_{REF,P} - V_{REF,N}}{2^{i+1}} \tag{20}$$

In contrast to equation (19), this value always decreases[11], being its maximum the same input common mode. As it will be seen in the following section, this can affect substantially the comparator performance. Then a new DAC topology was used, this seen in Figure **3.8a**, where this effect is attenuated dividing the MSB capacitors in two, one controlled by B and the other for the negation of B_N.

The main difference is that after the first comparison, the bit decision affects both DACs, splitting the differential effect in half. For the previous example, using (17) we find that $V_{DAC,P(1)} = V_{in,P} + KV_{DD}/4$ and $V_{DAC,N(1)} = V_{in,P} - KV_{DD}/4$, preserving the change

[20] $sgn(x)$ represents the sign function

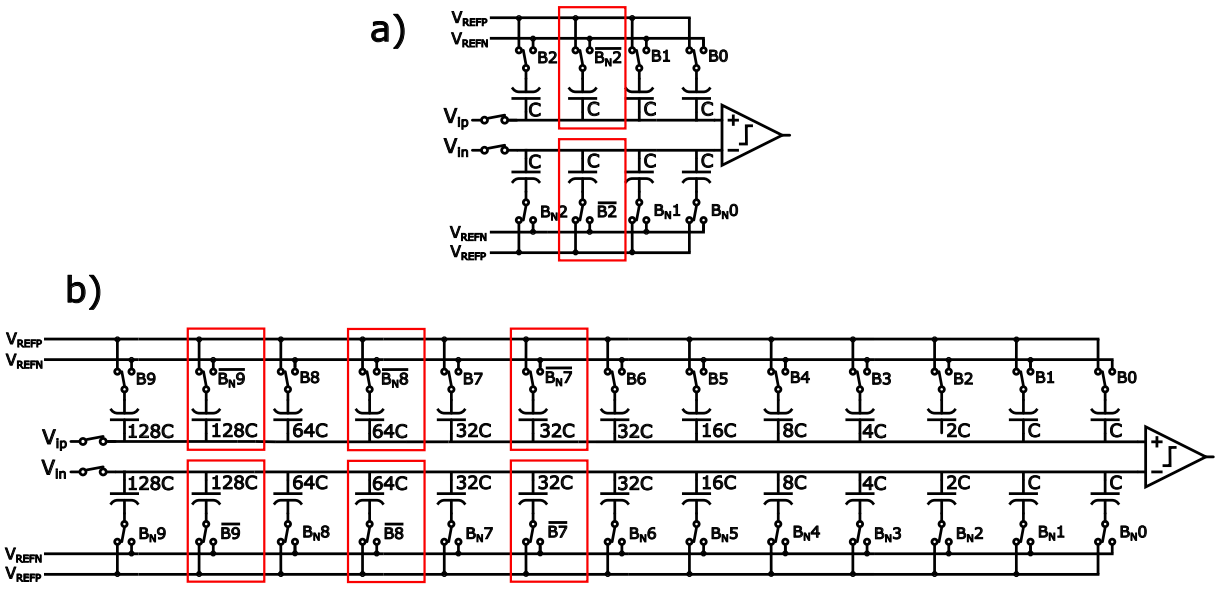

Figure 3.8. 3-Bit DAC Divided Capacitor

predicted by (19) without lowering the input common mode in this iteration.

The 10-bit DAC implementation is shown in Figure **3.8b**, the division will only be done for the three most significant bits, avoiding the largest common mode decrease without a high increase in control and layout complexity. It will then go from a decrease of $0.5V_{DD}$ volts in the final iteration to a change of approximately $0.062V_{DD}$ in $V_{DAC,CM}$. It is important to mention, that the DAC switches were implemented using $W_n = 10[\mu m]$ while the bit inverters used $W_n = 1[\mu m]$. Both maintained the PMOS to NMOS ratio of 1.8 described in section **3.2**.

3.3.2. Capacitance Selection After defining the DAC architecture, the next step in its designing process is to choose the unit capacitance[21]. This step is critical for the converter's performance since the capacitive DAC is the primary source of nonlinearity errors across the ADC, due to mismatching among the elements that compose it. On

[21] Hesham OMRAN et al. "Direct Mismatch Characterization of Femtofarad Capacitors". In: *IEEE Transactions on Circuits and Systems II: Express Briefs* 63.2 (2016), pp. 151–155. DOI: 10.1109/TCSII.2015.2468919.

one hand, a small value is desired, to optimize area and power consumption. However, it is also necessary to have a large enough capacitor so that neither the device's thermal noise nor the matching among them affects the quality of the conversion, these last two factors being the main constraints to be considered.

For the quantization process to remain unaffected by thermal noise, the latter must be less than or equal to the quantization noise [22]. Thus, the equation 21 is derived.

$$\bar{V_q}^2 = \frac{V_{FS}^2}{12 * 2^{2N}} = \frac{kT}{C_u} \tag{21}$$

Where $\bar{V_q}^2$is the quantization noise, V_{FS} is the ADC's full scale conversion range, N the number of bits, k the Boltzmann constant, T the temperature in Kelvin, and C_u the unit capacitance value. Using this equation, C_u is calculated to be $0.161fF$.

It's worth noting that the matching between the capacitors in the DAC is another potential source of error [21]. To determine the minimum value required to account for matching, we can define the maximum standard deviation allowed for an N-bit converter [22], taking into account that the maximum error due to matching can't be greater than $1/2LSB$. This condition is expressed in equation (22).

$$\sigma \leq \frac{(\sqrt{2}-1)2^N}{3.5[2^{N+1}(\sqrt{2^N}-1)+(\sqrt{2}-1)\sqrt{2^N}]} \tag{22}$$

Mismatch simulations were performed by increasing the capacitance value until the calculated σ was reached, and the value obtained for C_u was $13.396fF$. Finally, the larger value was chosen since both were the minimum for each requirement.

$$C_u = 13.396[fF] \tag{23}$$

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[22] Xicai YUE. "Determining the reliable minimum unit capacitance for the DAC capacitor array of SAR ADCs". In: *Microelectronics Journal* 44.6 (2013), pp. 473–478. DOI: 10.1016/j.mejo.2013.03.011.

3.4. Comparator

In a SAR converter, the comparator acts as an 1-Bit ADC, generating two digital signals with inverse logic depending on the sign of the differential DAC output. Its functional diagram [23] is represented in Figure **3.9**. It is controlled by a high frequency clock signal CLK. Initially, when CLK is low, both outputs are set to zero. When this is ON an amplifier magnifies the differential input, it enters a latch, which raises to V_{DD} the output corresponding to the higher value, while grounding the other.

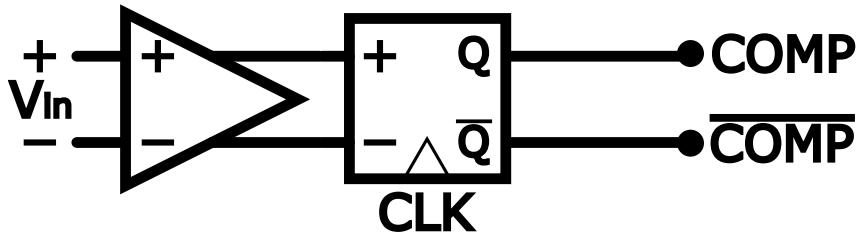

Figure 3.9. Comparator Functional Schematic

One of the main factors taken into account for the selection of the comparator architecture is the power consumption. In our case, with a synchronized circuit, the StrongARM was an interesting alternative[24], since it has no direct current pass between V_{DD} and GND, reducing the static consumption to just the leakage effect[19]. Its schematic is shown in Figure **3.10** where it is accompanied by a previous PMOS-based pre-amplifier stage, which also ensures only dynamic consumption, and provides a wider common-mode range for low voltages, something desirable given the decrease of $V_{DAC,CM}$.

The operating principle of the comparator [23] is as follows, first, when CLK is low $M_{N1,2}$ are closed, grounding $V_{\pm A}$ and then also closing $M_{SL1,2}$ and $M_{SP1,2}$, this charges each

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[23] Behzad RAZAVI. "The StrongARM Latch [A Circuit for All Seasons]". In: *IEEE Solid-State Circuits Magazine* 7.2 (2015), pp. 12–17. DOI: 10.1109/MSSC.2015.2418155.

[24] Behzad RAZAVI. "The Design of a Comparator [The Analog Mind]". In: *IEEE Solid-State Circuits Magazine* 12.4 (2020), pp. 8–14. DOI: 10.1109/MSSC.2020.3021865.

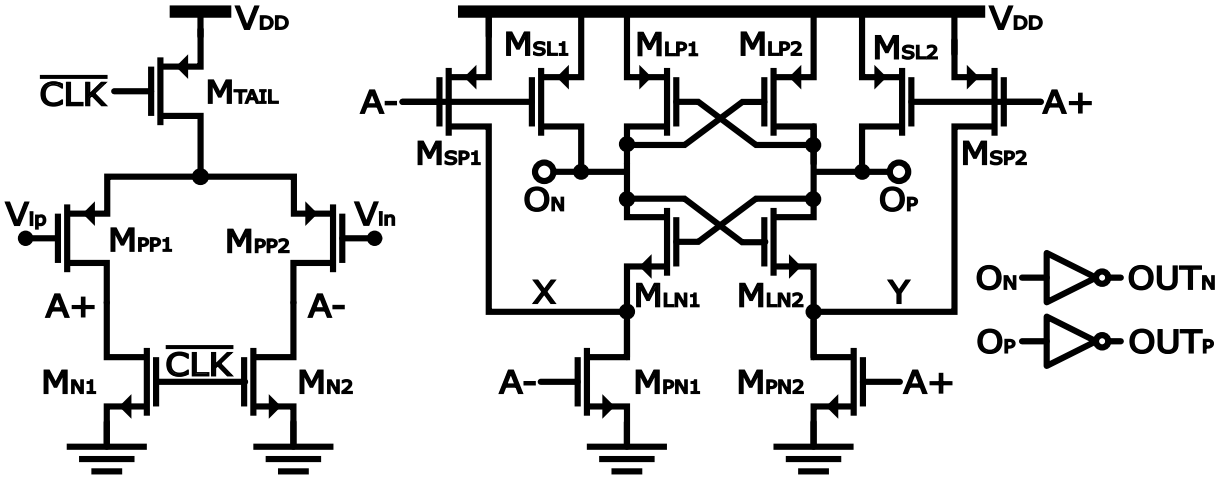

Figure 3.10. Comparator Schematic

internal node of the StrongARM to V_{DD}. Then when CLK is ON, M_{TAIL} closes allowing the differential input to be amplified by $M_{PP1,2}$ and $M_{PN1,2}$. Since the latter transistors are allowing current, V_X and V_Y begin to discharge, thus allowing $M_{LN1,2}$ to start conducting after their V_{GS} is greater than V_{TH}, thus discharging $V_{ON,P}$ as well. Next, the cross-coupled $M_{LP1,2}$ pair latches the highest node, the one that started to be discharged later and which corresponds to the highest input, between $V_{OP,N}$ via positive feedback. Finally, the signals $V_{OUTP,N}$ are generated by inverting the voltage $V_{OP,N}$.

3.4.1. Design Considerations In this comparator implementation, two main factors are critical. The first is its *offset*[24], this effect arises as a result the schematic asymmetries (systematic offset)[25], or caused by device mismatch as a result of device manufacturing process limitations (random offset)[25]. In both cases, this affects the input, causing the comparator to ”think” that it is slightly different, affecting mainly the smaller ones, which can be confused delivering an erroneous output. It is usually modeled as seen in the Figure **3.11a**, as a constant voltage at the input terminals.

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[25] Peter R KINGET. “Device mismatch and tradeoffs in the design of analog circuits”. In: *IEEE Journal of Solid-State Circuits* 40.6 (2005), pp. 1212–1224.

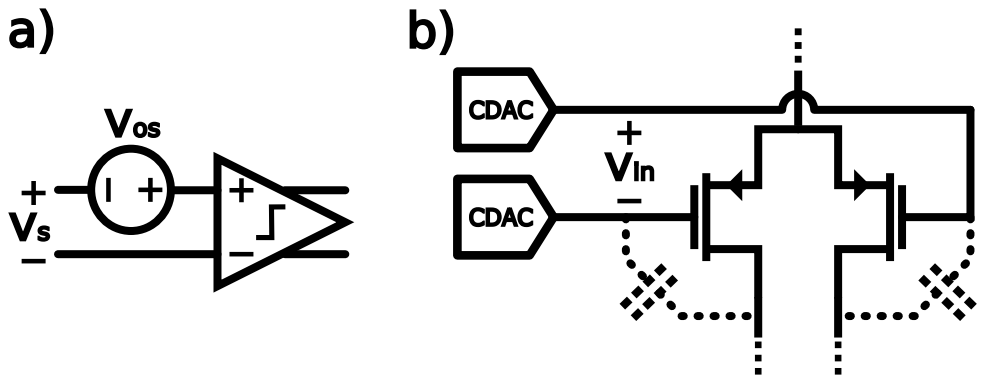

Figure 3.11. Comparator Offset Modelling and Kick-back noise

The other one is known as *kick-back noise*[26] which is represented in Figure **3.11b**, this is produced during the input amplification as a consequence of the high current required during this stage, since during the transient part of it crosses the parasitic capacitances of the transistors of the differential pair, affecting the input of the circuit if the output impedance of the preceding circuit is not zero. This being so, as the two capacitive DACs are connected to the comparator, the overall performance degrades.

In both cases it is observed that the main transistors to take into account are the $M_{PP1,2}$[24], being the one with the largest offset referred to the input since it conforms the first amplification stage, suggesting to increase its dimensions in order to decrease the missmatch variations with a high W/L ratio to also decrease noise. However, in this way the parasitic capacitances are also increased, and thus the *kick-back noise*.

On the other hand, to reduce the contribution of load capacitance mismatch to the offset [27], an appropriate size for the output nodes should be chosen. Therefore, it is important that the inverters are wide, since they have to control the input capacitance

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[26] P.M. FIGUEIREDO and J.C. VITAL. "Kickback noise reduction techniques for CMOS latched comparators". In: *IEEE Transactions on Circuits and Systems II: Express Briefs* 53.7 (2006), pp. 541–545. DOI: 10.1109/TCSII.2006.875308.

[27] Dai ZHANG. "Design of Ultra-Low-Power Analog-to-Digital Converters". Thesis. Sweden: Linkopings universitet, 2012.

of the digital logic, which is considerably large.

3.4.2. Simulations Although the comparator offset changes as this common mode voltage does, it was important to measure its amount as it will affect the digital output of the ADC. To do this, a differential ramp input was used, such that an ideal comparator would change its output in the middle of the simulation. As this is not the case, this point is found and the offset will be the variation with the ideal point.

Doing Monte-Carlo simulation, its mean and standard deviation were found, finding then the systematic and random offset, obtaining for a test with 1024 samples doing a missmatch and process variation simulation respectively $42.44[\mu V]$ and $2.113[mV]$ which were appropriate since this σ was less than 1 LSB.

4. RESULTS

In this chapter, the final dimensions of all devices from each block are presented, as well as the final layout. It is worth noting two things: firstly, all transistors employed were $28[nm]$ TSMC standard $1.8[V]$ model; secondly, unless stated otherwise, all transistors used the minimum length of 150nm. Subsequently, the post-layout simulation results of ENOB, SNDR, Power, DNL, and INL, across corners and Monte Carlo process variations, have been included. The chapter concludes with a performance comparison with other ADCs presented in the literature.

4.1. Final Dimensions

4.1.1. Sample and Hold The table 4.1 describes the width of each transistor seen in the Figure **3.3**. It is important to mention that the M_4 bootstrap switch has a multiplier of 5 to increase the equivalent W, being the only one that used this feature.

Table 4.1. Final dimensions for the Sample and Hold

Name	**W**$[\mu m]$
M_0	0.27
M_1	0.27
M_2	3
M_3	1
M_4	1
M_5	1
M_6	0.27
M_7	0.54
M_8	2
M_9	1

The C_0 capacitance was implemented using a metal-oxide-metal (MOM) capacitor,

considering its linearity[21] and availability in TSMC 28 nm PDK. For the layout connections, the capacitor was placed between the first and fourth metal layers, using a finger number of 54, having $50[nm]$ for its width and spacing, and $10.2[\mu m]$ for its length. The final capacitance was $208,138[fF]$.

4.1.2. Digital Blocks As stated in section **3.2**, a width ratio of 1.8 PMOS to NMOS was used for most of the digital domain devices, using only a ratio of 2 for the $SAMP$ bootstrap inverter due to its small dimensions. With this fact in mind, the Table 4.2 includes the equivalent NMOS width W_N, the number of fingers $N_{Fingers}$ and the width finger W_{NF} used for each constituent digital block in the ADC.

Table 4.2. Final dimensions for the Digital Domain circuits in the ADC

Name	**W$_N$**$[\mu m]$	**N$_{Fingers}$**	**W$_{NF}$**$[\mu m]$
Flip-Flop	0.5	1	0.5
Digital Buffers (1st Inverter)	1	2	0.5
Digital Buffers (2nd Inverter)	3	6	0.5
DAC switches	10	8	1.25
DAC Bit inverters	1	1	1
Comparator Out Inverters	3	1	3
Comparator CLK Inverters	2	2	1
Digital Logic $SAMP$ Inverter	3	6	0.5
Bootstrap $SAMP$ Inverter	0.27	1	0.27

4.1.3. CDAC Capacitors As for the sample and hold, MOM capacitors were used for the DAC array. In this case the unit capacitance was the one obtained in (23), the fingers were a total of 14, they were located between 4 and 6 metal layers, the width and spacing were also $50[nm]$ just like the bootstrap case. Their length was $4[nm]$.

4.1.4. Comparator Finally, table **4.3** highlights the width, length and the number of multipliers for the transistors shown in Figure **3.10**.

Table 4.3. Final dimensions for the Comparator

Name	**W**$[\mu m]$	**L**$[\mu m]$	**Multiplier**
$M_{PP1,2}$	5.2	0.5	6
M_{Tail}	0.75	0.6	1
$M_{N1,2}$	0.3	0.6	1
$M_{PN1,2}$	2.5	0.15	2
$M_{LN1,2}$	0.9	0.15	2
$M_{SL1,2}$	0.3	0.15	1
$M_{SP1,2}$	0.3	0.15	1
$M_{LP1,2}$	0.3	0.15	1

4.2. Layout Considerations

After doing schematic level verification of the ADC overall performance, the circuit's layout was done, this is shown in Figure 4.1. Several strategies were employed to facilitate the connections and reduce parasitic effects that could affect ADC performance.

The first was the metal distribution, determining odd ($M_{3,5}$) and even ($M_{2,4}$) layers for horizontal and vertical connections, respectively. For the first metal layer (M_1), it was mostly used for small connections without thinking about its orientation. For the connections between all these metals, there were used at least two vias, except for the digital logic, to reduce the resistance and improve the reliability of each connection.

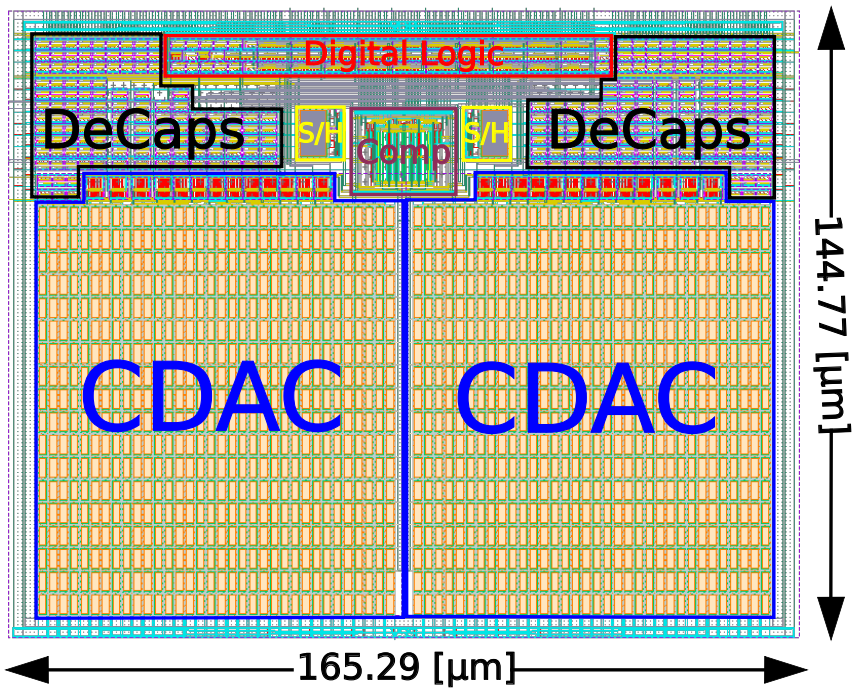

Figure 4.1. Circuit's layout

Layers $M_{1,2,4}$ were used for the power pins (V_{DD} and GND), with wide wires and vias between both layers to reduce their resistance[28]. Also for this type of nodes, a "ring" topology was utilized to facilitate the connection regardless of the origin. This topology was also used for bulk connections in groups of MOS transistors of the same type, as the reduced resistance helps to reduce latch-up[28].

For placement, symmetry was considered to reduce offset, applying overall ADC, especially in the comparator and DAC, where dummy devices were also implemented, for the input comparator differential pair and the capacitor arrays, as these two were the

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[28] R. Jacob BAKER, Harry W. LI, and David E. BOYCE. *CMOS. Circuit design layout and simulation*. IEEE Press, 1998.

most critical parts for the ADC performance. In addition, for the DAC, a spiral [29] capacitor distribution was employed to decrease mismatch and gradient variations. Finally, to fill the gaps in the ADC design, MOS [30] capacitors were introduced between both power pins to reduce power noise, mainly generated by digital logic switching.

4.3. Post-Layout Simulations

After finalizing the design connections, design rule checking (DRC) and compared the design with the schematic (LVS) were conducted. Subsequently, the circuit underwent parasitic extraction (PEX), followed by simulations to assess the ADC performance. To this end, two distinct sets of tests were executed. Firstly, a dynamic performance test employed a sinusoidal input covering 90% of the total input range to prevent ADC saturation at extreme values [31], with a common mode voltage of $V_{DD}/2 = 0.9[V]$, using $F_{in} = F_s/10$ for the main test and an $F_{in} = F_s/2$ for an additional one at Nyquist frequency. This setup facilitated the measurement of parameters including the effective number of bits (ENOB), power consumption, and spurious-free dynamic range (SFDR).

The second test-bench employed the histogram method [32] to find differential and integral non-linearity. It utilized a full-scale increasing input ramp, ensuring ideally 8 samples for each code. Subsequently, the output waveforms were exported from the

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[29] Chun-Cheng LIU et al. “A 10-bit 50-MS/s SAR ADC With a Monotonic Capacitor Switching Procedure”. In: *IEEE Journal of Solid-State Circuits* 45.4 (2010), pp. 731–740. DOI: 10.1109/JSSC.2010.2042254.

[30] Xiongfei MENG, Resve SALEH, and Karim ARABI. “Layout of Decoupling Capacitors in IP Blocks for 90-nm CMOS”. in: *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 16.11 (2008), pp. 1581–1588. DOI: 10.1109/TVLSI.2008.2001240.

[31] Tarciso Alvim MARTINS. *SAMPA ADC ENOB Verification Guide*. 2017.

[32] Haideh KHORRAMABADI. *EE247: Lecture Notes*. [Online]. University of California, Berkeley. 2007. URL: https://inst.eecs.berkeley.edu/~ee247/fa07/index.html.

Cadence Virtuoso environment to a *Python* script to execute the aforementioned algorithm. The resulting code can be accessed via Google Colab **here**.

4.3.1. Process-Voltage-Temperature (PVT) Corner Simulations The selected corners used the automotive standard[33], considering slow/fast process variation for MOSFET and high/low value for passive devices, as MOM capacitors. Supply voltage varied by ±10% and temperature ranged from -40 to 125 ℃. The simulation results for dynamic test are shown in Table 4.4, were minimum, maximum and typical corner results for ENOB, power and SFDR at both input frequencies.

Table 4.4. PVT Corners PEX Simulation Results

Specification	Requirement	Min	Typ	Max
ENOB (bit) @Fin = Fs/10	$>$9	9.564	9.863	9.996
SFDR (dB) @Fin = Fs/10	-	65.79	68.52	70.58
ENOB (bit) @Fin = Fs/2	-	9.129	9.777	9.986
SFDR (dB) @Fin = Fs/2	-	59.73	68.98	70.42
Power (mW)	$<$1	0.33	0.49	0.881

The simulation results show that the ENOB and power specifications were met for all scenarios, even with an input frequency at the Nyquist limit. The worst ENOB result occurred at a temperature of 125℃, a supply voltage of 1.62V, and a process variation SSH (Slow-NMOS/Slow-PMOS/High-Capacitance). The maximum power consumption was observed at a temperature of 125℃, a supply voltage of 1.98V, and a process variation FFH (Fast/Fast/High), which was as expected. It's also worth noting that the

[33] Boris MURMANN. *Analysis and Design of Elementary MOS Amplifier Stages*. NTS Press, 2013.

best power case of 0.33 mW was observed at a temperature of -40℃, a supply voltage of 1.62V, and a process variation SSL (Slow/Slow/Low).

In the case of DNL and INL, the typical ENOB corner was tested with only the worst case, this was mainly due to the duration of the simulation, which lasted on average a little less than two days for each sample. These results are shown in Figure 4.2, where it can be seen that the specifications in 2.1 are met as DNL were +0.1586/-0.2276 and +0.1577/-0.2282 for the typical and worst case test, and INL were +0.3944/-0.3944 and +0.4106/-0.3806 respectively.

4.3.2. Monte Carlo Variations Simulation A Monte Carlo simulation was also performed to characterize the ADC performance under random process variation and device mismatch. The dynamic test had 128 different samples, and the results are shown in Table 4.5, where minimum, mean, maximum and standard deviation are reported. For the static measurements, only 5 samples were taken, due to the long duration of the simulations, which amounted to more than a whole week. The Table 4.6 shows again the same metrics than in Table 4.5 but for the static specifications.

Table 4.5. PEX Monte Carlo simulation results

Specification	Requirement	Min	Max	Mean	Sigma
ENOB (bit) @Fin = Fs/10	>9	9.583	~ 10	9.846	0.126
ENOB (bit) @Fin = Fs/2	-	9.616	9.897	9.76	0.092
SFDR (dB) @Fin = Fs/10	-	65.44	72.92	69.33	1.438
SFDR (dB) @Fin = Fs/2	-	64.58	71.01	68.48	1.367
Power (mW)	<1	0.482	0.583	0.53	0.021

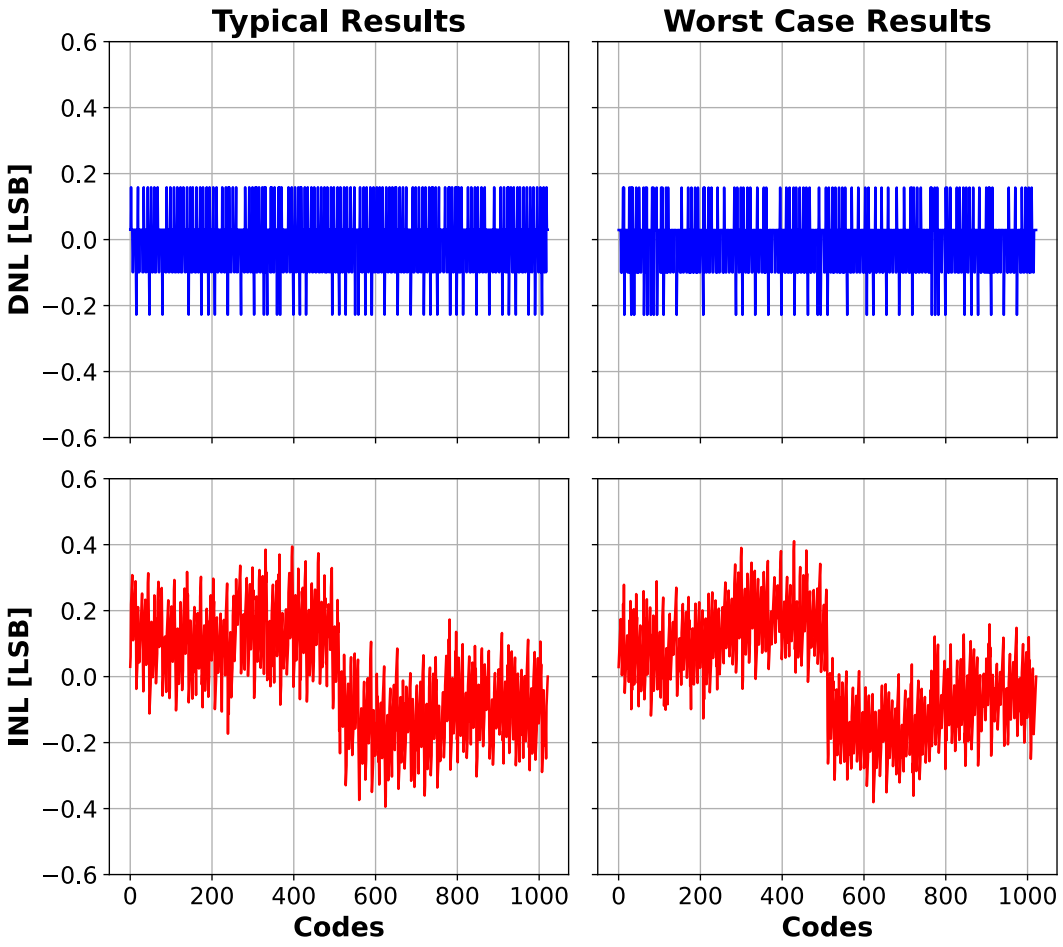

Figure 4.2. DNL and INL Results

Table 4.6. PEX Monte Carlo simulation results

Specification	Requirement	Min	Max	Mean	Sigma
DNL (LSB)	<0.7	0.2273	0.3559	0.2532	0.0574
INL (LSB)	<0.8	0.388	0.4762	0.4283	0.0345

Finally, in Table 4.7, there is a comparison of the specifications at typical corner of this converter with other SAR designs in the literature. These designs also handle 10 bits, are implemented in sub-100 nm CMOS technologies, have a sampling rate in the range

of 10-30 MS/s. For the reader's clarity, these will be referred to as Campos[34], Huang[35] and Haenzsche[36]. Additionally, a number called the Figure of Merit (FOM) is used to compare the performance of the ADCs. This number condenses sampling frequency, ENOB, and power, and is given by:

$$FOM = \frac{Power}{F_S * 2^{ENOB}} \left[\frac{fJ}{Conv * Step}\right]. \tag{24}$$

Table 4.7. Performance Comparison.

Specification	**Campos**	**Huang***	**Haenzsche***	This Work
Architecture	SAR	SAR	SAR	SAR
Technology	65nm	90nm	28nm	28 nm
Supply Voltage (V)	1.2	1	1.8 / 1	1.8
Sampling Rate (MS/s)	12	30	16	10
Resolution (bit)	10	10	10	10
ENOB @Fin = Fs/2 (bit)	9.65	9.16	9.1	9.777
|DNL| (LSB)	0.55	0.88	0.3	0.23
|INL| (LSB)	0.56	1.32	0.6	0.39
Power (mW)	0.151	0.98	0.71	0.49
FOM (fJ/Conv.-step)	15.8	57	81	55.82
Active Area (mmˆ2)	0.074	0.13	0.0094	0.024

*On Silicon measurements

In the evaluation of linearity measures, this work emerges as the best performing

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[34] Arthur Lombardi CAMPOS, João NAVARRO, and Maximiliam LUPPE. "Design of a low power 10-bit 12MS/s asynchronous SAR ADC in 65nm CMOS". in: *2019 32nd Symposium on Integrated Circuits and Systems Design (SBCCI)*. 2019, pp. 1–6.

[35] Guan-Ying HUANG et al. "10-bit 30-MS/s SAR ADC Using a Switchback Switching Method". In: *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 21.3 (2013), pp. 584–588. DOI: 10.1109/TVLSI.2012.2190117.

[36] Stefan HAENZSCHE, Sebastian HÖPPNER, and Rene SCHÜFFNY. "A 10 bit 16 MS/s redundant SAR ADC with flexible window function for a digitally controlled DC-DC converter in 28 nm CMOS". in: *2014 NORCHIP*. 2014, pp. 1–4. DOI: 10.1109/NORCHIP.2014.7004704.

among the selection, showing the most favorable values for ENOB, INL and DNL. It is closely followed by Campos, which is the only one presenting simulation rather than experimental results. The rest of the designs show a more noticeable performance difference, with the exception of DNL by the Haenzsche's design.

In terms of power consumption, both Huang and Haenzsche fall short compared to the proposed ADC with 0.98 and 0.71 mW respectively against 0.49 mW, while Campos outperforms it, achieving the highest figure of merit (FoM) among the chosen designs. Huang ranks third, showing slightly higher FoM than this work. Finally, in terms of area, this design secures the second best position, only surpassed by Campos, the only contender fabricated on the same 28 nm CMOS technology node. It should be noted that this study employs high voltage transistors (1.8 V) and a non-minimum channel length (L), which translates into each transistor occupying a larger area.

5. CONCLUSIONS AND FUTURE WORK

5.1. Conclusions

This work describes the design of a 10-bit analog-to-digital converter (ADC) fabricated on a TSMC 28 nm CMOS technology node. The project began with a thorough evaluation of application requirements, intending to develop a converter for a general-purpose system-on-chip (SoC), requiring then moderate resolution and low power consumption. An extensive literature review revealed that the successive approximation register (SAR) topology was the most suitable option to meet these specifications.

Each constituent block of the ADC underwent individual design process to meet specific performance criteria. The sample-and-hold circuit was built to achieve an ENOB of 12.43 bits to ensure optimal linearity for the entire converter, while an PMOS-to-NMOS width ratio of 1.8 was implemented in the custom digital logic section to achieve balanced transition times. The digital-to-analog converter (DAC) employed a unity capacitance of 13.4 fF to minimize noise power and mismatch variations, complemented by a novel technique that reduces the common-mode variation of the monotonic switching scheme from $0.5V_{DD}$ to $0.062V_{DD}$. In addition, the comparator stage was designed to have a random offset of approximately 2 mV, less than 1 least significant bit (LSB), to ensure high conversion accuracy.

Following the individual block testing, the entire ADC performance verification was done initially using schematic-level simulations, to assess compliance with each circuit specification. Subsequently, layout design was done, with a total area usage of approximately 165x145 μm^2, prioritizing strategies to optimize performance. Circuit symmetry was meticulously maintained to minimize offset, while careful consideration was given to metal distribution to mitigate parasitic capacitances at critical nodes resulting from

overlap. Additionally, power rings were strategically implemented to facilitate bulk connections and mitigate MOSFET latch-up risks.

Finally, post-layout simulations were done using a new circuit model with extracted parasitics. This indicated a worst-case ENOB of 9.564 bits, a worst case DNL of approximately 0.356 [LSB], an INL of 0.476 [LSB] and, finally, an maximum power consumption of 0.8856 [mW], meeting all the specifications required in each corner and in Monte-Carlo tests with at a maximum sampling frequency of 10 [MHz]. Doing a comparison of the typical specifications of this converter with some others of the literature, it was found a good improvement of linearity measurements (ENOB, DNL and INL), while having a good power performance with a small area, being only surpassed by one circuit in each of the last mentioned categories.

5.2. Future Work

- For the final implementation of the ADC for the general purpose microcontroller, the reference voltages of the $V_{REFP,N}$ converter will need to have a dedicated system to ensure robustness to process and environmental variations. At this time, the OnChip research group has built a bandgap reference circuit for this and related needs, however, a buffer will need to be included to ensure adequate drive capability and minimize the effects of supply noise.

- The ADC input tests were performed using an ideal voltage source, however, in a practical application this will not be the case, since there is an equivalent external impedance that can affect the overall performance of the converter. Making it necessary to also use a buffer for the differential input, in order to minimize the exterior disturbance without affecting the specifications met.

- Once the A/D conversion is finished, several challenges appear in the link between the main microcontroller processor and the ADC, one of its peripherals, being these problems related to data integrity and synchrony. Then, for the overall implementation of the system, it is necessary to establish a suitable communication protocol and a digital interface to handle it.

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