DESIGN OF A 28NM CMOS CTLE FOR HIGH-SPEED SERDES INTERFACES

JULIÁN FRANCISCO ROMERO AMAYA
JEANPAULL VALENCIA QUINTERO

UNIVERSIDAD INDUSTRIAL DE SANTANDER
FACULTAD DE INGENIERÍAS FISICOMECÁNICAS
ESCUELA DE INGENIERÍA ELÉCTRICA, ELECTRÓNICA Y DE TELECOMUNICACIONES
BUCARAMANGA
2025

DESIGN OF A 28NM CMOS CTLE FOR HIGH-SPEED SERDES INTERFACES

JULIÁN FRANCISCO ROMERO AMAYA
JEANPAULL VALENCIA QUINTERO

Degree work presented as a requirement to qualify for the title of Electronic Engineer

Advisors:
JEISON HERNEY ACEVEDO VELASQUEZ
B.Sc.
JAVIER FERNEY ARDILA OCHOA
PhD

UNIVERSIDAD INDUSTRIAL DE SANTANDER
FACULTAD DE INGENIERÍAS FISICOMECÁNICAS
ESCUELA DE INGENIERÍA ELÉCTRICA, ELECTRÓNICA Y DE TELECOMUNICACIONES
BUCARAMANGA
2025

Dedicated to our families and friends.

ACKNOWLEDGEMENTS

I would like to express my deepest gratitude to my family for the teachings they have given me and for shaping me into the person I am today. Especially to my mom Adriana, for her unconditional support, her love, and for always believing in me. Without her encouragement and example, this achievement would not have been possible.

I would also like to thank the Onchip research group and all its members, who welcomed me and made me feel part of the team. Their ideas, discussions, and companionship were a constant source of learning and motivation throughout this process.

I extend my gratitude to my colleague Jeanpaul, whose perseverance and patience during this journey were invaluable. Working alongside him has been both a challenge and a source of great satisfaction. Likewise, I am deeply grateful to my advisor Jeison, whose consistency and dedication—even in his spare time—filled my mind with new perspectives and fascinating circuit ideas, contributing significantly to the completion of this work.

Finally, I want to give special thanks to Professor Javier Ardila, whose passion for teaching and microelectronics inspired me throughout my academic journey. His guidance opened my eyes to the beauty of this field and motivated me to pursue it with dedication.

With appreciation, **Julián Francisco Romero Amaya**

ACKNOWLEDGEMENTS

I would like to express my deepest gratitude to my parents, whose unconditional love, guidance, and support have been the foundation of my efforts throughout this journey. I am also thankful to my family as a whole, to whom I owe the greatest appreciation for always being present and encouraging me at every stage.

My sincere thanks also go to my friends and colleagues, whose companionship, motivation, and willingness to share experiences have made this process more meaningful and much easier to carry out. I am especially grateful to my colleague Julián Romero, for his collaboration, dedication, and the valuable lessons I have learned while working alongside him.

I would like to extend special appreciation to the director of this thesis project, Jeison Acevedo, for his patience, guidance, and continuous support. His commitment and generosity in dedicating his time were fundamental to the completion of this work. Likewise, I would like to thank Professor Javier Ardila, whose contributions were instrumental in moving this project forward.

Finally, I would also like to acknowledge my cat Hanna, whose company and affection have provided comfort during long hours of work, making the process lighter and more enjoyable.

With appreciation, **Jeanpaull Valencia Quintero**

TABLE OF CONTENTS

LIST OF FIGURES

Page.

LIST OF TABLES

Page.

RESUMEN

TÍTULO: DISEÑO DE UN CTLE CMOS DE 28NM PARA INTERFACES SERDES DE ALTA VELOCIDAD [*]

AUTORES: JULIÁN FRANCISCO ROMERO AMAYA
JEANPAULL VALENCIA QUINTERO [**]

PALABRAS CLAVE: CTLE, CMFB, Ecualizador, Microelectrónica, AFE, Comunicación de alta velocidad, Integridad de la señal, Diseño de circuitos analógicos, Respuesta en frecuencia.

DESCRIPCIÓN:

Este proyecto tiene como objetivo diseñar un ecualizador de tiempo continuo (CTLE), capaz de compensar las pérdidas de un canal para interfaces SerDes de alta velocidad en un proceso CMOS de 28 nm.

El CTLE es típicamente utilizado en receptores de datos, específicamente en el analog front-end (AFE), cuyo propósito es recuperar la integridad de la señal degradada por el canal. El diseño propuesto busca generar una respuesta en frecuencia tal que la función de transferencia del CTLE actúe como la inversa de la función de transferencia del canal, el cual se comporta como un filtro pasa-bajos. De esta manera, se logra una banda de respuesta plana gracias a la combinación de ambas funciones de transferencia, siendo el CTLE responsable de amplificar los componentes de alta frecuencia.

El ancho de banda de esta función de transferencia estará determinado por la frecuencia de Nyquist, la cual, dependiendo de la modulación empleada en el sistema de comunicación, será definida por la tasa de datos. La ecualización proporcionada por el CTLE es esencial para asegurar una recuperación precisa de los datos en las etapas posteriores del sistema.

Como aporte innovador, este trabajo implementa una nueva técnica de expansión en el diseño del CTLE, la cual no se encontraba reportada en el estado del arte. Alcanzando asi una figura de mérito (FoM) competitiva en comparación con otros diseños de referencia.

---

[*] Trabajo de Grado

[**] Facultad de Ingenierías Físico-Mecánicas. Escuela de Ingenierías Eléctrica, Electrónica y de Telecomunicaciones. Director: JEISON HERNEY ACEVEDO VELASQUEZ

ABSTRACT

TITLE: DESIGN OF A 28NM CMOS CTLE FOR HIGH-SPEED SERDES INTERFACES [*]

AUTHORS: JULIÁN FRANCISCO ROMERO AMAYA
JEANPAULL VALENCIA QUINTERO [**]

Keywords: CTLE, CMFB, Equalizer, Microelectronics, AFE, High-Speed Communication, Signal Integrity, Analog Circuit Design, Frequency Response.

DESCRIPTION:

This project aims to design a Continuous-Time Linear Equalizer (CTLE) capable of compensating channel losses for high-speed SerDes interfaces in a 28 nm CMOS process.

The CTLE is typically used in data receivers, specifically in the analog front-end (AFE), whose purpose is to restore the integrity of the signal degraded by the channel. The proposed design seeks to generate a frequency response such that the CTLE transfer function behaves as the inverse of the channel transfer function, which typically acts as a low-pass filter. In this way, a flat overall response is obtained by combining both transfer functions, with the CTLE amplifying the high-frequency components.

The bandwidth of this transfer function is determined by the Nyquist frequency, which, depending on the modulation employed in the communication system, is defined by the data rate. The equalization provided by the proposed CTLE is essential to ensure accurate data recovery in subsequent stages of the system.

As an innovative contribution, this work implements a new expansion technique in the design of the CTLE, which has not been previously reported in the state of the art. As a result, the design achieves a competitive Figure of Merit (FoM) compared to existing reference works.

---

[*] BSc Thesis

[**] Facultad de Ingenierías Físico-Mecánicas. Escuela de Ingenierías Eléctrica, Electrónica y de Telecomunicaciones. Advisor: JEISON HERNEY ACEVEDO VELASQUEZ

INTRODUCTION

Nowadays, communication systems are absolutely essential for data transmission between servers, data centers, and networks in general. However, data rates between chips in wired communications are rapidly increasing over time. With the fast advancement of technology and the growing demand for higher rates, high-speed circuits or interfaces have become essential. [1]

One of the fundamental mediums of these interfaces is the electrical channel. However, it presents a critical issue: the electrical channel exhibits a low-pass frequency response, where each frequency component experiences losses due to dielectric losses and skin effect. As frequency increases, the channel limitations become more significant, leading to signal degradation, which in turn worsens signal performance and increases error in transmitted information, not only due to attenuation of the individual bit, but also due to interaction with adjacent data.

There are many ways to recover this degraded information, and equalization proves to be a common technique for this. There are several equalization methods, but the most common are the feedforward equalizer (FFE), the decision feedback equalizer (DFE), and the continuous-time linear equalizer (CTLE).[2] The first two rely on digital approaches for recovery and equalization, directly affecting the frequency range where losses are to be corrected. However, these architectures are not usually applied individually; in the state of the art, they are often combined. Since the CTLE can serve as

---

[1] Hongyang ZHANG. "CMOS Continuous-Time Linear Equalizers for High-Speed Serial Links". PhD thesis. University of Pavia, 2017.

[2] Sam PALERMO. *ECEN720: High-Speed Links Circuits and Systems*. Lecture slides, Lecture 8: RX FIR, CTLE, DFE, & Adaptive Eq. Spring 2025. 2025.

a stage that balances performance for subsequent blocks, it is commonly chosen as the initial reception stage or analog front end (AFE).

To carry out this design, it was necessary to understand the circuit topology and the parameters that affect its performance. This work outlines the decisions made throughout the design process. Thus, this document presents detailed information on equalization techniques and the parameters that directly influence the design. It then discusses the design decisions based on the state of the art and the characteristics of the chosen architecture. Finally, the results are presented along with conclusions and recommendations for future work.

OBJECTIVES

0.1. General Objectives

- To design a continuous time linear equalizer (CTLE) in a 28nm CMOS process to compensate for channel losses in a high-speed SerDes interface.

0.2. Specific Objectives

- To select an architecture to design a CTLE in a 28nm CMOS node based on state-of-the-art exploration.
- To apply bandwidth extension techniques to reduce power consumption.
- To validate the CTLE design based on PVT and Monte Carlo simulations.

1. PROJECT OVERVIEW

This chapter presents the key concepts underlying the design. It begins with an overview of the communication interface, followed by fundamental definitions such as the pulse amplitude modulation, the Nyquist frequency, the channel and its effects, including inter-symbol interference, and the concept of equalization. It then covers signal integrity parameters, including bit error rate, jitter, and the eye diagram.

1.1. High-Speed Interface

Communication systems are composed of a *transmitter* (TX), a transmission medium or channel, and a *receiver* (RX), which together form what is known as a *transceiver* (TRX) [3]. The Fig **1.1** presents a general system, where the three main blocks can be described as follows.

The **transmitter** refers to the system responsible for conditioning the input signal before it has been transmitted through the channel. This stage includes operations such as serialization, which converts the frame into a serial data stream, and equalization, which pre-shapes the signal before injection into the channel [4]. On the other hand, the **receiver** consists of circuits that condition the input signal after transmission through the channel. Its architecture typically includes recovery and synchronization mechanisms to ensure the highest possible signal integrity [4].

To understand how the signal is interpreted by the receiver, it is essential to consider how it was originally encoded for transmission. A common encoding scheme used in such systems is *pulse amplitude modulation* (PAM).

---

[3] Kyung Suk (Ken) HAN. *High-Speed Signaling: Jitter Modeling, Analysis, and Budgeting*. Prentice Hall, 2013.

[4] Davide MENIN. "Modelling and Design of High-Speed Wireline Transceivers with Fully-Adaptive Equalization". Doctor's thesis. Università degli Studi di Udine, 2021.

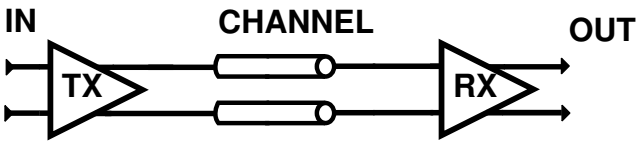


Figure 1.1. Transceiver generic structure.

1.2. Pulse Amplitude Modulation

PAM is generally used in signaling for wired communication. A simple and widely used form of PAM is *Non-Return-to-Zero* (NRZ), it consists of two levels in a series of pulses [1]. as shown in Fig **1.2**.

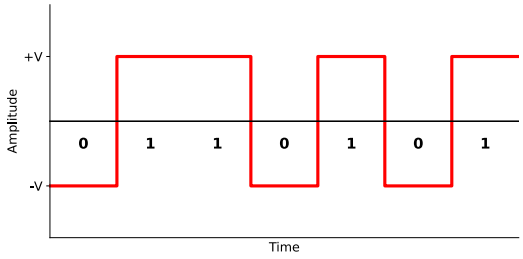


Figure 1.2. NRZ Modulation.

From Fig **1.2**, the following parameters can be defined: the distance between pulses corresponds to the *bit duration* (Tb), also known as the *unit interval* (UI), where the inverse of this period corresponds to the modulation data rate ($\frac{1}{T_b}$).

1.3. Nyquist Frequency

When transmitting a signal, regardless of whether it uses PAM or another modulation scheme, it is essential to preserve all its information without distortion. To ensure this, the condition $T_b < \frac{1}{2W}$ must be satisfied, where W is the maximum frequency component present in the signal [5]. This guarantees that the signal can be fully represented by

[5] Rodger E. ZIEMER. *Principles of Communications*. Wiley, 2015.

its sampled values and perfectly reconstructed by passing it through an ideal low-pass filter with appropriate bandwidth. The minimum sampling frequency required for this reconstruction is known as the Nyquist frequency, and is given by $2W$, meaning the sampling frequency must satisfy $f_s = \frac{1}{T_b} > 2W$ [5].

1.4. Channel

The channel is the medium through which information is transmitted. In the case of a high-speed interface, it consists of transmission lines, which in this context are data cables used to transmit electrical signals at high frequencies or in the GHz range such as universal serial bus (USB) [4].

These communication channels are bandwidth-limited, since a conventional high-speed interface channel behaves like a linear system that attenuates high-frequency components of the transmitted signal. This is mainly due to electromagnetic effects, such as the skin effect and dielectric losses. As a result, signal reflections may occur at the ends of the transmission line. To minimize these reflections, the channel is typically designed with a characteristic impedance of 50 Ω at the frequency of interest [3].

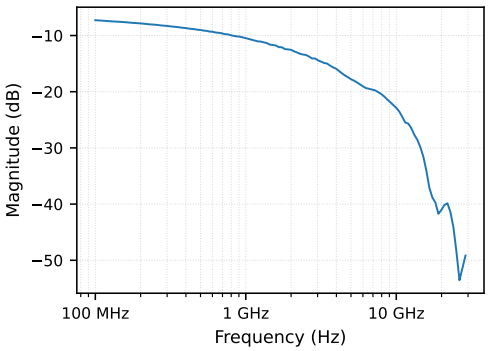


Figure 1.3. Frequency response of a channel.

Fig. **1.3** shows the common channel frequency response behavior, primarily affected by attenuation caused by the effects mentioned above.

1.5. Inter-symbol Interference

Due to the attenuating introduced by the channel and its frequency-dependent behavior, the signal experiences losses that vary across the frequency spectrum, as a result, the high-frequency components of the signal are filtered out by the channel, causing the pulses to attenuate or distort, deviating from their original shape. This attenuation affects the transmission, leading to errors in its interpretation. The attenuation of the bits pulses is known as interference, as it prevents the information from being recovered in its original form. This effect is most pronounced when the bit sequence changes rapidly, at the system's highest frequency. Channel losses are typically quantified at the Nyquist frequency, where the impact of attenuation is most significant [4].

1.6. Equalization

Because of the effects of the channel, equalization is used as a solution to create an inverse transfer function that can counteract these high-frequency effects. The goal is to compensate for the lost frequency components, thereby restoring the signal's integrity [1]. The system can be considered equalized if the combined transfer function of the channel and receiver exhibits a flat response beyond the Nyquist frequency, indicating that the most significant distortion has been mitigated like in Fig. **1.4**.

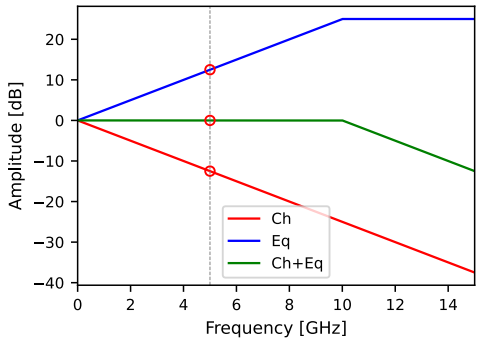


Figure 1.4. Ideal equalization response in the frequency domain.

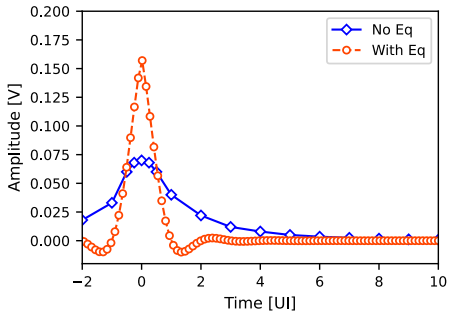


Figure 1.5. Ideal equalization response in the time domain.

In the time domain, equalization is evaluated using a test called single bit response (SBR), which involves sending a single pulse through the system or channel. The system's response to this impulse produces a set of points known as cursors. These cursors represent time points where the pre-cursors and post-cursors are null or approximately zero, indicating the absence of ISI or distortion [4]. This behavior can be observed in Figure **1.5**.

Equalization can be implemented in various ways; however, one of the most common approaches is the use of a continuous-time linear equalizer (CTLE). This circuit takes advantage of the mostly on the frequency-domain characteristics of equalization, aiming to attenuate the effects introduced by the channel through a transfer function similar to the one shown in Fig. **1.4**.

1.7. Signal Integrity Parameters

Signal integrity can be understood as the metric that indicates how accurately a signal has been received. In turn, it also reflects how correctly the signal has been recovered after passing through the transmission channel.

Equalization can be evaluated using several parameters that helps to assess signal integrity. Among these parameters are bit error rate (BER), jitter, and the eye diagram.

BER

Due to the presence of ISI, the system experiences a loss in the ability to recognize individual bits correctly. This leads to received bits being incorrectly interpreted. Such performance is measured through the BER, which corresponds to the ratio between the number of erroneous bits and the total number of received bits [5].

Jitter

Jitter refers to deviations of a signal from its ideal timing, becoming critical at high data rates. It can be analyzed in the time domain (waveforms), frequency domain (spectral density), and statistically (probability distributions), forming part of Total Jitter (TJ), jitter can be either deterministic or random [6].

- **Deterministic Jitter**

  Deterministic jitter (DJ) is bounded and repeatable, measured peak-to-peak, this representing the variations in the timing of the signal. It stems from channel attenuation, crosstalk, and ISI, leading to Data-Dependent Jitter (DDJ), or from Periodic Jitter (PJ), which is unrelated to data patterns [36].

- **Random Jitter**

  Random jitter (RJ) is unbounded and modeled with a Gaussian distribution. It arises from noise and is quantified using its standard deviation (σ) [3].

  A statistical plot of jitter is shown in Fig. **1.6** to illustrate its ideal behavior.

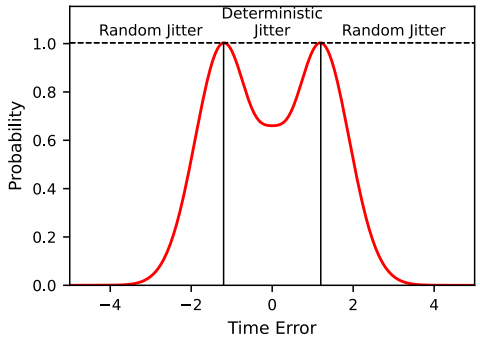


Figure 1.6. Jitter distribution.

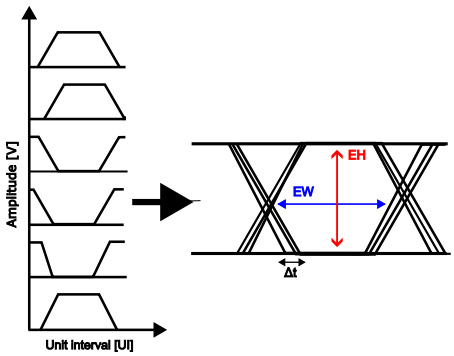


Figure 1.7. Eye diagram.

Eye-Diagram

---

[6] AGILENT. *Using Clock Jitter Analysis to Reduce BER in Serial Data Applications*. Application Note 5989-5718EN, December 1. Agilent Technologies. 2006.

The eye diagram is an important tool for signal analysis, as it provides some insight into what affects signal reception and how the system behaves overall based on the structure of the eye [4].

To obtain the eye diagram, the signal is captured over a unit interval (UI), and each period is superimposed such that all transitions of the transmitted data can be observed like in Figure **1.7**. From the resulting eye figure, several figures of merit can be extracted to evaluate system performance. Among these, the eye height (EH) and eye width (EW) stand out, as they indicate the timing and voltage margins available for correct sampling [6].

2. SPECIFICATIONS AND ARCHITECTURE

This section presents an analysis of the main architecture of the CTLE, the CMFB and the specifications that must be met, these arise from the need to meet some opening parameters necessary for subsequent stages to correctly identify the information received.

2.1. Analog Front End

Typically, the CTLE is only one part of a complete AFE system; therefore, in a larger project it is necessary to give specifications to each component. APPDX. *APPENDIX A*. 2025 provides further details on the AFE characteristics; the CTLE specifications are taken from this study and can be seen in Table **2.1**.

Table 2.1. CTLE specifications

Parameters	**Units**	**Design Target**		
		Min	**Typ**	**Max**
Bit Rate	Gbps	-	20	-
EH	mV	20	-	-
EW	UI	0.4	-	-
VDD	V	-	0.9	-
BER	–	-	-	1×10^{-12}

2.2. CTLE Architecture

The architecture used habitually for the CTLE is a differential pair with capacitive degeneration as shown in Fig. **2.1**. Neglecting the body effect and channel modulation, the circuit has the transfer function shown in Eq. **1**;

$$H(s) = \frac{gm}{C_L} \frac{s + \frac{1}{R_s C_s}}{(s + \frac{1+gmR_s/2}{R_s C_s})(s + \frac{1}{R_D C_L})} \tag{1}$$

where gm is the small signal transconductance of the transistors M_1 and M_2, C_L represents the load of the next stage. The roots of the system are defined from this equation (one zero ω_z and 2 poles ω_{p1} & ω_{p2}), in addition to the DC gain in Eq. **2** and the ideal peak gain in Eq. **3**.

$$A_{DC} = \frac{gmR_D}{1 + gmR_s/2} \qquad (2) \qquad\qquad A_{hfrq} = gmR_D \qquad (3)$$

In an optimal design, the zero satisfying than $\omega_z < \omega_{p1}$ and $\omega_z < \omega_{p2}$. With these conditions, the frequency response is expected to exhibit the behavior show in Fig. **2.2**. If this constraint is not met, there will be no gain increase at high frequencies.

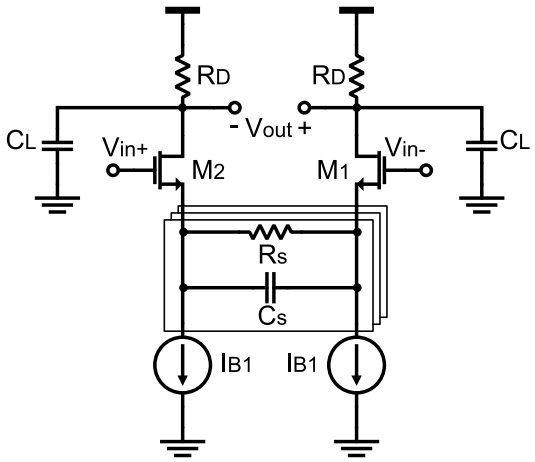


Figure 2.1. Basic CTLE.

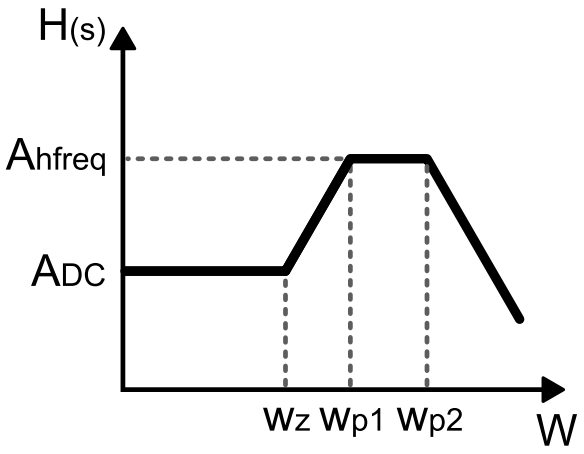


Figure 2.2. CTLE frequency response.

This behavior in the circuit is expected if certain idealities are taken into account, such as:

- The analysis is performed without any channel length modulation effect, a phenomenon that strongly affects this circuit.
- This circuit is very sensitive to process, voltage and temperature (PVT) variations [2], due to the need to use short channel transistors.

- The trade-off between power and bandwidth is well known, keeping in mind that in this circuit will operate at a high speed, a relatively high power consumption is expected, which translates into large transistors and significant parasitic capacitances.
- Due to the high current consumption, the common mode output node voltage is expected to be very sensitive in PVT.

To counteract these negative effects, we propose the use of the bandwidth expansion techniques described below.

2.3. Inductive peaking

One of the simplest ways to compensate the capacitive effect of the load is to add an inductor at the output node, as shown in Fig. **2.3**, thus generating a zero in the impedance of this node, which will increase the gain at high frequencies. This improvement in performance can increase the bandwidth by up to 70%. However, implementing the inductor has a strong area penalty in wafer area and these do not have a large quality factor [7].

There are circuits capable of emulating inductive behavior through the use of active components, and they can significantly reduce area consumption and enable tunable inductance. However, this approach has certain disadvantages, such as lower inductance ideality, higher power consumption, sensitivity to PVT variations, and limitations in the operating range. Despite these restrictions, the state-of-the-art shows successful

---

[7] Cristhian Rolando Torres DELGADO. "Front-end Circuit Techniques for High-Speed Interfaces". Master's thesis. Universidad Industrial de Santander, 2019.

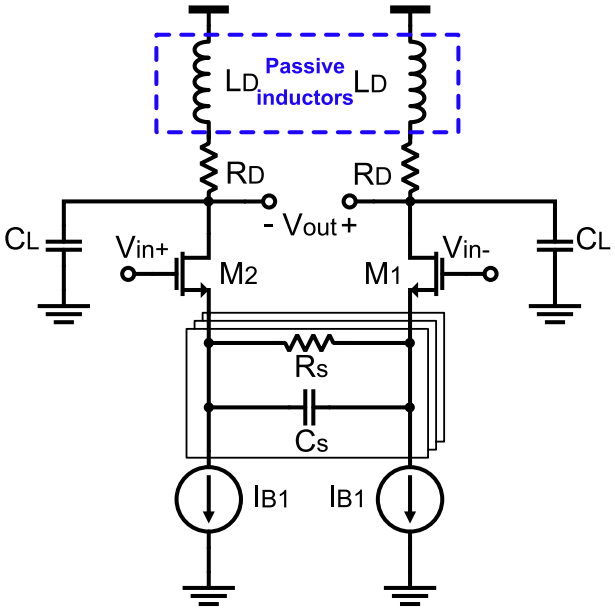


Figure 2.3. CTLE with inductors.

implementations of active inductors [8][7][9]. Some of these techniques have been implemented in this project and are described in detail in the next chapter.

2.4. Common mode feedback

The Common-Mode Feedback (CMFB) circuit is commonly used in systems with differential outputs. Due to imperfections such as voltage mismatch, current mismatch, and PVT variations, the CMFB circuit stabilizes the common-mode voltage of the differential branches based on a reference voltage due to the need to keep the transistors

---

[8] Jonghyuck CHOI et al. “A single-ended nrz receiver with gain-enhanced active-inductive ctle and reference-selection dfe for memory interfaces”. In: *IEEE Journal of Solid-State Circuits* 59.4 (2024), pp. 1261–1270.

[9] Behzad RAZAVI. “Design techniques for CMOS wireline NRZ receivers up to 56 Gb/s”. In: *IEEE Open Journal of the Solid-State Circuits Society* 3 (2023), pp. 118–133.

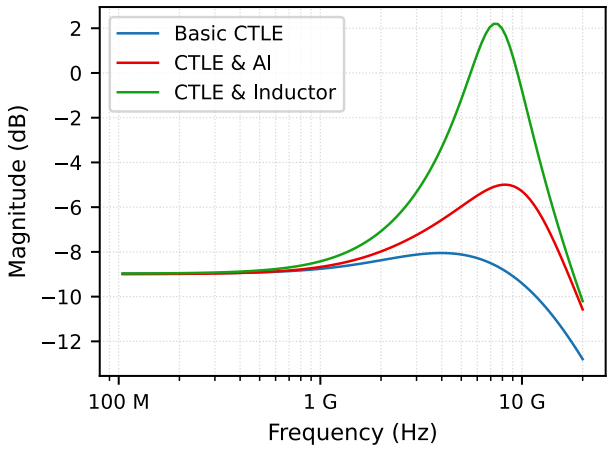


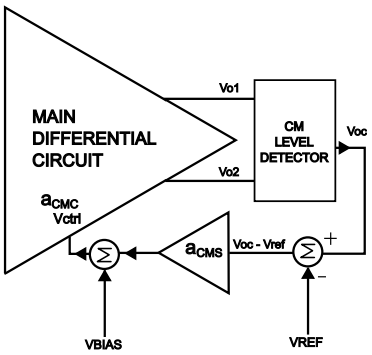
Figure 2.4. Frequency response of CTLE with different bandwidth expansion techniques.

biased in the correct region [10]. This makes the transistor biasing procedure dependent of the CMFB performance.

The core structure of a CMFB circuit consists of a sensing block and an error amplifier. The CMFB adjusts the common-mode voltage by implementing a feedback loop. To achieve this, a reference voltage is provided, and an error amplifier generates a bias voltage, which is then used in the main differential circuit. This loop can be observed in Fig. **2.5**

The loop consists of the path from the reference voltage to the output V_{oc}. From this, the equations in Eq. **4** can be derived. Here, A_{CMC} corresponds to the gain from the control voltage to the common-mode output voltage V_{oc}. In this case, the CM level detector averages the signals V_{o1} and V_{o2} to obtain a single average value to be processed. The gain A_{CMS} represents the gain of the error amplifier, while the CMFB gain corresponds to the overall system gain. The objective is to achieve a CMFB gain equal to 1, meaning that the common-mode output voltage matches the reference voltage. This ensures

[10] Paul R. GRAY et al. *Analysis and Design of Analog Integrated Circuits*. 5th ed. Wiley, 2021.



$$A_{cmc} = \frac{V_{oc}}{V_{ctrl}}$$
$$A_{cms} = \frac{V_{ctrl}}{(V_{oc} - V_{ref})} \quad @V_{bias} = 0 \tag{4}$$
$$A_{CMFB} \approx \frac{V_{oc}}{V_{ref}} \approx 1$$

Figure 2.5. Basic Common Mode Feedback.

that the common-mode voltage at the output of the differential circuit is properly fixed or follows the reference, which is the purpose of the system.

With these equations in mind, it is possible to generalize the system into a single expression for A_{CMFB}, as shown in Eq. **5**. The purpose of this equation is to analyze the conditions required for the optimal setting of the common-mode voltage.

$$A_{CMFB} = \frac{V_{oc}}{V_{oc} - \frac{V_{ctrl}}{A_{cms}}} = \frac{1}{\frac{V_{ctrl}}{V_{oc} \cdot A_{cms}}} = \frac{1}{1 - \frac{1}{A_{cmc} \cdot A_{cms}}} = \frac{(-A_{cmc}) \cdot A_{cms}}{(-A_{cmc}) \cdot A_{cms} + 1} \tag{5}$$

From this equation, we conclude in Eq. **6** that, in order to properly fix the common-mode voltage, the loop gain must be much greater than 1. This ensures a significant reduction of the error in regulating the common-mode voltage, allowing the system to correctly fix or track the reference. Furthermore, to maintain the loop operation, this condition also implies stability requirements, where the phase margin plays an important role.

$$a_{cms}(-a_{cmc}) \gg 1, \quad A_{CMFB} \approx 1 \tag{6}$$

Although the CMFB is designed for DC operation, in reality common-mode variations are not limited to DC; they can also appear in AC, such as certain types of channel noise, electromagnetic effects, among others. Therefore, the CMFB must be capable

of enforcing the common-mode value over frequency as well. In this way, the bandwidth is taken into account in the CMFB design, without overlooking the fundamental parameters, which are the loop gain and the stability of the circuit.[10]

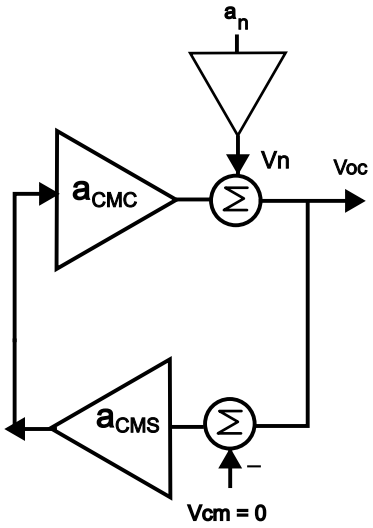


Figure 2.6. AC common-mode variations on Common Mode Feedback.

In Fig. **2.6** an alternative block diagram of the CMFB is shown, where noise is injected into the system through a_n, with v_n representing the noise voltage that is added. From this block diagram, the equations in Eq. **7** can be derived, where the first term a_n corresponds to the noise contribution at the output, and the term A_n represents the output noise but attenuated by a factor of $1 + a_{CMS}(-a_{CMC})$. As this value increases, the common-mode variation becomes smaller. It is worth noting that $V_{cm} = 0$ implies that the small-signal component inserted into the system is zero; this applies only when the system is considered without bandwidth.

$$\begin{aligned} a_n &= \left.\frac{v_{oc}}{v_n}\right|_{\text{no CMFB}} = \left.\frac{v_{oc}}{v_n}\right|_{v_{cm}=0} \\ A_n &= \left.\frac{v_{oc}}{v_n}\right|_{\text{with CMFB}} = \frac{a_n}{1 + a_{cms}(-a_{cmc})} \end{aligned} \tag{7}$$

3. CTLE DESIGN PROCESS

This chapter discusses circuit design in detail. The architecture of CTLE and CMFB is presented at the transistor level, along with an exploration of the design equations and essential characteristics to be considered during the design phase.

3.1. Design methodology

Fig. **3.1** shows the methodology flow diagram implemented to meet the specifications of Table **2.1**. The first step is characterize the PDK, from which the curves are extracted and analyzed to estimate the possibilities and limitations of the technology. After this, an analysis of some of the bandwidth expansion techniques conventionally used in CTLE is performed, obtaining the design equations for them. With these equations, it is proposed to develop a behavioral model in verilog-A [11] in which the frequency behavior of the circuit is described. When it comes to solving equations to obtain roots in desired positions, the task is repetitive and error prone, therefore, a Python function is implemented to receive as input the position where the roots of the system are to be located [12].

Once the small-signal parameters required in the circuit are established, the operating point is set to dc, and here the power consumed by the circuit and the saturation margins are established. At this point a definition of the ranges for the R_s and C_s banks was made, then the bandwidth expansion circuits were designed, this is reviewed in depth in the following sections.

---

[11] APPDX. *APPENDIX B*. 2025.

[12] APPDX. *APPENDIX C*. 2025.

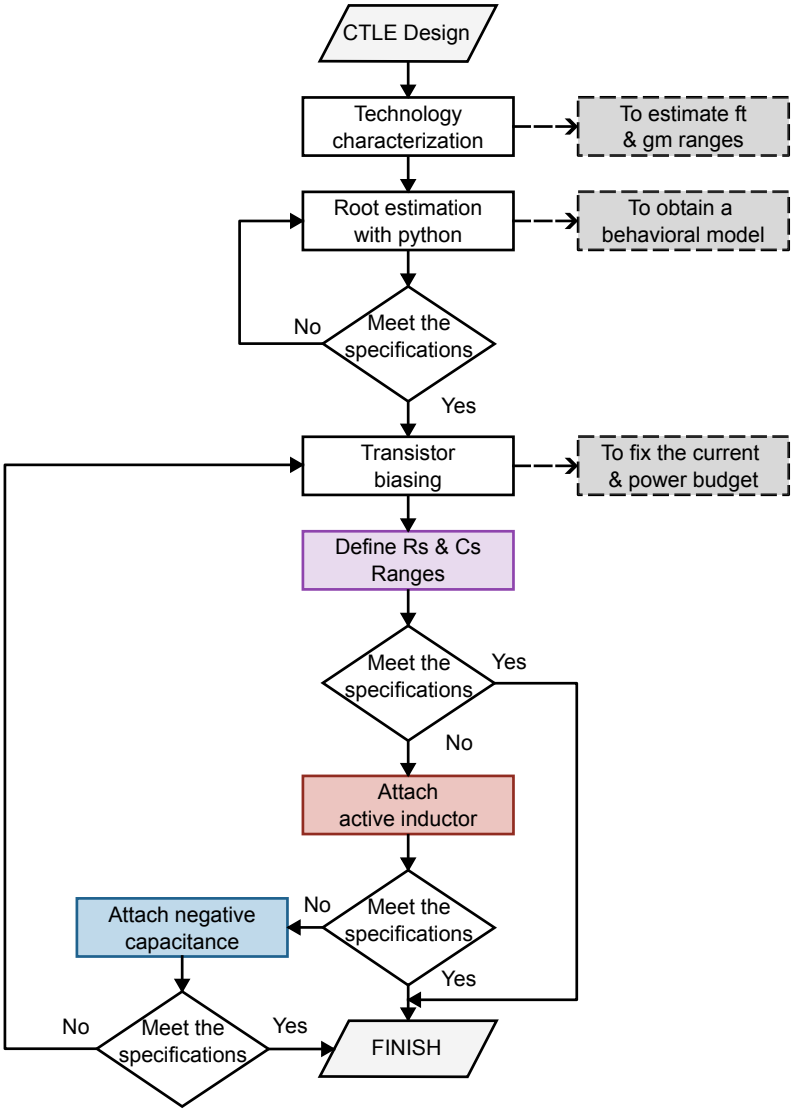


Figure 3.1. CTLE design methodology flowchart.

3.2. R_s & C_s banks

Considering that a high frequency response sensitivity is expected from the circuit in PVT, the use of a variable degeneration resistor and capacitance is proposed. As can be seen in the equations of the Eq.**2** and **1** R_s can control the gain of the circuit at low frequencies and C_s the main zero position [13]. Each bank can be seen in Fig. **3.2** and Fig. **3.3**.

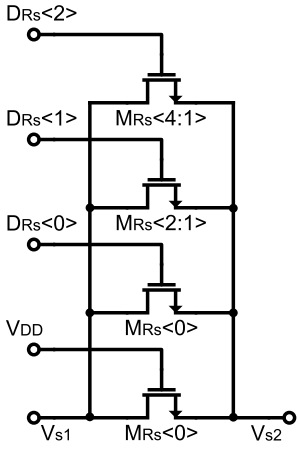


Figure 3.2. R_s circuit.

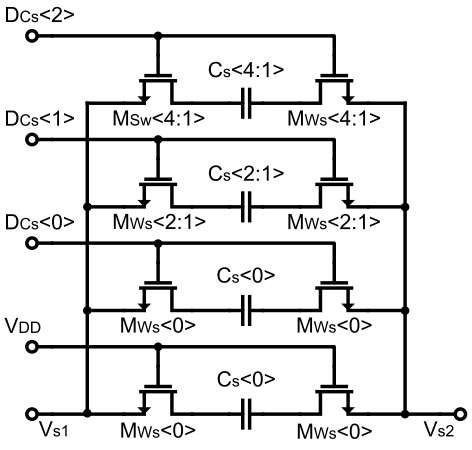


Figure 3.3. C_s circuit.

Each circuit is controlled with 3-bit as shown in the table 3.1. Both circuits operate on the principle of operating transistors in their triode region, i.e. as resistors. An approximation of the equivalent resistance between source and drain of a transistor whose V_{ds} is significantly small can be seen in Eq. **8**. For R_s the size of each resistor was adjusted to obtain the desired resistance, and in C_s the transistors sizes were set so that these transistors have a very low resistance.

$$R_{ON} \approx \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{gs} - V_{TH})} \tag{8}$$

---

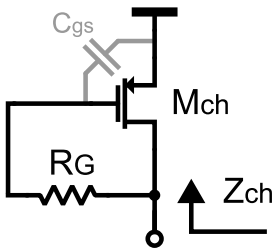
[13] David Alejandro Reyes GONZÁLEZ. "Diseño de un ecualizador lieal de tiempo continuo (CTLE) para interfaces de alta velocidad integrado en tecnología CMOS". Bachelor's thesis. Universidad Industrial de Santander, 2017.

Table 3.1. Bank combinations

Digital code	**R**$_{seq}$	**C**$_{seq}$
000	R_s	C_s
001	$R_s/2$	$2C_s$
010	$R_s/3$	$3C_s$
011	$R_s/4$	$4C_s$
100	$R_s/5$	$5C_s$
101	$R_s/6$	$6C_s$
110	$R_s/7$	$7C_s$
111	$R_s/8$	$8C_s$

3.3. Bandwidth expansion techniques

Initially the use of the cherry-hooper circuit was proposed and can be seen in Fig. **3.4**. This circuit has a diode-type connection, and a resistor between the gate of the transistor and the drain represents an impedance with 2 poles and 1 zero. In Eq. **9** can be seen as an approximation of this impedance with dominant C_{gs}.



$$Z_{ch}(s) = \frac{1}{gm}\frac{1 + R_g C_{gs} s}{1 + \frac{C_{gs}}{gm} s} \tag{9}$$

Figure 3.4. Cherry-hooper circuit and equivalent impedance.

In [7], the use of this circuit in conjunction with the cross-coupled pair (XCP) technique is proposed. Our initial objective was to implement both techniques simultaneously, in order to increase the gain at high frequencies and bandwidth; however, a problem related to polarization was identified. Both the Cherry-Hooper circuit and the XCP have a diode-type connection, and the gate voltage of $M_{3,4}$ and $M_{5,6}$ are determined by the same node, as shown in Fig. **3.5**.

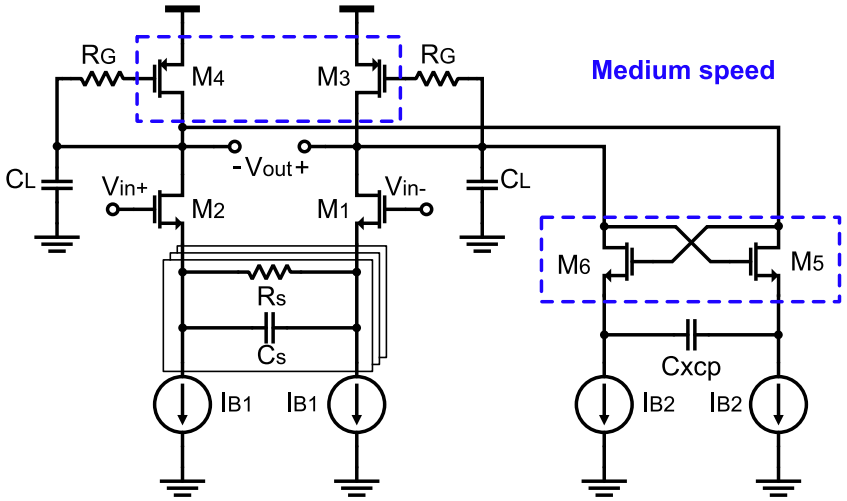


Figure 3.5. CTLE with cherry-hooper and XCP.

The transition frequency (f_T) of transistor is given by Eq. **10** for long-channel devices, while its dependence for short-channel devices is expressed in Eq. **11**. These equations highlight how the transistor speed depends on the overdrive voltage, the channel length, and the g_m/I_D ratio; it is necessary to reduce L if speed is to be maximized. In addition, it is known that the gm/I_D curve is inversely dependent to V_{ov}, this relation is countered by the quadratic proportionality of ft to V_{ov}, so it is concluded that the higher the V_{ov}, the faster the transistor will operate.

$$ft = \frac{gm}{I_D} \cdot \frac{\mu_n \alpha V_{ov}^2}{L^2} \qquad (10) \qquad\qquad f_T \propto \frac{v_{\text{sat}}}{L} \qquad (11)$$

Since the supply voltage range is limited (0.9 V under typical conditions), it is not possible to bias both pairs of transistors at a point where their f_T exceeds at least ten times the operating frequency of the circuit [14]. Consequently, this architecture only allows for achieving a moderate velocity (near to half of the required f_T as can be seen in the Fig. **3.7**) for both pairs, which is insufficient to meet the implementation speed requirements.

[14] Behzad RAZAVI. *Design of Analog CMOS Integrated Circuits*. 2nd. McGraw-Hill Education, 2017.

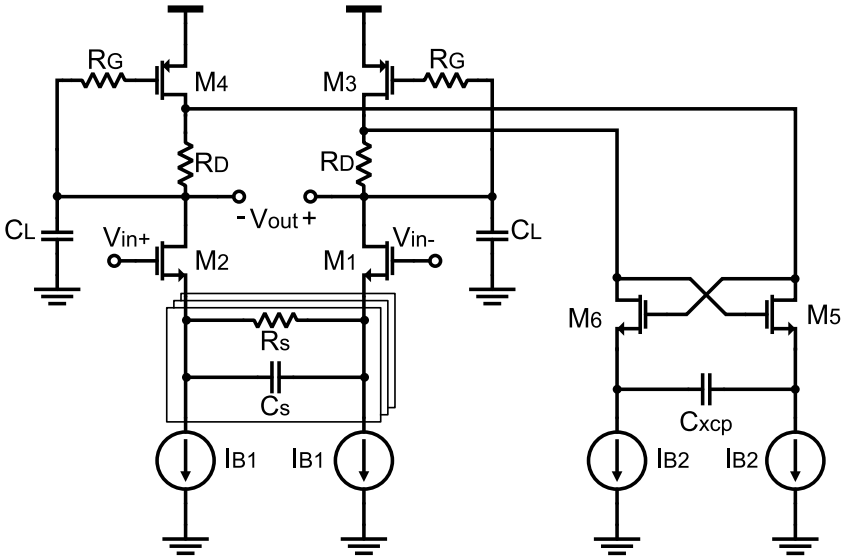


Figure 3.6. Proposed CTLE with GE-AI and XCP.

To solve this problem, the architecture in Fig. **3.6** was proposed for the equalizer. This circuit uses as active inductance the circuit proposed in [8], combined with the XCP. The objective of implementing a gain-enhanced active inductor (GE-AI) is to generate a potential difference between R_D sufficient to operate both the $M_{3,4}$ and $M_{5,6}$ transistors at an acceptable f_T as show in Fig. **3.8**.

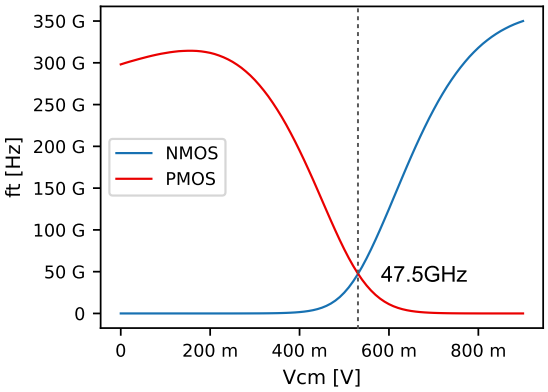


Figure 3.7. V_{cm} vs f_T in cherry-hooper & XCP.

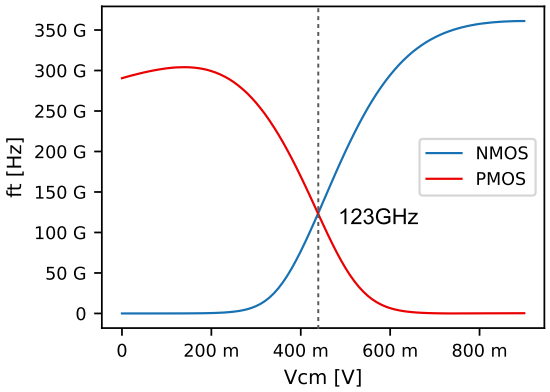


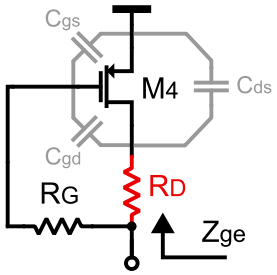
Figure 3.8. V_{cm} vs f_T in GE-AI & XCP.

In this way, it is possible to work with two bandwidth expansion techniques simultaneously in a very efficient way.

3.4. Gain-enhanced active inductor

The circuit of Fig. **3.9** presents an impedance that has 2 poles and 2 zeros, thanks to the resistor Rd, this allows to have a greater control over the frequency response of the circuit (in comparison with the Cherry-Hooper); however, this degrades the performance of the system. In [8] this circuit is used as the only method of bandwidth expansion, in order to compensate for the lack of control over the frequency response of the Cherry-Hooper.

In this work, the purpose is to give a different approach to the GE-AI circuit, using it exclusively to improve the operating point, by not implementing the GE as a control method, this need must be supplied; this function is fulfilled by the XCP providing an impedance independent of the GE-AI.



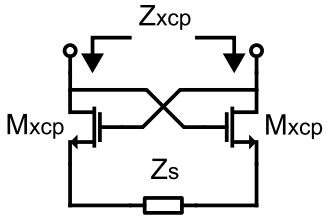
$$Z_{\text{ge}} \approx \frac{s \cdot C_{\text{GS}} \cdot (r_o + R_D) \cdot R_G + R_D + r_o}{s \cdot C_{\text{GS}} \cdot [(R_D + R_G) + r_o] + g_m \cdot r_o + 1} \tag{12}$$

Figure 3.9. GE-AI and equivalent impedance approximation

To achieve a behavior as close as possible to the Cherry-Hooper topology, the size of the transistors was minimized to reduce parasitic capacitances and thus bring the circuit response closer to the desired function. To meet the required value of C_{gs}, which is a design parameter, an additional capacitor was used. The equation **12** is an approximation of the impedance seen, considering $C_{gs} >> C_{gd}$ and $C_{gs} >> C_{ds}$.

3.5. Cross-coupled pair

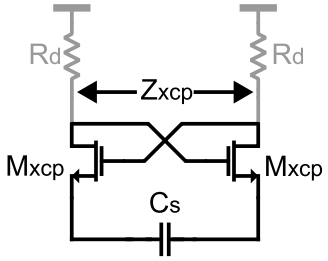
The XCP circuit presented in Fig. **3.10** consists of a pair of transistors whose drains and gates are cross-connected. When the voltages at these nodes are equal or very similar, the circuit is in an equilibrium state [15]. Under these conditions, the circuit behaves as a negative impedance given by Eq. **13**.



$$Z_{\text{xcp}} = -\frac{2}{gm} - Z_s \qquad (13)$$

Figure 3.10. XCP and equivalent impedance.

This analysis is studied in depth in [16]. It is possible to show that, in the frequency domain, a negative capacitance exhibits a behavior equivalent to that of an inductor.



$$Z_{\text{xcp}} = R_d \frac{1 + s\frac{2C_{xcp}}{gm_{xcp}}}{1 + s\frac{2 - R_d gm_{xcp}}{gm_{xcp}}} \qquad (14)$$

Figure 3.11. XCP with equivalent resistors and equivalent impedance.

The position of the zero in the frequency spectrum is designed to be below the Nyquist frequency. The setting of this root does not involve great complexity, since it is determined by Eq. **14**. The real challenge in the design of this circuit lies in maintaining a

---

[15] Behzad RAZAVI. “The cross-coupled pair-part i [a circuit for all seasons]”. In: *IEEE Solid-State Circuits Magazine* 6.3 (2014), pp. 7–10.

[16] APPDX. *APPENDIX D*. 2025.

voltage on the gates high enough to ensure the correct biasing of the current sources, while ensuring a sufficiently high f_T.

3.6. Common Mode Feedback

For the design of the CMFB, the conditions previously discussed in Section **2.4** were considered. These conditions relate directly to stability, loop gain, and bandwidth, with priority given to the first two in order to ensure the best circuit performance. The proposed design employs a current mirror amplifier, which enables a trade-off between bandwidth and gain, thereby satisfying two of the specified conditions. This configuration is illustrated in Fig. **3.12**, where current mirrors with a 1:B ratio are used.

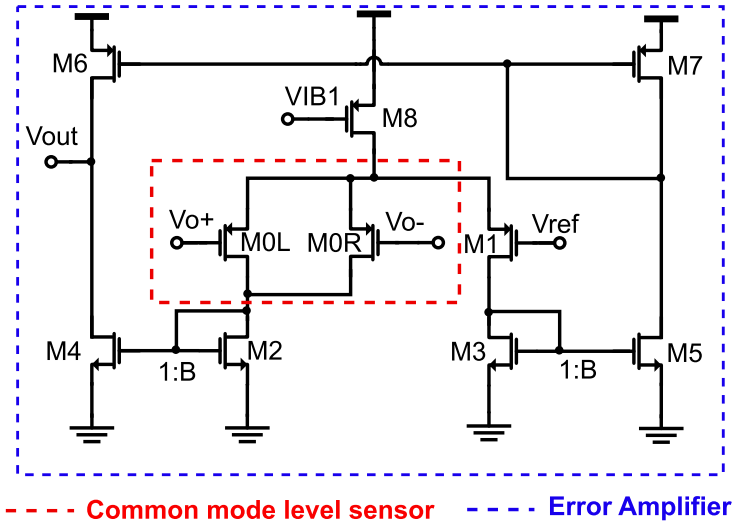


Figure 3.12. Error Amplifier for Common Mode Feedback.

To meet the sensing requirements, a current-sensing technique is applied. The input transistor is divided into two devices, each with half the channel width, so that only half of the current flows through each. This leads to Eq. **15**, where the sum of these drain currents in M2 corresponds to their average. Through the feedback loop, this current is corrected with respect to the reference current injected by M1, which is biased with the common-mode reference voltage required in the system.

$$I_{CM} = \frac{I_{o+} + I_{o-}}{2} \tag{15}$$

where I_{o+} represents the current flowing through transistor M0L, while I_{o-} represents the current flowing through transistor M0R.

The signal flow of the CMFB can be seen in Fig. **3.13**, where it passes through the common-mode sensing transistors, is mirrored, and then leaves the circuit. The goal is for the common-mode voltage (Vcm) to track the reference voltage (Vref). This is achieved through the loop action, which progressively reduces the error. The corrected voltage is then applied to the control transistor Mctrl, as shown in Fig. **3.14**. Mctrl injects a current that adjusts the common-mode voltage by setting the circuit bias, repeating the cycle until the desired potential is reached.

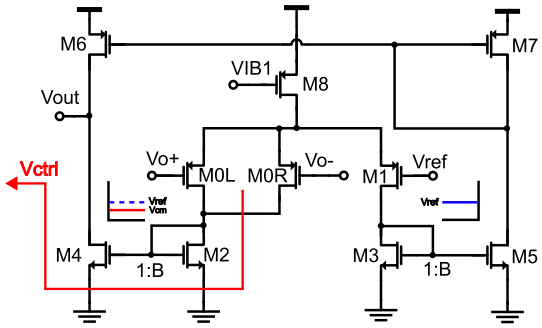


Figure 3.13. Common Mode Feedback signal path through the Amplifier.

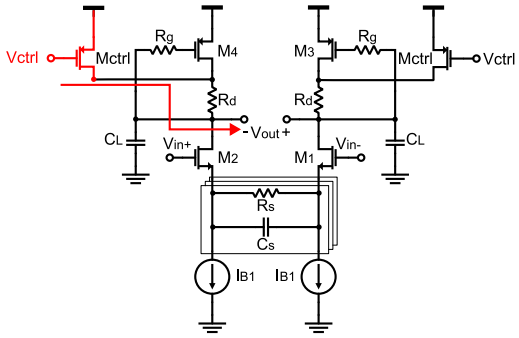


Figure 3.14. Common Mode Feedback signal path through the CTLE.

Since the CMFB must not interfere with the operation of the main differential circuit, it takes advantage of the low impedance provided by the current mirrors in the first stage. As a result, the sensing circuit does not significantly affect the frequency response of the main circuit. The corresponding equations that describe this behavior are shown in Eq. **16**.

$$
\begin{aligned}
A_v &= B g_{m0,1}(r_{on} \parallel r_{op}) \\
\omega_{p1} &= \frac{1}{C_L * (r_{on} \parallel r_{op})} \\
\omega_{p2} &= \frac{g_{m2,3}}{C_{M2,3}} \approx \frac{g_{m2,3}}{(1+B)C_{gs2,3}}
\end{aligned}
\tag{16}
$$

Here, two key parameters are identified: B, which represents the ratio between M2, M3 and M4, M5; and CMP, which corresponds to the capacitance observed at the gate-to-ground node of the current-mirror transistors.

Since the CMFB must satisfy stability requirements, the proposed topology prioritizes phase margin. To achieve this, compensation techniques are employed—in this case, Miller compensation. The small-signal model of the amplifier with the implemented technique is shown in Fig. **3.15**. Compensation is achieved by inserting a compensation capacitor C_z, which separates the poles as expressed in Eq. **16**. Additionally, a compensation/nulling resistor R_z is used, since the capacitor introduces a zero. By properly selecting its value, based on the equations in Table **3.2**, this zero can be canceled, resulting in an improved trade-off among gain, bandwidth, and phase margin. Given that an error of less than or equal to 5% is required, this approach provides a suitable solution to meet the design specifications.

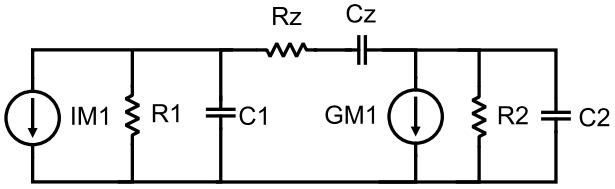


Figure 3.15. Small-signal compensation model for Common Mode Feedback.

Table 3.2. Equations used for compensation

Parameter	Expression
R_1	$\frac{1}{g_{m2,3}} \parallel r_{o0,1}$
R_{2A}	$r_{o4} \parallel r_6$
R_{2B}	$\frac{1}{g_{m7}} \parallel r_{o5}$
P_1	$-\frac{1}{G_{M1}R_2R_1C_Z}$
P_2	$-\frac{g_{m1}C_Z}{C_1C_2+C_Z(C_1+C_2)}$
P_3	$-\frac{1}{R_ZC_1}$
Z	$-\frac{1}{\left(\frac{1}{G_{M1}}-R_Z\right)C_Z}$

The equations shown in Table **3.2** are derived from the analysis of Fig. **3.15**, thus allowing further analysis by taking them into account. Due to the use of compensation on both sides of the circuit, R_{2A} and R_{2B} are shown in Table **3.2**.However, the compensation technique applies the same expressions to both sides of the circuit. Implementing compensation symmetrically takes advantage of the system's ability to maximize pole separation.

The implementation of this technique is shown in Fig. **3.16**., where a transistor operating in the triode region is used as a resistor. This approach minimizes the use of components other than the transistors available in the technology. In addition, a biasing or tuning system is included in the design of this resistor to make it more robust against PVT variations, since the bias voltage may change under such conditions, and it is desirable for the zero to track these variations as closely as possible.

3.7. Polarization current mirrors

The circuit shown in Fig. **3.17** is responsible for biasing the CTLE. These transistors, represented as I_{B1} and I_{B2} in Fig. **3.6**, receive special attention because they must deliver a current in the order of milliampere units, stay in saturation, and ideally have a high dynamic resistance (r_o). Due to the low margin for the V_{ds} consumed by these

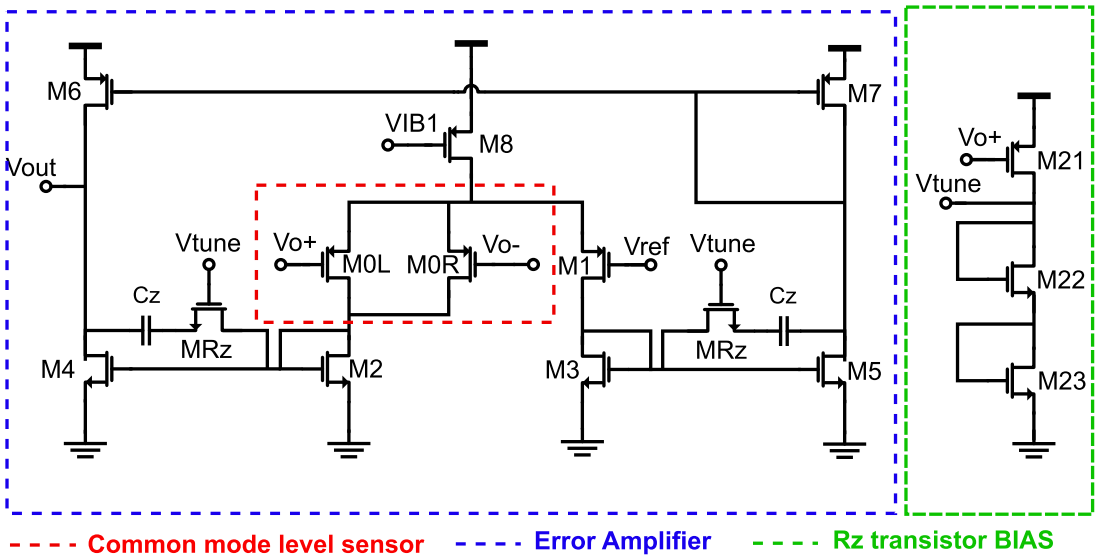


Figure 3.16. Compensated Error Amplifier for Common Mode Feedback.

transistors, the low power supply, and the V_{gs} requirement of the input transistors, the conventional architecture was chosen, taking a reference current of $50[\mu A]$.

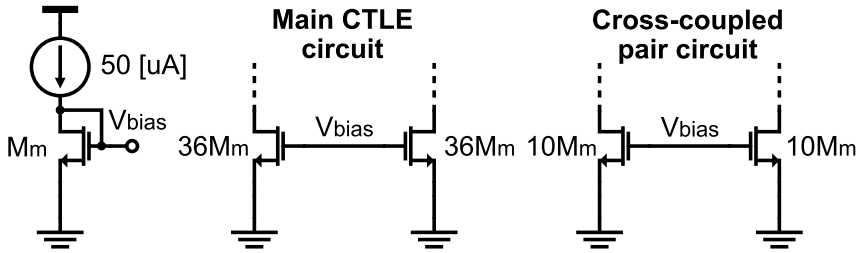


Figure 3.17. Current mirrors.

A total of 36 times the reference current was mirrored into the input branch, and 10 times into the XCP branch. Under nominal conditions, the output resistance r_o of the mirrors that feed the input transistors is approximately $9.6[k\Omega]$,, which is relatively low. However, if the model is analyzed in small-signal conditions, as shown in Fig. 3.18, this resistance appears in parallel with the equivalent $R_s/2$. Considering this, an adjustment was made to the resistor bank, which conveniently avoids the need for a high resistance at the node connected to the source of the M_{in} transistor.

The mirrors that feed the XCP as they need fewer multiplayers have a higher resistance,

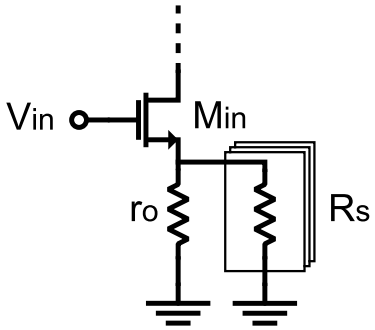


Figure 3.18. Equivalent dc circuit of current mirror.

this is $16.4k\Omega$, this non-ideality worsens little the performance of the circuit.

3.8. Operation point

For the validation simulations, operating point checks, ac and transient analysis were performed. For the operating point, all transistors were verified to meet the saturation condition. The CMFB transistors are expected to change region between strong and weak saturation, depending on the variation of the VDD corner, as explained below.

- Fig. **3.19** shows the typical operating state: both the GE-AI transistor and the CMFB transistor operate in strong inversion and remain in saturation. In this region, they are expected to consume significant current and exhibit high speed, characterized by a high transition frequency f_T.

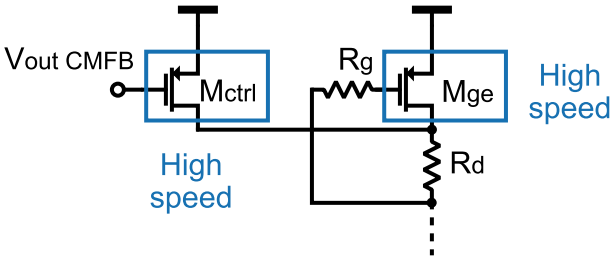


Figure 3.19. Typical VDD corner, speed of M_{ctrl} and Mge.

- Fig. **3.20** presents the corner $V_{DD} = 0.81[V]$, M_{ge} has its gate voltage fixed by the CMFB. As a result, its V_{sg} decreases, reducing its speed and pushing it into weak

inversion. M_{ctlr} compensates by acquiring higher Vsg, higher current, and thus very high speed.

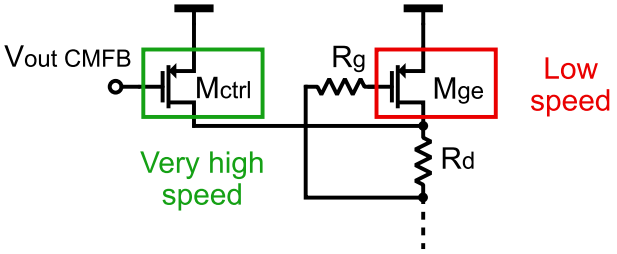


Figure 3.20. Low VDD corner, speed of M_{ctrl} and Mge.

- Fig. **3.21** presents the corner $V_{DD} = 0.99[V]$, M_{ge} operates with a high (V_{sg}), resulting in a large drain current and a high f_T, which provides very high speed. As the operating conditions evolve, M_{ctrl} reduces its current, entering weak inversion and consequently exhibiting a lower transition frequency and reduced speed.

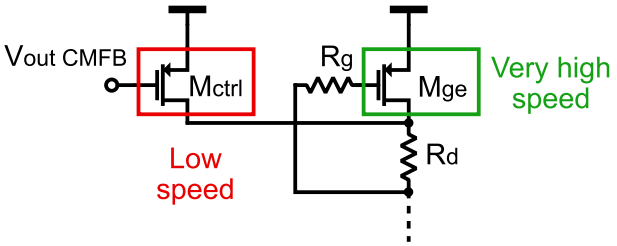


Figure 3.21. High VDD corner, speed of M_{ctrl} and Mge.

3.9. AC analysis

This simulation was performed to have an approximation of the circuit behavior in the frequency spectrum, an ac source was used to observe the response of the channel to be equalized, the frequency response of the equalizer, and the product of both systems.

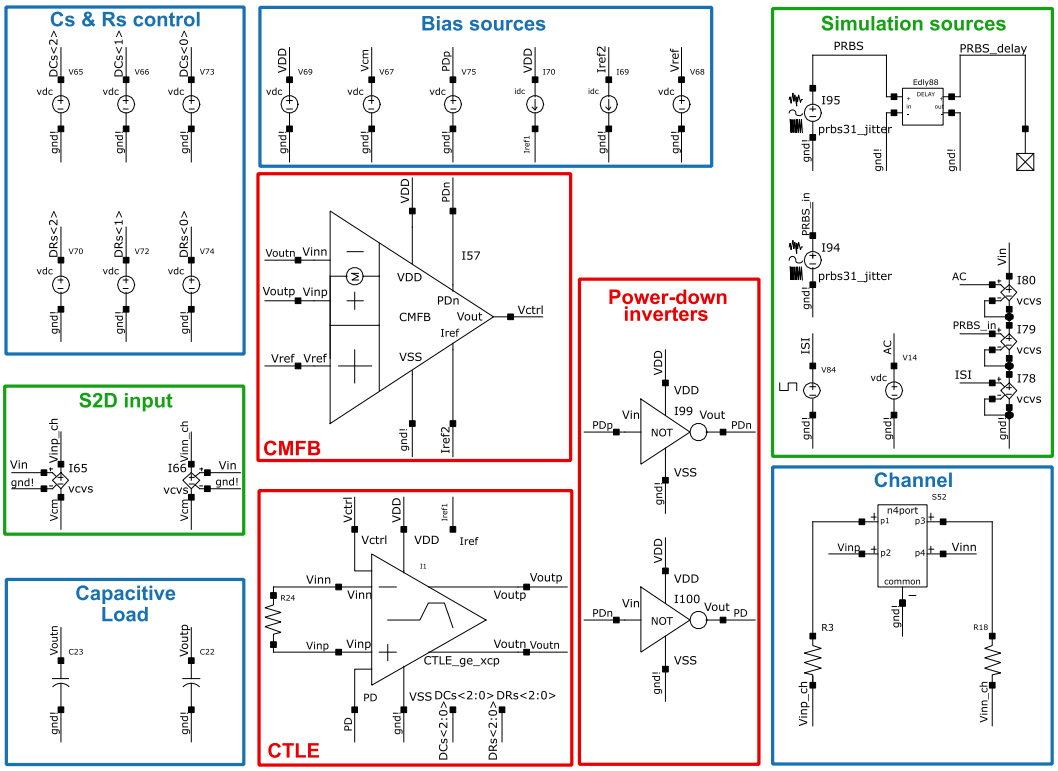


Figure 3.22. Test-bench for OP, AC and transient simulation.

3.10. Transient

This is the most relevant simulation, as it allows to verify in a concrete way the behavior of the system, since it is in the time domain that the circuit will work, and it is here where the tool uses its most accurate models.

Fig. **3.22** shows the testbench performed; as a first step, the impulse response (single bit) is analyzed, which allows to clearly observe the improvement in the inter-symbol interference (ISI) **1.5**. Then a transient response is performed with a series of random bits generated with a pseudo-random bit sequence (PRBS) from the transmitter, this source has the properties shown in Table **3.3**, the amount of jitter was taken from USB4

Gen3 [17].

Table 3.3. PRBS source properties

Characteristic	Value
Type	PRBS31
T_b	$50[ps]$
t_r	$5[ps]$
t_f	$5[ps]$
RJ	$0.14[UI]$
SJ	$0.085[UI]$
UJ	$0.085[UI]$
TJ	$0.31[UI]$

These specifications are intended to represent the worst-case scenario in which the transmitter sends a signal. Under these conditions, a minimum aperture specification is aimed to be met in the eye diagrams.

For the simulation to determine the compliance of the circuit, the superposition of the eye diagrams for a quantity of $10^6[bits]$ [17] was performed to verify the aperture value and the BER of the system.

[17] USB IMPLEMENTERS FORUM. *USB4™ Specification Version 2.0 with Errata and ECN REDLINE*. `https://www.usb.org/document-library/usb4r-specification-v20`. 2024.

4. RESULTS

In this chapter, the final dimensions of all devices are presented. Subsequently, the simulation results of Eye Diagram, offset across corners, Monte Carlo and process variations, have been included, at the end a comparison with other works in the state of the art is done.

4.1. Transistor sizing

CTLE

Table **4.1** lists the dimensions of each transistor shown in Fig. **3.6**. It is important to clarify that the MIB transistors correspond to those in the bias branch (current mirror). In this case, long-channel transistors are employed in the current mirrors to minimize copying errors and to avoid the non-ideal effects associated with short-channel devices, as illustrated in Fig. **3.17**.

The Mctrl transistors correspond to the CMFB control devices, as shown in Fig. **3.19**, while the MPD transistors are used for the power-down functionality.

Finally, the column of multipliers in Table **4.1** indicates the number of transistors connected in parallel. This technique allows achieving a total effective width larger than the maximum width permitted by the technology design rules.

Table 4.1. CTLE transistor dimensions.

Parameter	**M1/M2**	**M3/M4**	**M5/M6**	**MIB1**	**Mctrl**	**MIB2**	**Mm**	**MPD1**	**MPD2**
Width [μm]	3	3	3	2.8(35)	2.7	2.8(35)	2.8	0.5	1
Length [μm]	0.03	0.03	0.03	1	0.03	1	1	0.1	0.03
Multipliers	26	9	10	204	6	60	6	5	10

Table **4.2** shows the dimensions of the capacitors and resistors used in the circuit. In

this case, the capacitors were implemented using metal-oxide-metal (MOM) structures, and the resistors were implemented using P+ poly resistors, as shown in Fig. **3.6**, considering their availability in the TSMC 28nm PDK.

Table 4.2. CTLE capacitor and resistor Dimensions.

Parameter	**Cgs**	**Cxcp**	**Rg**	**Rd**
Finger width [μm]	0.05	0.05	-	-
Finger length [μm]	1	1	-	-
Finger space [μm]	0.05	0.05	-	-
Fingers	220	70	-	-
Segment width [μm]	-	-	2	2
Segment length [μm]	-	-	2	3
Number of segments	-	-	2	10

where C_{gs} is the gate-source capacitor in the gain-enhanced inductance (Fig. **12**); C_{xcp} the cross-coupled capacitance (Fig. **3.11**); R_g the gate resistance (Fig. **12**); and R_d the drain resistance (Fig. **12**).

The properties shown in the table correspond to the physical structure of the resistors and capacitors used to achieve the desired value, such as the width and length of the materials employed.

R$_s$ & C$_s$ banks

Table **4.3** summarizes the dimensions of the transistors, as well as the values of the capacitors (C_s) and resistors (R_s) used in the corresponding banks, shown in Fig. **3.2** and Fig. **3.3**.

Table 4.3. Dimensions for C_s and R_s banks.

Parameter	MRs	MWs	Cs
Width [μm]	3	3	0.05
Length [μm]	0.03	0.15	10
Multipliers	10	1	–
Fingers	1	1	18
Finger space [μm]	–	–	0.05

Digital Blocks

Due to the use of power-down devices in Fig.**3.6**, inverters are required to control them. The corresponding inverter sizes are provided in Table **4.4**. These inverters are external to the main circuit.

Table 4.4. Inverter transistor dimensions.

Parameter	$\mathbf{M}_{INV}$
Width [μm]	0.1
Length [μm]	0.03
Multipliers	1
Fingers	1

CMFB

Tables **4.5** and **4.6** highlights the dimensions of the transistors used in the CMFB circuit, as shown in Fig.**3.16**. In this case, **MRef** corresponds to the BIAS transistor, **MPD1** and **MPD2** are power-down devices for the error amplifier, and **MRz** defines the dimensions of the active resistor transistor.

Table 4.5. Transistor dimensions of the error amplifier (Part 1).

Parameter	M0R/L	M1	M2/3	M4/5	M6/7	M8	MRef
Width [μm]	1.4	2.8	1.7	2.3	0.9	2.0	0.8
Length [μm]	0.03	0.03	0.1	0.1	0.15	0.5	0.5
Multipliers	1	1	1	2	1	4	1

Table 4.6. Transistor dimensions of the error amplifier (Part 2).

Parameter	MRz	M21	M22	M23	MPD1	MPD2
Width [μm]	1.7	2.0	1.3	0.5	1.0	0.5
Length [μm]	0.03	0.5	0.03	0.1	0.03	0.1
Multipliers	1	1	1	1	10	5

Table **4.7** highlights the capacitors dimensions used for the error amplifier in the CMFB, MOM capacitors were chosen as well for their availability in the technology.

Table 4.7. Capacitor dimensions of the OTA.

Parameter	C17/C18
Finger width [μm]	0.06
Finger length [μm]	3
Finger space [μm]	0.06
Fingers	6

4.2. Performance Simulations

In relation to Section **3.8**, several simulations are carried out using the characteristics described therein. Fig. **4.3** presents the frequency response at three key points: the output of the communication channel, the output of the CTLE, and the standalone response of the CTLE.

The PVT and Monte Carlo simulations are presented in order to evaluate robustness, performance compliance, and variability impact on the design.

In Fig. **4.1** and **4.2**, we can observe how variations in R_S and C_S affect the CTLE transfer function. Specifically, changes in C_S shift the peaking frequency, while modifications in R_S alter the DC gain level of the equalizer, thereby shaping its frequency response.

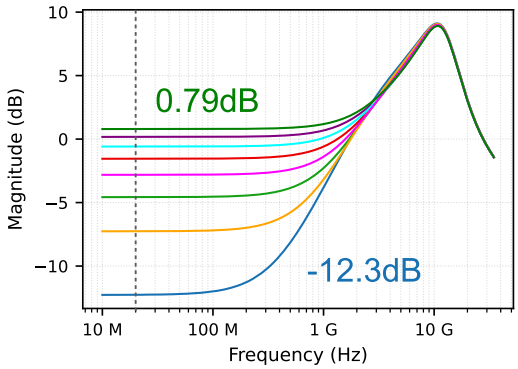


Figure 4.1. CTLE Frequency response on R_s variations.

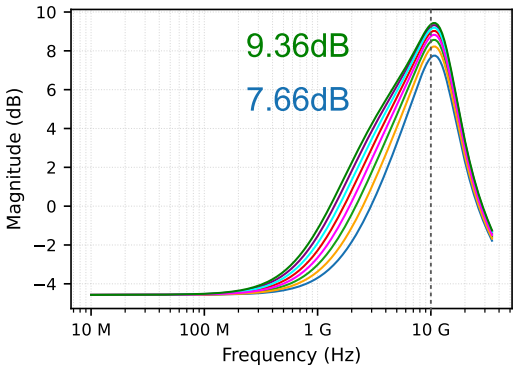


Figure 4.2. CTLE Frequency response on C_s variations.

Once equalization is applied, as shown in Fig. **4.3**, it can be observed that the channel loss is reduced to a total of $-13.85\,\mathrm{dB}$ at the Nyquist frequency, compared to the original $-22.92\,\mathrm{dB}$.

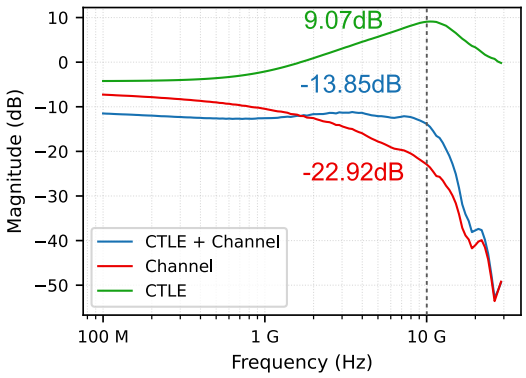


Figure 4.3. Frequency response of all system stages.

Furthermore, the eye diagram shown in Fig. **4.4** and **4.5** illustrates the evolution from

a degraded signal condition to a significantly improved open-eye diagram after equalization. Initially, as seen in Fig. **4.4**, the signal suffers from severe intersymbol interference, resulting in both horizontal and vertical eye closure, which compromises timing accuracy and amplitude margin, It is important to note that, for the generation of these eye diagrams, a total of 100,000 sample was used in order to cover as many cases as possible.

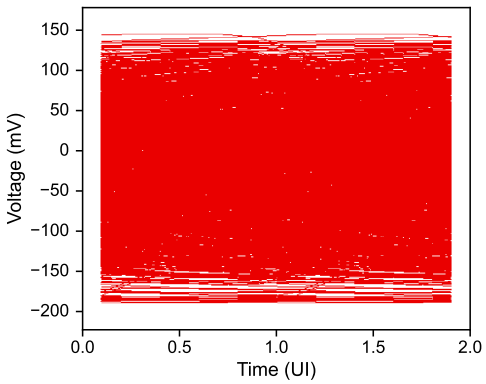


Figure 4.4. Eye Diagram before equalization.

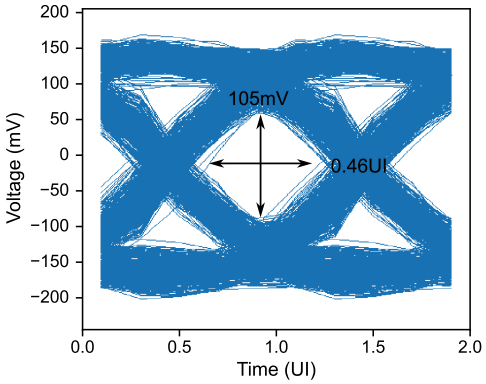


Figure 4.5. Eye Diagram after equalization.

After applying the CTLE, Fig. **4.5** reveals a substantial enhancement in the eye opening. As can be seen, the main characteristics of the eye—its width and height—can be clearly extracted from the graph.

4.3. Process-Voltage-Temperature (PVT) Corner Simulations

Table **4.9** summarizes the worst-case, best-case and typical PVT corners taken from Table **4.8** and validates that the circuit consistently satisfies the design criteria.
Table **4.9** then shows the conditions under which the system was evaluated. It includes different simulation corners: the SS **(Slow-Slow)** corner represents a slow process variation where carrier mobility is reduced, which can negatively affect the performance of high-speed circuits. Conversely, the FF **(Fast-Fast)** corner corresponds to the fastest scenario, with increased mobility, while TT represents the typical process

corner. These corners are defined based on the simulations performed on the system.

Table 4.8. Corner Conditions: Temperature, Supply Voltage, and Process Variations.

Parameter	Worst	Best	Typical
Temperature [℃]	-40	125	25
VDD [V]	0.81	0.81	0.9
Process (MOS)	SS	SS	TT
Capacitor (MOMCAP)	FF	SS	TT
Resistor (DISRES)	FF	FF	TT

Table 4.9. Corners compliance table with Design Criteria.

Parameter	Worst	Best	Typical	Criterion	
Width [ps]	20.33	22.27	20.96	$\geq$ 20p	✓ Met
Height [mV]	71.745	48.094	105.605	$\geq$ 20m	✓ Met

In this context, corner 1 corresponds to the worst-case scenario (SS), corner 2 to the best-case (FF), and corner 3 to the typical case (TT).

As shown in Table **4.9**, the design maintained consistent performance across the three worst-case corners, successfully meeting the criteria defined by both PVT and Monte Carlo analyses. In each corner, a margin with respect to the specification was achieved. This consistency was made possible through the use of the R_s and C_s banks, which enable tuning of the CTLE, as illustrated in Fig. **3.2** and **3.3**. From the results obtained, the typical corner stands out as it shows no significant alteration in the system's performance. However, once PVT variations are applied, *corner 2* achieves the best horizontal eye opening. This specification is particularly important, as vertical eye opening can be addressed in subsequent stages. Therefore, based on this criterion, *corner 2* is considered the most favorable among the process variations. Nevertheless, the performance under *corner 1* does not show a significant degradation, indicating good

consistency and robustness of the design under variations. Additionally, the CMFB circuit played a vital role in maintaining proper transistor biasing, ensuring the optimal operating conditions of the circuit.

The maximum power consumption observed across the simulated corners was 4.421 mW, which meets the system's power specification, defined as a maximum of 4.5 mW. This limit was set to ensure proper system operation. It is important to note that this power value corresponds to the total consumption from VDD, and therefore includes all devices within the system.

4.4. Monte Carlo Offset Variation

In addition to PVT analysis, Monte Carlo simulations were carried out to check variations in offset voltage at the output of the CTLE.
An offset analysis was performed over 1000 simulations. A variation lower than 25 mV was observed, which is particularly beneficial as it allows subsequent stages to be properly biased. Mainly, this deviation was significantly reduced due to the implementation of the CMFB circuit, which enforces a fixed common-mode (DC) voltage at the output, thus stabilizing the output level. Fig. **4.7** shows the histogram of the simulated offset distribution.
The Monte Carlo simulation plays a critical role, as it becomes essential to verify whether the conditions required for the proper operation of subsequent system blocks are met.
In comparison with Fig. **4.6**, it can be observed that the inclusion of the CMFB block significantly improves the output offset. Without it, the variation reaches approximately 30mV, which could critically affect the biasing of the following stage. Thus, the CMFB effectively addresses this issue by reducing the offset variation.

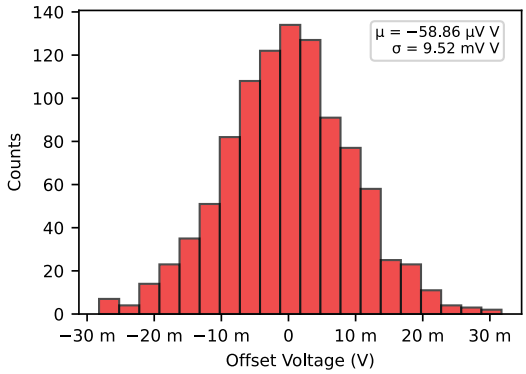


Figure 4.6. Without CMFB

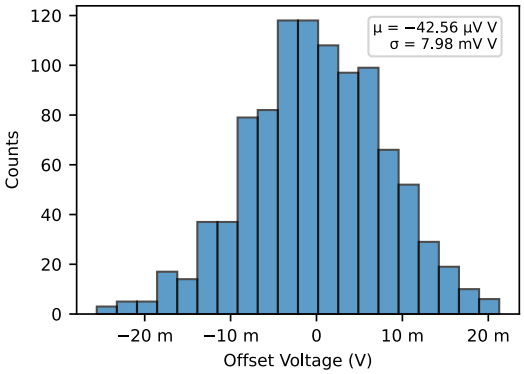


Figure 4.7. With CMFB

4.5. Comparision

Table 4.10. Performance comparison between design target and proposed work.

Parameter	**Design target**			**Our work**			**Judgment**
	Min	Typ	Max	Min	Typ	Max	
Bit Rate [Gbps]	-	20	-	-	20	-	✓
EH [mV]	20	-	-	48.064	105.608	105.608	✓
EW [UI]	0.4	-	-	0.4066	0.4192	0.4454	✓
VDD [V]	0.81	0.9	0.99	0.81	0.9	0.99	✓
BER	-	-	1×10^{-12}	-	-	1×10^{-12}	✓

As shown in Table **4.10**, the results demonstrate that the proposed work meets the design targets across all evaluated parameters, including bit rate, eye height, eye width, supply voltage, and BER.

Table 4.11. Comparison with state-of-the-art equalizer designs.

Parameter	**This Work**	[18]	[19]	[20]	[21]
Technology	28nm	28nm	65nm	28nm	55nm
Equalizer	CTLE	CTLE+DFE	CTLE	CTLE	DFE
Data Rate (Gb/s)	20	18	15	20	10.4
Loss [dB]	23	15	21	30	8.3
V-Eye [mV]	105.6	–	150	43.5	–
H-Eye [UI]	0.454	–	0.73	0.611	–
Power [mW]	4.42	2.44	5.40	7.57	1.71
FOM (fJ/bit/dB)	9.65	9.03	17.0	12.6	19.0
BER	1×10^{-12}	1×10^{-12}	1×10^{-12}	1×10^{-12}	1×10^{-12}

Considering all the results, Table **4.11** presents a comparison with state-of-the-art works. The table includes the type of equalization, data rate, channel loss, eye diagram openings, power consumption, and the FOM. The FOM is defined as the power divided by the data rate, and then divided again by the channel loss at the Nyquist frequency.

From Table **4.11**, it can be observed that the proposed design achieves a good FOM, which can be attributed to its low power consumption despite significant channel loss. It is worth noting that the system does not yet include the subsequent processing stages, so characteristics such as the eye openings are expected to improve under those conditions.

5. CONCLUSIONS AND FUTURE WORK

5.1. Conclusions

This work describes the design of a 20 Gbps CTLE on a TSMC 28 nm CMOS technology node. The project began with a thorough evaluation of application requirements, intending to develop an equalizer for an Analog Front End (AFE), requiring enough equalization to ensure the proper working of the AFE, this equalization was based on compensating for the losses caused by the channel, understood as the physical medium through which the data travels, using in this case the CTLE.

Each individual block of the CTLE underwent a design process to meet specific performance criteria. The CTLE was built to achieve a minimum of 20mV on height of the eye diagram and 0.4 UI on the width. The CTLE itself was complemented by a novel technique that expands the bandwidth with a greater ratio of peaking magnitude order more than 2dB at the nyquist frequency defined. to mantainn this condition an resistor and capacitor bank was implemented in the main CTLE circuit to reduce PVT variations. In addition, the Common mode level of the CTLE was set by a CMFB which was designed to have enough gain and phase margin to keep the loop gain significant and have an error less than 5%.

After the CTLE design was completed, individual schematic-level tests were conducted to evaluate the integrity of the circuit. These tests confirmed that the design met the established conditions, both under PVT variations and Monte Carlo analysis.

Thus, based on the mentioned conditions, it can be concluded that the proposed design objectives have been met, as all the specified requirements have been satisfied.

5.2. Future Work

- The implementation of the full Analog Front-End (AFE), which includes not only the first CTLE stage presented in this work, but also a secondary CTLE, a variable gain amplifier (VGA).

- The development of a full-custom layout of the proposed circuit. This includes accurate transistor placement, routing strategies to minimize parasitics, post-layout simulations are necessary to validate the actual performance of the circuit in silicon-like conditions as well.

- Layout Recommendations for the CTLE: Since the design involves differential signals, symmetry is a critical aspect of the layout. Any asymmetry can degrade the signal quality and introduce unwanted offset. Therefore, careful mirroring and matching of the differential paths is essential to ensure proper circuit behavior.

  For matching critical elements, such as the input transistor pair (M1 and M2) show in Fig. **3.6**, simple interdigitated topologies are sufficient. Using more complex arrangements, like common-centroid structures, increases the number of required interconnections, which in turn raises the risk of parasitic impedance coupling and degrades the overall performance of the block.

  It is also important to consider the high current levels handled by the CTLE core, typically around 1.6 mA. To support this, these current-carrying paths should be routed using upper metal layers, which provide lower resistance and help maintain signal integrity by minimizing voltage drops and local heating

BIBLIOGRAPHY

AGHIGHI. “A Low-Power 10 to 15 Gb/s Common-Gate CTLE Based on Optimized Active Inductors”. In: *2020 IFIP/IEEE 28th International Conference on Very Large Scale Integration (VLSI-SOC)*. IEEE, Oct. 2020, pp. 171–175. DOI: 10.1109/vlsi-soc46417.2020.9344076 (cit. on p. 56).

AGILENT. *Using Clock Jitter Analysis to Reduce BER in Serial Data Applications*. Application Note 5989-5718EN, December 1. Agilent Technologies. 2006 (cit. on pp. 21, 22).

APPDX. *APPENDIX A*. 2025 (cit. on p. 23).

— *APPENDIX B*. 2025 (cit. on p. 30).

— *APPENDIX C*. 2025 (cit. on p. 30).

— *APPENDIX D*. 2025 (cit. on p. 37).

CHOI, Jonghyuck et al. “A single-ended nrz receiver with gain-enhanced active-inductive ctle and reference-selection dfe for memory interfaces”. In: *IEEE Journal of Solid-State Circuits* 59.4 (2024), pp. 1261–1270 (cit. on pp. 26, 35, 36, 56).

DELGADO, Cristhian Rolando Torres. “Front-end Circuit Techniques for High-Speed Interfaces”. Master’s thesis. Universidad Industrial de Santander, 2019 (cit. on pp. 25, 26, 33).

GAGGATUR. “A power efficient active inductor-based receiver front end for 20Gb/s high speed serial link”. In: *AEU - International Journal of Electronics and Communications* 111 (Nov. 2019), p. 152886. DOI: 10.1016/j.aeue.2019.152886 (cit. on p. 56).

GONZÁLEZ, David Alejandro Reyes. “Diseño de un ecualizador lieal de tiempo continuo (CTLE) para interfaces de alta velocidad integrado en tecnología CMOS”. Bachelor’s thesis. Universidad Industrial de Santander, 2017 (cit. on p. 32).

GRAY, Paul R. et al. *Analysis and Design of Analog Integrated Circuits*. 5th ed. Wiley, 2021 (cit. on pp. 27, 29).

HAN, Kyung Suk (Ken). *High-Speed Signaling: Jitter Modeling, Analysis, and Budgeting*. Prentice Hall, 2013 (cit. on pp. 16, 18, 21).

MENIN, Davide. “Modelling and Design of High-Speed Wireline Transceivers with Fully-Adaptive Equalization”. Doctor’s thesis. Università degli Studi di Udine, 2021 (cit. on pp. 16, 18–20, 22).

PALERMO, Sam. *ECEN720: High-Speed Links Circuits and Systems*. Lecture slides, Lecture 8: RX FIR, CTLE, DFE, & Adaptive Eq. Spring 2025. 2025 (cit. on pp. 13, 24).

RAZAVI, Behzad. *Design of Analog CMOS Integrated Circuits*. 2nd. McGraw-Hill Education, 2017 (cit. on p. 34).

— “Design techniques for CMOS wireline NRZ receivers up to 56 Gb/s”. In: *IEEE Open Journal of the Solid-State Circuits Society* 3 (2023), pp. 118–133 (cit. on p. 26).

— “The cross-coupled pair-part i [a circuit for all seasons]”. In: *IEEE Solid-State Circuits Magazine* 6.3 (2014), pp. 7–10 (cit. on p. 37).

USB IMPLEMENTERS FORUM. *USB4™ Specification Version 2.0 with Errata and ECN REDLINE*. `https://www.usb.org/document-library/usb4r-specification-v20`. 2024 (cit. on p. 46).

YI, I.-M. “A Time-Based Receiver With 2-Tap Decision Feedback Equalizer for Single-Ended Mobile DRAM Interface”. In: *IEEE Journal of Solid-State Circuits* 53.1 (Jan. 2018), pp. 144–154. DOI: 10.1109/JSSC.2017.2765818 (cit. on p. 56).

ZHANG, Hongyang. “CMOS Continuous-Time Linear Equalizers for High-Speed Serial Links”. PhD thesis. University of Pavia, 2017 (cit. on pp. 13, 17, 19).

ZIEMER, Rodger E. *Principles of Communications*. Wiley, 2015 (cit. on pp. 17, 18, 20).