IMPEDANCE MATCHING CIRCUIT FOR HIGH SPEED APPLICATIONS.

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Trabajo de grado presentado como requisito para optar al título de

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DEDICATORIA

A mis padres Hernando Dovale y María Irene Vargas, quienes son mi mayor motivación para ser cada día una mejor persona, por todo sus esfuerzos y apoyo.

Lizeth mi hermana de alma, mi compañera incondicional, mi mayor consejera.

Juan mi hermano y mejor amigo, mi apoyo, mi fuerza.

Rodolfo mi compañero de largas noches.

Felipe por todo el apoyo brindado durante estos años, por compartir a mi lado este camino y por enseñarme a creer como persona.

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RESUMEN

TÍTULO: Circuito de adaptación de impedancias para aplicaciones de alta velocidad. *

AUTOR: Luisa Fernanda Dovale Vargas **

PALABRAS CLAVE: código binario, evento ESD, protección ESD, red de adaptación de impedancias, código termómetro.

DESCRIPCIÓN:

Este trabajo presenta la metodología de diseño de una red de adaptación resistiva variable de forma integrada utilizando la tecnología estándar CMOS tsmc 180nm, para lograr la máxima transferencia de potencia en aplicaciones USB 3.0. Las descargas electrostáticas (ESD) se consideran durante el diseño de la red de adaptación para garantizar la seguridad del óxido de los transistores. Además, se consideran las altas densidades de corriente y los altos voltajes producidos por diferentes modelos de ESD, como el modelo de máquina (MM) y el modelo de cuerpo humano (HBM) para el dimensionamiento de los elementos, a fin de asegurar su integridad física. La topología presentada en este trabajo está compuesta por una resistencia en serie con un transistor NMOS en función switch para variar el valor equivalente de la red de resistencia. Se propone la inclusión de un divisor de tensión de bajo consumo compuesto por transistores PMOS, para evitar superar la tensión de ruptura en los terminales puerta-surtidor de los transistores NMOS durante una descarga electrostática.

La red de adaptación tiene un rango de operación de 65Ω a 35Ω distribuidos en 30 ramas de resistencia diferentes en paralelo. La acción de control de la red de adaptación se logra mediante la implementación de códigos termómetro y binario. Se implementa un bloque de calibración para mitigar las variaciones debidas a las variaciones de Proceso-Voltaje-Temperatura (PVT), garantizando siempre el correcto rango de operación para diferentes condiciones extremas. Se obtiene un consumo de corriente estático máximo de aproximadamente 8mA para los resultados de simulaciones de esquina (corners).

*Trabajo de investigación

** Facultad de Ingenierías Fisicomecánicas. Escuela de Ingeniería Eléctrica, Electrónica y de Telecomunicaciones. Director: Juan Sebastián Moya Baquero, MEng. Ingeniera, Codirector: Elkim Felipe Roa , Philosophy Doctor

ABSTRACT

TITLE: Impedance matching circuit for high speed applications. *

AUTHOR: Luisa Fernanda Dovale Vargas **

KEYWORDS: binary code, ESD event, ESD protection, impedance matching network, thermometer code.

DESCRIPTION:

This work presents the design methodology of an integrated variable resistance adaptation network using a standard CMOS tsmc 180nm technology, for achieving maximum power transfer in USB 3.0 applications. Electrostatic discharges (ESD) are considered during the design of the adaptation network for guarantying transistor oxide safety value. Additionally, high current densities and high voltages produced by different ESD models such as the machine model (MM) and the human body model (HBM) are considered for elements dimensioning, in order to assure its physical integrity.

The topology presented in this work is composed by a resistance in series with an NMOS switching transistor for varying the equivalent resistance network value. A proposed low power consumption voltage divider paths composed by PMOS transistors are included, for avoiding overtaking NMOS transistor breakdown voltages branches during an electrostatic discharge.

The adaptation network has an operating range from 65Ω to 35Ω distributed in 30 different resistance branches in parallel. The control action of the adaptation network is achieved by implementing both thermometer and binary codes. A calibration block is implemented for mitigating Process-Voltage-Temperature (PVT) variations, to ensuring always correct operation range in different extreme conditions. An 8mA maximum static current consumption is achieved for corner simulations results.

*Bachelor Thesis

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INTRODUCTION

Consumer demand pushed by media-data usage has led an increment of high-speed interface development. For instance, from 1996 to 2016, USB standard increase speed specification from 1.5Mb/s to 10Gb/s [3].

In the case of integrated circuits, device interfaces might be modeled as transmission lines as operating frequency increases considering signal integrity [7]. In order to keep power losses at minimum and preserve data integrity, impedance matching is required. It is common practice to build a circuit that adjusts the termination impedance at the receiver/transmitter side ensuring maximum power transfer.

In addition, integrated protection circuits at the device may impact speed of data transmission. Load added by parasitic capacitances of the protection circuits are substantial considering that large dimensions are necessary to deflect large current densities during electrostatic events. Although the complex part due to capacitance loading of the impedance might be compensated by a T-coil circuit [7], this work develops just the real part matching considering that pads with their respective inductances are proportioned.

One of the main challenges of this design is the lack of information present in the literature concerning methodologies for constructing an impedance matching network. T-coil structure design is well-documented for canceling the channel imaginary part of the receiver/transmitter, specially for high-speed applications [4], [6]. Another device correctly described in the literature is voltage-mode transmitter [11] that is in charge of equalizing the channel and also matching the impedances. However, this device is composed only by transistors and is directly connected to the pad, increasing transistor oxide rupture probabilities when an ESD event occurs. Finally, a 50Ω impedance matching network is apparently assumed to be easily constructed, however as it is presented in this document, important considerations must be taken into account for achieving a correct implementation.

This work presents the study and design of a variable impedance network for maximum power transfer in USB 3.0 applications. Considerations about ESD events on pads, transistor breakdown voltage and technology current density are developed in order to obtain a more robust integrated impedance network.

This work is divided into the following sections: Chapter 1 shows an study of ESD electrostatic models. Chapter 2 explains the design features for the impedance matching network and Chapter 3 presents corners and Monte Carlo Post-layout results. Finally Chapter 4 concludes this work and describes considerations for future works.

static electricity is an accumulation of electrical charge by an imbalance of electrons on the surface of a material. When two objects with different electrical potentials are in contact, a charge transfer occurs between them. This phenomenon is called electrostatic discharge and is one of the most important reasons of integrated circuit failures in industry [2].

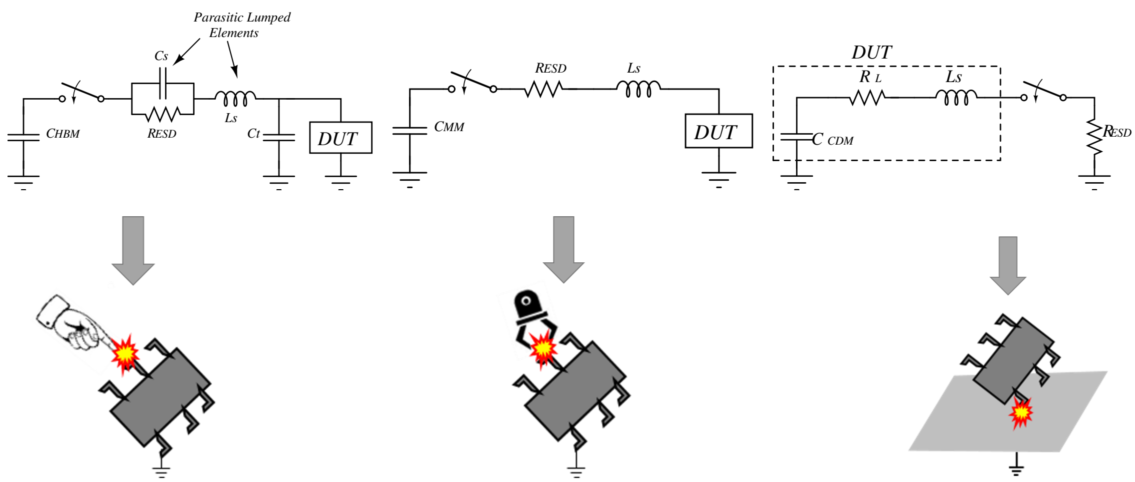
The models that describe ESD discharge standards are composed of passive elements (resistors, capacitors and inductances), with different transient responses. This section presents the most common models of electrostatic discharges: human body model (HBM), machine model (MM) and charge device model (CDM) [5] [10]. Each of these models can be described as an RLC network.

Table 1: Passive component values for ESD models.[5]

Parameter	HBM	MM	CDM
V_{ESD} [V]	4000	200	500
R_{ESD} $[\Omega]$	1.5K	5	10
C_{ESD} [pF]	100	200	10
L_S [nH]	5000	750	10
R_L		10	
I_{ESD_max} [A]	2.6	2.8	10.4
T_{rise} [ns]	≈ 7	≈ 11	$\approx 0{,}3$

In Table. 1 R_L is the load resistance, R_{ESD} is the resistance of the model, C_{ESD} is the capacitor initially charged with a voltage V_{ESD} and the series inductance L_s associated to the integrated circuit bonding wire of the discharge path. T_{rise} and I_{ESD_max} define rise time and peak current values respectively, for each of the models.

Figure 1: ESD Circuits Models [1], [10].



(a) HBM model. (b) MM model. (c) CDM model.

1.1 HBM MODEL

Under different conditions the human body can be charged electrostatically by interacting with the environment. It can produce large accumulations of charges that are transferred to the IC when hand contact occurs [8]. The human body is represented by the equivalent circuit in Fig. 1.2(a), the values for each of its elements are specified in Table 1 according to the standard and C_t is the parasitic capacitance of the test board. In green, the HBM current is presented in Fig 2 with a 2.6A maximum peak value.

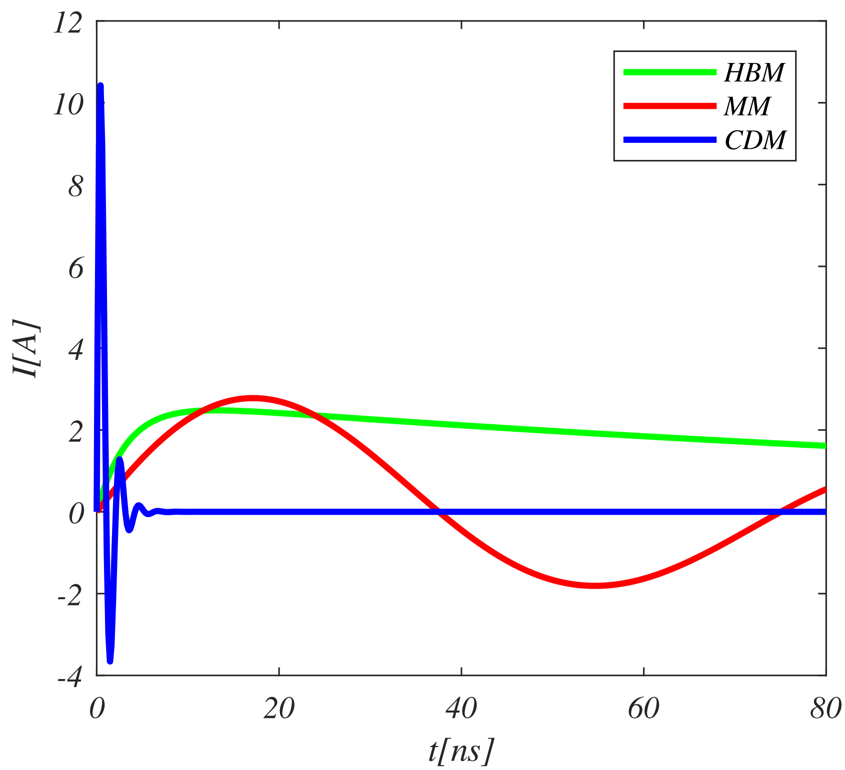
1.2 MM MODEL

This model attempts to represent the damage caused by a manufacturing equipment during IC assembly. As shown in Table 1, this model has the highest capacitance value and lower inductance discharge path, both in comparison to the HBM model parameters, hence, resulting in higher current densities and causing damage similar to that produced by the HBM discharge. The equivalent circuit is shown in Fig. 1.2(b) and its current waveform is observed in red as illustrated by Fig. 2. This current has approximately a 2.8A peak value, caused by the 200V initial condition and has the longest time duration of the three ESD models, hence turning out to be the most harmful of the ESD discharges.

1.3 CDM MODEL

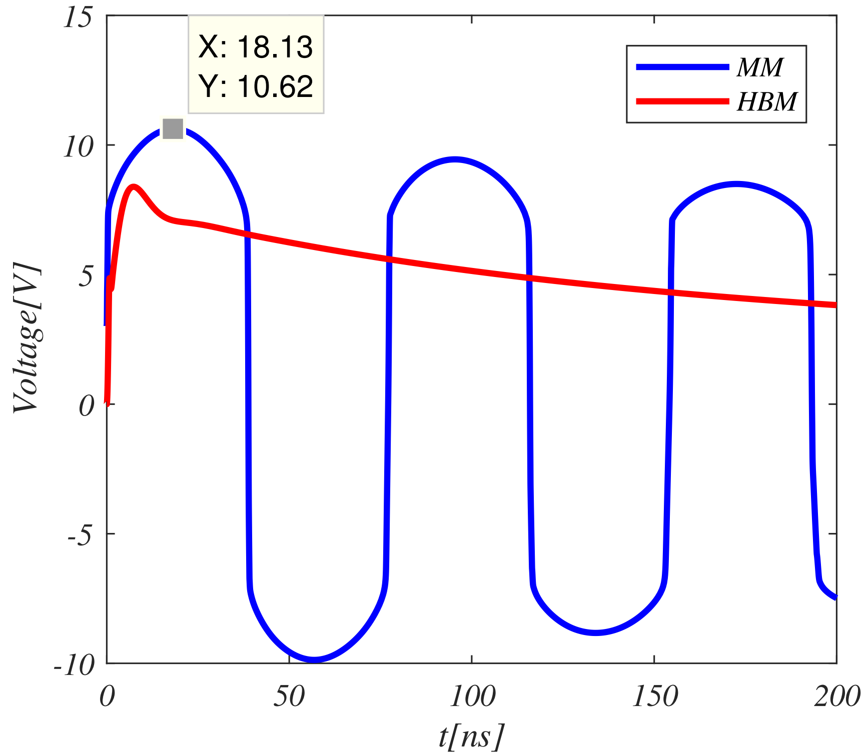
When an integrated circuit accumulates electrical charge during manufacturing processes, once the process has finished, it is possible that a discharge path occurs when a package pin has contact with a grounded object. This discharge action is represented by the CDM model illustrated in Fig. 1.2(c). This model waveform is presented in blue in Fig. 2 and is considered the most aggressive model for the IC because it generates the highest current peak value in a short time interval, therefore, forcing the protection circuit to respond faster.

Figure 2: ESD model discharge waveforms. [8]



The ESD protection circuit was tested for both MM and HBM models, because the technology power clamp used, has a response time constant much higher than the rise time of the CDM model. The resulting voltage in the I/O pad during an electrostatic event is shown in Fig. 3 and presents a simulated maximum voltage peak of 10.62V for the MM discharge model.

Figure 3: Residual voltage produced by the ESD protection circuit for MM and HBM events.



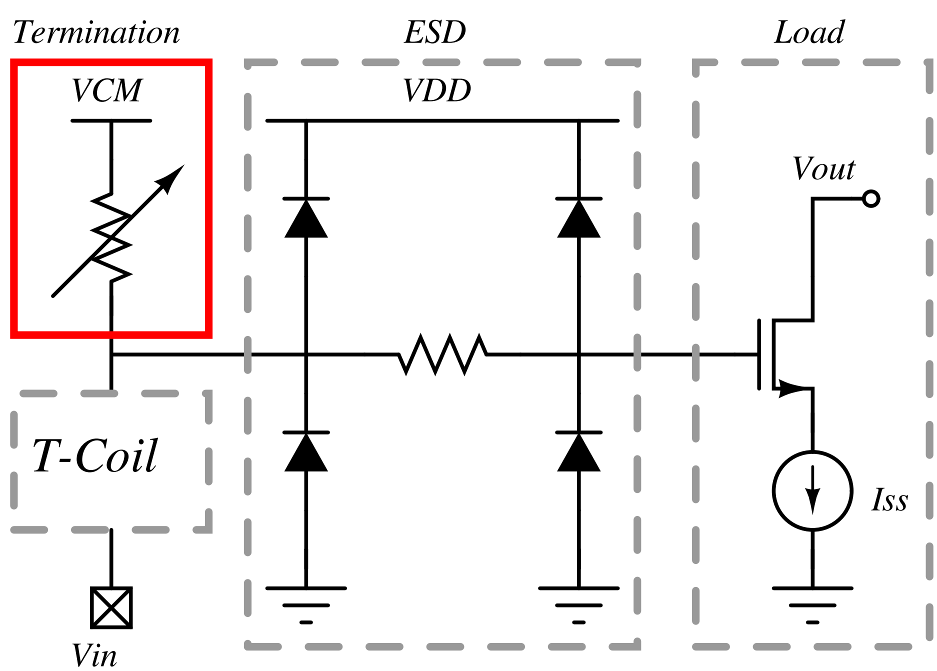
This voltage is crucial for designing the termination network due to transistor oxide rupture and is considered in the next chapter.

2. IMPEDANCE ADAPTATION NETWORK DESIGN

This chapter describes the design of an impedance matching network with an adjustable value between 35Ω and 65Ω. The network has the ability to change its value by using binary and thermometer codes.

The termination circuit is connected between the T-coil and the common mode voltage (V_{CM}) associated to the polarization voltage level of the load, along with the ESD protection circuit [4], as illustrated in Fig. 4.

Figure 4: ESD protection circuit with termination circuit for single-ended input, adapted to [4].



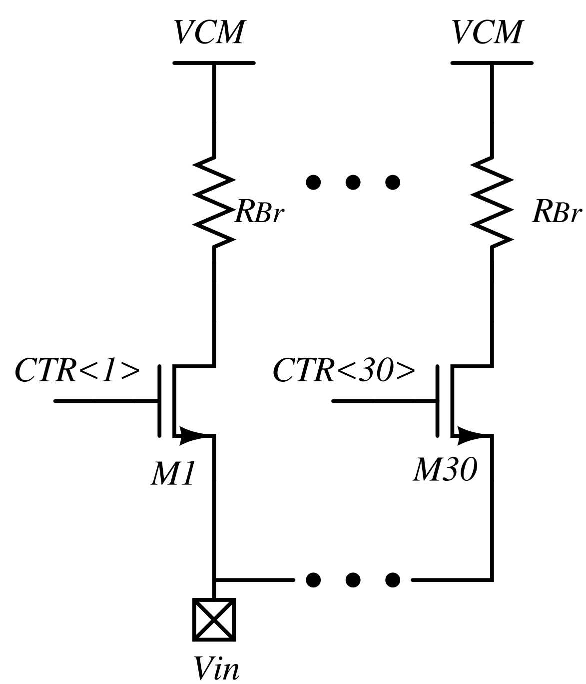
The average power transfered to the load is maximized when both the input impedance of the receiver and the equivalent impedance observed from the receiver to the transmitter (channel and transmitter) are complex conjugated with each other. Equation 1 represents the maximum power transfered, where $Z_L = R_L$ is the real part of the receiver impedance and $Z_g = R_g$ is the equivalent real part of the channel and the transmitter impedance. The maximum power transfered is where $R_L = R_g = R_{th}$ and $V_{g\_max} = \frac{V_{th}}{2}$

$$P_{max} = \frac{V_{th}^2}{4R_{th}} \tag{1}$$

2.1 ADAPTATION NETWORK TOPOLOGY

The proposed topology is presented in Fig. 5 and is composed by an array of parallel branches, each of these, formed by a resistance ($R_{Br}(n)$) in series with an NMOS working as a switch controlled by external signals $(CTR < 1..,30 >)$. The control signals are responsible for turning the branches on and off according to the variable impedance of the channel and the transmitter. For this design R_{Br}, is composed only by parallel resistances for area minimization at the expense of precision lost. For better precision, a combination of series and parallel resistances must be used.

Figure 5: Termination circuit connection scheme.



For changing the resistance value of the termination, the binary code gives the freedom to choose the value of the network (58Ω and 42Ω) without passing through the intermediate values. Whereas, the thermometer code let the user achieve 1Ω resolution in the 35Ω-65Ω range.

The value of each branch resistance can be found by using equation 2; where R_{Br} is the value to be found, $R_{des}(n-1)$ is the previous equivalent value and R_{des}(n) is the value to be reached. For example if the equivalent actual value of the resistance is 65Ω ($R_{des}(n)$) and the desired value is 64Ω ($R_{des}(n+1)$), by applying equation 2, a 4160Ω value is expected for R_{Br}(n).

$$R_{Br}(n) = \frac{R_{des}(n)\ \ R_{des}(n+1)}{R_{des}(n) - R_{des}(n+1)} \tag{2}$$

This equation is only valid for the exact equivalent R_{Br} value, however as only parallel resistances are used, the real R_{Br} value is an approximation.

Each of these values are distributed in thirty different branches and divided into four blocks, that are organized as follows:

- **Block 1:** Modifies the resistance by using thermometer code from 59Ω to 65Ω.
- **Block 2:** Modifies the resistance by employing binary code from 58Ω to 65Ω and thermometer code from 58Ω to 50Ω.
- **Block 3:** It only works correctly if block 2 is on. Modifies the resistance by adopting thermometer code from 50Ω to 43Ω.
- **Block 4:** It only works correctly if block 2 is on. Modifies the resistance by applying thermometer code from 42Ω to 35Ω and binary code from 50Ω to 43Ω.

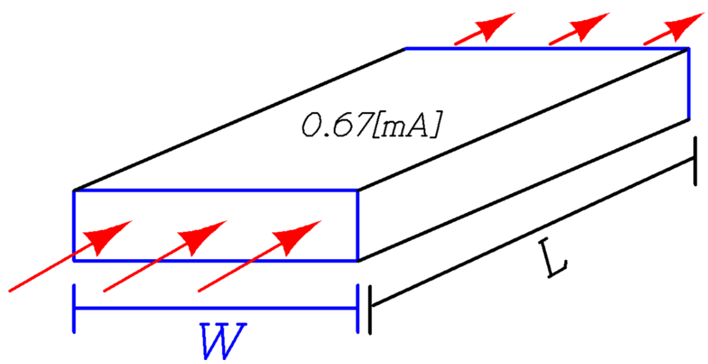
The initial value of the network is 65Ω and the different values of the specified network range are obtained by including or removing resistances in parallel. Regarding the corresponding layout, a unitary resistance for all R_{Br} network values is chosen by considering both area minimization and current density.

Additionally, two important aspects must be addressed in order to have a robust network design: element current density and transistor breakdown voltage.

2.2 CURRENT DENSITY

Each of the elements of the matching network must support high current densities caused by the magnitude of ESD residual voltage as presented in Fig. 3. The selection of the unitary resistance is based on finding the value of the resistance with a specific density current and the residual voltage at the input of the pad. Both dimensions and resistance linearity are determined from the information provided by the foundry. The current density crosses the material by the width (W) as Fig. 6. The minimum current density for technology used (180nm) is 0.67mA.

Figure 6: Resistance Cross-section



Thinking in terms of area minimization, it is desirable to use the minimum dimensions, hence, using the smallest width (W) is expected (1μm). However using the minimum dimensions is not recommended due to variability during fabrication process and foundry characterization document, therefore a W of 1.5μm is selected for avoiding unexpected effects. For this value, the current density is approximately 1.05mA and by using the maximum residual voltage (10.62V) obtained, the unitary resistance value is approximately 10kΩ.

In order to obtain the 65Ω resistance value with the previously unitary resistance, approximately 153 resistances in parallel must be connected, hence impacting considerably the area. An study of area reduction is realized by increasing the W dimension of the resistance in order to decrease its value. By selecting 19μm for the transistor width, a unitary resistance of 806Ω is obtained. With these new values the layout area reduction is 45.77 $\%$ compared to the layout using the $1{,}5\mu m$ resistance width (0.21mm^2). Regarding the NMOS in series with the 65Ω resistance, its R_{on} resistance must be very small in comparison with the branch resistance in order to avoid impacting the expected value. Consequently, the NMOS dimensions must be very big in order to withstand high current values, causing area penalization. Based on this, the 65Ω resistance is fixed, i.e. directly connected to the network terminals, sacrificing static current consumption. Therefore, the 65Ω branch has a unitary resistance different from the rest of the blocks ($1{,}5\mu$m) due to the current magnitude passing through it.

2.3 BREAKDOWN VOLTAGE

When an electrostatic discharge event occurs at the I/O pad and the resistance branch is inactive, i.e. the control signal value is 0V, a voltage higher (10.62V, Fig. 3) than the technology breakdown voltage (less than 9V) is fixed between NMOS switching transistor source and gate terminals, causing oxide rupture. Based on the above, the structure presented in Fig. 5 must be modified to ensure switching component protection.

The termination protection proposal is presented in Fig. 7 in order to decrease the residual voltage set by the ESD discharge. In this figure, the NMOS transistor interchanges its position with the resistance and a PMOS transistor is connected for decreasing the NMOS gate-source voltage. This circuit works as follows, two possible discharge paths depending on the control signal value can occur.

Case 1: If Control Signal value is 0V, the NMOS transistor is off and all the current flows through the PMOS transistor. For protecting and decreasing the NMOS source voltage, the PMOS on resistance value R_{onM1} must be small compared to the resistance branch for voltage division as presents equation 3.

$$V_{GS_{M0}} = V_{in} \ \frac{R_{onM1}}{R_{Br} + R_{onM1}} \tag{3}$$

It is important to say that there exists a trade off between power consumption and PMOS transistor dimensions, so R_{onM1} cannot have very small dimensions.

Case 2: If Control Signal value is 3.3V (case 2), the PMOS transistor is open and all the current flows through the NMOS transistor and its V_{GS} voltage is defined by equation 4.

$$V_{GS_{M0}} = V_{ControlSignal} - \frac{V_{in} * R_{onMo} + V_{CM} * R_{Br}}{R_{Br} + R_{onM0}} \quad (4)$$

The problem of this proposal is the static power consumption of the PMOS transistor when the control signal is low, therefore the current of this transistor must be negligible respect to the termination power consumption.

2.4 CALIBRATION BLOCK

A calibration block is included for mitigating process-voltage-temperature (PVT) variations. T1, T11, T1158 and T1142 represent the control signals of the nominal case, the adjustment of 65Ω, 58Ω and 42Ω values respectively in the case of the upper corner. The initial variations are presented in Table 5.

Table 2: Variation for initial 65Ω value for PVT variations.

Spec	Upper Corner unadjusted	Downer Corner unadjusted
65Ω	73.015Ω	57.922Ω

Finally, the termination schematic with all the blocks and its corresponding control signals, is presented in Fig. 8, CTR $< 30 : 1 >$ are the control signals for the blocks. The control signals are activated or deactivated digitally by a state machine, that must be implemented in a future work.

Figure 8: Termination block schematic.

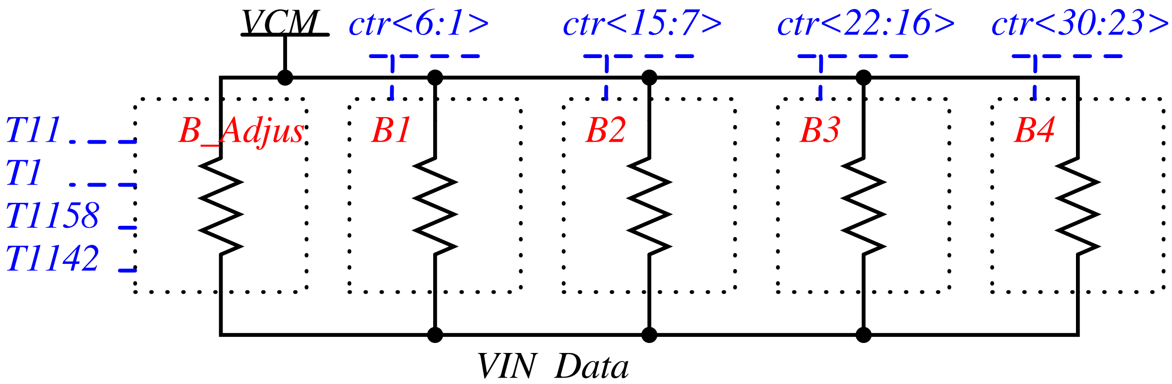
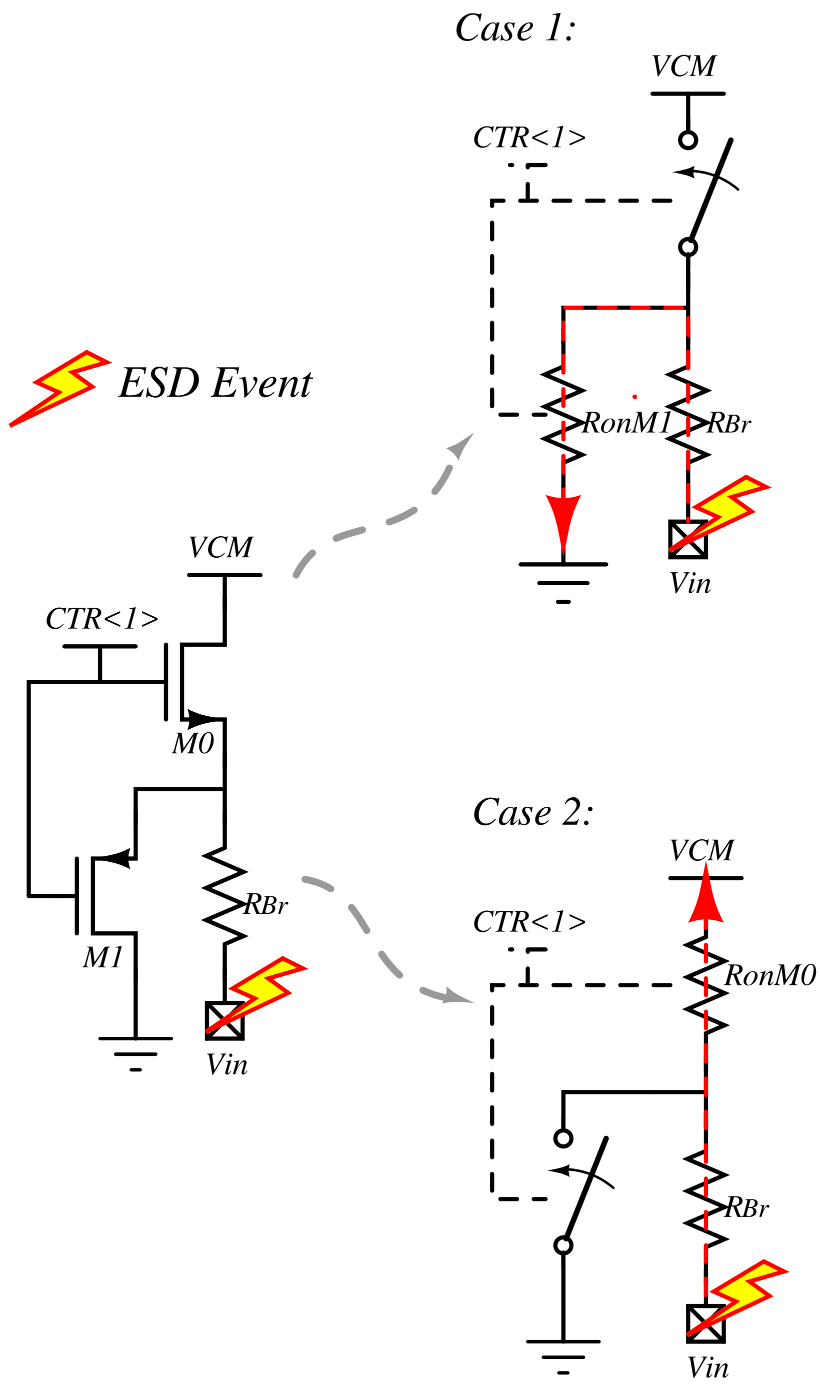


Figure 7: Proposal topology with additional discharge path for lowering residual voltage.



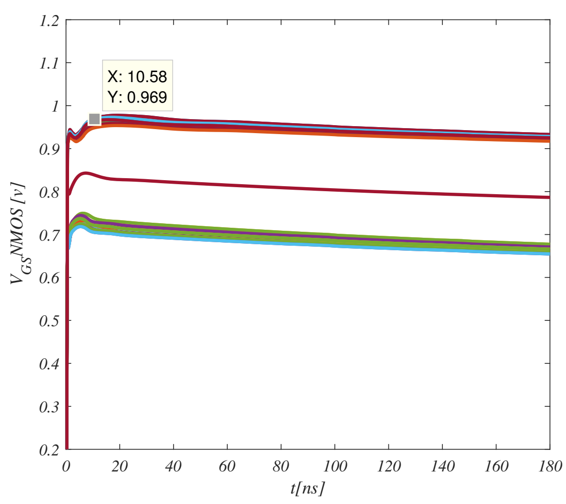
3. RESULTS

Firstly, this chapter presents the methodology to obtain the resistance measurement due to its time variable value. Secondly, the voltages of the proposed protection circuit are verified in order to guarantee safety voltage values for HBM model. Finally, the Post-layout results for PVT variations and Monte Carlo (MC) simulations are illustrated with the calibration block. The measurement of the resistance is determined by using the dynamic resistance technique that is commonly used in switched capacitors [9], where the resistance measured value corresponds to its average value.

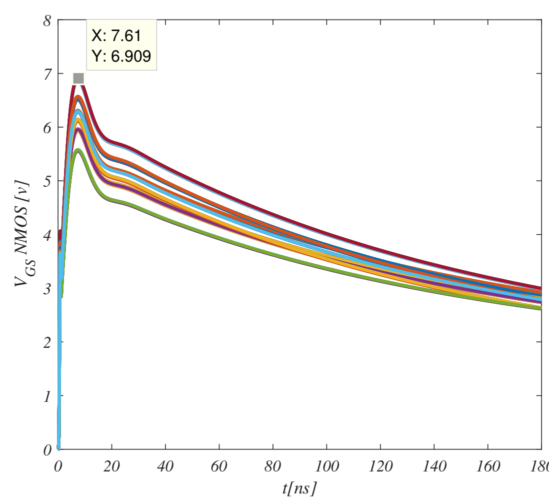
3.1 BREAKDOWN VOLTAGE

When an HBM model discharge occurs, the residual voltage on the I/O pad is imposed directly in the NMOS source and gate terminals. In Fig. 9 presents the effect with (Fig. 3.10(a)) and without (3.10(b)) the proposed PMOS transistor.

Figure 9: Gate-Source voltage during an HBM discharge event.



(a) V_{GS} NMOS with PNMOS protection



(b) V_{GS} NMOS without PNMOS protection

As observed, an evident decrease in the source-gate voltage of NMOS terminals is achieved with PMOS transistor acting as a resistor for voltage division. NMOS gate-source voltage value decreases from 6.3V to 0.84V approximately, protecting transistor oxide from rupture. Once the resistance measurement methodology is defined and the proposed protection circuit is verified, Post-layout results for PVT and MC simulations are presented in the next subsection.

3.2 POST-LAYOUT CORNERS AND MONTE CARLO RESULTS

The results presented correspond to the typical and extreme corner cases, assuming that all the other corner results are within this values. Its corresponding parameter setups are presented in Table 3.

Table 3: Worst corners cases.

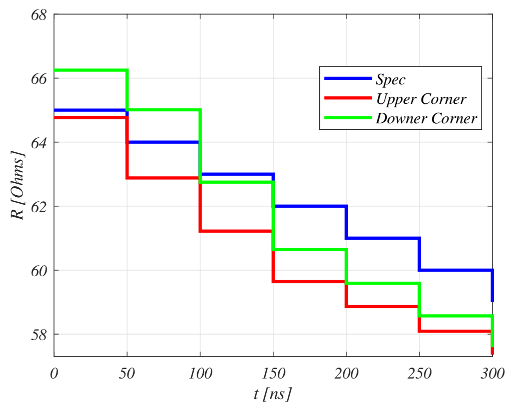
	Temperature[^oC]	V_{CM} Voltage[V]
SSHLL upper corner	-40	0.9
SSLHH downer corner	125	1.1
Typical	50	1

Post-layout results presented in Fig. 10 cover the specification range for worst cases in corners. The finally value of the impedance network varies in time due to control signals varies in time too and in Fig. 11 present the results of Monte Carlo simulation with 200 runs only for B2 and B4 are ON.

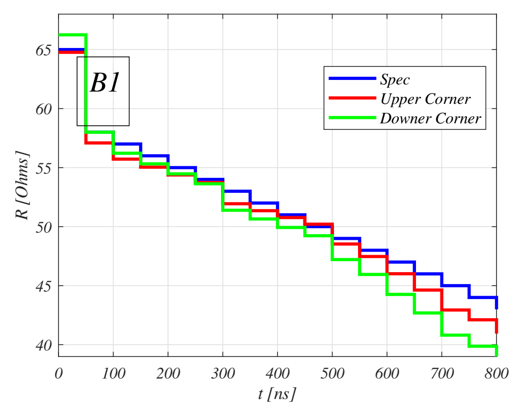
The critical values for the resistance occur when blocks B2 and B4 are connected or disconnected to the network due to the abrupt transient step, i.e. binary steps (58Ω and 42Ω). During this transitory, the value of the resistance can experience the highest deviation from its expected value as presented in the results. In order to correct this effect, a combination of parallel and series resistances can be implemented for achieving better precision, but as mentioned, layout area is penalized.

Regarding static current consumption, both 65Ω block and PMOS currents are taken into account, its typical values are 4.7mA and 336nA respectively.

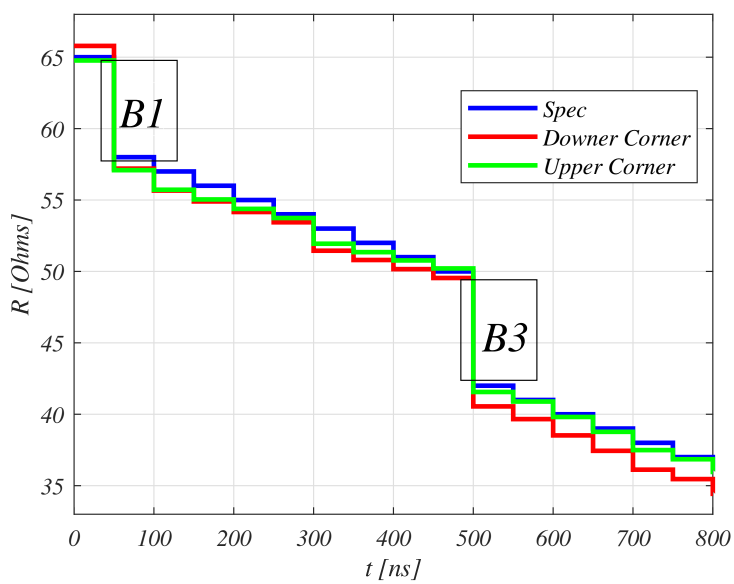
Figure 10: Post-layout results for corner cases.



(a) B1 ON.



(b) B2 and B3 ON.



(c) B2 and B4 ON.

Table. 4 presents the current consumption results for each of the blocks when all resistances and corresponding PMOS transistors are activated.

Figure 11: Monte Carlo results for variation $\pm 3\sigma$

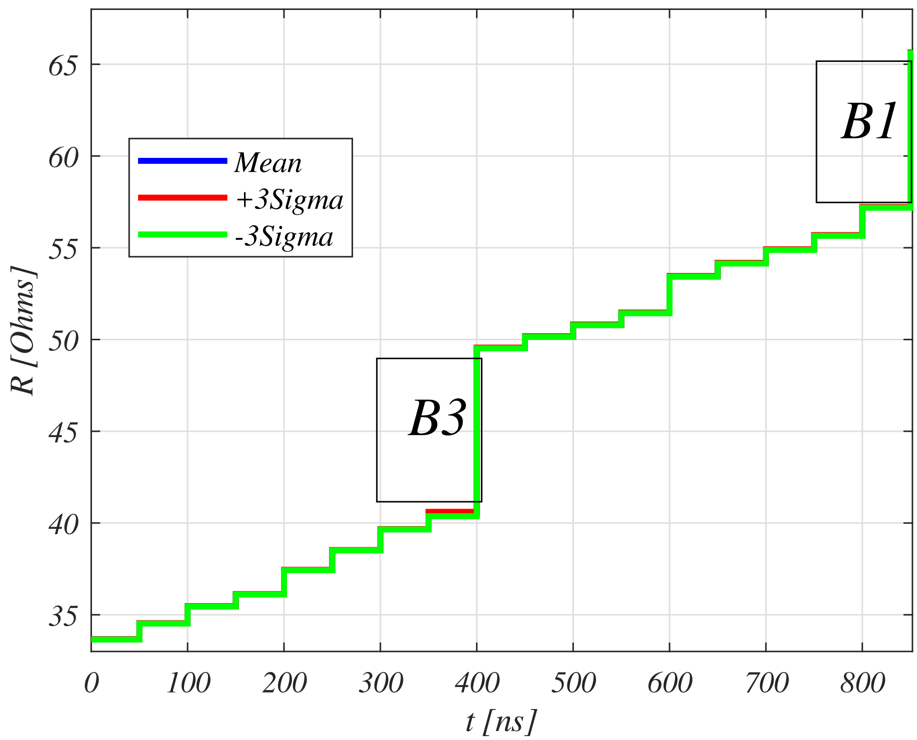


Table 4: Current consumption of individual blocks and corresponding PMOS transistors.

	B1	B2	B3	B4	B_{Ajus}
I_{Block} $[mA]$	5.16	1.11	0.28	0.41	1.43
I_{PMOS} $[nA]$	93.1	30.3	68.9	39.6	104
I_{Rfixed} [mA]			4.70		

The maximum current consumption occurs when the network presents the minimum resistance value (35Ω), i.e. blocks two and four, PMOS transistors and the fixed resistance are activated, yielding to a maximum current consumption of approximately

7.14mA.

3.3 CORNER CORRECTION

As mentioned, PVT variations are solved by including an additional block that modifies the initial resistance value. Results with and without adjustment block are presented in Table.5, demonstrating the importance of this block.

Table 5: Corner verification with and without adjustment.

Spec	Upper Corner unadjusted	Downer Corner unadjusted	Upper Corner adjusted	Downer Corner adjusted
65Ω	73.015Ω	57.922Ω	64.77Ω	66.25Ω

3.4 LAYOUT

The final layout consists of the interconnection of all the blocks as shown in Fig. 12. Dummy elements for both resistances and transistors and interdigitalization of the unitary elements are used as layout techniques. The layout occupies a 0.03mm^2 (200μm x 150μm) area. Excepting for the 65Ω resistance, all the metal connections between resistors and transistors have a width of 1.5μm. The dimensions used for each of the elements are shown in the Table 6.

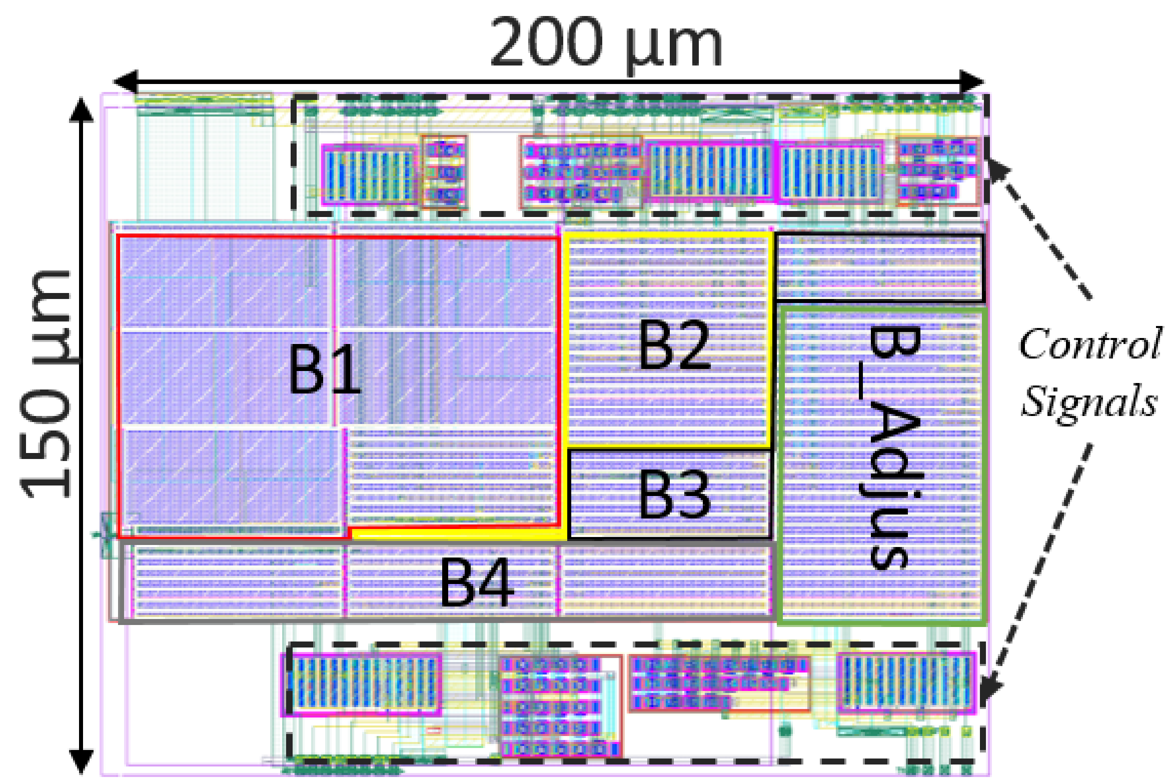
Table 6: Dimensions of the unitary elements used in the layout.

Element	W [μm]	L [μm]
$R_{unitary}$	1.5	45.2
$M_{Unitary}NMOS$	10	0.35
$M_{Unitary}PMOS$	2	2
R_{fixed}	19.3	47.8

Where R_{fixed} is the unitary resistance of the 65Ω resistance, $M_{unitary}$ NMOS and

$M_{unitary}$ PMOS are the PMOS and NMOS unitary transistors and $R_{unitary}$ is the resistance used for the resistances branches.

Figure 12: Layout in 180nm CMOS standard technology.



4. CONCLUSIONS

- Impedance matching network for USB 3.0 applications is designed in a 180nmn CMOS standard technology. Its value varies in the 35Ω - 65Ω range by using binary and thermometer codes. A design methodology is developed by considering ESD events, ESD protection circuits, current densities and transistor breakdown voltages for targeting both area minimization and desired impedance range. Post-layout results for both corners and Monte Carlo simulations are within the specifications. A calibration block is included for compensating PVT variations by adjusting the initial resistance value at 65Ω, while impacting both real state and switching power.

5. FUTURE WORKS

- Regarding future works, the inclusion and selection of an external T-coil network for canceling the impedance imaginary part is desired.

- The implementation of own pads, primary ESD and secondary ESD circuits are expected in order to identify the impedance added by these components.

- The inclusion of ESD transistor models in the simulation tool must be done to guarantee safety voltage values of all the integrated circuit elements while an ESD event occurs.

- The design of a power clamp that responds to the CDM model must be effectuated.

- Finally, the definition of the experimental set up must be implemented in order to test the impedance network.

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