DESIGN OF A REPLICA-DRIVING REFERENCE BUFFER FOR A 28NM SAR ADC

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Degree work presented as a requirement to qualify for the title of Electronic Engineer

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RESUMEN

TÍTULO: DISEÑO DE UN BUFFER DE REFERENCIA CON ARQUITECTURA DE RÉPLICA PARA UN ADC SAR DE 28 NM [*]

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PALABRAS CLAVE: SAR, ADC, MICROELECTRÓNICA, DISEÑO DE CIRCUITOS ANALÓGICOS, BUFFER DE REFERENCIA, ARQUITECTURA DE RÉPLICA, TIEMPO DE ESTABLECIMIENTO.

DESCRIPCIÓN:

En los convertidores analógico-digitales de aproximaciones sucesivas (SAR ADC), el buffer de voltaje de referencia es un bloque crítico, ya que debe suministrar una tensión estable y de baja impedancia al convertidor digital-analógico capacitivo (CDAC) durante cada evento de conmutación. La redistribución de carga introduce perturbaciones transitorias en los nodos de referencia, por lo que el buffer debe restaurar rápidamente el voltaje antes de cada comparación.

En este trabajo se diseña un buffer de referencia con arquitectura de conducción por réplica (Replica-Driving Reference Buffer, RVB) para un ADC SAR de 10 bits y 10 MS/s en tecnología CMOS de 28 nm. La arquitectura emplea una rama réplica que emula la carga del DAC, permitiendo suministrar la corriente dinámica de forma más eficiente y mejorar el comportamiento de asentamiento bajo condiciones de conmutación.

El diseño está guiado por requerimientos a nivel de sistema, donde el error combinado de asentamiento y ruido debe ser menor a 0.5 LSB para preservar la precisión. El buffer se implementa mediante una arquitectura folded-cascode con etapas de polarización y desplazamiento de nivel, y se valida mediante simulaciones esquemáticas y post-layout, incluyendo variaciones PVT y análisis de Monte Carlo.

Los resultados muestran un consumo de potencia de 1.24 mW y un ENOB en peor caso de 8.81 bits, manteniéndose cercano al objetivo de 9 bits y cumpliendo con los requerimientos de asentamiento derivados de las especificaciones del ADC. Aunque el ruido excede la especificación en la condición más crítica, su impacto en el desempeño global es limitado, ya que no domina el presupuesto total de error. Estos resultados indican que la arquitectura propuesta es una solución viable para el buffer de referencia en ADCs SAR de resolución media, proporcionando un compromiso adecuado entre velocidad de asentamiento, comportamiento de ruido y consumo de potencia.

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[*] Trabajo de Grado

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ABSTRACT

TITLE: DESIGN OF A REPLICA-DRIVING REFERENCE BUFFER FOR A 28NM SAR ADC [*]

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KEYWORDS: SAR, ADC, MICROELECTRONICS, ANALOG CIRCUIT DESIGN, REFERENCE BUFFER, REPLICA ARCHITECTURE, SETTLING TIME.

DESCRIPTION:

In successive approximation register (SAR) analog-to-digital converters (ADCs), the reference voltage buffer plays a critical role in ensuring accurate conversion, as it must provide a stable and low-impedance voltage to the capacitive DAC (CDAC) during each switching event. The dynamic charge redistribution inherent to the SAR operation introduces transient disturbances at the reference nodes, requiring the buffer to rapidly restore the voltage before each comparison cycle.

In this work, a replica-driving reference voltage buffer (RVB) is designed for a 10-bit, 10 MS/s SAR ADC implemented in 28 nm CMOS technology. The proposed architecture employs a replica branch that emulates the DAC loading conditions, enabling efficient delivery of dynamic current and improving the settling behavior of the reference voltage under switching conditions.

The design is guided by system-level requirements derived from ADC operation, where the combined error due to settling and noise must remain below 0.5 LSB to preserve conversion accuracy. The buffer is implemented using a folded-cascode-based architecture with dedicated biasing and level-shifting stages, and its performance is validated through schematic and post-layout simulations, including process, voltage, and temperature (PVT) variations and Monte Carlo analysis.

The results show a power consumption of 1.24 mW and a worst-case ENOB of 8.81 bits, remaining close to the 9-bit target while meeting the settling requirements derived from the ADC specifications. Although the noise exceeds the target in the worst-case condition, its impact on the overall performance is limited, as it does not dominate the total error budget. These results indicate that the proposed architecture is a viable solution for reference buffering in medium-resolution SAR ADCs, providing an effective trade-off among settling speed, noise behavior, and power consumption.

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[*] BSc Thesis

[**] Facultad de Ingenierías Físico-Mecánicas. Escuela de Ingenierías Eléctrica, Electrónica y de Telecomunicaciones. Director: JORGE EDUARDO ANGARITA PEREZ

INTRODUCTION

Analog-to-digital converters (ADCs) enable the interface between real-world analog signals and digital systems, making them essential components in modern electronic devices such as communication systems, sensors, and system-on-chip (SoC) platforms. Among the different ADC architectures, successive approximation register (SAR) ADCs have gained significant attention due to their high energy efficiency and compatibility with scaled CMOS technologies.

Medium-resolution SAR ADCs (9–12 bits) with sampling rates in the range of tens of MS/s are widely used in applications such as wireless communications and digital television receivers (DVB-T, DVB-H). In these systems, the overall performance of the ADC depends not only on the core architecture but also on auxiliary blocks such as reference generators, reference voltage buffers, and variable gain amplifiers. In particular, the reference voltage buffer is a critical component, as it directly impacts the speed and dynamic performance of the conversion process [1]. The linearity and dynamic performance of SAR ADCs are affected by several non-idealities, including capacitor mismatch, kT/C noise, comparator kick-back noise, reference noise, and incomplete reference settling.

In SAR ADCs, the reference voltage is directly connected to the capacitive digital-to-analog converter (CDAC), which undergoes charge redistribution during each conversion cycle. This switching activity generates dynamic current demands and voltage disturbances at the reference nodes, requiring the buffer to rapidly restore the reference voltage before each comparison. Several approaches have been studied in the

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[1] Prakash HARIKUMAR and J Jacob WIKNER. “Design of a reference voltage buffer for a 10-bit 50 MS/s SAR ADC in 65 nm CMOS”. in: *2015 IEEE International Symposium on Circuits and Systems (ISCAS)*. 2015.

literature to provide the reference voltage, including direct connection to the supply, capacitive reference drivers, and active reference buffers. Direct connection is generally undesirable due to supply coupling, while capacitive drivers reduce static power but provide limited regulation under dynamic loading. For this reason, active reference buffers are often preferred in medium-resolution, high-speed SAR ADCs, particularly in mixed-signal multichannel ASICs.

As a result, the reference buffer must satisfy strict system-level requirements. In particular, the combined error due to incomplete settling and noise must remain below 0.5 LSB in order to preserve the target resolution of the ADC. In addition, the settling requirement is imposed by the SAR ADC timing, since the reference voltage must recover after each CDAC switching event before the next comparator decision. For the target converter, this translates into an available settling interval below 7.69 ns. Therefore, the buffer must provide low output impedance, low noise, fast settling, and sufficient dynamic current capability.

The design of high-performance reference buffers becomes increasingly challenging in scaled CMOS technologies, where reduced voltage headroom and parasitic effects constrain circuit operation. Traditional buffer architectures may fail to meet the required settling speed or output impedance under dynamic loading conditions, making them unsuitable for high-speed, high-resolution SAR ADCs. [2].

To address these limitations, this work proposes a replica-driving reference buffer architecture. The proposed design includes an open-loop main branch supported by slow feedback loops that regulate internal node voltages, ensuring accurate reference levels. A replica branch, scaled by a factor of 1:M, emulates the CDAC loading conditions, allowing the buffer to supply the required dynamic current more efficiently. Additionally,

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[2] Yi ZENG et al. “An Auxiliary-Loop-Enhanced Fast-Transient FVF LDO as Reference Buffer of a SAR ADC”. in: IEEE. 2018.

source followers provide isolation between the load and the control loops, while a level shifter extends the output voltage swing [3].

The remainder of this document is organized as follows: Section 2 presents the project overview; Section 3 describes the specifications and architecture; Section 4 details the buffer design process; Section 5 presents the layout implementation and post-layout simulation results; and Section 6 presents the conclusions and future work.

[3] Weitao LI et al. “A power-efficient reference buffer with wide swing for switched-capacitor ADC”. in: *Microelectronics Journal* 46.5 (2015), pp. 410–414.

1. OBJECTIVES

1.1. GENERAL OBJECTIVE

- To design a reference buffer using a Replica-Driving topology for a 10-bit, 10MS/s SAR ADC in a 28nm standard CMOS process.

1.2. SPECIFIC OBJECTIVES

To apply optimization techniques for improving the speed and stability of the reference voltage while minimizing power consumption.

To certify the proper functioning of the reference voltage buffer by successfully meeting PVT (Process, Voltage, and Temperature) and Monte Carlo simulation corner requirements across varying operating conditions.

To integrate the reference voltage buffer with the target ADC and evaluate its performance in terms of accuracy, speed, and power efficiency.

To design the layout of the reference voltage buffer in compliance with 28nm CMOS design rules and certify its correct operation through post-layout simulations, including parasitic extraction analysis.

2. PROJECT OVERVIEW

This chapter introduces the key concepts underlying the system and establishes the corresponding design specifications. It begins with a brief overview of analog-to-digital converters and the SAR ADC operating principle. Then, the adopted SAR architecture is described, emphasizing the CDAC and its interaction with the reference voltage. Finally, the reference voltage generation and the target performance parameters derived for the reference buffer are presented.

2.1. THE ADC

An analog-to-digital converter (ADC) transforms a continuous-time analog signal into a discrete digital output by sampling and quantizing its amplitude.
Common ADC architectures include flash, pipeline, SAR, and sigma–delta converters, each offering different trade-offs between speed, resolution, power consumption, and complexity. Among these, the SAR architecture provides an efficient trade-off between resolution and energy consumption.

2.2. SAR ADC OPERATING PRINCIPLE

A successive approximation register (SAR) ADC determines the digital output through an iterative binary search. After sampling the input, the DAC generates a comparison voltage that is compared with the sampled input signal. Starting from the most significant bit (MSB), the converter refines its estimate over N comparison cycles.

2.3. THE ADOPTED SAR ADC ARCHITECTURE

2.3.1. Basic architecture The SAR ADC adopted in this work is a 10-bit fully differential architecture with a sampling frequency of $f_s = 10$ MHz, implemented in a

28 nm CMOS process, as reported in [4]. It consists of four main functional blocks: a sample-and-hold (S/H) circuit, a capacitive digital-to-analog converter (CDAC), a dynamic comparator ($f_{cmp} = 130$ MHz), and a digital logic unit, as shown in Fig. 2.3.1.

At the start of each conversion, the input signal is acquired using a bootstrapped sample-and-hold circuit, which improves linearity by maintaining a nearly constant switch resistance across the input range. The sampled differential signal is then processed by the CDAC, which performs both the sampling function and the generation of the comparison voltage V_{DAC} through charge redistribution.

The CDAC is implemented using a binary-weighted capacitor array with a unit capacitance $C_u = 13.39$ fF. A split-capacitor technique is applied to the most significant bits in order to reduce common-mode voltage variations and improve linearity.

The comparator is based on a dynamic StrongARM latch preceded by a preamplifier stage, enabling low static power consumption while maintaining high sensitivity. The SAR logic employs a monotonic switching scheme, sequentially determining each bit based on the comparator output.

Because the CDAC is directly connected to the reference nodes during switching, each bit decision draws transient charge from V_{REF}, making the reference buffer a critical component of the system.

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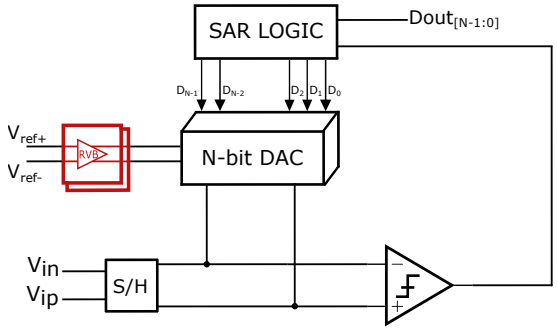
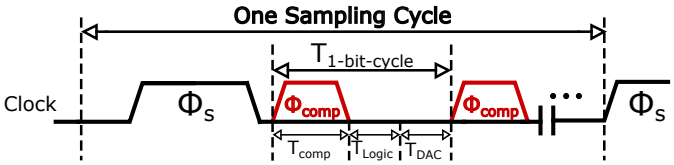
[4] Jorge Eduardo Angarita PEREZ and Nicolas Orcasitas GARCIA. “Design of an Analog to Digital Converter (ADC) in a 28 nm CMOS Process”. MA thesis. Universidad Industrial de Santander, 2024.

Figure 2.3.1. Block diagram of the 10-bit fully differential SAR ADC architecture.



Source: Own work.

Figure 2.3.2. SAR ADC timing diagram.



Source: Own work.

2.3.2. Cdac operation and load on the reference The capacitive DAC (CDAC) is the main source of dynamic loading for the reference buffer. For a 10-bit architecture with a unit capacitance of $C_u = 13.4$ fF, the total capacitance is:

$$C_{tot} \approx 2^N C_u = 2^{10} \cdot 13.4 \text{ fF} \approx 13.7 \text{ pF} \tag{1}$$

Due to the differential structure, each reference branch drives approximately half of this capacitance.

Sampling Phase During the sampling phase (Φ_s), the entire CDAC is connected to the reference, resulting in the maximum load:

$$C_{load,sampling} \approx C_{tot} \tag{2}$$

Conversion Phase During conversion (Φ_{comp}), capacitors are switched sequentially, producing a code-dependent dynamic load. The effective switched capacitance at the i-th bit is:

$$C_{sw}(i) \approx \frac{C_{tot}}{2^i} \tag{3}$$

The largest transient occurs at the MSB:

$$C_{sw,MSB} \approx \frac{C_{tot}}{2} \approx 6.85 \text{ pF} \tag{4}$$

2.3.3. Timing of the sar adc The timing diagram in Fig. 2.3.2 shows that each conversion consists of a sampling phase followed by sequential bit cycles.
Each bit cycle is defined by:

$$T_{1-bit-cycle} = T_{comp} + T_{logic} + T_{DAC} \tag{5}$$

From the perspective of the reference buffer, T_{DAC} is critical, as it defines the available settling time after each switching event.
To ensure correct operation, the reference voltage must settle within ± 0.5 LSB during this interval, imposing strict requirements on the buffer bandwidth and transient response. This requirement can be translated into an exponential settling constraint for the reference buffer.

2.3.4. Parameters of the sar adc Certain SAR ADC parameters directly constrain the design of the reference buffer, since specifications such as ENOB and comparator operating frequency determine the required noise performance, settling behavior, and linearity.

Resolution:

The resolution of an N-bit SAR ADC defines the number of discrete levels, 2^N, used to represent the input signal. A higher resolution increases the ability of the converter to distinguish small variations in the input, resulting in finer quantization steps.

LSB:

The least Significant Bit (LSB) is defined in terms of the full-scale reference range (V_{FSR}) and the N-bit resolution as:

$$LSB = \frac{V_{FSR}}{2^N} = \frac{V_{REFP} - V_{REFN}}{2^N} \tag{6}$$

The reference voltage must settle to within ± 0.5 LSB before each comparison, imposing settling and noise constraints on the reference buffer.

ENOB:

The Effective Number of Bits (ENOB) represents the practical resolution of the ADC when noise, distortion, and other non-idealities are taken into account. It reflects how many bits of the converter are actually useful in practice, rather than the theoretical resolution.

INL:

Integral Nonlinearity (INL) quantifies the cumulative deviation of the ADC transfer function from an ideal straight line over the full input range. It is typically expressed in LSBs and reflects low-frequency errors in the conversion characteristic. INL is mainly influenced by capacitor mismatch in the CDAC, comparator offset, and reference-voltage errors.

DNL:

Differential Nonlinearity (DNL) measures the variation in the width of each output code compared to the ideal value of 1 LSB. It indicates how uniformly the quantization levels are distributed across the input range. DNL is primarily affected by mismatches in the capacitive array and switching errors.

2.4. REFERENCE VOLTAGE

The reference voltage is one of the most critical elements in a SAR ADC, as it defines the full-scale input range and directly determines the value of the least significant bit (LSB). Any deviation in V_{REF} is directly translated into conversion error, affecting both the linearity and effective resolution of the system.

In the adopted architecture [4], the reference voltage is not only a static parameter but also a dynamic node, since it is directly connected to the CDAC during both sampling and conversion phases. As previously discussed, the CDAC introduces a time-varying load that draws transient charge from the reference during every bit decision.

2.4.1. Reference voltage delivery methods Connecting the power supply directly to V_{REF} is generally undesirable, as supply noise and switching disturbances propagate to the ADC. Common approaches include active reference buffers and capacitive drivers, as shown in Fig. 2.4.1. The former offers better driving capability, while the latter reduces power consumption at the expense of area. [5]

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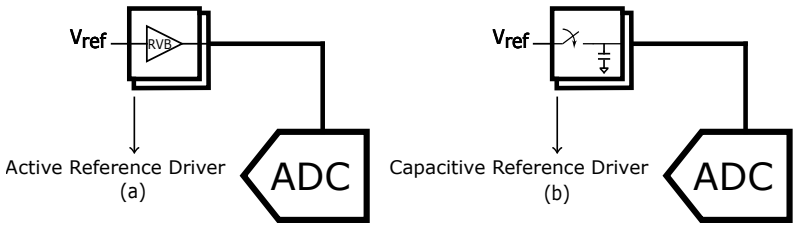
[5] Hyungyu JU, Sewon LEE, and Minjae LEE. “A 12-bit 40-MS/s SAR ADC with Calibration-Less Switched Capacitive Reference Driver”. In: *Electronics* 9.12 (2020), p. 2116.

Figure 2.4.1. Two types of reference drivers: (a) Buffer and (b) Capacitive driver.



Source: Own work.

2.4.2. Parameters of the reference voltage buffer The performance of the reference voltage buffer (RVB) is defined by key parameters that determine its ability to maintain a stable and accurate reference under dynamic conditions.

Settling Time:

The settling time defines how fast the reference voltage recovers after a disturbance caused by CDAC switching. During each bit cycle, charge redistribution produces transient voltage deviations at the reference node, and the buffer must restore the voltage within the available time T_{DAC}.

To ensure correct operation, the settling error must be smaller than ± 0.5 LSB. This requirement imposes strict constraints on the buffer bandwidth and transient response, as incomplete settling directly results in conversion errors and degradation of linearity.

Power Supply Rejection:

Power-supply rejection (PSR) defines the ability of the buffer to attenuate supply-voltage variations. Since the reference node is sensitive to disturbances, any coupling from VDD can introduce errors in the DAC output, affecting the decision error of each comparison.

Strong supply-noise rejection is therefore required to ensure that supply noise does not propagate to V_{REF}, particularly in mixed-signal environments where digital switching activity is present.

Output Noise:

The output-referred noise of the buffer is a critical parameter, as it directly adds uncertainty to the reference voltage. This noise is composed of thermal noise, flicker (1/f) noise, and other device-related contributions. Since this noise is directly seen by the CDAC during each comparison, it degrades the signal-to-noise ratio and limits the achievable ENOB of the ADC.

3. SPECIFICATIONS AND ARCHITECTURE

This chapter presents the reference voltage buffer architecture and the definition of the key specifications that must be satisfied. These requirements arise from the need to provide a stable and low-noise reference voltage to the 10-bit, 10 MS/s SAR ADC, ensuring accurate charge redistribution in the capacitive DAC and reliable bit decisions during the conversion process.

3.1. DESIGN SPECIFICATIONS

In general, the reference buffer specifications are directly defined by the SAR ADC parameters. These parameters determine both the maximum allowable reference-voltage perturbation and the required dynamic behavior. In particular, the discrete-time operation of the SAR ADC imposes strict constraints on the settling error, noise performance, and driving capability of the reference circuitry.

Settling Time and Dynamic Requirement:

During the conversion process, each switching event of the capacitive DAC introduces a disturbance in the reference voltage, as shown in Fig. 3.1.1. These disturbances manifest as undershoot or overshoot followed by an exponential recovery, determined by the dynamic response of the reference buffer.

To ensure correct operation, the reference voltage must settle sufficiently close to its final value before the next comparison takes place. Therefore, the available time per bit is defined by the inverse of the clock frequency, as expressed in (7):

$$T_{bit} = \frac{1}{f_{clk}} \tag{7}$$

However, not all this time is available for settling, since part of the cycle is consumed

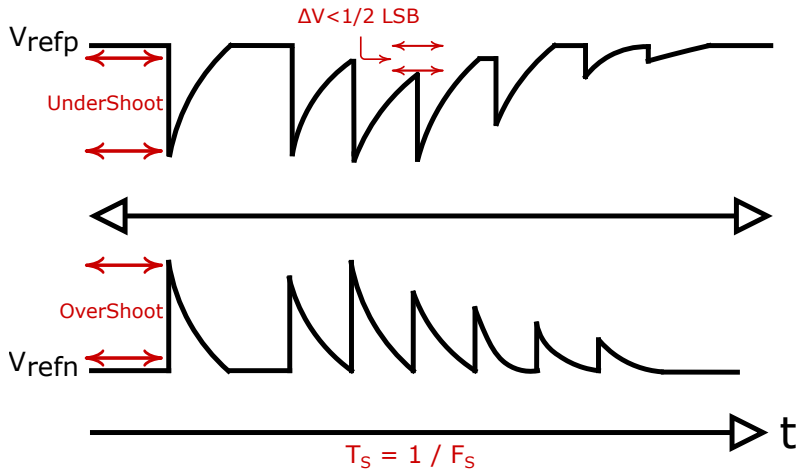
by DAC switching and comparator decision time. This leads to the effective settling constraint given in (8):

$$T_{settling} \leq T_{bit} - T_{comp} - T_{switch} \tag{8}$$

For a comparator clock frequency of 130 MHz, the bit period can be computed using (7), resulting in:

$$T_{bit} = \frac{1}{130\,\text{MHz}} = 7.69\,\text{ns} \tag{9}$$

Figure 3.1.1. Reference voltage transients caused by CDAC switching, showing undershoot and overshoot followed by finite settling.



Source: Own work.

Error Budget and LSB Constraint:

The maximum allowable error in the reference voltage is determined by the ADC resolution. A deviation comparable to the least significant bit (LSB) directly leads to an incorrect comparison result. Therefore, the total error must satisfy the condition given in (10):

$$V_{error,total} \leq \frac{1}{2} LSB \tag{10}$$

However, this total error is composed of multiple contributions, as expressed in (11):

$$V_{error,total} = V_{settling} + V_{noise} + V_{dynamic} \tag{11}$$

where:

- $V_{settling}$ is the residual error due to incomplete settling,
- V_{noise} is the output noise of the buffer,
- $V_{dynamic}$ accounts for voltage variations due to charge redistribution.

To ensure robust operation, the total error budget is distributed among these contributions. A conservative allocation is defined in (12):

$$V_{settling} \leq \frac{1}{4} LSB, \quad V_{noise} \leq \frac{1}{4} LSB \tag{12}$$

The LSB value is computed from the full-scale range using (13):

$$LSB = \frac{V_{FSR}}{2^N} = \frac{1.5 - 0.3}{2^{10}} = 1.17\,\text{mV} \tag{13}$$

Using this result, the maximum allowable noise level can be obtained from (12) as:

$$V_{n,rms} \leq \frac{LSB}{4} \approx 293\,\mu\text{V} \tag{14}$$

It is important to note that noise is inherently a stochastic quantity and should strictly be treated in an RMS sense and compared against the quantization noise level. The previous allocation of $LSB/4$ represents a conservative error-budget partition intended to separate the noise and settling contributions. However, using this value as the direct

design target for the reference buffer would impose an overly restrictive noise requirement, leading to a considerable increase in power consumption and area.
Therefore, in this work the output-noise target is defined as half of the LSB value, as expressed in (15). This value is still below the maximum allowable reference error of the ADC and provides a practical trade-off between noise performance, power consumption, and area. The impact of this design choice is finally verified at system level through the achieved ENOB of the complete ADC.

$$V_n \leq \frac{1}{2} LSB \tag{15}$$

This target is interpreted as an RMS output-noise requirement and is not intended to bound every instantaneous noise excursion. Its validity is verified at the system level through the achieved ENOB of the complete ADC, which includes the effect of the reference-buffer noise.

Settling Error Constraint:

Assuming a first-order approximation for the buffer response, the settling behavior is described by the exponential expression in (16):

$$V_{settling}(t) = V_{step} \cdot e^{-t/\tau} \tag{16}$$

To meet the allocated error budget, the condition in (17) must be satisfied:

$$V_{step} \cdot e^{-T_{settling}/\tau} \leq \frac{LSB}{4} \tag{17}$$

From (17), the required time constant τ (and thus the bandwidth) of the buffer can be derived, directly linking the dynamic performance to the SAR ADC specifications.

Average Power (P_{av}):

Based on state-of-the-art designs, the power consumption of the reference buffer is

typically higher than that of the ADC core due to the dynamic load it must drive. Considering an ADC power consumption of $0.37\,\mathrm{mW}$, the design target is defined in (18):

$$P_{av,Buffer} \leq 4 \cdot P_{av,ADC} = 1.48\,\text{mW} \approx 1.5\,\text{mW} \tag{18}$$

Based on the specifications presented above, Table **3.1** summarizes the reference buffer parameters, including the ENOB, which verifies the system-level integration with the ADC; the phase margin, which guarantees circuit stability; and the PSR, which quantifies the sensitivity to disturbances from both the supply voltage and ground. The listed specifications are defined for both the positive and negative reference voltages.

Table 3.1. Parameters and design targets for the reference voltage buffer

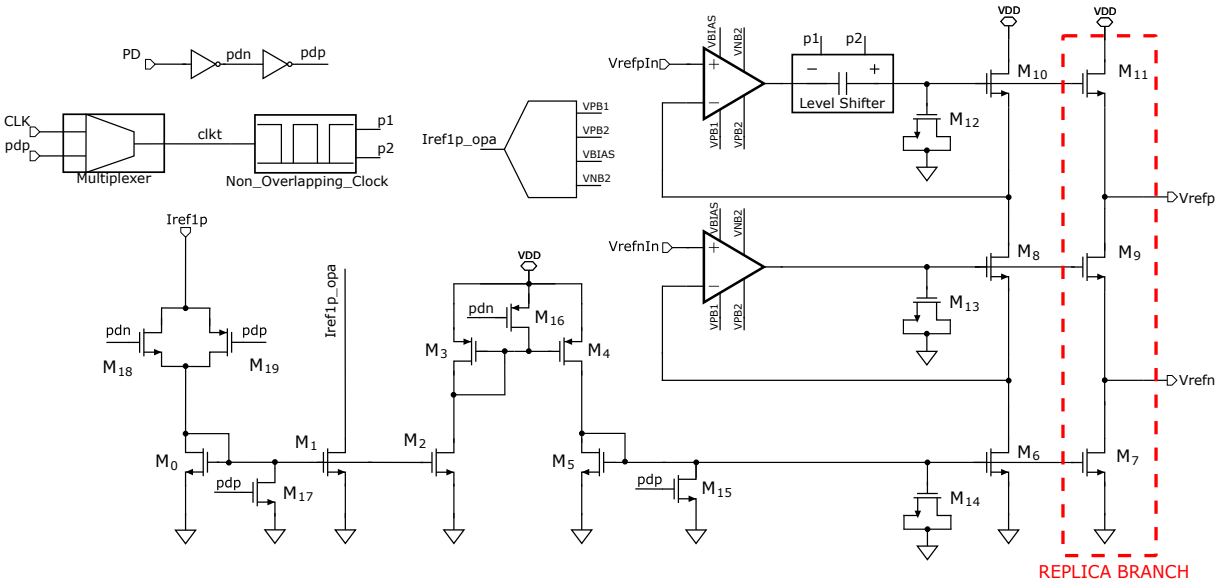
Parameters	**Units**	**Design Target**		
		Min	**Typ**	**Max**
Power Consumption	mW	-	-	1.5
Settling Time	ns	-	-	7.69
Output Noise Voltage (rms)	µV	-	-	586
Phase Margin	°	60	-	-
Power Supply Rejection (GND)	dB	-	TBM	-
Power Supply Rejection (VDD)	dB	-	TBM	-
ENOB w/ RVB	bit	9	-	-
Area	mm^2	-	TBM	-

3.2. RVB ARCHITECTURE

Based on the previously defined specifications, an NMOS replica-branch topology [3] was selected for the reference voltage buffer, as shown in Fig. 3.2.1.The architecture consists of a replica branch responsible for driving the CDAC load, whose operating point is regulated by slow negative feedback loops. These loops are implemented using N-type and P-type folded-cascode OTAs to properly handle V_{refpIn} and V_{refnIn}, respectively. By sensing internal feedback voltages, the OTAs adjust the gate voltages of the control transistors to force their source nodes toward the target reference levels.

The stability of this multi-loop architecture is supported by the dominant-pole behavior of the regulation stages. Since each OTA output is loaded with a large capacitance, the feedback loops behave as first-order systems where the dominant pole is positioned at a sufficiently low frequency to isolate the loop response from high-frequency parasitic effects. Furthermore, source followers isolate the large capacitive load from the regulation loops, preserving stability under dynamic switching conditions, while a level shifter extends the output swing under the limited headroom of 28 nm CMOS technology. Compared to a PMOS-based buffer operating at the same bias current [6] , the NMOS-only implementation achieves higher transconductance with reduced parasitic capacitances.

Figure 3.2.1. Core Architecture of the Proposed Reference Buffer.



Source: Own work.

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6 Wenbin HE, Fan YE, and Junyan REN. “A Fast Response Reference Voltage Buffer for 12b 200MS/s SAR ADC”. in: *2020 IEEE 63rd International Midwest Symposium on Circuits and Systems (MWSCAS)*. 2020, pp. 1–4.

3.3. CIRCUIT IMPLEMENTATION OF THE BUFFER BLOCKS

Specific topologies were selected for the internal building blocks of the buffer, namely the OTAs with their corresponding bias circuits, the non-overlapping clock generator, and the level shifter (LS) implementation.

3.3.1. Transconductance amplifier For the implementation of the OTAs, the folded-cascode topology was selected. This architecture provides a voltage gain comparable to that of a two-stage OTA while allowing single-stage compensation. As a result, no additional compensation networks are required, which simplifies the stability design across process corners [7]. Stability is favored by the single-stage nature of the topology, where the output node is designed to be the dominant pole of the system. By ensuring that the load capacitance at this node significantly exceeds any internal parasitic capacitances, the OTA maintains a first-order response with a robust phase margin, thereby reducing the risk of oscillations within the regulation loops.
As shown in Fig. 3.3.1, two folded-cascode variants were implemented: one employing an NMOS input differential pair and another employing a PMOS input differential pair, corresponding to the reference input ports V_{refpIn} and V_{refnIn} , respectively.

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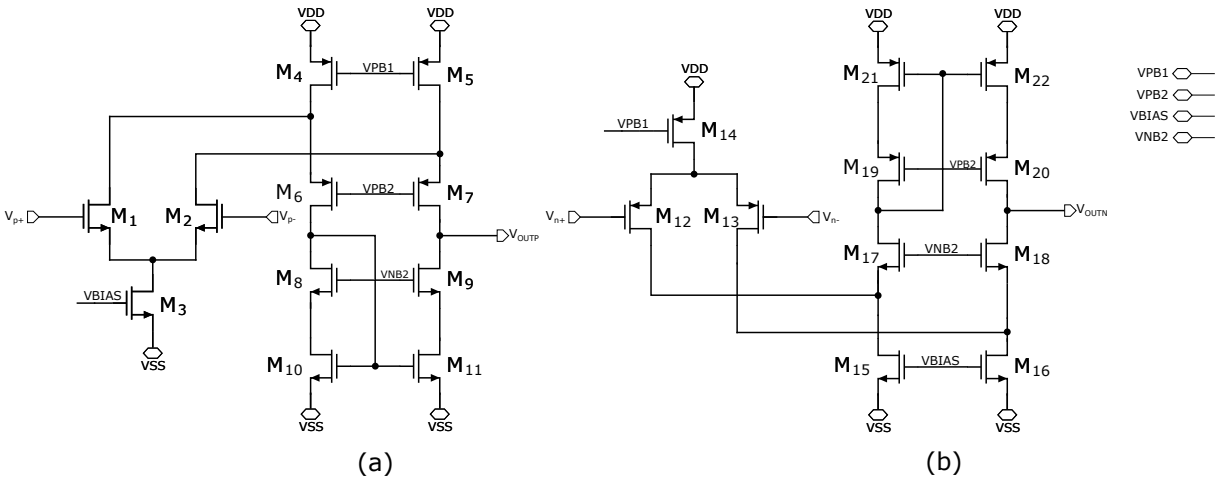
[7] Phillip E. ALLEN and Douglas R. HOLBERG. *CMOS Analog Circuit Design, Third Edition*. 3rd. p. 316. New York, Oxford: Oxford University Press, 2012.

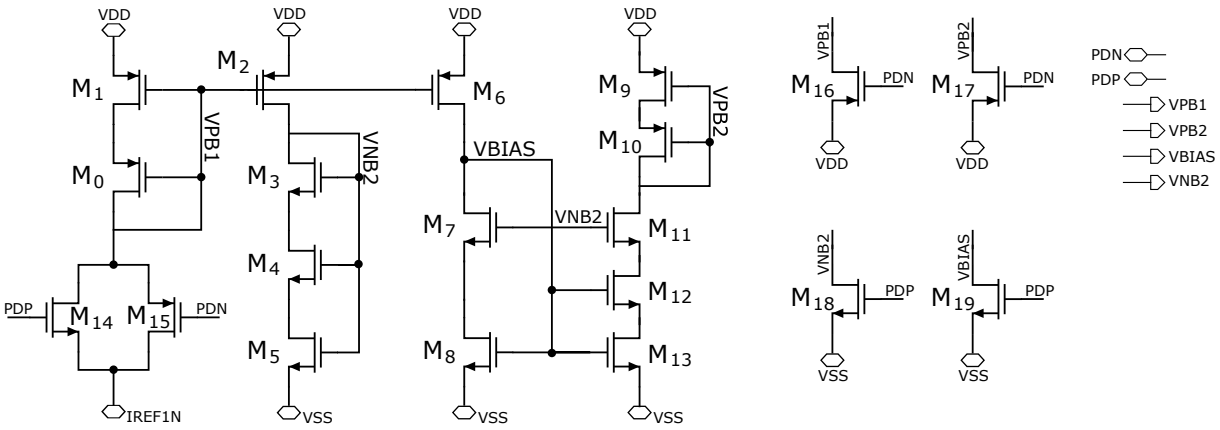
Figure 3.3.1. Folded-Cascode OTAs: (a) NMOS-input, (b) PMOS-input.



Source: Own work.

The circuit topology illustrated in Fig. 3.3.2 was selected for the biasing of both folded-cascode OTAs. As shown in the schematic, power-down circuits are included to allow the buffer to be turned off when not in use. Several transistors have been stacked to significantly reduce power consumption within the bias network. This biasing scheme is critical, as it maintains the operating point under process, voltage, and temperature (PVT) corners, while the folded-cascode OTAs themselves also experience corner-dependent changes. Consequently, the bias network helps stabilize the operating point and minimizes the variation of key specifications across corners.

Figure 3.3.2. Bias Circuit for the Folded-Cascode OTAs.



Source: Own work.

3.3.2. Level shifter To increase the output swing and properly bias the replica transistors, a level shifter is required. Since the positive reference voltage is close to V_{DD}, the OTA output alone does not provide sufficient headroom for correct biasing. Therefore, a level shifter is introduced to elevate the OTA output voltage. The selected topology, shown in Fig. 3.3.3, is clocked at the SAR ADC comparator frequency and operates using a non-overlapping clock scheme to prevent charge sharing and ensure proper switching behavior. [8]

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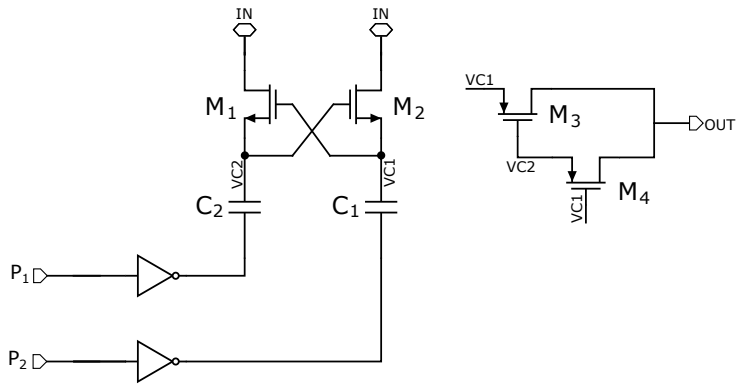
[8] Hugo HERNANDEZ, Jonathan SCOTT, and Wilhelmus VAN NOIJE. “DPA Insensitive Voltage Regulator for Contact Smart Cards”. In.

Figure 3.3.3. Selected Topology of Level Shifter.

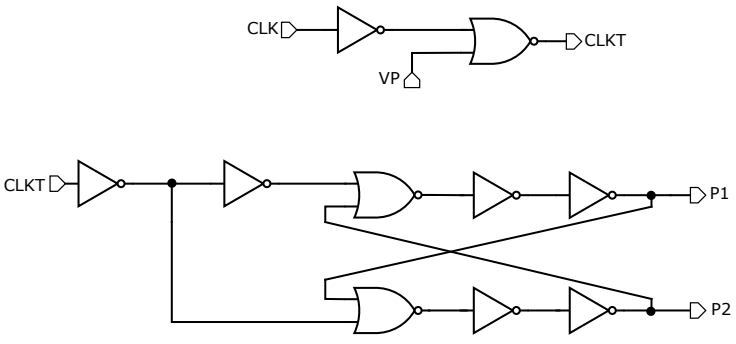


Source: Own work.

3.3.3. Non-overlapping clock As shown in Fig. 3.3.3, the proposed level shifter requires two non-overlapping clock phases. These signals are generated using the topology in Fig. 3.3.4, which introduces a controlled dead time between phases, ensuring that one clock fully transitions low before the other rises. This prevents short-circuit currents and guarantees efficient charge transfer toward the next stage.

Additionally, two extra logic gates were incorporated with a VP control input, which allows the clock signals to be isolated when the power-down (PD) mode is active.

Figure 3.3.4. Non-Overlapping Clock Topology.



Source: Own work.

4. RVB DESIGN PROCESS

This chapter describes the step-by-step design methodology used to implement the transistor-level circuits presented in the previous chapter. The design process is supported by first-order analytical calculations, fundamental design equations, and the technical considerations that guided device sizing, bias definition, and stability verification.

4.1. DESIGN METHODOLOGY OVERVIEW

The design process began with a preliminary characterization of the CMOS technology in order to understand the main device limitations and operating ranges. Subsequently, the top-level buffer architecture was implemented using ideal operational amplifiers to evaluate the system behavior and derive the required amplifier specifications without being limited by non-ideal circuit effects.

Once these specifications were defined, the level shifter was designed to enable the required voltage swing. The buffer was then integrated with the DAC and the sample-and-hold stage of the ADC, which significantly reduced simulation time compared with simulations of the complete ADC. The bias network was then implemented to generate the required operating currents, and the power-down circuitry was added to disable the buffer when required.

After completing the schematic design, the circuit was verified across PVT corners, iteratively refining the design until the target specifications were satisfied. Finally, the buffer was integrated with the complete SAR ADC for system-level validation. The circuit layout was then implemented and verified through layout versus schematic (LVS), followed by post-layout simulations including extracted parasitic elements.

4.2. BUFFER DESIGN

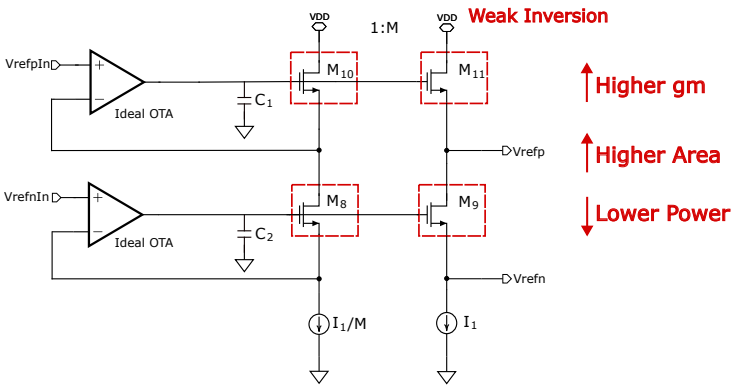
After the technology characterization, the design began with transistors M11 and M9, which form the replica branch of the buffer. As shown in (19), the circuit bandwidth is mainly determined by the transconductance of these devices. Therefore, the minimum channel length allowed by the technology was selected in order to maximize the transit frequency f_T and reduce parasitic capacitances.

$$f_{out} \approx \frac{1}{2\pi R_{eq} C_{dac}} \approx \frac{g_{m11}}{2\pi C_{dac}} \tag{19}$$

$$gm_1 = f_{out} \cdot 2\pi \cdot Cdac \tag{20}$$

As shown in Fig. 4.2.1, the devices were biased in weak inversion to increase the transconductance efficiency (g_m/I_D), allowing the required g_m to be achieved with a lower bias current. The bias current was then adjusted to obtain the target transconductance required by the settling speed of the circuit.

Figure 4.2.1. Top-level circuit without bias network and with ideal OTAs.



Source: Own work.

Next, a scaling factor M was defined in order to establish a trade-off between power consumption and area. Based on this factor, transistors M10 and M8 were properly

sized to obtain the desired current scaling in the replica branch.

Afterward, an AC analysis was performed, as shown in (21), to evaluate the stability of the loop. It can be observed from (21) that the system stability is governed by the dominant pole. By sizing C_1 such that ω_p is significantly lower than the frequency of non-dominant parasitic poles, the loop stability is improved and the impact of parasitic capacitances is minimized.

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{A_0}{\left(\frac{1}{g_m r_o} + 1 + A_0\right) + \left(\frac{1}{g_m r_o} + 1\right) r_{\text{out}} C_1 s} \tag{21}$$

This design approach prioritizes the use of the replica branch as the main path to deliver the required dynamic current to the load, while effectively decoupling the reference nodes from the slow feedback loops. As a result, the transient response at the outputs is primarily governed by the open-loop behavior of the replica path rather than by the closed-loop regulation. Consequently, the OTAs are not required to operate at high speed, since their role is limited to establishing the operating point and not to directly controlling the settling dynamics. This allows the OTAs to be designed with reduced bandwidth and lower bias current, improving power efficiency while still preserving the overall stability and settling performance of the system.

4.3. OTAS DESIGN

For the design of the OTAs, two main considerations were taken into account. First, each amplifier was required to provide high gain while maintaining a controlled bandwidth, allowing the OTAs to operate with low power consumption and reserving most of the power budget for the replica branch.

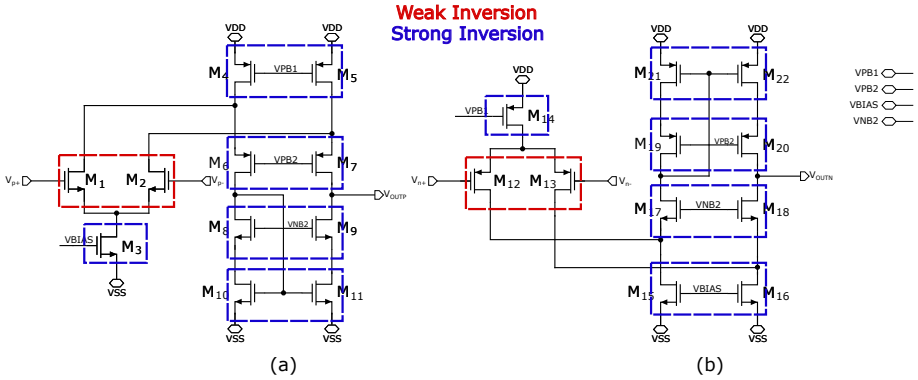
The input differential pairs were biased in weak inversion in order to increase the transconductance efficiency (g_m/I_D), enabling the required bandwidth to be achieved with lower current. The remaining transistors were biased in strong inversion and sized

accordingly to ensure proper operation, as shown in Fig. 4.3.1.

Furthermore, the maximum power consumption of the circuit can be expressed as a function of the current flowing through transistor M3, as shown in (22). Considering that the current through M4 is defined to be 1.5 times the current of M3, this relationship establishes the maximum bias current that can flow through the branch without exceeding the power consumption specified in the design requirements.

$$P_{av} = V_{DD} \cdot (3I_{M3}), \qquad I_{M3} \leq \frac{P_{av}}{3V_{DD}} \tag{22}$$

Figure 4.3.1. OTAs schematic indicating the operating region of the transistors: (a) NMOS-input, (b) PMOS-input.



Source: Own work.

To improve the intrinsic gain of the amplifier, the transistors were designed using long-channel devices, which increase the output resistance and therefore the overall gain, as indicated in (23).

$$|A_v| \cong g_{m1}\{g_{m4}r_{o4}r_{o5} \parallel [g_{m3}r_{o3}(r_{o1} \parallel r_{o2})]\} \tag{23}$$

4.4. LEVEL SHIFTER DESIGN

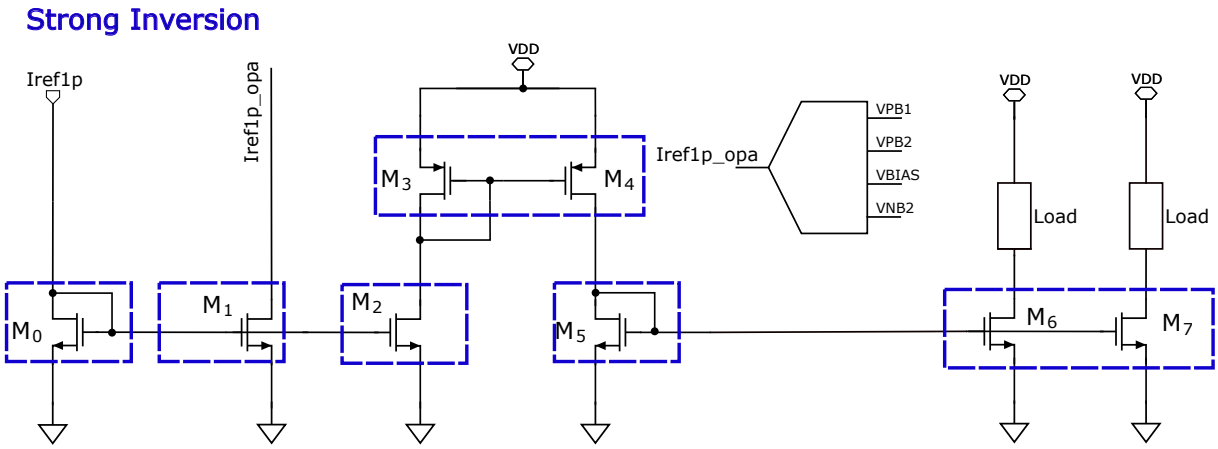
For the design of the level shifter, the transistors mainly operate as switching devices. Therefore, the default device dimensions provided by the technology were adopted, since the switching performance is mainly determined by the comparator clock frequency ($f_{CMP} = 130$ MHz) and it does not impose strict requirements on intrinsic gain or matching.

The design primarily focused on selecting the Metal-Oxide-Metal (MOM) capacitance value ($C_{1,2} = 32$ fF), balancing two competing constraints. First, the capacitance must be limited to minimize settling time and ensure high-speed operation. At the same time, it must remain sufficiently large to mitigate the impact of parasitic currents on the stored charge.

4.5. BIAS NETWORK DESIGN

The bias circuit is shown in Fig. 4.5.1. All transistors were biased in strong inversion in order to reduce sensitivity to process corner variations. The OTA bias voltages were selected, as previously discussed, to guarantee proper biasing of all the transistors within the folded-cascode architecture. Additionally, a PMOS current mirror was included, since directly mirroring the reference current would have significantly increased the circuit area.

Figure 4.5.1. Bias Circuit for the Folded-Cascode OTAs.



Source: Own work.

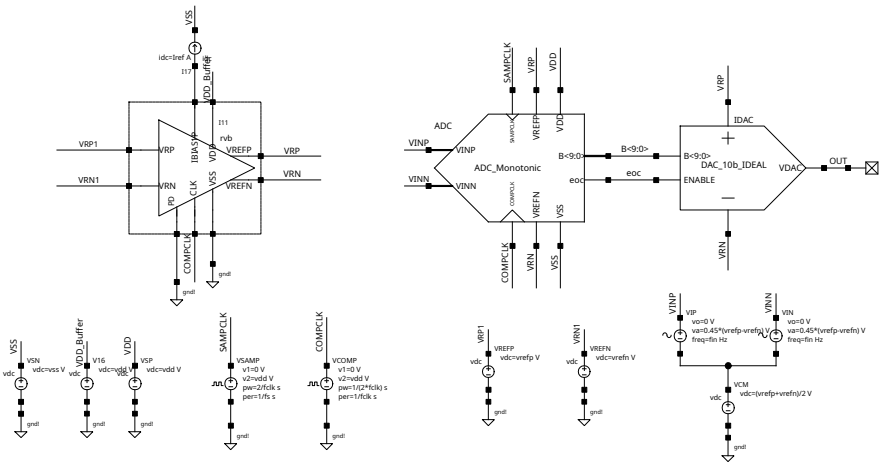
4.6. VERIFICATION

As mentioned in the design methodology, two different testbenches were used to evaluate the buffer. The first testbench includes only the relevant ADC front-end blocks, while the second contains the complete ADC. This approach was adopted because simulations with the full ADC are considerably longer.

Figure 4.6.1 shows the buffer connected to the complete ADC. This testbench was used to evaluate the integration of the proposed circuit with the ADC.

In this setup, power consumption and ENOB were measured. The ENOB results were used to verify the correct integration of the buffer with the SAR ADC.

Figure 4.6.1. Testbench including the complete SAR ADC.



Source: Own work.

5. RESULTS

In this chapter, the final device dimensions of each circuit block and the corresponding layout implementation are presented. All transistors were implemented using the standard 1.8 V device models provided by the TSMC 28 nm technology and using a single-finger layout. Post-layout simulations of the parameters defined in the design specifications are then presented, including verification across PVT corners and Monte Carlo variations. Finally, a performance comparison between the proposed buffer and other buffers reported in the literature is provided.

5.1. TRANSISTOR SIZING

Bias OTA

Table 5.1 presents the transistor dimensions of the bias circuit used in both folded-cascode OTAs shown in Fig. 3.3.2. A reference transistor was used throughout the circuit, and the required current ratios were obtained by adjusting the number of multipliers. Additionally, transistors M2, M4, M5, M11, and M13 were stacked to obtain a larger effective channel length. Transistors M14–M19 were implemented as power-down devices and also used as dummy devices in the layout.

Table 5.1. Bias OTA Transistor dimensions.

Parameter	M0/M1	M2	M3–M11	M12/M13	M14–M19
Width [μm]	0.5	0.5	0.5	0.5	0.5
Length [μm]	2	2	2	2	0.15
Multipliers	2	6	1	2	4

Folded Cascode N-type

Table 5.2 presents the transistor dimensions of the N-type folded-cascode OTA shown in Fig. 3.3.1(a).

Table 5.2. N-Type Folded-Cascode OTA transistor dimensions.

Parameter	M1/M2	M3, M8, M9	M4/M5	M6/M7	M10/M11
Width [μm]	1	1	1	1	2
Length [μm]	1	1	1	1	0.4
Multipliers	20	1	2	4	1

Folded Cascode P-type

Table 5.3 presents the transistor dimensions of the P-type folded-cascode OTA shown in Fig. 3.3.1(b).

Table 5.3. P-Type Folded-Cascode OTA transistor dimensions.

Parameter	M12/M13	M14–M18, M21, M22	M19/M20
Width [μm]	1	1	0.75
Length [μm]	1	1	1
Multipliers	20	1	4

Level Shifter and Digital Blocks

Table 5.4 presents the transistor dimensions of the level shifter shown in Fig. 3.3.3. Additionally, Table 5.5 shows the dimensions of the NAND and inverter gates used in the non-overlapping clock generator, as well as the MUX employed for the clock power-down shown in Fig. 3.3.4.

Table 5.4. Level Shifter transistor dimensions.

Parameter	M1–M4
Width [μm]	0.32
Length [μm]	0.15
Multipliers	1

Table 5.5. Digital Blocks transistor dimensions.

Parameter	M_{INV}	M_{NAND}
Width [μm]	0.32	0.32
Length [μm]	0.15	0.15
Multipliers	1	1

Top-Level Circuit

Table 5.6 presents the transistor dimensions used in the top-level circuit shown in Fig. 3.2.1. Transistors M12–M14 are implemented as MOSCAP devices, which provide higher capacitance per area than standard capacitors. Transistors M15–M18 were

used as power-down devices and were sized to also serve as dummy devices in the layout.

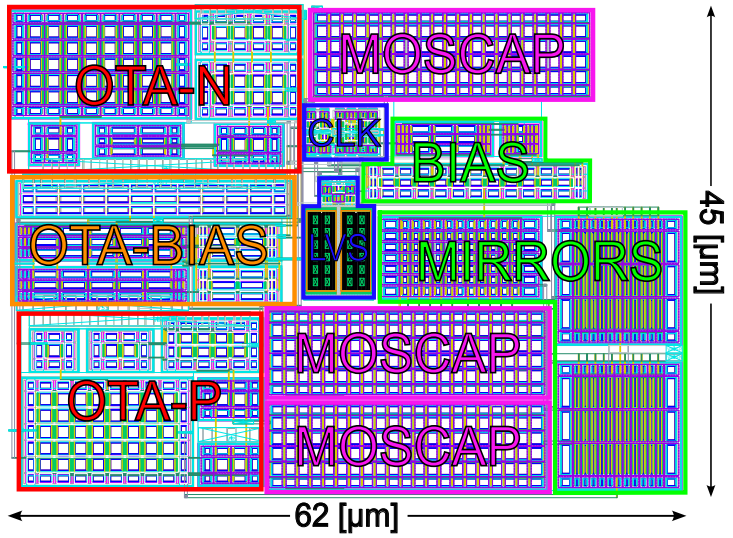
Table 5.6. Top Level transistor dimensions.

Parameter	M0–M2	M3	M4	M5	M6	M7	M8/M10	M9/M11	M12–M14	M15/M17	M16/M19	M18
Width [μm]	0.5	0.5	0.5	0.5	0.5	0.5	2.56	2.56	1	0.5	0.5	0.5
Length [μm]	1.5	1	1	0.4	0.4	0.4	0.15	0.15	1	0.15	0.15	0.15
Multipliers	1	1	10	1	5	50	3	30	76	12	2	4

5.2. LAYOUT CONSIDERATIONS

Accurate post-layout simulation required careful layout practices to minimize performance degradation, including proper transistor matching through common-centroid structures. Besides, dummy devices were incorporated in each stack to reduce edge effects and improve process uniformity, while a detailed understanding of the technology helped address layout-dependent phenomena. Particular attention was given to shallow trench isolation (STI), well proximity effect (WPE), latch-up, and electromigration, which were mitigated through device characterization and close adherence to TSMC design guidelines.

Figure 5.2.1. Reference Voltage Buffer Layout.



Source: Own work.

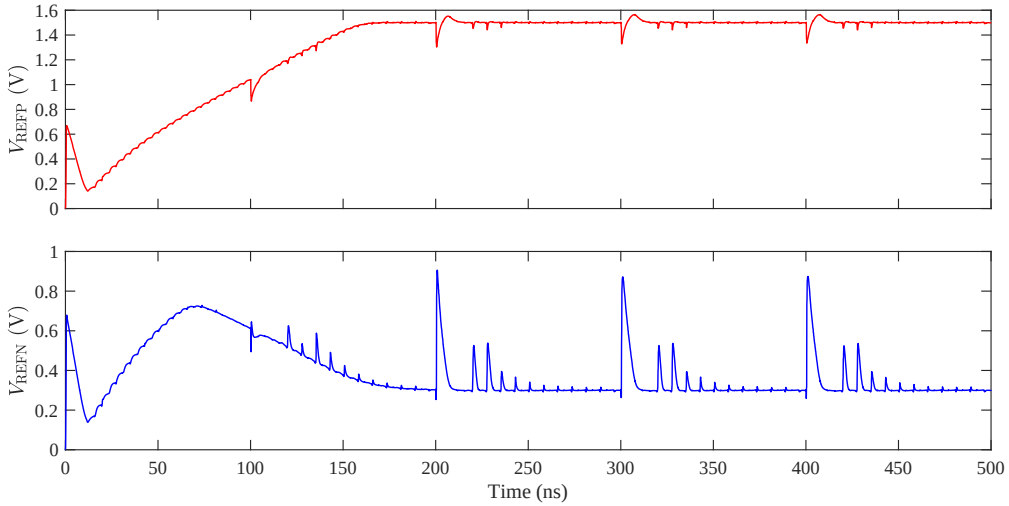
5.3. POST LAYOUT SIMULATIONS

After completing the layout design, design rule checking (DRC) and layout-versus-schematic (LVS) verification were performed. Subsequently, parasitic extraction (PEX) was carried out and post-layout simulations were executed to evaluate the impact of the reference voltage buffer (RVB) on the ADC dynamic performance.

A sinusoidal input with an amplitude corresponding to 90% of the full-scale input range was applied to avoid saturation, with a common-mode voltage of $V_{DD}/2 = 0.9\,\text{V}$. The input frequency was set to $F_{in} = F_s/2$ (Nyquist), representing a worst-case condition where the CDAC switching activity is maximized, producing the largest load transients on the RVB. Under this configuration, key dynamic metrics such as ENOB, SFDR, and total power consumption were obtained. Additional buffer metrics were evaluated by extracting the steady-state operating point and performing small-signal analyses. ST, noise, PSR, phase margin, and other AC-based metrics were obtained for each process corner.

5.4. STABILITY VALIDATION

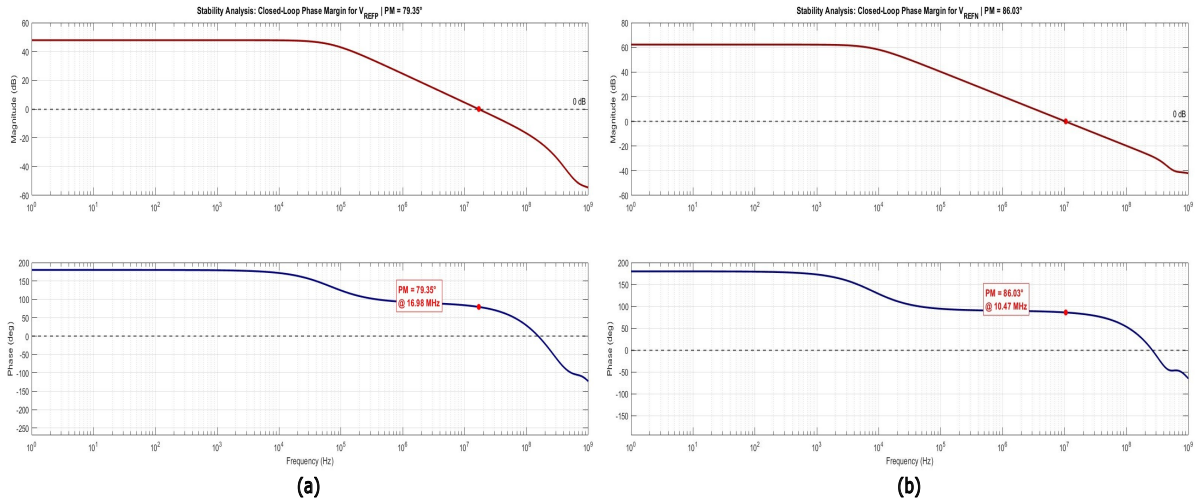
Figure 5.4.1. Reference settling waveforms of the Reference Voltage Buffer.



Source: Own work.

Beyond adhering to the target design specifications, verifying the overall system stability is crucial. Such verification is derived from the transient analysis of the reference outputs (Fig. 5.4.1), where the expected settling levels of 1.5 V and 0.3 V are clearly observed, confirming the absence of unstable oscillations. The voltage spikes present in the waveforms are expected switching transients caused by the CDAC's operation during conversion. These spikes are effectively suppressed by the buffer, ensuring the references fully settle to their target values within the 7.69 ns time window available before each comparison step.

Figure 5.4.2. Closed Loop Bode Diagram: (a) Positive reference, (b) Negative reference.



Source: Own work.

Additionally, stability was evaluated in the frequency domain through closed-loop Bode analysis of both reference paths, as shown in Fig. 5.4.2. The responses show a clear dominant pole behavior, consistent with the single-stage behaviour of the OTAs and the large capacitive loading at their outputs. In all cases, the phase margin exceeds 60 °, ensuring robust stability. The lack of gain peaking and the smooth phase transition indicate sufficient separation of non-dominant poles from the unity-gain frequency, confirming stable operation and complementing the transient results.

5.5. PROCESS-VOLTAGE-TEMPERATURE (PVT) CORNER SIMULATIONS

For corner verification, the supply voltage was varied from 1.62 V to 1.98 V and the temperature from $-40°$C to $125°$C. Process variations were evaluated using the SS, TT, and FF corners, representing slow, typical, and fast device conditions, respectively. Table 5.7 summarizes the overall system specifications, while Tables 5.8 and 5.9 present the individual specifications of the positive and negative reference buffers.

Table 5.7. Performance summary of the ADC with the proposed reference buffer and comparison with ideal references

Parameters	Units	Min	Typ	Max
Power Consumption	mW	0.86	1.05	1.24
ENOB w/ RVB	bit	8.81	9.64	9.98
ENOB w/ Ideal References	bit	9.12	9.77	9.98
Area	μm^2	-	2790	-

Table 5.8. Positive reference buffer results

Parameters	Units	Min	Typ	Max
Settling Time	ns	3.19	4.17	5.1
Output Noise Voltage (rms)	µV	64.4	301	639
Phase Margin	°	73.50	79.35	89.5
Power Supply Rejection (GND)	dB	-39.54	-43.7	-50.08
Power Supply Rejection (VDD)	dB	-26.862	-87.8	-95.4

Table 5.9. Negative reference buffer results

Parameters	Units	Min	Typ	Max
Settling Time	ns	3.34	4.82	6.2
Output Noise Voltage (rms)	µV	20.74	230	520.5
Phase Margin	°	85.9	86.03	86.5
Power Supply Rejection (GND)	dB	-29.5	-46	-86.7
Power Supply Rejection (VDD)	dB	-47.5	-60.2	-81

As shown in Table 5.7, the buffer meets the project specifications in most conditions. In the worst-case corner (SS, 1.62 V, $125°$C), the ADC already exhibits marginal performance, with an ENOB of 9.12 bits using ideal references. With the proposed RVB, this degrades by 0.31 bits to 8.81 bits. This reduction is mainly due to the slower device speed in the SS corner, which limits the buffer's dynamic response, particularly at the negative reference, where the settling time approaches the 7.69 ns DAC window. Although the 9-bit target is missed, this behavior is consistent with the initial ADC limitations.

Tables 5.8 and 5.9 summarize the main performance metrics of the positive and negative reference buffers across PVT corners. The settling time requirement is satisfied in all cases. The positive reference exhibits a fast response, reaching values as low as 3.19 ns, while the negative reference remains within the specification, with a worst-case settling time of 6.2 ns. These results confirm that both references are able to settle within the available 7.69 ns DAC window under all operating conditions.

The phase margin remains consistently high for both references, always above 70°, which confirms that the stability observed in the frequency-domain analysis is pre-

served across PVT corners. This behavior is consistent with the dominant-pole response imposed by the OTAs topology, ensuring robust operation of the multi-loop system.

The power supply rejection shows some variation across corners, mainly due to process-dependent changes in gain and bias conditions. Despite this variability, the achieved PSR levels are sufficient to attenuate supply disturbances and prevent significant coupling into the reference nodes.

The output noise exceeds the target specification of 586 µV in the worst-case corner (FS, 1.62 V, 125°C) for the positive reference. However, this does not degrade the overall system performance, since the measured ENOB in this condition is 9.69 bits. As discussed in section 3.1, the total error is determined by the combined contributions of settling, noise, and dynamic effects. In this case, the settling error remains low due to the fast response of the buffer, with a settling time of 3.56 ns, and dynamic errors are also well controlled. As a result, the noise contribution, although above the target specification, does not dominate the total error budget, allowing the overall ADC accuracy to be preserved.

5.6. MONTE CARLO VARIATIONS SIMULATION

A Monte Carlo analysis was performed to evaluate the impact of random process variations and device mismatch. Since post-layout transient simulations of the complete SAR ADC with the integrated reference buffer are computationally very expensive, Monte Carlo verification at the system level was not considered practical for dynamic specifications such as ENOB and total power consumption. In this case, 50 Monte Carlo transient samples require approximately three days of simulation, while 100 samples require about one week using significant computational resources. Moreover, the ENOB showed negligible variation under the limited number of evaluated samples, which does not justify a more exhaustive statistical verification at the full-system level.

For this reason, the Monte Carlo analysis was focused on small-signal parameters of the reference buffers around the nominal operating point, since these quantities are more sensitive to mismatch and can be verified more efficiently with a larger number of samples. A Monte Carlo simulation with 500 samples was therefore performed for the positive and negative reference buffers. The numerical results are summarized in Tables 5.10 and 5.11, while the corresponding histograms are presented for the parameters whose distributions provide additional insight into the statistical behavior of the buffer.

Table 5.10. Monte Carlo results of the positive reference buffer

Parameters	Units	Min	Max	Mean	σ
Settling Time	ns	3.59	4.75	4.21	0.4
Output Noise Voltage (rms)	µV	268	348	303	12.5
Phase Margin	°	74.72	81.13	79.5	0.63
Power Supply Rejection (GND)	dB	-54.82	-39.12	-44	2.38
Power Supply Rejection (VDD)	dB	-112.8	-48.25	-63.6	9.26

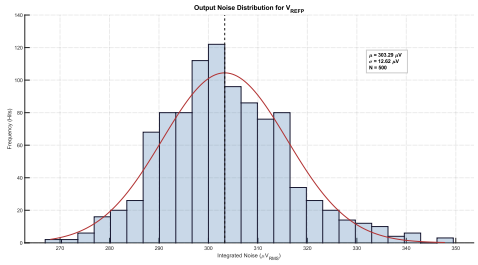
Table 5.11. Monte Carlo results of the negative reference buffer

Parameters	Units	Min	Max	Mean	σ
Settling Time	ns	3.98	5.70	4.75	0.2
Output Noise Voltage (rms)	µV	219	250	231.7	4.87
Phase Margin	°	85	86.5	86.11	0.29
Power Supply Rejection (GND)	dB	-92.72	-39.20	-46.7	5.25
Power Supply Rejection (VDD)	dB	-100.9	-50.2	-61.15	6.63

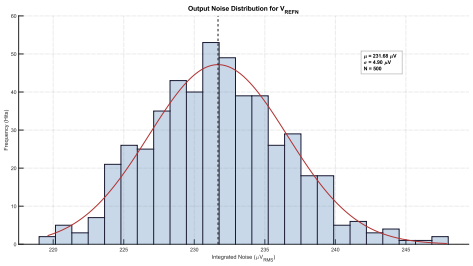
The Monte Carlo settling-time results indicate that both reference buffers are weakly affected by random mismatch variations. The full statistical range remains below the 7.69 ns timing constraint, with no critical outliers close to the limit. Therefore, the settling-time specification is statistically satisfied, and the tabulated minimum, maximum, mean, and standard-deviation values are sufficient to assess this parameter without including an additional histogram.

The output-referred noise distributions in Fig. 5.6.1 of both reference buffers exhibit an approximately Gaussian behavior. For the 500 evaluated Monte Carlo samples, the noise remains below 350 μV_{rms} in all cases, indicating that the circuit noise performance is robust against random process variations and device mismatch.

Figure 5.6.1. Output Noise Histograms.



(a) Positive Reference Output Noise

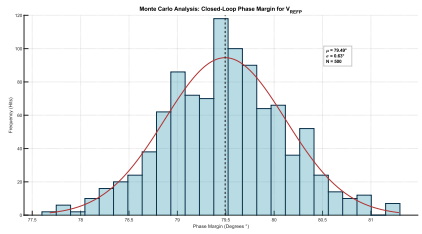


(b) Negative Reference Output Noise.

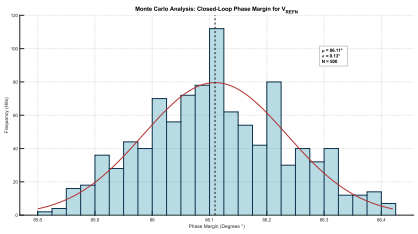
Source: Own work.

The phase-margin distributions in Fig. 5.6.2 show that loop stability is not significantly affected by Monte Carlo variations. The phase margin presents a very small dispersion, with a standard deviation of only 0.63°, confirming that both regulation loops remain stable under random process variations and device mismatch.

Figure 5.6.2. Phase Margin Histograms.



(a) Positive Reference Phase Margin.



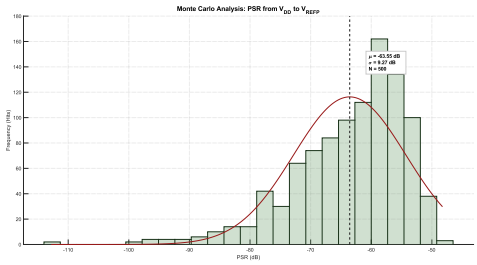
(b) Negative Reference Phase Margin.

Source: Own work.

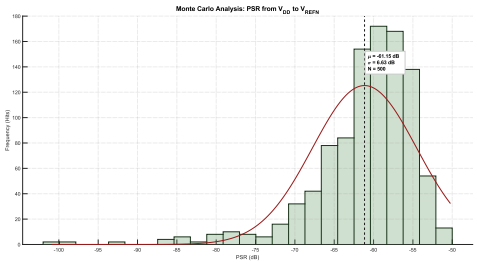
Unlike the other evaluated specifications, the PSR results do not follow an approximately Gaussian distribution. The histograms in Fig. 5.6.3 exhibit a skewed behavior toward more negative PSR values. This indicates that most Monte Carlo samples remain close to the nominal value, while the largest deviations occur in the direction of stronger supply-noise attenuation. Since PSR is expressed in negative dB, more negative values correspond to better rejection, whereas degradation would appear as a shift

toward less negative values. Therefore, although PSR presents higher statistical dispersion, this variation does not indicate a significant degradation of the supply-rejection performance within the evaluated samples.

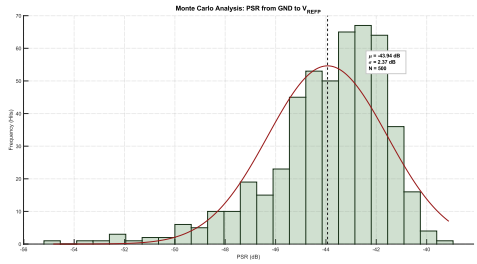
Figure 5.6.3. PSR Histograms.



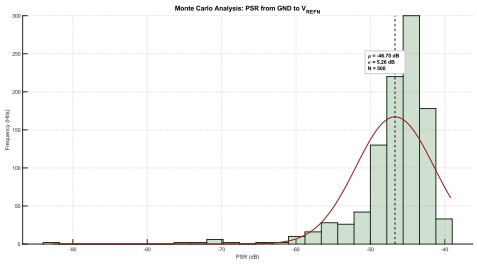
(a) Positive Reference PSR (VDD).



(b) Negative Reference PSR (VDD).



(c) Positive Reference PSR (GND).



(d) Negative Reference PSR (GND).

Source: Own work.

From the numerical results and the corresponding histograms, most specifications proved robust under Monte Carlo analysis, with the exception of the PSR, which exhibited relatively higher dispersion. This behavior can be attributed to mismatch effects that alter the gain from VDD to both reference outputs.

5.7. PERFORMANCE COMPARISON

To evaluate the buffer performance with respect to the state of the art, Table 5.12 compares several ADC implementations reported in the literature. Since the reference

buffer operates as part of the ADC system, evaluating it in isolation is not meaningful. It is important to note that the buffer specifications are defined by the ADC requirements; therefore, parameters such as power consumption may vary significantly among the compared designs.

Table 5.12. Performance summary and comparison

Parameter	**This work**	**[1]**	**[2]**	**[6]**	**[9]**
Technology (nm)	28	65	65	28	28
Supply voltage (V)	1.8	1.2	1.2	0.9	0.9/1
Sampling rate (MS/s)	10	50	100	200	200
Resolution (bit)	10	10	12	12	12
ENOB (bit) @ $f_{in} = f_{nyq}$	9.64	9.25	11.7	10.56	10.56
SNDR (dB) @ $f_{in} = f_{nyq}$	59.472	N/A	66.3	65.39	65.4
ADC power (mW)	0.378	0.69	1.05	3.63	1.88
RVB power (mW)	1.05	20	0.57	14.11	2.4
P_{RVB}/P_{ADC}	2.78	28.98	0.54	3.89	1.27

As shown in Table 5.12, the SAR ADC exhibits a balanced performance profile when compared to recent literature. While designs like **6** [6] and **9** [9] operate at higher sampling rates (200 MS/s), they require significantly more power for their reference generation, reaching up to 14.11 mW. In contrast, this work maintains a low RVB power consumption of 1.05 mW in a 28 nm process, proving to be more efficient than other sub-100 nm implementations such as **1** [1], which reports an overhead of 20 mW for the reference buffer.

The design efficiency is further highlighted by the P_{RVB}/P_{ADC} ratio. With a value of 2.78, this work demonstrates a moderate overhead compared to the high ratio of **1**

[9] Wenbin HE et al. “A Low Power Reference Voltage Buffer and High Density Unit capacitor in a 12b 200MS/s SAR ADC”. in: *2020 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*. 2020, pp. 82–85. DOI: 10.1109/APCCAS50809.2020.9301670.

[1] (28.98). Although **2** [2] and **9** [9] show lower ratios, they target different architectural trade-offs or technology nodes. Thus, the results confirm that the developed buffer is effectively optimized to meet the 10-bit resolution requirements while minimizing the power impact on the overall ADC system.

6. CONCLUSIONS AND FUTURE WORK

6.1. CONCLUSIONS

This work presented the design of a replica-driving reference buffer for a 10-bit, 10-MS/s SAR ADC in 28-nm CMOS technology. The design process started from ADC-level requirements, allowing the main buffer specifications to be derived from settling, noise, and power constraints while targeting low power consumption.

Each block of the buffer was designed according to its specific function and performance requirements. In particular, the OTAs and the level shifter were carefully dimensioned to satisfy gain, stability, swing, and dynamic response constraints. MOSCAP devices were also employed to reduce area while providing the required voltage headroom. After schematic-level verification, the complete buffer was implemented in layout, occupying approximately 62×45 μm^2. Symmetric layout practices, optimized metal routing, and power rings were adopted to reduce offset, mitigate parasitic effects, and ensure robust bulk connections.

Post-layout simulations with extracted parasitics showed a worst-case ENOB of 8.81 bits, a maximum output noise of 638.93 μV, a settling time of 6.2 ns, and a maximum power consumption of 1.24 mW. These results indicate that the proposed buffer preserves the target ADC performance with limited degradation under the most critical operating condition. In the worst-case corner, the ENOB reduction is mainly associated with the slower settling of the negative reference, whose settling time becomes comparable to the DAC settling window. In the remaining evaluated conditions, the buffer satisfied the intended settling, noise, and stability requirements.

Overall, the proposed reference buffer demonstrates that the replica-driving approach is a practical solution for reference regulation in medium-resolution SAR ADCs, providing an adequate trade-off among dynamic performance, power consumption, and area

in a scaled CMOS technology.

6.2. FUTURE WORK

Although the proposed replica-driving reference buffer successfully meets the performance requirements for the 10-bit SAR ADC in 28 nm technology, several opportunities exist for future improvements and extensions. One natural direction is the optimization of dynamic power consumption. While the current design achieves the required settling time and preserves the system-level ENOB, the power consumption of the buffer relative to the ADC remains significant. Future work could explore alternative topologies, such as self-biased or auxiliary-loop-enhanced circuits, that maintain performance while reducing power. Additionally, implementing more aggressive power gating strategies for idle sections of the OTAs could further minimize energy usage without impacting settling behavior.

Another important area is the enhancement of noise and power-supply rejection (PSR). Monte Carlo simulations indicated relatively high variability in PSR, suggesting sensitivity to device mismatch and parasitic effects. Future designs could employ improved cascode configurations, active feedback, or layout-level shielding to mitigate these effects, resulting in lower output noise and improved reference stability. Such improvements would be especially valuable in high-precision or low-noise ADC applications, where even minor voltage fluctuations can degrade performance.

Furthermore, a promising extension is the development of a programmable or adaptive buffer. By enabling dynamic adjustment of output current or voltage headroom based on DAC load, sampling frequency, or supply voltage, such a design could offer real-time power optimization and greater operational flexibility. This approach would make the buffer suitable for ADCs with varying operating conditions or multiple resolution modes.

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