DEVELOPMENT OF A 130NM DIGITAL STANDARD CELL LIBRARY

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Julián Humberto Sierra Pérez

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TITULO: DISEÑO DE UNA LIBRERÍA DE CELDAS DIGITALES ESTANDAR EN TECNOLOGIA CMOS DE 130NM*.

AUTOR: **JULIAN HUMBERTO SIERRA PEREZ** **

PALABRAS CLAVE: Celdas digitales, 130nm, compuertas digitales, flip-flop, circuitos integrados.

DESCRIPCION

Se propone el diseño de un conjunto de celdas digitales estándar incluidas dentro de una librería para aplicaciones de alta frecuencia en tecnología CMOS de 130nm. La librería cuenta con trece circuitos digitales los cuales son ocho compuertas de lógica combinacional, tres flip-flops para lógica secuencial y dos estructuras de optimización de circuitos integrados. Dos Flip-flops dinámicos con topologías “True Single Phase Clock” (TSPC) y “StrongArm” (SA) son optimizados para operar en frecuencias sobre los 4.45 GHz. Comúnmente estas arquitecturas son usadas para bajo consumo y frecuencia de reloj moderada, pero en este trabajo se plantea un diseño de estas para alta velocidad con un incremento relativo en la potencia consumida. Se usa una estrategia de iteración para calcular las dimensiones del transistor para alcanzar la frecuencia de operación requerida. Las celdas diseñadas pueden ser usadas para diseñar sistemas digitales complejos de alta velocidad. El flujo de diseño usado incluye la selección del tamaño de los transistores, esquemáticos, implementación layout y simulaciones post-layout. Además se presenta un ejemplo de síntesis digital con las celdas estándar propuestas. Para realizar una comparación relativa entre los flip-flops diseñados, este trabajo usa una figura de mérito (FOM) en unidades de pW/Hz. Los Flip-flops de alta frecuencia TSPC y SA presentan una FOM de 0.2392 pW/Hz y 1.0126 pW/Hz respectivamente mientras que el “Pass-gate Based D FF” tiene una FOM de 0.1146 pW/Hz.

* Trabajo de Grado.

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ABSTRACT

TITLE: DEVELOPMENT OF A 130NM DIGITAL STANDARD CELL LIBRARY [*]

AUTHOR: JULIAN HUMBERTO SIERRA PEREZ [**]

KEYWORDS: Standard Cell, 130nm, CMOS, digital gates, Flip-Flop, Strong Arm, TSPC, ASIC.

DESCRIPTION

Digital standard cells designed for high frequency applications in 130nm CMOS technology is proposed in this work. The library has thirteen digital circuits, these circuits are eight combinational logic gates, three flip-flops for sequential logic and two structures for optimization of integrated circuits. Two dynamic Flip-Flops with True Single Phase Clock (TSPC) and StrongArm (SA) topologies were optimized to operate up to 4.45GHz. Commonly these architectures are used to low power and moderate clock frequency, but in this work a design of these circuits is developed with the objective of reach high speed with relative increment of power consumption. An iterative strategy to calculate the transistor dimensions to achieve the requested operation frequency was used. The designed cells can be used to design complex high speed digital systems. The used design flow includes the transistors size selection, schematic and layout implementation and post-layout simulation. Also, an example of digital synthesis with the proposed standard cells is presented. To do a fair comparison between designed flip-flops, this work uses a figure of merit (FOM) in pW/Hz. High frequency flip-flops TSPC and SAFFs present a FOM of 0.2392 pW/Hz and 1.0126 pW/Hz respectively whereas the Pass-Gate Based D FF has a FOM of 0.1146 pW/Hz.

[*] Degree work

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INTRODUCTION

Semiconductors technology continues year by year reducing its sizes to develope devices that can be more faster and take up a smaller area. Nevertheless, the previous technologies do not lose validity due to a smaller cost in their fabrication[1], what makes them relevant. The 130nm CMOS technology offers high performances in terms of design/functionality characteristic in comparison with the cost. Today, this technology is considered the most used in the design of electronic devices for uses such as wireless transmission of data, automation and industrial applications. For this reason, the characteristics offered by the technology must be exploited, making desirable to push the capabilities of less expensive technology in order to reach higher frequencies than recurring to state-of-the-art technologies that are more expensive. Consequently in this paper the schematic and layout design of two flip-flops for high frequency are presented.

In addition, it is known that any combinational logic and consequently any digital circuit can be implemented by means of combinations between three basic gates NAND, NOR and NOT. Therefore, additional to the two mentioned previously flip-flops, these three basic gates are designed with different sizes or drives of charge. Moreover, a static flip-flop for low power consumption applications with less frequency than the mentioned above was designed.

The access to sequential circuits, specially of high frequency have a considerable price. For this reason, the design of the circuits described in this paper will allow to the researching group CIDIC from the Universidad Industrial de Santander the use of these models to design and implement more complex circuits and application-

[1] BAKER R., Jacob. *Circuit design, layout and simulation. 2* ed. Wiley-IEEE 2008. p. xxix. ISBN 978-0-470-22941-5.

specific integrated circuit (ASIC). This methodology allows to build complex circuits with these cells by means of digital synthesis and to interconnect resulting layouts using place and route tools.

1. 130 NANOMETER CMOS TECHNOLOGY

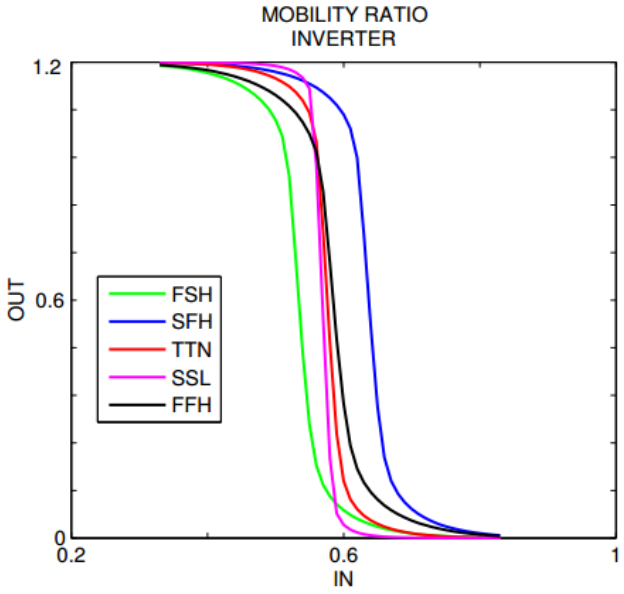
The 130nm CMOS process is refered as the semiconductor level technology reached in the 2000-2001 timeframe. Although the period of validity of the 130nm CMOS process is around 15 years, it continues being used thanks to the performance/cost profit it provides, along with the low cost solutions for applications such as wireless, automotive, industrial and security. Consequently, 130nm is the mainly used technology by the research group CIDIC of the Universidad Industrial De Santander to design and manufacture their integrated circuits.

To design the logic gates used in this library, MOS transistors with a minimum channel length of 130nm were used. Furthermore, eight metal layers are available with the purpose of setting connections between the different gates. There's one layer of poly-silicon for the construction of the gate and many dielectric layers, such as SiO_2, that allows the creation of many digital circuits. Although there are many different transistors with different characteristics, general purpose or regular VTH" transistors were initially used. These transistors are designed to work with a nominal voltage of 1.2 Volts [V] in a temperature range that goes from -40 to 125 Celcius degrees, and enough noise immunity, which is useful in digital applications. These transistors' models meet the requirements of low power consumption circuit structures without leaving aside features such as maximum operation speed and leakage currents.

The main parameter to be tuned at the design stage is the size of the transistor. The PMOS transistor's width is evaluated by means of the mobility ratio between the two types of transistors; it is therefore necessary to check this value by simulation. A simulation profile is created and an inverter with 1.2[V] supply is

used. A PVT corners analysis is made. In order to find the most suitable PMOS finger width size, different values of this parameter are tested. For each value of the PMOS finger width, a DC sweep is made by varying the inverter's input from 0[V] to 1.2[V] and observing the midpoint inversion. It is considered the most suitable PMOS finger width value the one for which the inversion point and the input voltage sweep meet at 0.6[V]. The found value is an average of the five evaluated critical corners.

Figure 1. Corner's Analysis. Vout vs. Vin of an Inverter with Mobility ratio equal 2.6562



Curves displayed in Fig. 1 belong to an inverter circuit. The simulated inverter circuit has a PMOS transistor with a width ratio of 2.6562, compared to the NMOS transistor's width.

1.1 TECHNOLOGY'S CHARACTERISTICS

To understand the 130nm technology transistors behavior, a characterization of the transistors is performed through the use of simulation tools. Before showing the results of the characterization, a description simulation setup is presented. In order to characterize each type of transistor, a new circuit in which parameters such as

the input voltage at the gate or the supply voltage at the drain can be varied is created[2]. From this circuit, different simulation profiles are created, and relations such as I_{DS} vs. V_{DS} curves for different values of V_{GS}, I_{DS} vs. V_{GS} and g_m vs. V_{GS} for different values of V_{DS} can be obtained. A PVT corners analysis is made, which in this case allows to evaluate the transistor's characteristics under changes in the temperature and intrinsic properties. The corners analysis shows the circuit's behavior under the worst and the best case operating scenarios.

Figure 2. NMOS transistor. Characterization graphics. I_{DS} vs. V_{DS}, I_{DS} vs. V_{GS}, g_m vs. V_{GS}, Corner's Analysis I_{DS} vs. V_{GS}

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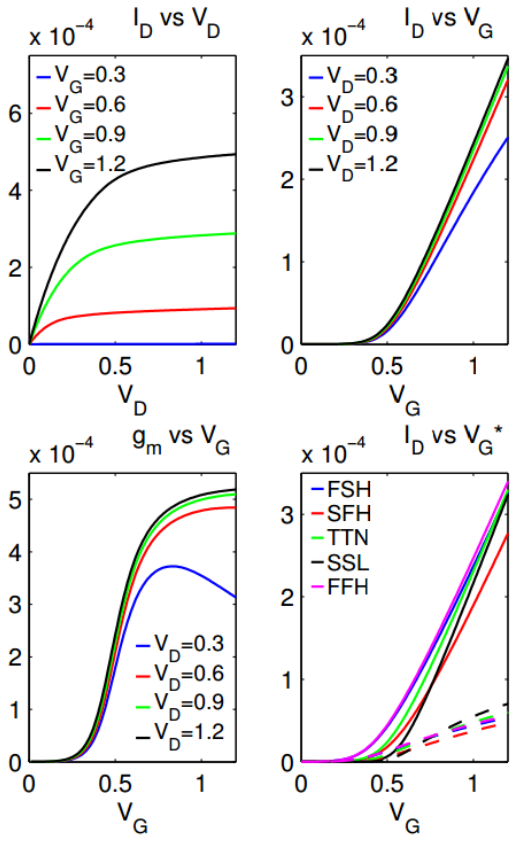
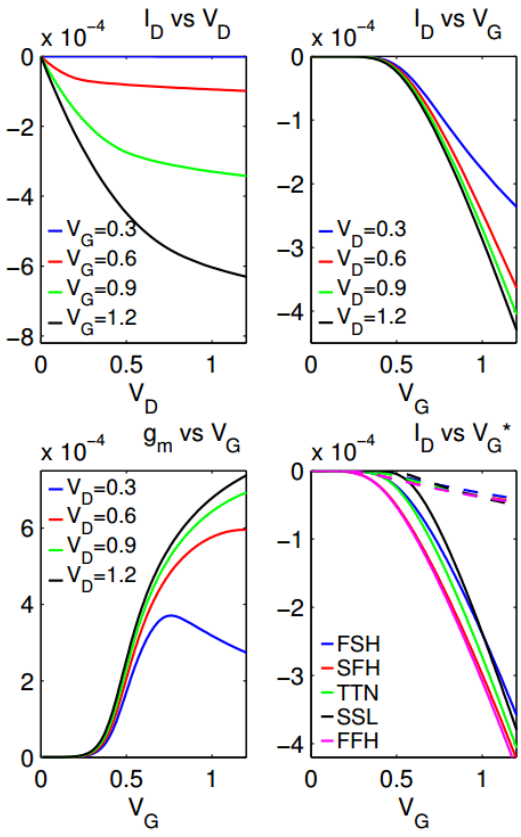


Fig. 2 shows the N-type transistor's performance. A V_{TH} value of 0.4[V] was extracted from the top right graph in Fig. 2 for four different cases of V_{DS}, taking

[2] SEDRA, Adel S. and SMITH, Kenneth C. *Microelectronic Circuits,* Fifth Edition, USA, O.rd Un.ty Press, 2003. Cap 4. ISBN 0195142519.

into account that for the smallest value of V_{DS} the curve presents a lower slope than in the remaining three cases. In the top left graph of Fig. 2, for the three cases of higher V_{GS}, V_{TH} is limiting triode zones ranging between 0[V] and 0.6[V]. From the bottom left graph of Fig. 2, the obtained values agree with the previous analysis. The transconductance has a positive slope change starting with a 0.4[V] V_{GS}, which is equivalent to the value of V_{TH}; for a 0.3[V] V_{DS}, the transconductance starts reducing since V_{GS} equals 0.9[V]; and for the remaining cases, the transconductance is stabilized since V_{GS} equals 0.9[V]. The bottom right graph in Fig. 2 shows that the transistor's behavior is similar for all corners, tending to an overall average between them. It is important to clarify that the SSL corner's (SlowN, SlowP, Low temperature) behavior of the circuit has lower currents than the others corners 0[V] and 0.8[V] V_{GS}, but since 0.8[V] V_{GS} increases its slope notoriously.

Figure 3. PMOS Transistor. Characterization graphics. I_{DS} vs. V_{GS}, I_{DS} vs. V_GS, g_m vs. V_{GS}, Corner's Analysis I_{DS} vs. V_{GS}.



The behavior of P-type transistor is shown in Fig. 3. In top left of the Fig. 3 is observed the range of triode's region ranging until 0.2[V] or 0.8[V] V_{DS}. In top right of the Fig. 3, a similar behavior to N-type transistor can be seen, a value of V_{TH} close to 0.4[V] for the four different cases has been found. In bottom left of the Fig. 3 are observed three V_{GS} important points, one of them is 0.4[V] V_{GS}, value from which the slope increases for the four cases. Another important point is 0.77[V] V_{GS}, point in the which the transconductance's values begins to decrease in the 0.3[V] V_{DS} case, while for the remaining three cases the transconductance values is stabilized since the last important point 1[V] V_{GS}.

Comparing the graphs of the two types of transistors, the maximum current achieved by NMOS transistor is lower than the maximum current reached by the PMOS transistor, therefore, the reached transconductance by the NMOS is a little smaller than the PMOS. From the corners' analysis is concluded that the dispersion in the transistor P is slightly lower than the transistor N, so the P-type presents a more uniform behavior against not desired changes in internal or external characteristics of the devices or the circuit.

2. THE STANDARD CELL METHODOLOGY

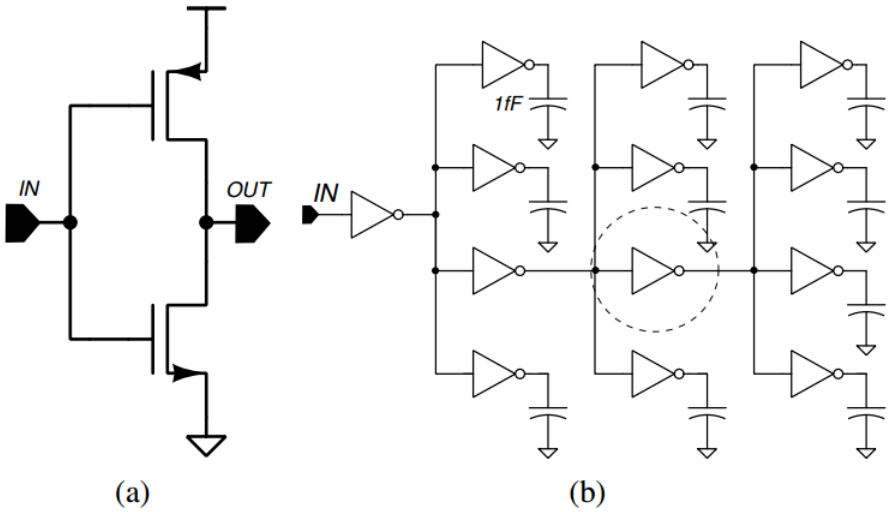
Standard Cell Methodology is a design method for application-specific integrated circuits (ASICs) based in the interconnection of logic gates to conform devices in system on a chip (SoC).The initial design is developed at the transistor level. In this work, the bottom level is created and analyzed, based in a schematic view generated with a Electronic Design Automation tool which transform the schematic (grahphical) view to the netlist. Later, a simulation profile is created to observe the electronic behavior of the circuit by an analysis of its time domain response. A prediction of the parameters can be seen through the simulation, such as maximum speed, delay times and power consumption. Standard Cell Methodology allows to route power and ground as well as substrate and well connections in a fashion that makes connecting the MOSFETs together simpler. These cells are full-custom realized with fixed-height and variable-width.

A Standard Cell library is a grouping of low-level electronic digital gates. The principal aspect with these libraries is that they are of a fixed height, which enables them to be placed in rows, easing the process of automated digital layout. In this library are included two types of digital cells: statics and dynamics. The Statics Cells are composed by the digital gates: NAND, NOR, NOT and a D-type static FF. Meanwhile, the Dynamic Cells are composed by two class of D-type FFs designed for high frequency. This paper shows the process performed to design and create the Standard Cell library focused in the procedure performed to the FFs. A brief description of the digital gates and its performance and characteristics will be made.

In this work, all simulations are made including a delay metric process which allows to see the behavior of the circuits and designs under conditions of charge at the

input and the output, this process is known as fan-out of 4 (FO4) and it consists in arrays of four inverters in cascade with the goal of that the indicated device be analyzed. An inverters based model of FO4 is shown at the Fig 4 (b).

Figure 4. (a) Schematic view of an inverter, (b) FO4 Process in an inverters array



The characteristics shown below describe the maximum frequency with two type of simulations which use two models to run the simulations: schematic (spectre) and post-layout (extracted). These simulations are analyzed in the worst speed case corner SSLL (Slow, Slow, Low temperature, Low supply voltage) with a FO4 process. In the case of the inverters, there are two types of models: the designed with regular VTH transistors and the designed with low VTH transistors. The lvt transistors reach a most high frequency but have a major power consumption[3].

2.1. NOT GATE

The inverter or NOT gate is the most basic gate which composes a digital library. This gate allows characterize the mobility ratio of the electrons which compose the

[3] PELLOUX-PRAYER B, BLAGOJEVIC M and HAENDLER S. *Performance analysis of multi-VT design solutions in 28nm UTBB FD-SOI technology.* SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), IEEE [online]. 2013. [cited 4 August 2015], pp. 1-2, 7-10. Avalaible from: Base de Datos Biblioteca Universidad Industrial de Santander.

transistors channel and consequently the sizes ratio between the two types of transistors. The sizes ratio is used how a base for design of all another cells. The inverters which compose the FO4 process in the post-layout simulation are simulated with its extracted model, which contain the extraction of capacitances and resistances parasitic.

Table 1: Inverters, Maximum frequency

Simulation	**Maximum Frequency [GHz]**							
Force and Type	1x RVT	2x RVT	4x RVT	8x RVT	1x LVT	2x LVT	4x LVT	8x LVT
Schematic View	3.1	3.8	3.6	3.5	4	4.9	4.8	3.9
Post-layout	2.5	3.05	3.1	2.9	3.3	4.05	3.95	3.2

2.2. NAND

The NAND gate is a logic gate that produces an output which is LOW (0) if its inputs are HIGH (1); this gate is known as negative-AND or complementary to the AND gate. The inverters which compose the FO4 process in the postlayout simulation are simulated with its extracted model.

Figure 5: Schematic view of: (a) NAND gate, (b) NOR gate.

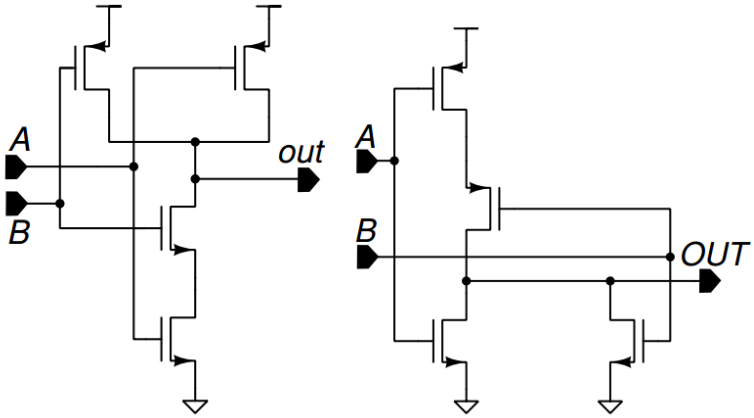


Table 2: NAND and NOR, Maximum frequency

Simulation Type	**Maximum Frequency [GHz]**			
	NAND		**NOR**	
	1x	2x	1x	2x
Schematic View	2.85	3.6	2.5	3.2
Post-Layout (extracted)	2.3	2.9	1.9	2.5

2.3. NOR

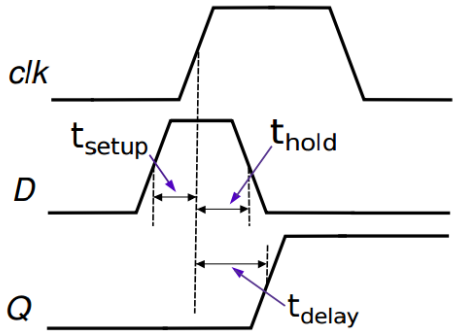
The NOR gate is a logic gate that implements logical NOR. The behavior of this gate is that a HIGH (1) output is the result if both inputs to the gate are LOW (0). The inverters which compose the FO4 process in the post-layout simulation are simulated with its extracted model.

The Flip-Flops and its design, schematics, simulations, behavior and layouts are shown in the next section.

3. FLIP-FLOPS

The library contain three different class of D-type rising edge Flip-Flops (FF), two dynamic: True Single Phase Clock FF (TSPC) and Strong Arm FF (SA). One static: Pass-Gate based D FF. In this section will be described the characteristics, the process of design and the final performance of these FFs.

Figure 6: Time Diagram for setup time, hold time and delay time.



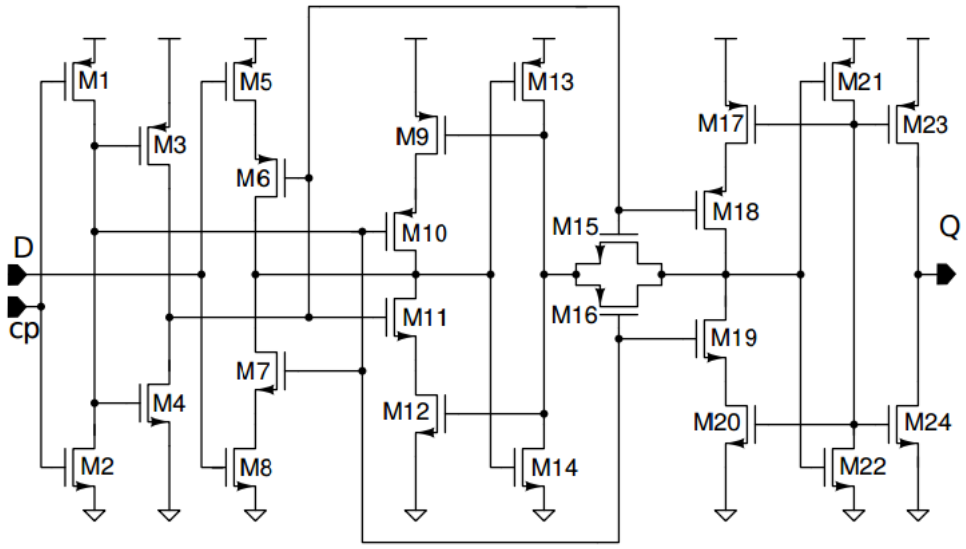
3.1. PASS-GATE BASED D FF

The Pass Gate Based D Flip-Flop (PGDFF) is designed to obtain a balanced output with equally delay times in both cases falling edge and rising edge and is mainly composed by inverters. An inverter is used to negate the clock in order to control the activation of a set of triestate inverters allowing to keep the output data until the input changes. The pass-gate or transmission-gate controls the passage of the signal to the latch in order to save the value of the D data or to impose a high impedance node to hold the previous. In other words the objetive is to obtain an output signal which take the input value when occur a rising edge in the clock using the transistors size such as natural multiples of the inverter 1x.

PGDFF is designed by defining the mobility ratio between the N-type and P-type transistors considering most part of the circuit is based on inverters. This mobility ratio defines the size of the transistors which compose the inverters. Once

dimensions are fixed, setup simulation based on fan-out-of 4 (FO4) is used to validate the design. FO4 allows to simulate the circuit under process-independent delay metric and to include load conditions.

Figure 7: PGDFF Schematic.



Inverters simulation shows that the variations in the sizes of the transistors by means of fingers increased slightly the operation frequency and the load capacity causing a bigger self capacitance. The design searches to obtain high operation frequency without increasing the self capacitance therefore initial sizes given by the mobility ratio and the invertir_1x are maintained.

Figure 8: PGDFF Inverters composition

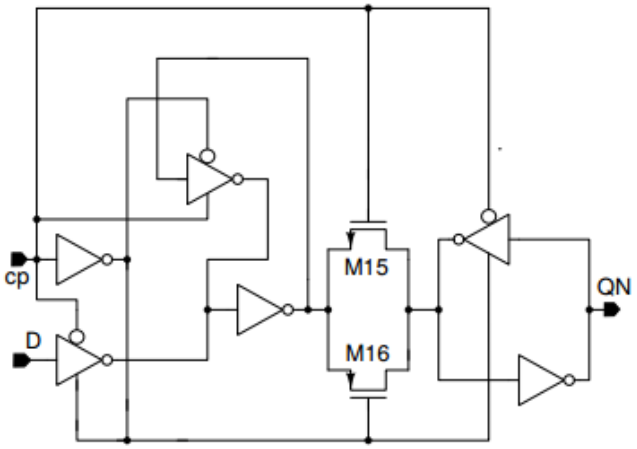
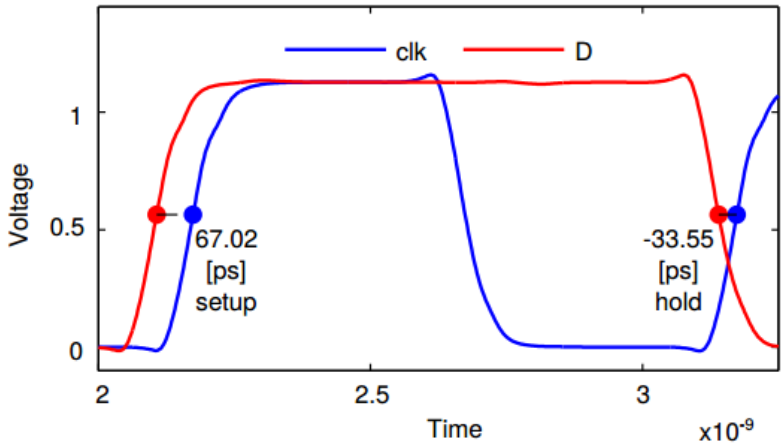
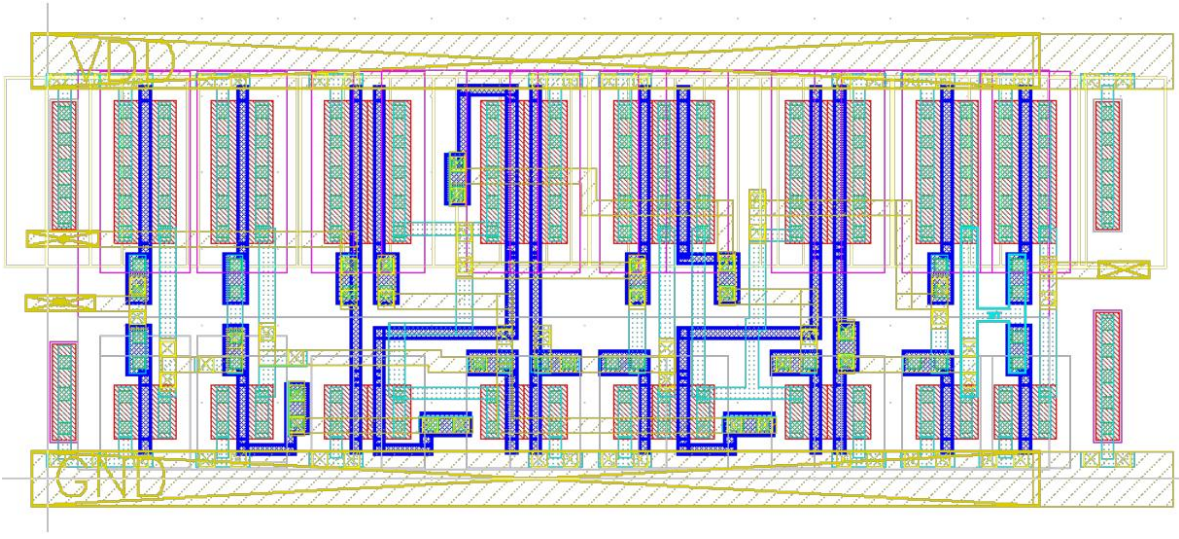


Figure 9: Setup and hold time of the PGDFF



The layout in the Fig. 10 shows the placement and area consumption by the transistors. The layout model is made through of a Standard Cell methodology which allows to connect the bottom-level circuits between them by means of a digital flow synthesis. The fixed height of the cell is defined by twelve tracks of metal2 used to make the horizontal connections, getting a height of 4.72um between the rails VDD and GND. The connections between layers are made with a minimum of two contacts or vias depending of the case with the objective of avoiding malfunction due to manufacturing errors and reducing the resistance in the transitions of layers.

Figure 10: Layout of the PGDFF



A post-layout simulation with the extracted parameters is performed to see the maximum frequency, the power consumption (Table 4), the balanced output (Fig. 18 and 19), and the setup and hold time (Fig. 9) of the FF.

3.2. TRUE SINGLE PHASE CLOCK FLIP-FLOP

The designed True Single Phase Clock FF (TSPC) in this work based its operation on a single-phase clock simplifying the “hold-time path”[4]. The advantage of this FF is that not changes such as delays in the clock appears before arriving to the transistors Gate terminal.

The behavior of the TSPC can be analyzed in different instants according to the states of the clock and/or input data signal. For example, when the clock signal is zero, the initial stage (M1, M2, M3 and M4) has a inverter behavior, thus the voltage at A node has now the value of negated clock, in this moment M2 is turn on by the same clock and M3 by the connection between B node and VDD through M8. When a rising edge occurs, the stage composed vertically by the transistors M13 to M16 gives the data to a ”data keeper” composed by the transistors M17 to M24 holding the data until a new value at input is loaded. In other words, the initial part of the circuit allows the input of data when the clock signal is zero. The middle part of the circuit delivers the value to a data keeper which operates like a Latch. When the clock is zero, the input is disconnected. Thus, the A node always has the negated input. The B node is always to VDD, except when the D input is 0 and the clock is 1; in this case the B node is changing from 1 to 0. This behavior can be seen in Table 3[4].

[4] KIM Yejoong, JUNG Wanyeong, LEE Inhee. *A Static Contentio-Free Single-Phase-Clocked 24T Flip-Flop in 45nm for Low-Power Applications.* Solid-State Circuits Conference Digest of Technical Papers (ISSCC) IEEE International [online]. San Francisco, CA, 2014, [cited 7 September 2015]. ISSN: 0193-6530, Print ISBN: 978-1-4799-0918-6. Avalaible from: Base de Datos Biblioteca Universidad Industrial de Santander.

Table 3: Truth Table of critical nodes in TSPC FF

cp	D	net1	net2	net1b
0	0	1	1	Floating
0	1	0	1	Floating
1	0	1	1 -> 0	1
1	1	0	1	1

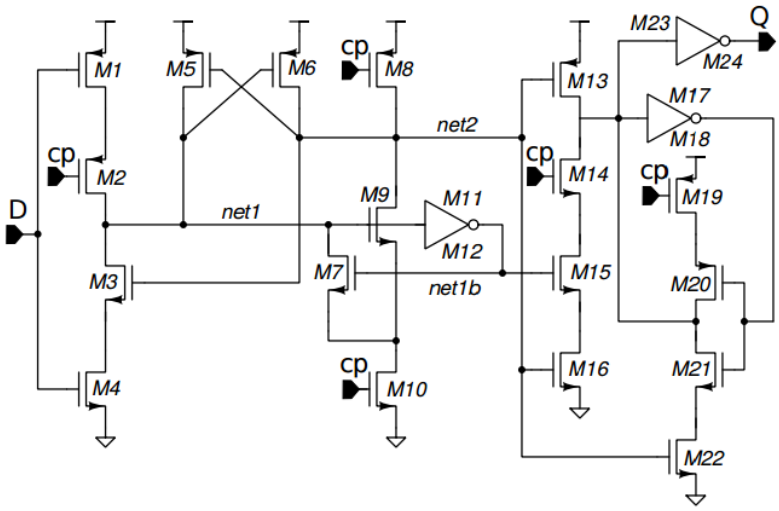
The methodology of design uses a initial model based on one finger transistors, minimum length (130nm) and the widths used in the PGDFF is proposed. Transistors with cascode connections increase the output resistance, as a result of this, the slope changes in current are reduced causing a lower slew rate that limits the maximum work speed[5]. For this reason, the transistors of the initial and middle zones must have a growth in their size to balance it and reduce the output resistance of these transistors. With this design, a simulation profile is performed to obtain high frequency operation. Exceeding slightly the higher frequency reached, the follow step is observe the expected behavior of the important internal nodes in the circuit such as connections between transistors which compose the main route, identifying those who do not comply with the expected behavior and get better it by means of changes in the fingers quantity of these transistors. It is good to clarify that a better performance in speed by causes a grown in the power consumption as evidenced in Table IV.

In the design phase, M8 and M13 satisfy a very important function due to them have the responsibility of send or keep the B node values to 1 for all moments except when a rising edge in the clock occurs. The design ends when a frequency

[5] JING Zhang. *A Low-Power and High Slew-Rate CMOS Voltage Follower.* Machine Vision and Human-Machine Interface (MVHI) [online]. International Conference on, Kaifeng, China, April 2010. [cited 4 September 2015], pp. 210-213. Avalaible from: Base de Datos Universidad Industrial de Santander.

above 5GHz is reached due to that this value of frequency meets the expectations of speed.

Figure 11: Schematic view of TSPC FF.



The Layout of the circuit is made in two rows due to that the size of the transistors is longer for only one row if a square structure is desired. On the other hand if the Fig. 11 is seen, some PMOS transistors (M5, M6, M8) do not have a cascode connection with a similar type, unlike NMOS transistors in the same branch (M9, M10 and M3, M4), as a result of this, the horizontal length occupied by NMOS transistors is greater than the occupied by PMOS transistors, this is observed in the bottom zone in the Fig. 12.

A post-layout simulation with the extracted parameters is performed to see the maximum frequency, the power consumption (Table 4), the balanced output (Fig. 18 and 19), and the setup and hold time (Fig. 13) of the FF.

Figure 12: TSPC FF Layout

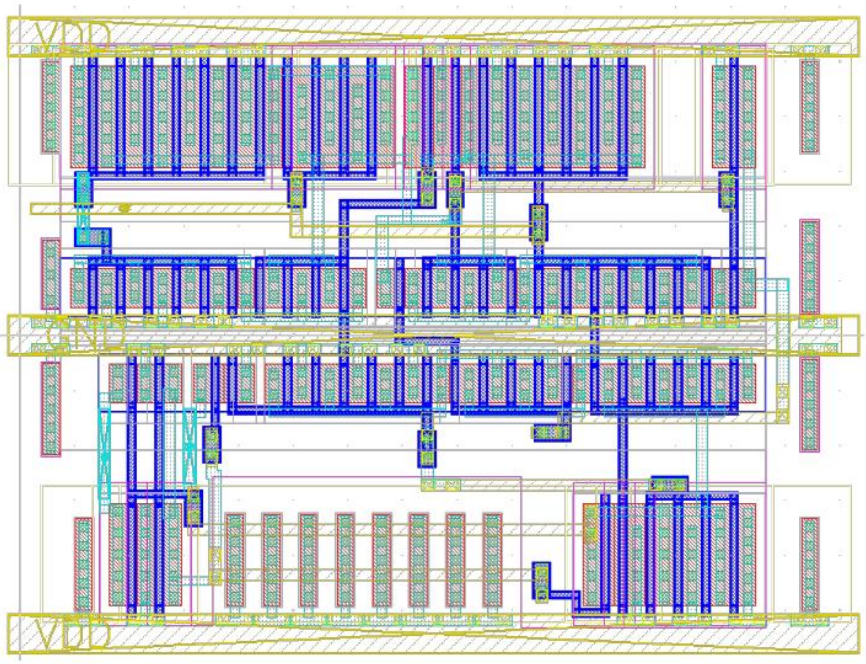
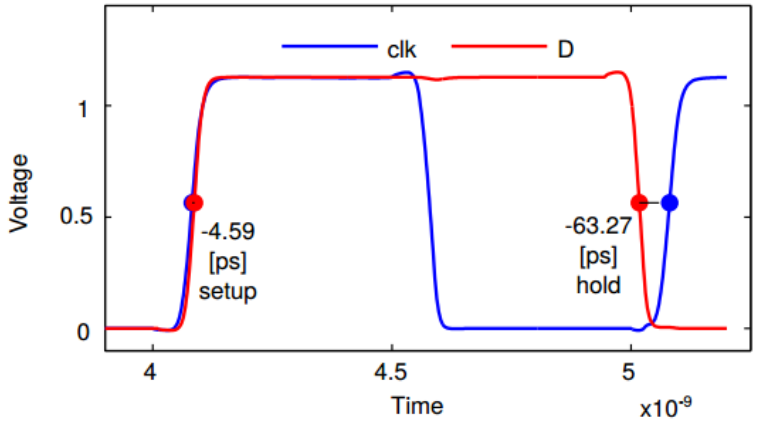


Figure 13: Setup and hold time, TSPC FF



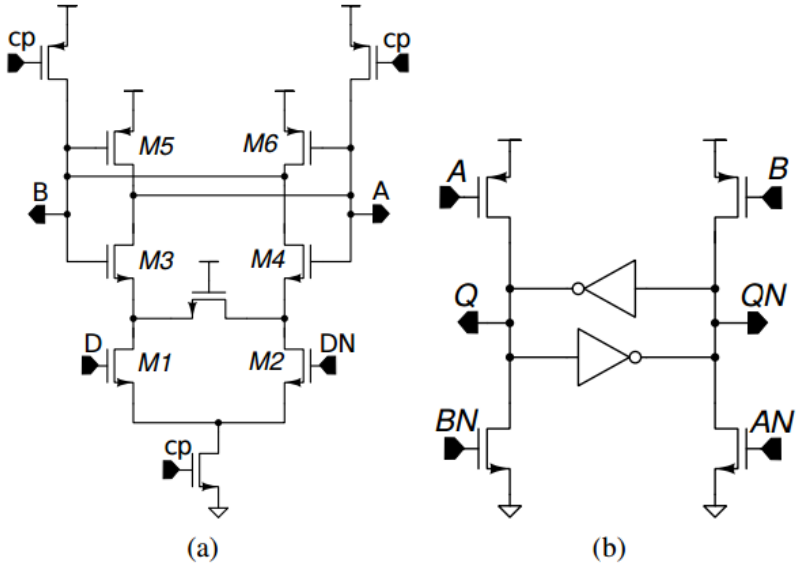
3.3. STRONG ARM FLIP-FLOP

The Strong Arm (SA) FF, shown in Fig. 14, is composed by a differential pair controlled by clock signals principally[6]; the SA FF can be use like a regenerative comparator because it is a differential amplifier circuit. Regenerative means that it

[6] KAWAI Natsumi, TAKAYAMA Shinichi and MASUMI Junya. *A Fully Static Topologically-Compressed 21-Transistor Flip-Flop With 75% Power Saving.* IEEE J. of Solid-State Circuits [online]. November 2014, vol. 49, no. 11 [cited 2 October 2015], Avalaible from: Base de Datos Universidad Industrial de Santander.

takes small signals and responds to any variation, so the FF sends the data to a high or a low; high and low are the two stability zones of SAFF, in which, theoretically only exists a metastability point (the middle). The differential pair has a big problem due to its balanced design, the mismatch errors which causes differences between the two outputs signals of the M1 and M2 transistors. This unbalance can generates offset voltage in the circuit.

Figure 14: Schematic view of Strong Arm FF.



The behavior of SAFF is based in the output amplified signal of M1 and M2. The differential current of M1 and M2 unbalances the cross coupled inverters composed by the M3, M4, M5 and M6 transistors, causing it to regenerate on this unbalance. Regeneration causes one MOSFET in each inverter be turn OFF, thus a current flow choking off path through M1 and M2. Consequently M1, M2 and the tail MOSFET are forced into deep triode[7]. The differential output given by the regenerative comparator reaches the desired data but the data are not kept, as a result besides the differential pair is necessary to implement a topology that allows to keep data until that a desired change occurs in the output of the comparator. A

[7] ABIDI A. and XU Hao. *Understanding the regenerative comparator circuit.* Custom Integrated Circuits Conference (CICC), IEEE Proceedings of the [online]. Sept. 2014, [cited 1 October 2015], pp. 1-8, 15-17. Avalaible from: Base de Datos Universidad Industrial de Santander.

versatile and useful design was found, this circuit shown in the Fig. 14(b), offers advantages like it consumes zero static power, it directly produces rail-to-rail outputs and the most important: its input-reffered offset arises from primarily one differential pair[8].

Statistically, a big size reduces the changes produced by the mismatch errors and increases the probability that the same quantity of errors occurs in the two transistors[9]. This big sizes in the input make necessary to increase the size of the tail's transistor and inverter's transistors too, because these must endure the current generated by the input transistors and balance the circuit. As a result of increase the size of the transistors, the power consumption of the circuit increases too as can be seen in the Fig. 16 and table 4, due to this the design of layout must be done with precaution considering the current flow through M1 and M2 transistors. However, this increase in the size helps to get better the force of the change unto a high or low, making that the FF reaches a higher maximum speed.

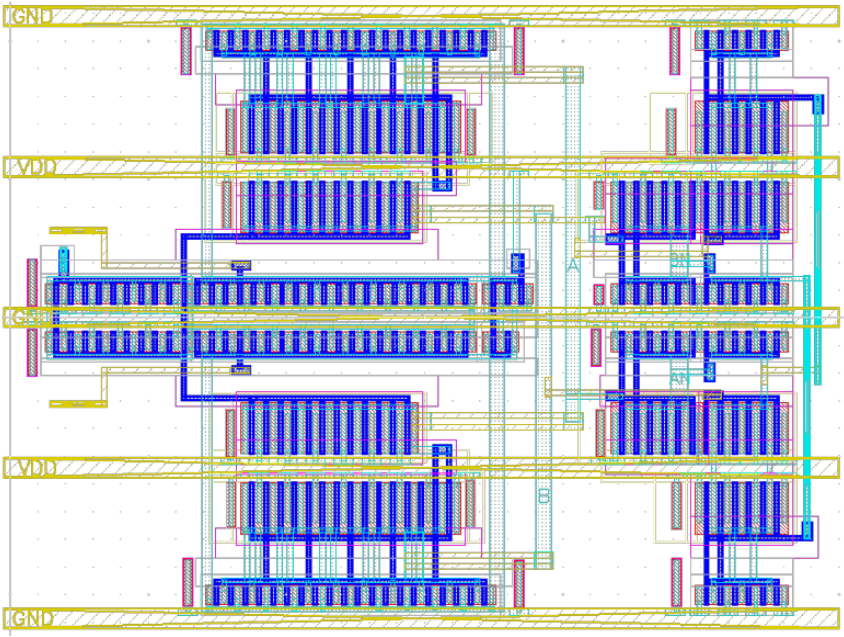
Before made the layout of SAFF was necessary observe the maximum current (Fig. 16) between two critical nodes with the purpose of consider the current density at the metal layers. This simulation was made in the highest speed corner: FFHH at maximum frequency (4.7GHz) (Fast, Fast, High temperature, High voltage).

The Layout of the SA was made under certain conditions, before, the careful that must be taking account with the currents density through the layer metals was named; moreover is necessary take account that due to the size of transistors and the Standard Cells disposition, for convenience, all the devices shouldn't be

[8] RAZAVI B. *The StrongARM Latch [A circuit for All Seasons].* IEEE Solid-State Circuits Magazine [online]. June 2015, vol 7, Issue 2 [cited 27 September 2015], pp. 12-17. Avalaible from: Base de Datos Universidad Industrial de Santander.
[9] JEPPSON K. *Comments on the metastable behavior of mismatched CMOS latches.* IEEE J. of Solid-State Circuits [online]. 1996, vol. 31, no. 2 [cited 12 October 2015], pp. 275-277. Avalaible from: Base de Datos Universidad Industrial de Santander.

located in an only space between VDD and GND, because the Layout's length would be bigger than the Layout's width. As a result, a square form is searched, the layout was designed with three GND's rails and two VDD's rails which form four spaces between them, where the transistors of the design can be put how is shown in the Fig. 15.

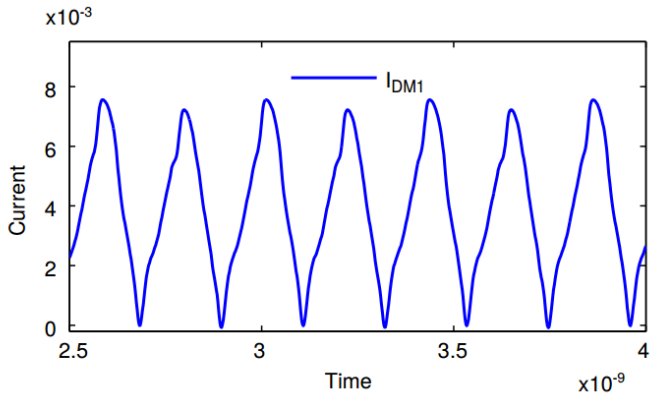
Figure 15: Strong ARM FF Layout.



The symmetry in the design of SA and the latch was utilized at the moment of make the layout, the symmetry of the layout is given by the central GND rail. For instance comparing the layout shown in Fig. 15 with the schematic view shown in Fig. 14, the layout disposition was made in such a way that the left schematic part belong to the top layout zones, while the right schematic part would the bottom layout zones. In the layout view, the left zone corresponds to the regenerative comparator and the right zone has the inverters of the output comparator signals and the latch. Also in the layout view is observed that the metal layers which correspond to the connections between the input amplifier transistors are made

with a metal layer more width than normal, taking in account the maximum current supported density of the metal for this technology.

Figure 16: Maximum current in the critical node at the FFHH corner and 4.7 GHz of the StrongArm Flip-Flop



A post-layout simulation with the extracted parameters is performed to see the maximum frequency, the power consumption (Table IV), the balanced output (Fig. 18 and 19), and the setup and hold time (Fig. 17) of the FF.

Figure 17: Setup and hold time of the StrongArm FF.

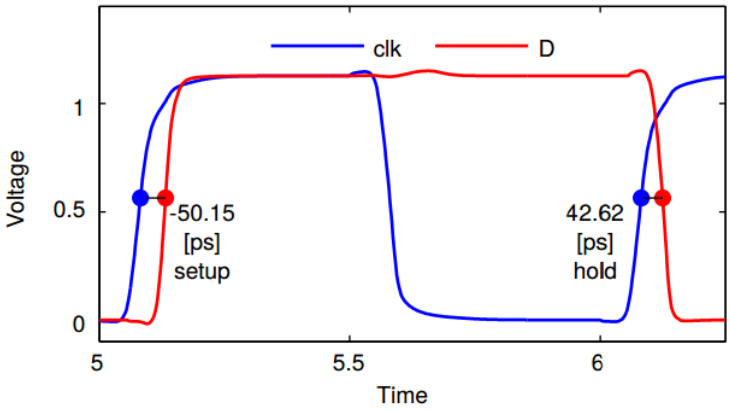


Table 4: Post-Layout Characterization Data of All FFs

FF	f_{max} SSLL [GHz]	P_{consum} at f_{max} FFHH	t_{delay} rising SSLL	t_{delay} falling SSLL	t_{setup} SSLL [ps]	t_{hold} SSLL [ps]	Layout Area [umxum]

		[pW/Hz]	[ps]	[ps]			
PGD	2.8	0.1146	300.76	308.55	67.02	-33.55	6.16x14.88
TSPC	4.45	0.2392	120.81	147.19	-4.59	-63.27	11.16x15.55
SA	4.7	1.0126	145.72	139.64	-50.15	42.62	22.48x30.2

Figure 18: Delay times in rising edges for all FF's

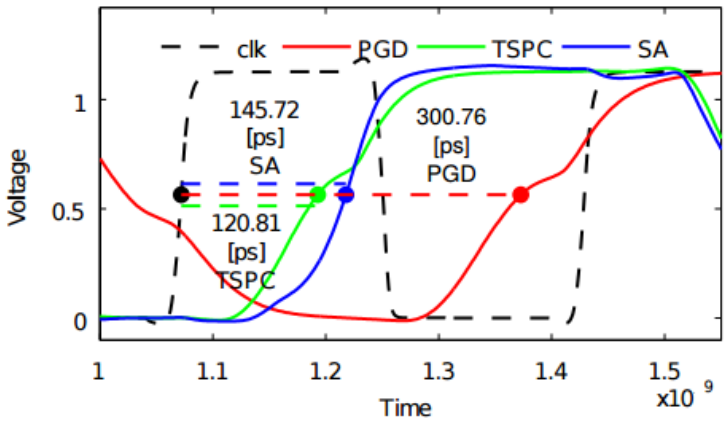
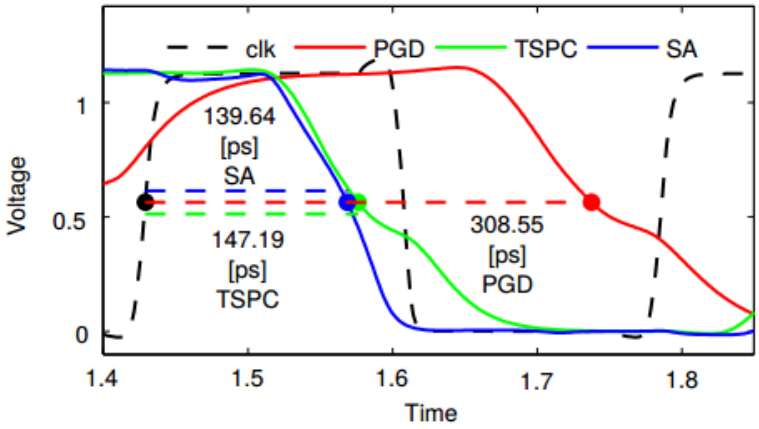


Figure 19: Delay times in falling edges for all FF's



4. APPLICATION

The fixed-height in the cells enables that the library be placed in rows, easing the process of automated digital layout. A typical standard-cell library contains the following files: a full layout of the cells, spice models of the cells, hardware description (verilog model or HDL-VIT model), parasitic extraction models, DRC rule decks and symbols. From this files, various information may be captured in a typical formats which contain information about the cell layouts for automated placed and route tools.

4.1. CRC16

A cyclic redundancy check (CRC) is an error-detecting code. There are different orders of CRC depending of the bits quantity that can be processed. Mathematically a CRC16 has a 16 bits polynomial responsible of divide the input data in 16 bit frame in order to obtain the residue of this operation, this residue is known as check sum (CS). Later, the CS is put at final of the input data and this value is divided by the CRC16's polynomial. If the residue is equal zero, then the frame data arrived correctly. In this work a CRC16 is presented, the CRC16 can implement any types of polynomial, like a CRC16ANSI or CRC16CITT.

The circuit of the CRC16 (Fig. 20) is implemented by means of sixteen D-FFs connected in cascade; in the moment of the division between the data and the characteristic polynomial, a subtraction is realized through XOR gates which change the data. The design have a XOR gate in the input of each FFs, this XOR gates are activated by means of an NAND gate array in the XOR input, this activation depend of the desired polynomial type. The NAND gates array have two inputs which allows define the XOR gates activated. The two inputs of the array are a polynomial which corresponding to a only value to each model of CRC16 and the last bit of the data in the output since the last FF. The output of each FF corresponds to one bit of the 16 bits data or CS.

4.2. DIGITAL FLOW (SYNTHESIS)

The configured flow used in this work has two main parts:

1) Configuration script in where the library, the geometric description of the cells, time description and parasitic extraction are charged. This script use the hardware descriptions where the behavior of the desired circuit to synthesize is described. Furthermore the script have proper commands of the synthesis and the desired reported results like time restrictions, used cells, used area, power consumption described in leakage and dynamic potency for each cell, netlist, among others.
2) Restrictions: Generally, there are sequential (like FFs) and combinational circuits causing a final delay. In this section the following parameters are defined: the clock period, the clock incertidumbre due to causes like jitter or noise, rising and falling edge, capacitive charge for each output, final delay time in which clock arrives to inputs. These declarations are made to verify the maximum operation frequency of the circuit.

The Layout view shown in Fig. 21 have two CRC16, one noise generator and one signal generator.

Figure 20: Block diagram of the CRC16

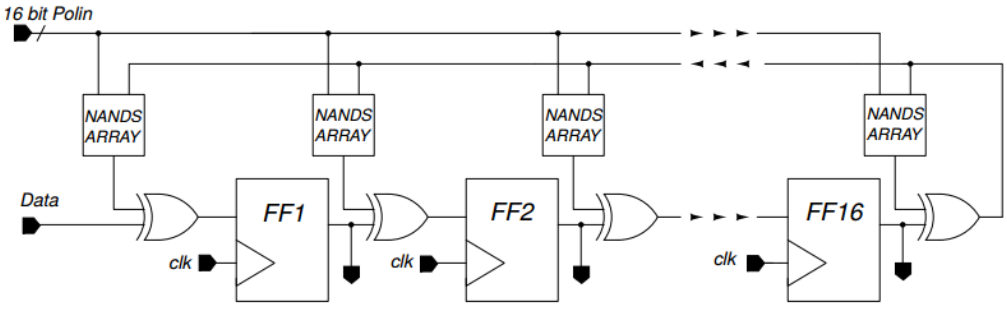
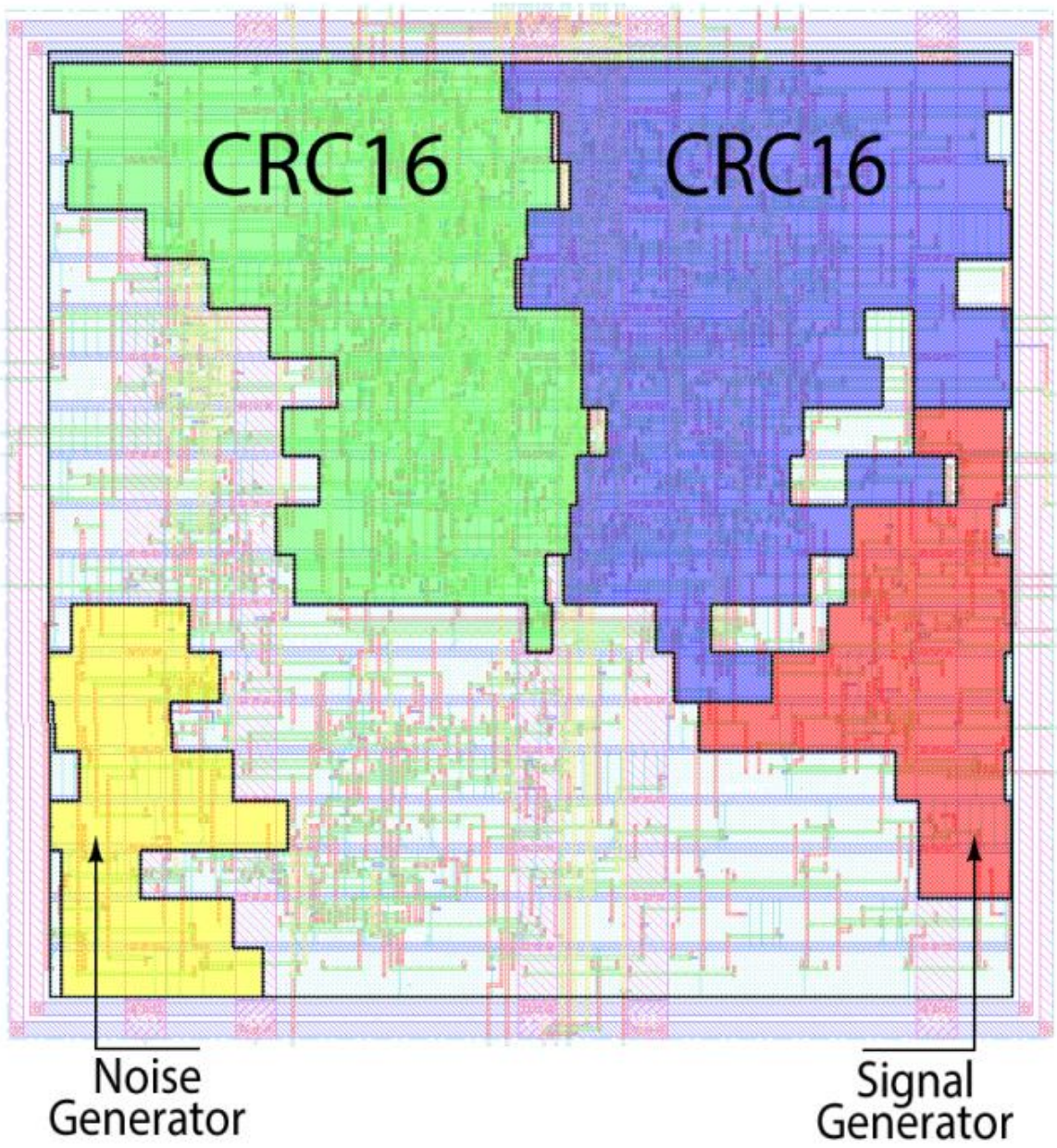


Figure 21: Final Layout of CRC16



5. CONCLUTION

A rise in the maximum frequency of the TSPC and SA FFs is obtained reaching the high frequency band, the substantial rise in the maximum speed of these circuits contrasts with the rise in the power consumption which reaching the scale of mW. All values were evaluated through a corner's analysis for the worst possible scenario for each case: frequency and power consumption. In addition to the frequency improvements, these two FFs have shorter delay times in comparison with the PGDFF. However the PGDFF is ideal to be used in lesser speed circuits because it have a lesser power consumption. The considerable influence of the parasitic capacitance and parasitic resistance in the behavior of the circuit was seen, for example in the maximum frequency of the digital gates which was reduced around 20% comparing the schematic simulation with the post-layout simulation.

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