Design of a 1 MHz Self-Trimmed RC-Based Oscillator in 28 nm CMOS Technology for Low-Power Applications

Joan Sebastian Torres Poveda

Angel Ricardo Castro Jaimes

Degree work presented as a requirement to qualify for the title of

Electronic Engineering

Advisor:

Alex Julian Mantilla Rios

Ingeniero Electrónico.

Co-Advisors:

Javier Ferney Ardila Ochoa

Ingeniero Electrónico. PhD.

Jaime Guillermo Barrero Perez

Ingeniero Electrónico. M.Sc.

Universidad Industrial de Santander

Facultad de Ingenierías Fisicomecánicas

Escuela de Ingeniería Eléctrica, Electrónica y de

Telecomunicaciones

Bucaramanga

2026

To our family, partners, teachers, friends and the onchip research group:

we dedicate this one to you.

Acknowledgments

First and foremost, I want to thank God for giving me life, and my parents for instilling in me principles and values, for walking beside me through every stage of my personal growth, and for giving me the will to pursue my dreams and never give up. To my partner, Erika, thank you for experiencing this entire journey by my side; for your company during those long nights and for encouraging me through every assignment, project, and achievement that led me to this point. To Bonnie and Luna, for your companionship during the difficult moments and for showing me that there is always more than one path to reach the goal.

I would also like to thank my director and friend, Alex, for teaching me that there are no obstacles in our way, only opportunities to learn—and there certainly were plenty. Thank you for your patience, mentorship, and friendship. To Jorge, Angel for the talks and Q&A sessions where work felt like play, making this whole process much more comfortable. To the Onchip Research Group, thank you for providing a "competitive family" that motivated me to strive and learn more day after day, and for the professional environment and those "outings" that were anything but professional. Finally, I would like to dedicate this document to my good friend, David Astro, who unfortunately did not finish this journey with us. He taught me that life is short and must be enjoyed.

Thanks to each and every one of you, I close this chapter of my life today.

with appreciation, **Joan Sebastian Torres Poveda**

Acknowledgments

I would like to dedicate this work, to God, to my mother, and to my father, who provided me with the tools, to walk this path and become an engineer. Without their guidance, effort, and unconditional love, this achievement would not have been possible.

To my Nonita Rafaela, my aunt Ruth, my aunt Judith, my cousin Ian, and my aunt Claudia, thank you for sharing with me part of your lives, your resources, your advice, and your wisdom, both in joyful moments and in difficult times.

To my friends José and Santiago, partners and colleagues in this academic journey, thank you for helping me successfully complete this degree.

To Professor Javier, who in the Fundamentals course helped me understand that everything we learn has a real and practical purpose, giving meaning to every effort invested; to Mr. Alex, Jorge, and Joan, thank you for your patience and willingness to help me understand the challenges presented by this project, as your guidance was key to overcoming every obstacle; and to the OnChip research group, for showing me a way of working different from what is traditionally taught in Colombia, demonstrating that there is no fixed ceiling to learning and that, even in a field as rigorous as engineering, there is not always absolute certainty about what is considered established.

Throughout this process, I was also fortunate to have understanding and patient supervisors as Leidy, Diana, and Javier in the post-graduate department, as well as the support of my friends Óscar and Argemiro, who provided me with opportunities that once seemed distant. Thanks to them, I was able to broaden my perspective of the world and of my own capabilities.

To my little sisters, Valentina and Sofía, who were a constant motivation to stay on the right path. I hope this experience inspires them to pursue their dreams and to continue being exactly how they are.

with appreciation, **Angel Ricardo Castro Jaimes**

Content

List of Figures

List of Tables

List of Appendices

Resumen

Titulo: DISEÑO DE UN OSCILADOR BASADO EN RC AUTOAJUSTABLE DE 1MHZ EN TECNOLOGÍA CMOS DE 28nm PARA APLICACIONES DE BAJO CONSUMO. *

Autores: JOAN SEBASTIAN TORRES POVEDA, ANGEL RICARDO CASTRO JAIMES. **

Palabras Clave: OSCILADOR, MICROELECTRÓNICA, MICROCONTROLADOR, SoC, SEMICONDUCTORES, DIGITAL, BAJA POTENCIA, AUTOAJUSTE, REFERENCIA DE RELOJ.

Descripción:

Los osciladores de relajación basados en RC (RCO) han demostrado ser una alternativa eficiente a los osciladores de cristal, ofreciendo ventajas en términos de tamaño, consumo de potencia y tiempos de arranque. Un diseño apropiado puede mejorar la estabilidad frente a variaciones de temperatura, voltaje y procesos de fabricación, haciéndolos adecuados para una amplia gama de aplicaciones de baja potencia. Este trabajo se centra en el diseño de un oscilador de relajación en tecnología CMOS de 28nm, como parte de la microarquitectura que está desarrollando el grupo de investigación OnChip. A partir de un análisis de sensibilidad de los parámetros no ideales , se implementó un mecanismo de ajuste digital (trimming) para compensar las variaciones de Proceso, Voltaje y Temperatura (PVT) . La validación del circuito se demuestra a través de simulaciones esquemáticas, logrando la frecuencia objetivo de 1.048 MHz con un error medio del 0.9334 % en análisis de Monte Carlo , ocupando un área total de 0.0069 mm^2.

---

* Trabajo de grado

** Facultad de Ingenierías Fisicomecánicas. Escuela de Ingenierías Eléctrica, Electrónica y de Telecomunicaciones. Director Alex Mantilla Rios

Abstract

Title: DESIGN OF A 1MHZ SELF-TRIMMED RC-BASED OSCILLATOR IN 28nm CMOS TECHNOLOGY FOR LOW-POWER APPLICATIONS. *

Authors: JOAN SEBASTIAN TORRES POVEDA, ANGEL RICARDO CASTRO JAIMES. **

Keywords: OSCILLATOR, MICROELECTRONICS, MICROCONTROLLER, SoC, SEMICONDUCTORS, DIGITAL, LOW POWER, SELF-TUNING, CLOCK REFERENCE.

Description: RC-based relaxation oscillators (RCOs) have proven to be an efficient alternative to crystal oscillators, offering advantages in terms of size, power consumption, and startup times. A proper design can improve stability against variations in temperature, voltage, and manufacturing processes, making them suitable for a wide range of low-power applications. This work focuses on the design of a relaxation oscillator in 28nm CMOS technology, as part of the microarchitecture being developed by the OnChip research group. Driven by a sensitivity analysis of the circuit's non-ideal parameters , a digital trimming mechanism was implemented to compensate for Process, Voltage, and Temperature (PVT) variations . The circuit validation is demonstrated through schematic simulations, achieving the target frequency of 1.048 MHz with a mean error of 0.9334 % in Monte Carlo analysis , while occupying a total area of 0.0069 mm^2.

* Trabajo de grado

** Facultad de Ingenierías Fisicomecánicas. Escuela de Ingenierías Eléctrica, Electrónica y de Telecomunicaciones. Director Alex Mantilla Rios

Introduction

In the context of ultra-low-power embedded systems, designing energy-efficient, compact, and adaptable oscillators remains a primary challenge. There is a burgeoning demand for clock-generation solutions capable of delivering stable, tunable signals across multiple System-on-Chip (SoC) subsystems while maintaining a rigorous balance between power consumption, silicon area, and performance. However, conventional architectures face significant hurdles when scaling to advanced CMOS nodes. Specifically, they often suffer from aggressive Process, Voltage, and Temperature (PVT) variations that compromise frequency stability, elevated leakage currents that penalize energy efficiency, and the substantial silicon area required for integrated passive components, which complicates the high-density integration required by modern systems.(Gomez et al., 2019).

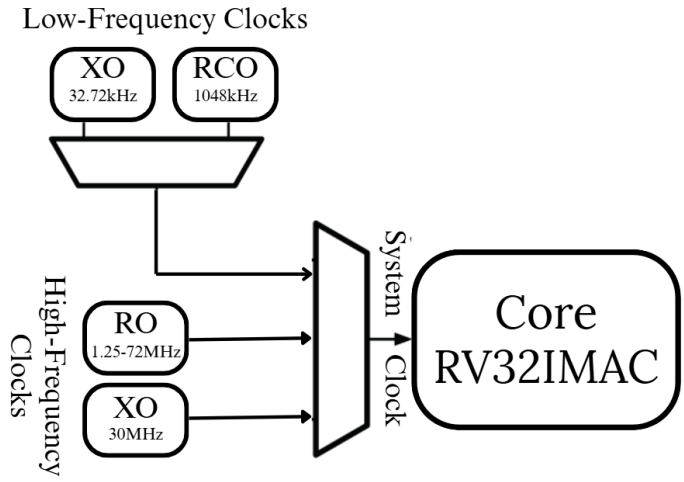
Relaxation Oscillators (RCOs) are attractive candidates for fully integrated clock sources because they avoid the area and integration challenges associated with LC oscillators and generally provide better voltage and temperature (V–T) stability than ring oscillators (ROs). (Anand et al., 2017). The oscillation period of an RCO is primarily determined by a timing resistor (R), a capacitor (C), and a reference voltage (V_{ref}), which enables a simple architecture with inherent frequency tunability.

Generally, when a SoC is in a low-activity state, the total power consumption depends largely on the quiescent power and the frequency stability at which it is operating in this state. For this reason, low-frequency crystal oscillators (XCOs) are commonly employed as off-timers due to their excellent long-term and temperature-related frequency stability. Nevertheless, XCOs typically consume power in the microwatt range or higher, and the need for an external crystal increases both system cost and printed circuit board area (Sebastiano et al., 2009)(Moreno & Sepúlveda, 2024). These drawbacks make crystal-based solutions unsuitable compared to other topologies for this type of applications. As an alternative, RC-based relaxation oscillators can be employed; however, their frequency variation must be carefully minimized to ensure a reliable clock signal (Griffith et al., 2014).

This work focuses on the design of one of the primary clock sources as part of the development of a complete low-power SoC microarchitecture in 28 nm (Arenas Peñuela, 2018; Gomez et al., 2019). The proposed system incorporates multiple clock references to support different operating modes and performance requirements, as illustrated in Figure 1.

Figure 1

Clock Architecture of the Proposed Low-Power SoC.



By reducing the technology node and power consumption, the proposed approach enables the implementation of more compact embedded systems with greater autonomy, suitable for operating in energy-constrained environments such as Internet of Things (IoT) devices, wearable electronics, and implantable medical systems. Furthermore, a key technical feature of RCOs is their ability to dynamically modulate frequency. While this design focuses on a fixed frequency, this versatility allows the performance of the SoC blocks to be adjusted in response to process, voltage, or temperature (PVT) variations, laying the groundwork for versatile power management in future applications. To overcome the lack of absolute accuracy typical of RC structures, the design incorporates a clipping technique used to minimize frequency instability and ensure signal reliability, and a dynamic tuning system based on a phase-frequency detector (PFD) and a charge pump, allowing the oscillator to adapt to different SoC performance requirements.

1. Objectives

1.1. General Objective

To design a relaxation oscillator with automatic trimming using 28nm CMOS technology.

1.2. Specific Objective

To model and simulate the RC oscillator to validate the behavior of the overall circuit.

To design and validate a relaxation oscillator at transistor level using PVT corner simulations and Monte Carlo analysis to ensure compliance with circuit specifications.

To develop an RC oscillator layout targeting an area of less than 0.05mm^2, complying with industry manufacturing standards to ensure fabricability.

2. Specifications and System Architecture

2.1. Specifications

To characterize the specifications of the RC oscillator, a review of literature and previous works in the field was conducted. Several studies address key parameters such as oscillation frequency, average power consumption, supply voltage, operating temperature, and start-up time. Table 1 summarizes the main parameters to be considered during the design process. Therefore, a proper understanding of each specification is essential to ensure stable and reliable oscillator operation.

Table 1

RC Oscillator Design Targets.

Parameters	**Units**	**Design Target**		
		Min	**Typ**	**Max**
V_{DD}	V	0.8	0.9	1
Temperature	°C	-40	27	125
Frequency	kHz	-	1048	-
Area	mm^2	-	0.05	-
Avg. Power	μW	-	TBM	-
Start-up Time	μs	-	TBM	-

The primary function of an RCO is to provide a low-frequency reference clock signal for systems in which high-frequency clock references are not required. It is commonly used in low-power applications and during sleep or idle modes, where reducing power consumption is a priority. A good RCO ensures that the output clock frequency remains within specified limits despite fluctuations in the supply voltage (VDD) and temperature (T) , providing a predictable timing reference under varying operating conditions.

2.2. Analysis

"A normal relaxation oscillator uses an error amplifier to generate a pulse that charges and discharges an RC bank. The oscillator frequency depends on the discharge of the capacitor by the resistor and the reference" (Arenas Peñuela, 2018). As shown in Figure 2. Similarly, M2 is charged when the clock signal (VCLK) signal is low. In this state, Vc must be greater than the error amplifier (OP1) reference voltage VREF. Note that Vc is connected to the non-inverting input of the OP comparator and VREF is connected to the inverting input.Then VCLK changes state and starts to grow as Vc rises. It then begins to discharge through the resistor until Vc approaches VREF, reducing the output signal of the error amplifier, charging the capacitance and restarting the loop.

Figure 2

RCO Architecture.

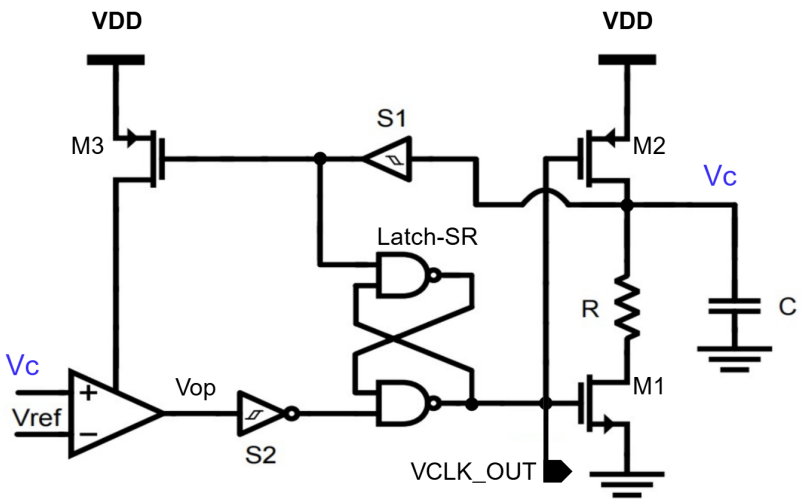
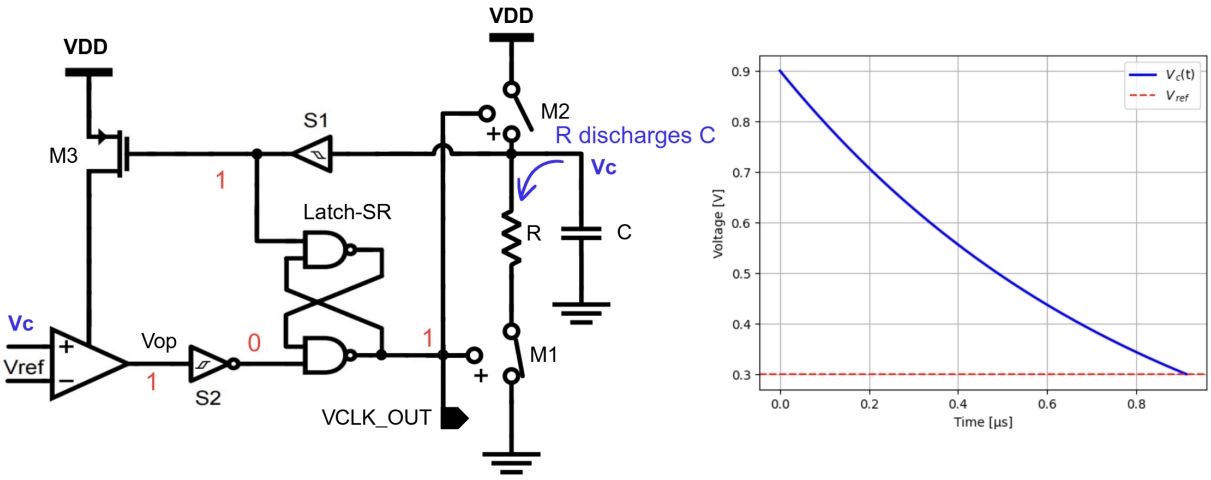


Figure 3

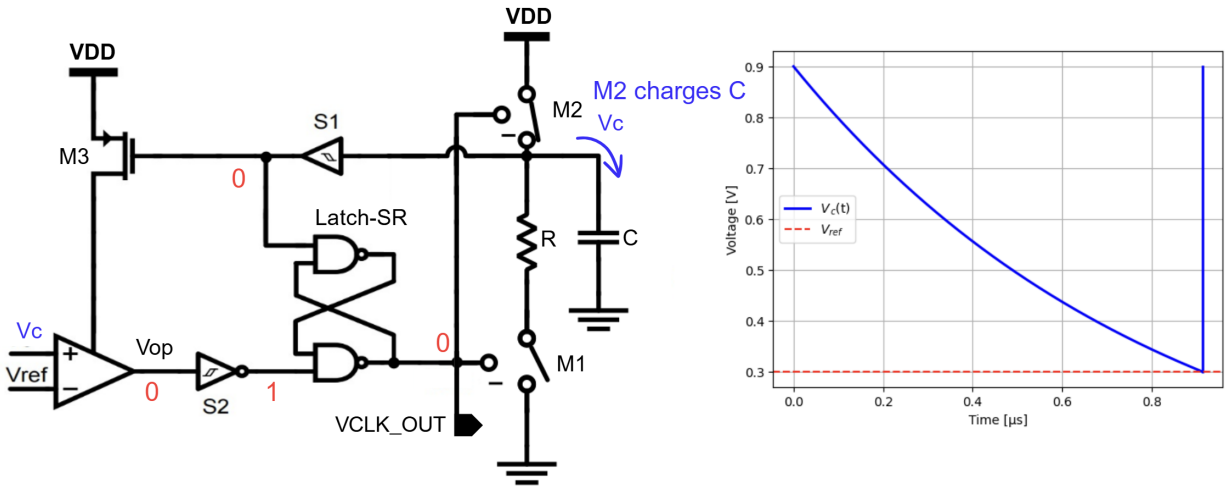
Relaxation Oscillator CLK High.



"The error amplifier only needs to operate when Vc is close to VREF. This feature allows the amplifier to be turned off for the remainder of the cycle time." (Arenas Peñuela, 2018). Therefore, the Schmitt trigger (S1) has a switching point close to VREF and, through M3, controls the turn-on or turn-off of OP1, so that OP1 is only activated when the comparison needs to be performed. OP1 is active for a short time, generating the VOP signal (difference of the comparator inputs). For the rest of the cycle, VOP is pulled high to keep VCLK high. "It is also worth noting that the Schmitt Trigger (S2) has a switching point close to the power supply" (Arenas Peñuela, 2018). So that it changes its value only when OP1 is turned off, thus avoiding charging disturbances. Once VOP is low enough, VCLK turns on the load transistor (M2) and the corresponding Schmitt trigger signal (S1) turns off OP1. Finally, a NAND-based latch adjusts the propagation delays between the on and off loops to avoid metastability glitches.

Figure 4

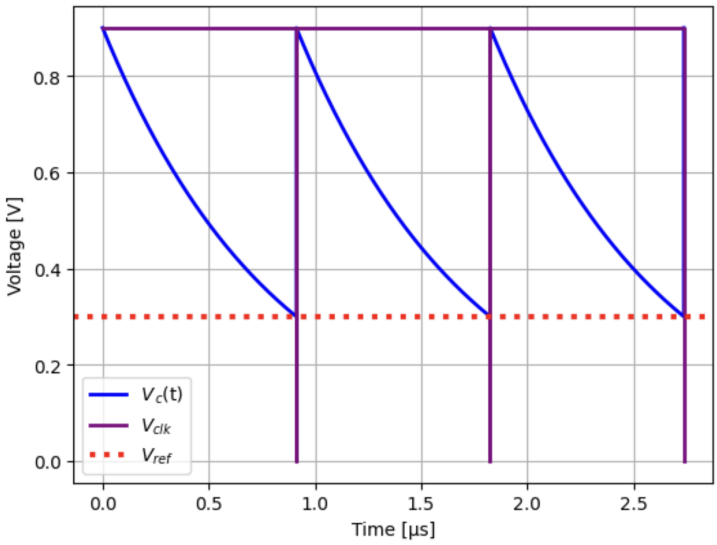
Relaxation Oscillator CLK Low.



In Figure 5, an approximation of the RC oscillator capacitor discharge is presented, serving as a basis for deriving an analytical expression for the oscillation frequency. The transient considered involves the capacitor discharging from an initial voltage of V_{DD} to the reference voltage V_{ref}, assuming an ideal instantaneous response due to the zero resistance of the switching element. Since the initial analysis was carried out using ideal models for all components, the result can be considered an approximation. Therefore, the curves are intended for illustrative purposes and do not reflect practical values. Finally, Equation (4), provides the resulting expression for the oscillation frequency.

Figure 5

RC Oscillator: Capacitor Voltage and Clock Signal.



$$V_C(t) = V_0 \cdot e^{-\frac{t}{RC}}$$

$$V_{\text{ref}} = V_{\text{DD}} \cdot e^{-\frac{t}{RC}}$$

$$t = RC \cdot \ln\left(\frac{V_{\text{DD}}}{V_{\text{ref}}}\right)$$

$$f \approx \frac{1}{RC \cdot \ln\left(\frac{V_{\text{DD}}}{V_{\text{ref}}}\right)} \tag{4}$$

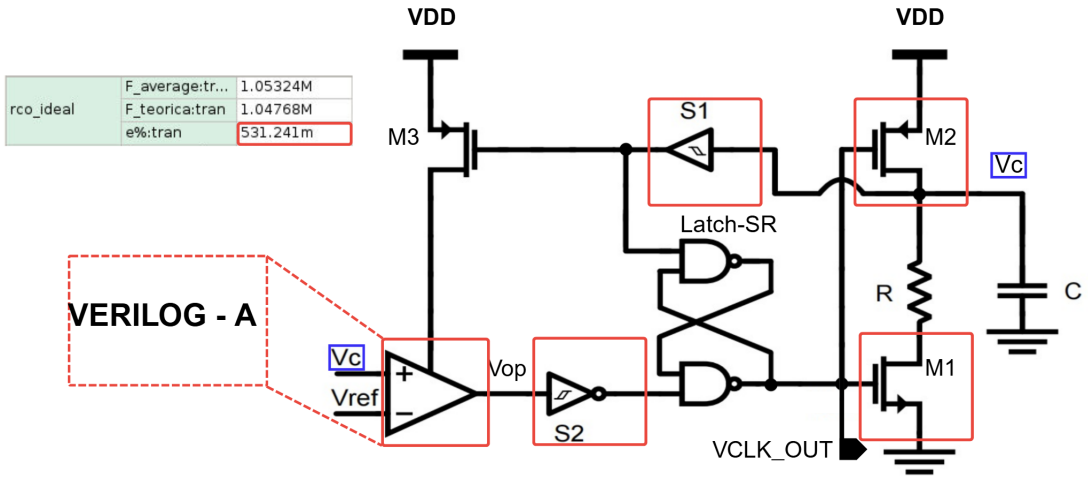
2.3. Modeling

After the initial analysis, in which (4) was derived assuming ideal behavior for all system components, various non-idealities that may directly impact the system's operation were subsequently incorporated. The following section describes the procedure used to include these non-idealities in (4). Once the modified equation was obtained, simulations were

performed to validate the model through Verilog-A, yielding a maximum error of less than 1 % as can be seen in Figure 6.

Figure 6

Validation of the mathematical model through Verilog-A.



2.4. Comparator Offset and Gain

Taking (4) into account, it can be observed that the comparator threshold voltage ideally corresponds to the reference voltage. However, this threshold can be directly affected by the input offset voltage of the operational amplifier, resulting in a shift with respect to the ideal reference. Additionally, the finite open-loop gain of the comparator introduces an extra deviation in the effective threshold voltage. To account for this effect, the gain-dependent term is incorporated into the threshold voltage analysis.

As the open-loop gain increases, a smaller (i.e., closer to zero) differential input voltage is required to drive the comparator into saturation. This behavior can be described by the ideal open-loop relationship of the operational amplifier:

$$V_{op} = A_o \left(V^+ - V^- \right)$$

The minimum differential input voltage required to trigger the comparator, such that the output reaches the supply rail V_{DD}, is given Equation (6).

$$V^+ - V^- = \frac{V_{DD}}{A_o} \tag{6}$$

Along these lines, it can be stated that both the offset and the gain can be considered as non-idealities that alter the comparator's triggering condition. Consequently, they can be incorporated into Equation (4) as modifications to the original triggering condition, which was previously determined only by V_{ref}.

$$f \approx -\frac{1}{RC \cdot \ln\left(\frac{V_{\text{ref}} - V_{\text{off}} - V_{\text{DD}}/A_o}{V_{\text{DD}}}\right)}$$

2.5. Schmitt Trigger Delays

The initial frequency equation assumes instantaneous charging of the capacitor. As shown in Figure 4, the equivalent impedance at node V_C can be considered infinite—excluding the capacitor itself—due to the intrinsic characteristics of the models. This is because the node sees a very high impedance toward S_1 while M_1 is open, and M_2 is assumed to be an ideal switch with zero impedance. However, when the on-resistance of switch M_2 is taken into account, a finite charging time arises. This charging time can be approximated as $5\,R_{\text{onM2}}C$, corresponding to five time constants of the RC charging network(5τ).

This charging interval is governed by the intrinsic switching delay of the Schmitt trigger S_2, denoted as t_{d2}. To ensure that the capacitor reaches its maximum voltage, a delay greater than 5τ is intentionally introduced. Since the system experiences two switching events per oscillation period, corresponding to the charging and discharging phases, this delay occurs twice and is therefore included in the period of the generated square wave, as reflected in Equation (8).

$$F \approx \frac{1}{-(RC)\ln\left(\frac{V_{ref} - V_{\text{off}} - \dfrac{V_{DD}}{A_o}}{V_{DD}}\right) + 2\,t_{d2}} \tag{8}$$

2.6. Switches Resistances

Considering that the oscillation frequency depends directly on the resistance seen by the capacitor during its charging and discharging processes, it is necessary to account for the resistance introduced by transistors M_1 and M_2 in the RCO architecture, as shown in Figure 2. Since transistor M_1 is connected in series with the resistor R, its on-resistance can be modeled as an additional term added to the nominal value of R.

In the case of transistor M_2, its on-resistance primarily affects the capacitor charging phase and is therefore taken into account when determining the maximum capacitor voltage. This effect is incorporated by analyzing the capacitor charging process, starting from an initial voltage equal to the reference voltage, modified by the previously discussed terms.

$$f \approx \frac{1}{-(R + R_{\text{onN}})\, C\, \ln\left(\frac{V_{ref} - V_{\text{off}} - \frac{V_{DD}}{A_o}}{\left(V_{th} - V_{\text{off}} - \frac{V_{DD}}{A_o}\right) e^{-\frac{t_{d2}}{R_{\text{onP}} C}} + V_{DD}\left(1 - e^{-\frac{t_{d2}}{R_{\text{onP}} C}}\right)}\right) + 2\, t_{d2}}$$

2.7. Sensitivity Analysis

After modeling the circuit, a sensitivity analysis was performed in order to identify which non-idealities have the greatest impact on the circuit performance. Based on the definition of sensitivity presented in (Sedra & Smith, 2015) a script, provided in Appendix 1, was developed to compute the partial derivatives of the design equation with respect to all relevant variables, including circuit components and non-ideal parameters. The normalized sensitivity of the oscillation frequency with respect to the Resistance is given by (10) (Joint Committee for Guides in Metrology, 2008; National Institute of Standards and Technology, n.d. Taylor & Kuyatt, 1994).

$$\frac{\Delta f}{f} \approx \left(\frac{R}{f}\frac{\partial f}{\partial R}\right)\frac{\Delta R}{R} \tag{10}$$

Equation (10) indicates how sensitive the circuit's frequency is to changes in a particular resistance. In other words, it allows us to quantify how a small variation in the value of R translates into a proportional change in the frequency f.

Due to their length and complexity, the complete set of partial derivatives is presented in Appendix 2. As an illustrative example, we include the partial derivative of the frequency with respect to the resistance, as given in equation (11):

$$\frac{\partial F}{\partial R} = \frac{C \log\left[\frac{V_{\text{off}} - V_{\text{TH}} + \frac{V_{\text{DD}}}{A_0}}{V_{\text{DD}}\left(\exp\left(-\frac{t_{d2}}{CR_{\text{ONP}}}\right)-1\right)+\exp\left(-\frac{t_{d2}}{CR_{\text{ONP}}}\right)\left(V_{\text{off}} - V_{\text{TH}} + \frac{V_{\text{DD}}}{A_0}\right)}\right]}{\left(2t_{d2} - C \log\left[\frac{V_{\text{off}} - V_{\text{TH}} + \frac{V_{\text{DD}}}{A_0}}{V_{\text{DD}}\left(\exp\left(-\frac{t_{d2}}{CR_{\text{ONP}}}\right)-1\right)+\exp\left(-\frac{t_{d2}}{CR_{\text{ONP}}}\right)\left(V_{\text{off}} - V_{\text{TH}} + \frac{V_{\text{DD}}}{A_0}\right)}\right]^2\right)(R + R_{\text{ONN}})} \tag{11}$$

Table 2

System Sensitivity Analysis

Parameter	**Ideal Value**	**Value Obtained**	**Sensitivity**	**abs Sensitivity**
R [Ω]	7,6920E + 05	−1,152	−8,66E − 01	0,8657
R_{ONN} [Ω]	400	1,152	4,50E − 04	0,0005
R_{ONP} [Ω]	400	8,3490E − 45	3,26E − 48	0,0000
C [F]	1,08E − 12	−8,2121E + 17	−8,66E − 01	0,8661
V_{REF} [V]	VDD/3	2,6934E + 06	7,89E − 01	0,7891
V_{OFF} [V]	−1,00E − 02	−2,6934E + 06	2,41E − 02	0,0241
V_{DD} [V]	0,9	−8,9780E + 05	−7,89E − 01	0,7891
A_0 [V/V]	316,22	2,4242E + 01	7,49E − 03	0,0075
td_2 [s]	49E − 09	−1,9259E + 12	−9,22E − 02	0,0922

Table 2 presents the conducted sensitivity analysis, which shows that the parameters R, C, V_{REF}, and V_{DD} exhibit the highest sensitivity. This suggests that the oscillator's frequency can be significantly affected by variations in these parameters.

3. Technology Characterization

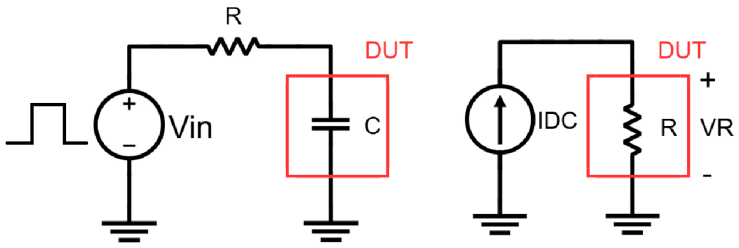
The design was implemented using a 28 nm CMOS technology and the corresponding TSMC PDK. The oscillator is expected to operate with a 0.9 V supply voltage,which is the typical VDD for low-voltage devices available with this technology.

To perform an accurate measurement of the capacitance, an RC network was implemented using an ideal resistor with a fixed and known value as is shown in Figure 7. By measuring the time constant, $C = \tau/R$, the corresponding capacitance value was obtained. Subsequently, PVT simulations were carried out to determine the variations in the capacitance.

In the case of the resistor, a DC current source with a known and fixed value was used to measure the corresponding voltage across the device. From this measurement, the resistance value was obtained from Ohm law $R = VR/IDC$. Finally, PVT simulations were performed to analyze its variations.

Figure 7

Testbenches for Passive Component Characterization.



3.1. Transistors

The design utilizes 'ch-mac' MOSFETs, specifically selected for their lower threshold voltage (V_{th}) and optimization for 0.9 V operation. Nevertheless, the adoption of minimum channel lengths introduces critical design trade-offs: it increase sensitivity to Process, Voltage, and Temperature (PVT) variations, intensifies short-channel effects (SCE), and inherently restricts the open-loop gain in amplifier-based topologies.

3.2. Selection of Resistors and Capacitors

Given that the frequency of our oscillator depends heavily on the capacitor and resistor, and considering process, voltage, and temperature (PVT) variations, it is essential to perform a selection process to ensure the use of passive components that minimize these variations while optimizing area during the validation procedures for fabrication.

In the context of our 28 nm CMOS technology, it is necessary to characterize the two fundamental passive components of the oscillator's RC circuit: resistors and capacitors.

For the available technology, capacitors can be classified into two main types: *MOM-CAP* and *CH18*. The *cfmom_mx_4t* and *cfmom_wo_mx* models were discarded from the first category because they require a considerable area to obtain the same capacity per area ($872\mu m^2$, $733\mu m^2$) and complicate routing due to their interaction with the guard ring. Similarly, the *CFMOM_WO_RF_110G* capacitor was excluded due to its limitations regarding supply variations (0.73 %), while other devices in this family require additional layers whose functionality is not clearly documented.

Regarding *CH18* capacitors, although alternatives exist, they all belong to the standard (core) line; therefore, adding extra layers to the manufacturing process would not be justified from either an economic or a design perspective.

Regarding resistors, those using metal layers were discarded due to their low resistivity. Similarly, the *rpod*, *rnodwo*, *rnod*, *rpmg*, and *rnmg* variants were excluded due to their high area consumption ($299\mu m^2$, $423\mu m^2$, $423\mu m^2$, $313\mu m^2$, $360\mu m^2$) per resistor. Finally, the *rnwod* and *rpodwo* resistors were also rejected because they exhibit significant variations to changes in temperature (22.5 %, 18.75 %).

Finally, the selected capacitor was the one with the *cfmom-wo_rf* ($467\mu m^2$, 0.00014 %) rating, and the *rupolym_m* ($59.93\mu m^2$, 3.22 %) resistor was chosen for its balance between area and resistance, as well as variations in stability and reliability in response to changes in temperature and voltage. Likewise, in table 3 below summarises the information described in this subsection.

Table 3

Summary of Resistors and Capacitors.

Component	**Name**	**Area [μm^2]**	**Temp. Variation [%]**	**Supply Variation [%]**
Capacitor	cfmom_mx_4t	872	1,23	0,00098
	cfmom_wo_mx	733	1,17	0,000982
	cfmom_wo_rf_110g	235	0,98	0,73
	cfmom-wo_rf	467	1,12	0,00014
Resistor	rpod	299	26,92	≈ 0
	rnodwo	423	25,54	≈ 0
	rnod	423	27	≈ 0
	rpmg	313	2,28	≈ 0
	rnmg	360	5,08	≈ 0
	rnwod	423	22,5	0,0065
	rpodwo	300	18,75	≈ 0
	rupolym_m	59,93	3,22	≈ 0

4. Static Comparator Design

A relaxation comparator compares any input signal to a predefined threshold voltage. This defines a digital output (low or high) depending on whether the threshold is exceeded. In this case, the comparator is used to determine the oscillator's switching point, i.e. the minimum discharge point of the capacitor. Note that this threshold is an external reference voltage equivalent to:

$$Vref = \frac{VDD}{3}$$

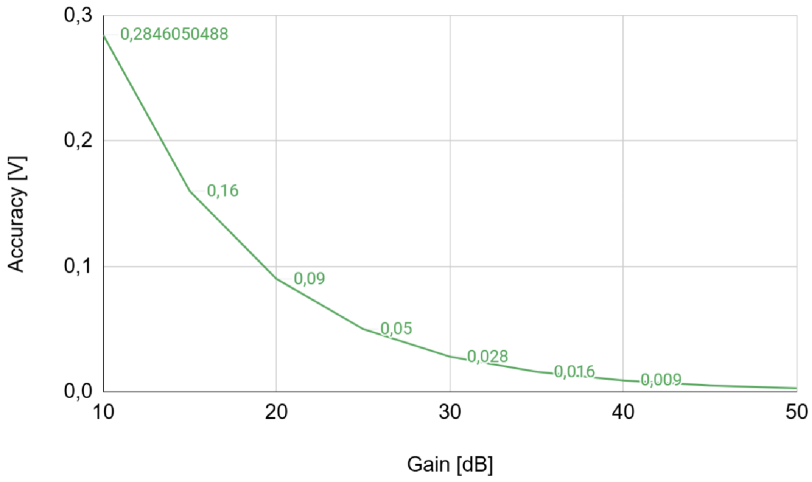
4.1. Open Loop Gain

The open-loop gain Ao determines the sensitivity of the comparator to small changes in the input. Ideally, the comparator would switch exactly when the inputs are equal; however, in practice, the finite gain introduces a deviation in the effective threshold. The effect of this on the oscillator frequency was previously explained in Section 2.3.1. Based on equation (6) and Figure 8. we can guarantee an accuracy of 2,84 mV.

Figure 8

Gain against accuracy.

Gain [dB]	Accuracy [mV]
10	284,6
15	160
20	90
25	50
30	28
35	16
40	9
45	5,06
50	2,84



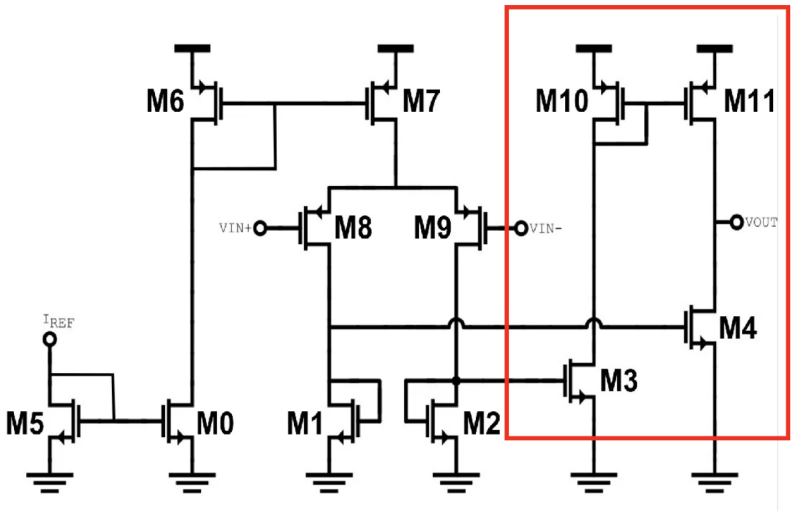
This means that the comparator is able to distinguish voltage differences at its inputs of up to 2.84 mV to perform a switching at its output. For a system operating with a signal range of 0.6 (discharge from 0.9V to 0.3V), this resolution represents an accuracy error of only:

$$Error\,\% = \frac{2{,}84mV}{300mV} \times 100 \approx 0{,}85\,\%$$

Likewise, in Figure 9 the topology used to implement the static comparator can be observed, and In equation 14 you can see the expression given for the open loop gain.

Figure 9

Schematic of the comparator, highlighting in red the transistors that contribute most to the gain.



$$A_o = gm_4 gm_8 \left(\frac{1}{gm_1} \parallel ro_8 \right) (ro_4 \parallel ro_{11}) \tag{14}$$

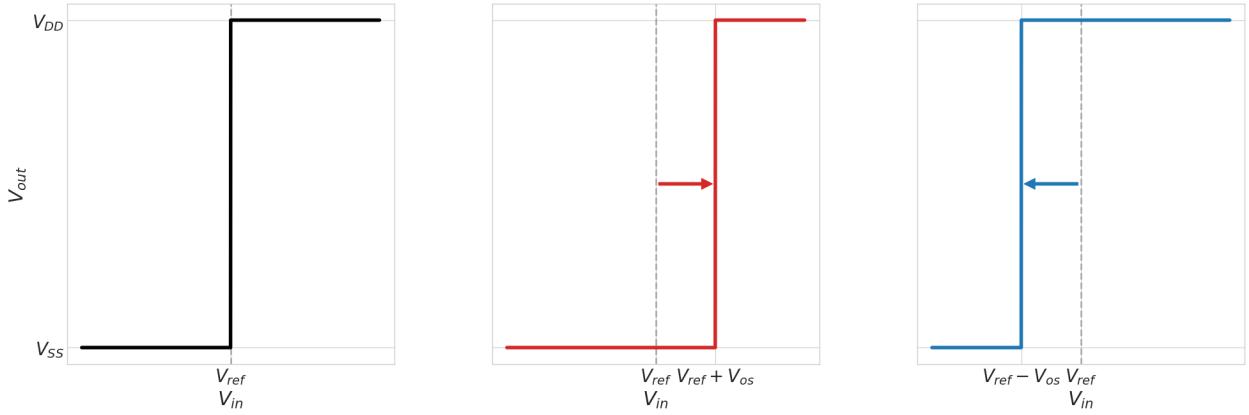
4.2. Input Offset Voltage

This phenomenon manifests as a shift in the switching point relative to the ideal reference. Physically, the offset *Vos* results from manufacturing imperfections, such as mismatches between the transistors in the input differential pair. For design analysis, this effect is modeled as an additional voltage source in series with one of the inputs, forcing the actual differential voltage to be higher or lower to compensate for this error and cause the output to change state.

For the oscillator, this results in a phase shift in the switching time, which can be either leading or lagging. This directly affects the signal period and inversely affects the frequency. Figure 10 illustrates this:

Figure 10

Contribution of the frequency offset.



4.3. Frequency Response and Unity Gain Bandwidth

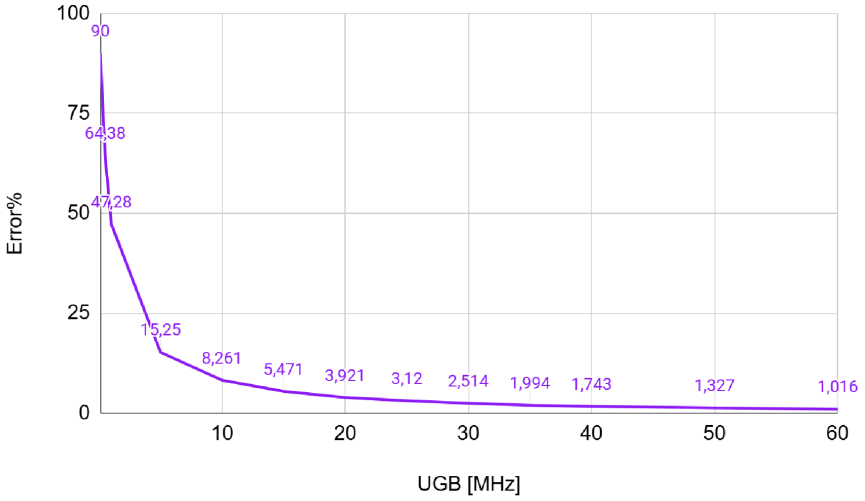
The unity-gain bandwidth (UGB) must exceed the frequency of the most dominant pole to ensure the amplifier maintains a predictable, constant response within the operating range without premature roll-off. Furthermore, maintaining a flat-band gain at least ten times the oscillation frequency is critical for signal fidelity and stable gain, as it minimizes phase shift and prevents amplitude attenuation, thereby ensuring that the output accurately tracks the 1048 kHz signal with minimal simulation error.. Figure 11 shows the results in percentage error of comparing the theoretical frequency (1048 kHz) against the frequency obtained through simulations by varying only the UGB.

$$error\,\% = \left(\frac{theoretical - measured}{theoretical}\right) * 100 \tag{15}$$

Figure 11

Theoretical vs simulated frequency.

UGB [MHz]	error %
0,1	90
0,5	64,38
1	47,28
5	15,25
10	8,261
15	5,471
20	3,921
25	3,12
30	2,514
35	1,994
40	1,743
50	1,327
60	1,016



Based on Figure 11, a minimum UGB of 60 MHz is determined to achieve a percentage error of 1 % which is calculated using the equation 15.

5. Schmitt Trigger Inverter Design

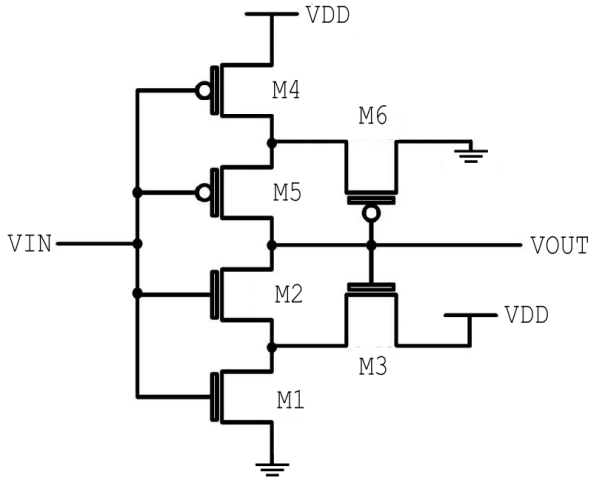
Within the oscillator, two *Schmitt trigger* circuits are implemented. Both circuits share the same architecture and are configured with identical threshold voltages. These circuits are used to control the voltage levels during the charging and discharging processes of the capacitor.

Furthermore, in the system analysis, the threshold voltages defined by the *Schmitt triggers* are used to establish and control the capacitor charging range from 0,3 [V] to 0,9[V].

The architecture employed is presented in Figure (12).

Figure 12

Schmitt Trigger Architecture



5.1. Design of Rising and Falling Threshold Voltages

The design of the *Schmitt trigger* threshold voltages follows the analytical approach presented in (Baker, 2019). According to this methodology, the switching points—specifically the low-to-high (V_{LH}) and high-to-low (V_{HL}) transitions—are determined by the sizing ratios of the transistors in the pull-up and pull-down networks. These points correspond to the moments when the output voltage changes from low to high or from high to low.

In particular, the low-to-high threshold voltage, V_{LH}, is determined by the sizing ratio of transistors M5 and M6, as expressed in Equation 16, while the high-to-low threshold voltage, V_{HL}, is defined by the sizing ratio of transistors M1 and M3, as shown in Equation 17.

The values of these thresholds were selected such that V_{LH} is designed close to the reference voltage V_{REF}, ensuring that the error amplifier is activated only for a short fraction of the oscillation period. Conversely, V_{HL} is designed close to the supply voltage V_{DD} to prevent discharge glitches originating from the operational amplifier OP1.

$$\frac{W_5 L_6}{L_5 W_6} = \left[\frac{V_{LH}}{V_{DD} - V_{LH} - V_{THP}}\right]^2 \tag{16}$$

$$\frac{W_1 L_3}{L_1 W_3} = \left[\frac{V_{DD} - V_{HL}}{V_{HL} - V_{THN}}\right]^2 \tag{17}$$

5.2. Delay's Adjustment

Another important parameter to consider in Schmitt triggers is the rise and fall delay of each stage. From the initial analysis of the oscillator, it was determined that the delay of **S1** must be significantly smaller than that of **S2** to ensure the correct operation of the latch logic. This prevents glitches during transitions and maintains output consistency, thereby guaranteeing the proper functioning of our clock signal VCLK.

In (Baker, 2019), a detailed analysis of these delays was performed, concluding that they depend on the R_{on} of transistors M1, M2, M4, and M5, and expressing them through Equations 18 and 19.

$$t_{DHL} = 0{,}7\,(R_{n1} + R_{n2})\,C_{\text{load}} \tag{18}$$

$$t_{DLH} = 0{,}7\,(R_{p4} + R_{p5})\,C_{\text{load}} \tag{19}$$

Based on these approximations, we can determine a way to control the Ron of the transistors, and consequently the delays of the Schmitt triggers. However, care must be taken when adjusting these values, as modifying them can alter the relative sizing of the transistors, which would in turn affect the threshold voltages.

The Ron of NMOS and PMOS transistors can be approximated as:

$$R_{on,n} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{th})} \tag{20}$$

$$R_{on,p} = \frac{1}{\mu_p C_{ox} \frac{W}{L}(V_{SG} - |V_{th}|)} \tag{21}$$

It is important to clarify that the R_{on} equations were used solely as a reference in

order to understand the relationship between the R_{on} resistances and the transistor sizing.

The delays obtained for the designed *Schmitt triggers* were, for $S2$, a t_{DHL} of 82.93 ns and a t_{DLH} of 37.62 ns, while for $S1$ the obtained values were a t_{DHL} of 3.85 ns and a t_{DLH} of 14.089 ns.This satisfies the requirement that the delay of $S2$ must be greater to ensure the correct operation of the oscillator.

6. Trimming Implementation

Based on the conclusions obtained from the sensitivity analysis, it was determined that the inherent variations in the manufacturing process of the resistors (R) and capacitors (C) significantly impact the circuit's accuracy. Due to this dependence, implementing a automatic trimming system is essential to compensate for deviations and minimize the final error caused by PVT (process, voltage, and temperature) variations. This approach ensures that the circuit maintains its design performance despite environmental and manufacturing fluctuations.

The starting point for this process is the availability of a stable external frequency reference (XTAL_REF), which is assumed to be an ideal input for the system and whose design is not part of this work. It is important to note that this reference should only be active during the oscillator's calibration or trimming phase to optimize power consumption, remaining off during normal circuit operation.

The implemented trimming system consists of several functional blocks responsible for processing the oscillator's output signal and dividing its frequency to approximately 32.76 kHz. This divided signal corresponds to the oscillator being adjusted. To perform the process, the aforementioned reference xtal signal is used, against which the frequency of the divided oscillator is compared to determine and apply the necessary digital adjustment to the C-channel arrays.

The following sections describe in detail each of the blocks that make up the designed trimming system.

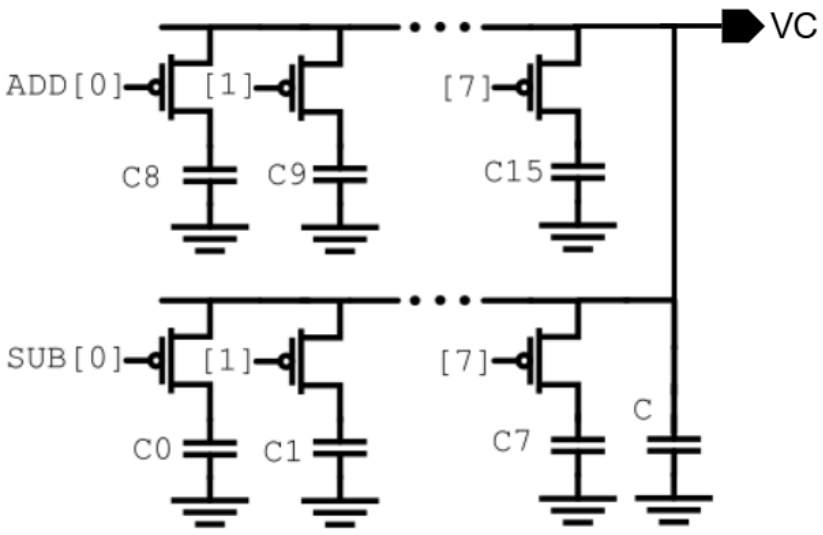
6.1. Capacitor Bank

Since the oscillation frequency of the circuit is strongly determined by the values of the timing resistor and capacitor, a digitally adjustable capacitor bank was implemented. This bank operates using a 8-bit frequency to digital converter (FDC) that system process to generate 16 control bits, where 8 bits function as control signals to increase the capacitance, referred to as *add*, and the remaining 8 bits act as control signals to decrease the capacitance, referred to as *sub*.

The capacitor bank is composed of 16 capacitors connected in parallel as can be seen in Figure 13. The parallel of these 8 capacitors defines a nominal capacitance corresponding to the typical value required for the oscillator to operate at an approximate frequency of 1.048 MHz. The most significant bit provides a coarse adjustment of the capacitance, either increasing or decreasing its value, while the lower-weight bits perform progressively finer adjustments. This hierarchical adjustment scheme allows the capacitance value to converge toward the value required to achieve the desired oscillation frequency. The architecture employed is presented in Figure 13.

Figure 13

Schematic of the Capacitor Bank implementation.



The capacitance values employed for this implementation are detailed in Tables 4 and 5. Table 4 corresponds to a frequency variation compensation of up to -32 %, while Table 5 addresses a variation of up to 64 %. This adjustment is achieved through incremental capacitance tuning; by connecting or disconnecting specific capacitor banks, the core frequency of the system can be precisely increased or decreased.

Table 4

Capacitance Tuning Steps for Negative Frequency Compensation (up to -32 %)

Iter	**Δf/f [%]**	**ΔC nom. [pF]**	**C [pF]**	**C schem. [fF]**
0	-	-	1,007	1008,513
1	-32,0	0,298	0,796	473,805
2	-19,04	0,259	0,498	236,902
3	-10,52	0,109	0,239	118,451
4	-6,43	0,065	0,129	69,648
5	-2,82	0,032	0,065	29,613
6	-1,44	0,016	0,032	14,806
7	-0,7299	0,008	0,016	7,403
8	-0,7299	0,008	0,008	7,403

Table 5

Capacitance Tuning Steps for Positive Frequency Compensation (up to 64 %)

Iter	**Δf/f [%]**	**ΔC nom. [pF]**	**C [pF]**	**C schem. [fF]**
0	-	0,211	1,007	1008,513
1	64	-0,298	0,796	795,841
2	34,56	-0,259	0,498	497,81
3	12,19	-0,109	0,239	238,93
4	6,86	-0,065	0,129	129,44
5	3,31	-0,032	0,065	64,72
6	1,63	-0,016	0,032	32,36
7	0,809	-0,008	0,016	16,18
8	0,809	-0,008	0,008	8,09

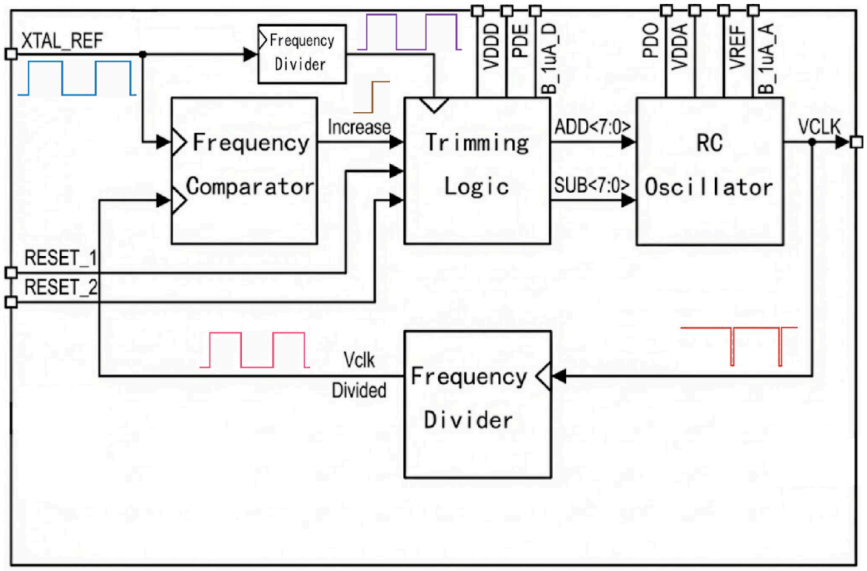
6.2. The Feedback Loop

The signal path used to perform the trimming process is illustrated in Figure 14. Initially, the oscillator clock signal, denoted as *VCLK*, is taken from the oscillator output and passed through a chain of five frequency divider stages to reduce its frequency to a value close to the reference (32.76kHz). The divided oscillator signal is then applied to a frequency comparator, where it is compared against a reference clock signal. The output of the frequency comparator is a digital signal which indicates whether the oscillator frequency must be increased or decreased in order to match the reference.

Instead of directly generating the complete control code, the SAR logic produces specific control bits and flags; these elements are then processed to derive the *ADD* and *SUB* signals, which govern the capacitor bank. This closes the feedback loop and enables automatic frequency trimming. Figure 14 shows the block diagram for the implemented feedback loop.

Figure 14

Simplification of the trimming feedback loop schematic.



6.3. Frequency Divider Implementation

To obtain a suitable clock signal for the comparison process, an asynchronous counter-based frequency divider has been implemented. This stage is crucial for reducing the high-

frequency input signal (1.048 MHz) to a level comparable with that of the precision reference. The implementation uses a chain of T-type flip-flops (TFFs) connected in a cascade configuration. In this structure, the complementary output (QN) of each stage serves as the clock signal for the next stage. Due to the nature of the T flip-flop, where the output changes state on each active edge if the input is high, each block performs an exact division by 2, or its equivalent of dividing the frequency in half (2^1)(Jr. et al., 1992). By connecting n stages in series, the final output frequency is defined by the relationship:

$$f_{out} = \frac{f_{in}}{2^n}$$

6.4. Frequency Comparator Implementation

To ensure that the oscillator operates at the desired frequency, a detection and adjustment system based on a phase and frequency comparator (PFD), a charge pump[1], and a capacitive loop filter has been implemented (Jr. et al., 1992). This block receives two signals: F_{ref}, The stable reference signal of 32,76 kHz. F_{RCO}, The signal coming from the oscillator's frequency divider.

The PFD generates pulses at the UP or DN outputs depending on which signal arrives first (leading or lagging). The width of these pulses is proportional to the phase error between the two signals. The UP and DN signals control a charge pump (CP), which acts as an interface between the digital and analog domains. When the UP signal is activated, the CP injects current into the storage capacitor (C_P), increasing the node (V_{TRIM}). When the DN signal is activated, the CP ejects charge from the capacitor, decreasing this voltage.

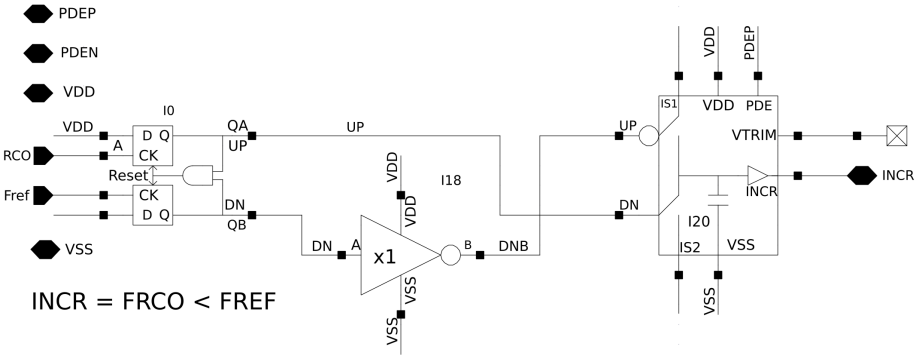
The voltage V_{TRIM} is the parameter that dynamically adjusts the oscillator's behavior. As shown in Figure 15, if the oscillator frequency is lower than the reference frequency ($F_{RCO} < F_{ref}$), the control loop generates an increment signal (INCR) to correct the deviation. This charge injection and ejection process continues until the last bit is defined, and

[1] A simplified version was used because for our particular case we are only interested in 1 or 0.

then it is turned off.

Figure 15

Schematic of the Frequency Comparator.



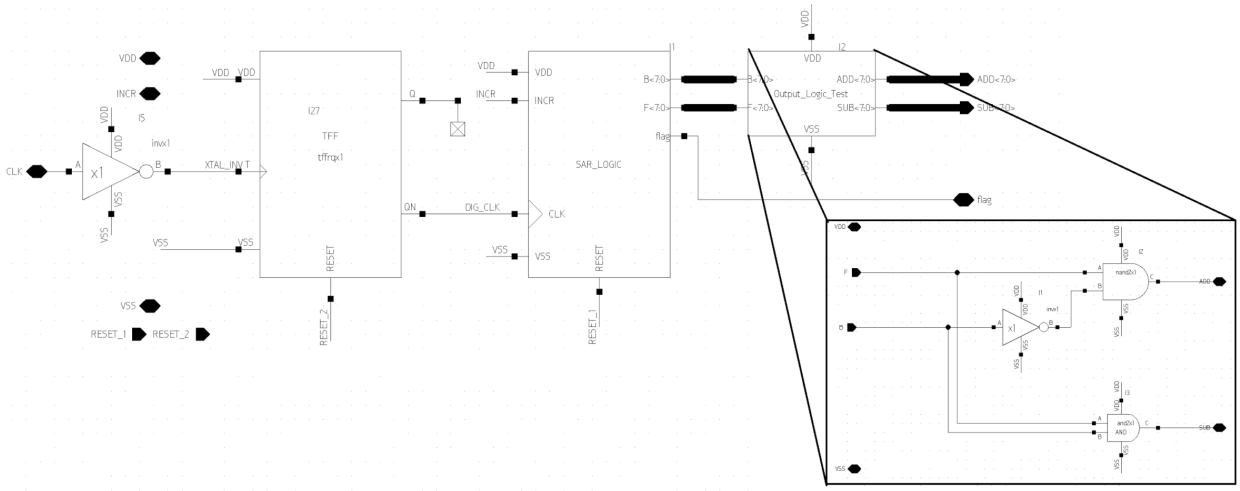
6.5. Trimming-Logic Implementation

The SAR logic is used as a method to define the increment and decrement bits of the capacitor bank. Through the SAR logic, the information provided by the frequency comparator is stored during the cycle corresponding to each bit, and is subsequently processed by a custom logic block that adjusts the add and sub values, respectively.

A block diagram representing the implemented trimming loop is presented in Figure 16.

Figure 16

Schematic of the Trimming-Logic Implementation.



7. Layout

The development of the layout focused on ensuring manufacturability by strictly adhering to the design rules of the technology (DRCs). In addition to minimum dimensions, a strategic floor plan was implemented to prioritise signal integrity and reduce lengths in critical paths, thereby minimising unmodelled parasitic effects. To ensure the robustness of the circuit against process variations and physical phenomena, the following techniques were integrated:

- **Matching and symmetry:** Matching techniques were applied to the differential pair to mitigate mismatches resulting from thermal and process gradients.
- **Well Proximity Effect Mitigation (WPE):** Safety distances of at least 1.45μm were established between the active regions and the well edge to reduce variations in the threshold voltage (V_{th}) caused by the well proximity effect.
- **Latch-up protection:** Critical blocks were surrounded by properly polarised guard rings to reduce substrate resistance and prevent the activation of parasitic thyristors.
- **Power integrity and electromigration:** The power rails (VDD/GND) were sized to withstand peak current densities, thus preventing failures due to electromigration and minimising ohmic drops.
- **Antenna effect:** The ratio of metal to gate area was managed to prevent damage from charge buildup during the plasma etching process.

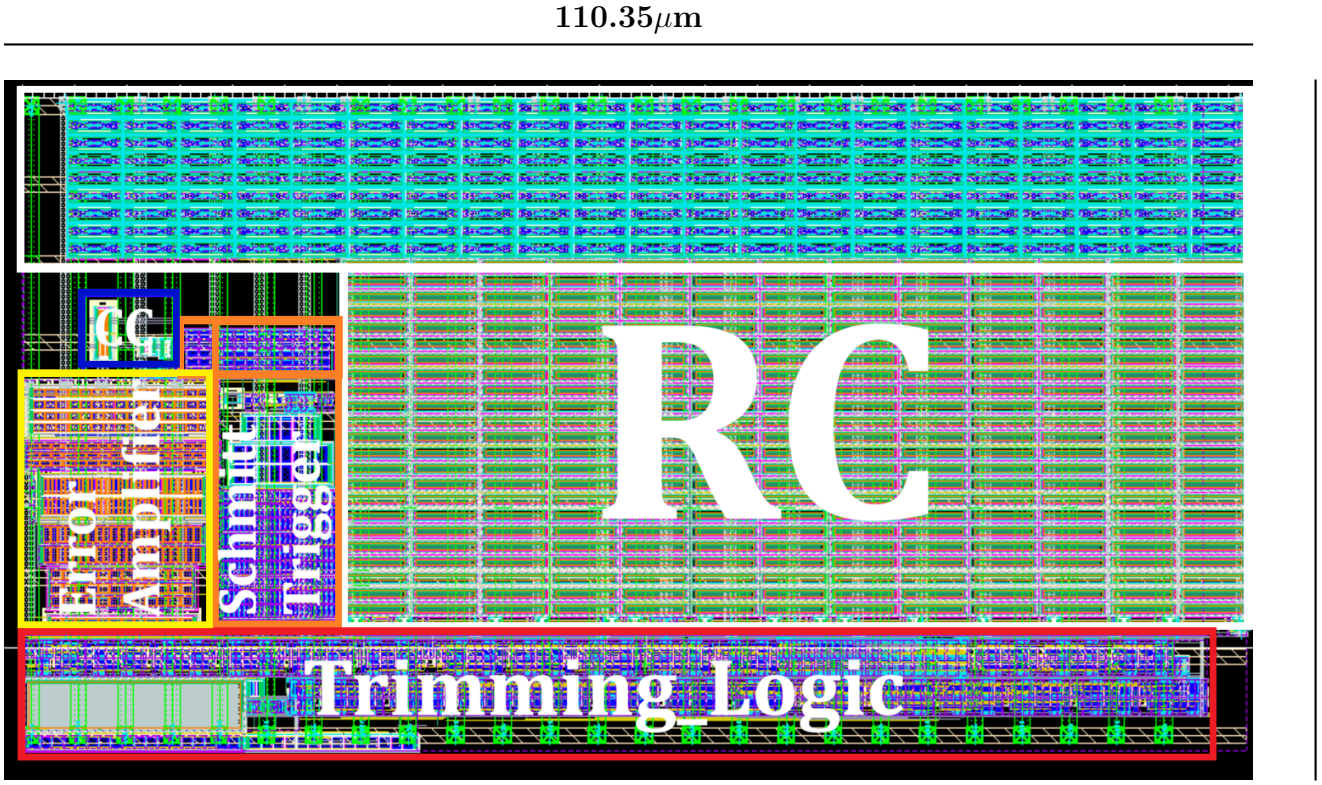
Figure 17 presents the layout with dimensions of 62.295μm high by 110.35μm long, giving a total area of 0.006874mm^2. Please note that the digital logic of the system is outlined in red, the RC bank in white, the error amplifier in yellow, the Schmitt triggers in orange and the complementary circuits of the oscillator (i.e. transistors acting as switches and digital gates) in blue. The metallization hierarchy implemented for system interconnections ranges from layer M1 to M7. The power delivery network (PDN) distribution has been

restricted exclusively to the upper levels, using layer M6 for horizontal routing and layer M7 for vertical routing in a power rail configuration. The allocation of I/O terminals (pins) has been optimized as follows:

- System signals: Located in layer M6.
- Power supply: Located in the M7 layer.

Figure 17

Layout of the RC Oscillator.



Regarding the spatial distribution of the floor plan, a organization is observed to mitigate parasitic effects and facilitate integration:

- Lower left side: Concentrates the polarization and reference signals IB_1uA_A, IB_1uA_D, PDO, VCLK and VREF.

- Lower central region: Concentrates the control and timing signals PDE, PDEN, PDEP, RESET_1, RESET_2 and XTAL_REF.
- Upper and lower periphery: The ends were reserved for the analog (VDDA), digital (VDDD) power domains and the common reference potential (VSS).

Finally, during the physical design phase, priority was given to minimizing the interconnection length for critical feedback loop signals (VCLK, RCO_divided, INCR, ADD<7:0>, and SUB<7:0>), as well as for the trimming logic reset lines. To ensure signal integrity and guarantee defined logic levels in the face of parasitic capacitances associated with long paths, a buffering stage (A regenerative and isolation stage used to decouple node loading and ensure signal integrity by maintaining logical fidelity against parasitic impedances within the layout) was implemented at each of the aforementioned nodes.

8. Results

8.1. Typical Behavior

Figure 18 illustrates the dynamic behavior of the calibration system. The oscillator output signal (VCLK), shown in red, undergoes a pre-scaling stage using a frequency divider with a factor of 2^5, resulting in the signal shown in pink. This node is evaluated against a precision reference signal (blue) using the frequency comparator detailed in Section 7.4. The logic tuning process is dominated by the following parameters:

- Synchronization: The rising edges of the trimming logic clock signal (purple) are used.
- Modulation: The INCR signal determines the transition of the logic states of the control bits, allowing the oscillation frequency to be increased or decreased according to the detected error.
- Termination: The system has an automatic switching mechanism that deactivates the trimming logic after the convergence of the last adjustment bit, triggered by the PDT (Power Down Trimming) control signal.

Figure 18

Typical behavior of system.

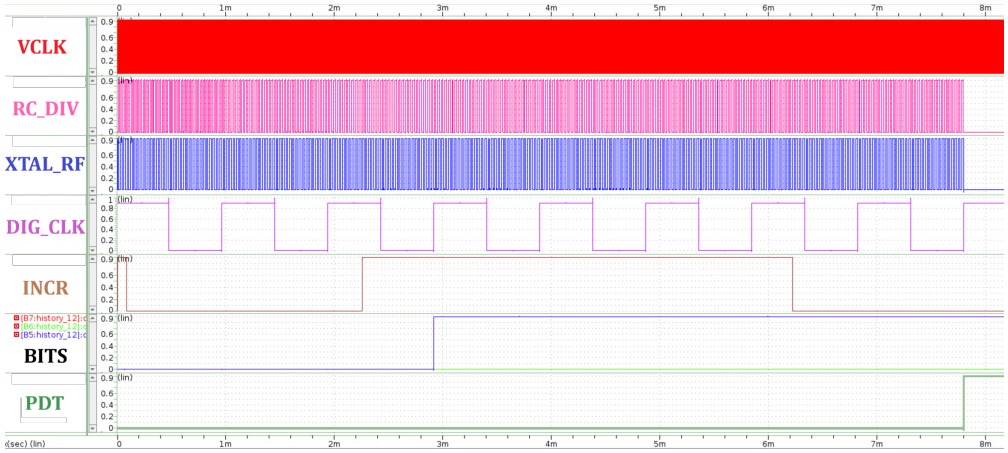


Figure 19 illustrates a time expansion of the transition corresponding to bit 5 of the trimming sequence in Figure 18, demonstrating the direct impact of the capacitor bank reconfiguration on the oscillator dynamics. After the logical assignment of this bit, there is a change in the effective capacitance of the node, which translates into an increase in frequency. The frequency, calculated using the inverse of the period, evolves from 30.12 kHz in the previous state (*) to 31.15 kHz in the subsequent state (**), corresponding to the bit assignment.

Figure 19

Frequency switching after bit allocation.

8.2. Simulation PVT Corners

It is imperative to validate the design's integrity under extreme operating conditions through PVT (Process, Voltage, and Temperature) corner simulations. In real-world applications, integrated circuits do not operate under ideal conditions; the supply voltage (V_{DD}) is susceptible to fluctuations, and the chip temperature can vary drastically depending on the environment and workload. As summarized in Table 6, to ensure that the oscillator maintains its frequency within functional ranges, the design was subjected to voltage variations between 0.8 V and 1.0 V, and an extended temperature range of -40°C to 125°C. Furthermore, the process corners for the transistors (SS, SF, FS, FF) and the overall variations in the passive components were evaluated, thus guaranteeing that the proposed architecture is robust and manufacturable under 28 nm technology standards.

The quantitative results presented in Table 7 confirm the robustness of the design against the stipulated variations. In terms of frequency stability, the oscillator maintained its operation within a narrow range between 1.028 MHz and 1.194 MHz. This translates to a frequency deviation that, in the worst-case scenario (FS, 0.8 V, -40°C corner), reached a maximum error of 13.95 % Primarily, the low supply voltage (0.8 V) limits the maximum charging voltage of the capacitor, thereby shortening the V_{CLK} signal period and increasing its frequency. Furthermore, the FS (Fast-Slow) process corner causes NMOS transistors to respond faster and PMOS transistors slower. This shift modifies the Schmitt Trigger switching thresholds, further reducing the V_{CLK} period. Additionally, the typical average power consumption was 37.51 µW, and even under the highest current demand conditions, the maximum recorded consumption was 98.1 µW.

Table 6

Corners definition.

Variable	**PVT**	**TYP**	**MC**
MOSFETsq	SS SF FS FF	TT	Global+Local
Capacitors	TT	TT	Global+Local
Resistors	TT	TT	Global+Local
VDD [V]	0.8, 1	0.9	0.9
Temperature [°C]	-40, 125	27	27

Table 7

Design performance and target comparison.

Parameter	**Units**	**Target**	**Design Obtained**			**Judge**
			Min	**Typ**	**Max**	
Frequency	MHz	1,048	1,028	1,044	1,194	Pass
Error	%	15	-1.91	-0.34	13.95	Pass
avr_power	μW	100	9.95	37.51	98.1	Pass

8.3. Monte Carlo Simulation

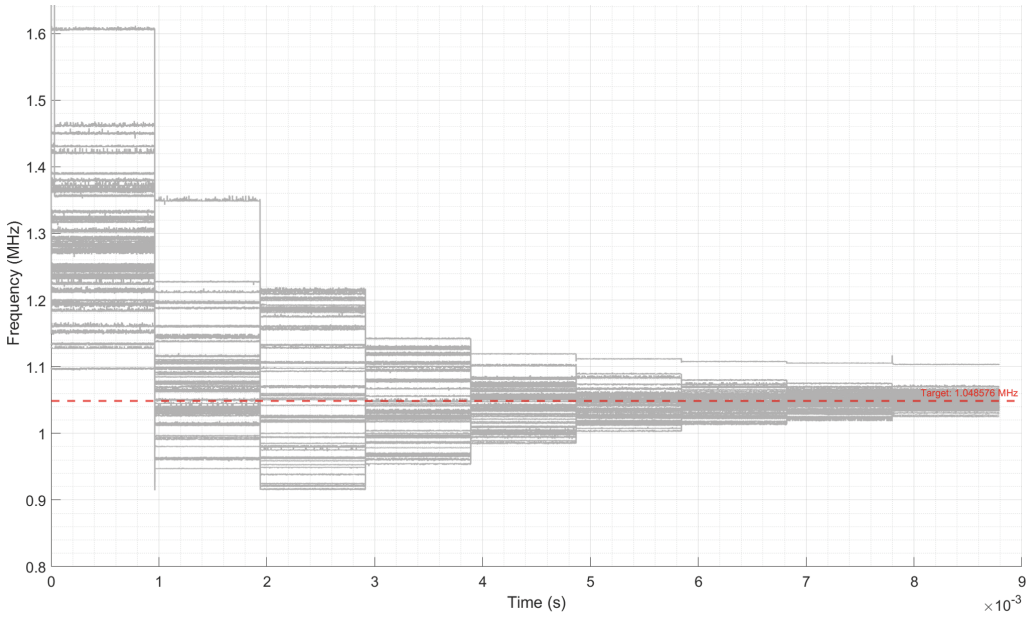
To ensure the oscillator's reliability despite the inevitable imperfections of the manufacturing process, Monte Carlo simulations were necessary. Unlike corner analysis (PVT), which considers global variations, this method evaluates the impact of local mismatches and random statistical variations between identical devices. These variations not only alter the nominal values of passive components, such as resistance (R) and capacitance (C), but also affect critical transistor parameters, specifically the threshold voltage (V_{th}). Since the design utilizes minimal channel lengths in 28 nm technology, the sensitivity to these variations intensify, which can modify the final system specifications and deviate the oscillation frequency from its design target.

The dynamics of the trimming are visualized in Figure 20, which illustrates the temporal evolution of the frequency for the different Monte Carlo samples. This graph demonstrates the corrective capacity of the trimming system: initially, the frequencies of the different sam-

ples are dispersed due to the process variations mentioned above. However, as time progresses and the control logic modifies the capacitor bank, the curves gradually converge towards the target frequency (dashed red line), drastically reducing the initial percentage error until the desired accuracy range is reached.

Figure 20

Frequency Trimming Evolution (70 MC Samples).



The statistical results obtained after simulating 70 representative samples are summarized in Table 8. This table shows that, after the calibration process, the system achieves a mean frequency of 1.0494 MHz with a standard deviation (σ) of 13.50 kHz. It is noteworthy that the mean percentage error remains at 0.9334 %, validating the effectiveness of the control loop even under misalignment conditions.

Table 8

Statistical results of the system simulation with 70 samples.

Parameter	**Min**	**Max**	**Mean**	**Std. Dev (sigma)**
Frequency [MHz]	1.023	1.1035	1.0494	0.0135
Error [%]	-2.870	5.2366	0.9334	1.306
avr_power [μW]	29.68	58.27	35.19	7.09

From an analytical standpoint, these frequency variations are expected if the circuit's constitutive equations are reviewed. Random variations in the transistors' (V_th directly impact the Schmitt Trigger's switching threshold voltages (V_LH and V_HL), defined in equations (16) and (17) by the transistor's aspect ratio and characteristics. Similarly, mismatches in the comparator's differential pair introduce an offset voltage (V_os), altering the triggering condition described in equation (6). Since the oscillator's frequency equation is intrinsically dependent on the charge and discharge times defined by these voltage levels (V_ref, V_LH, V_HL), any deviation in the transistors' physical parameters (V_th) results in a shift in the oscillation frequency, justifying the critical need for the implemented self-tuning mechanism.

Finally, to establish the relevance and competitiveness of the proposed design within the state of the art, a quantitative comparison is presented against other relaxation oscillators recently reported in the literature. Table 6 summarizes the critical performance metrics, contrasting this work with implementations across a wide range of technologies, from mature 180 nm nodes to advanced 12 nm FinFET nodes. This comparison allows visualization of the design trade-offs between power consumption, accuracy, and silicon surface area, particularly highlighting the achieved area efficiency of 0.0068 mm^2 and validating the scalability of the solution at the 28 nm node against equivalent architectures.

Table 9

Results comparison against other works.

Metric	**(Medeiros et al., 2020)**	**(Srivastava et al., 2025)**	**(Liao et al., 2023)**	**(Lei et al., 2021)**	**(Liu et al., 2024)**	**(Arenas Peñuela, 2018)**	**This Work**
Tech [nm]	40	28	28	16	12	180	28
Power (μW)	0.04	1.4	0.0276	0.0936	0.00605	1.5 @1MHz	37.5[2]
Freq [kHz]	32.7	2100	28.5	32	30.8	32.7–1024	1048
Area [mm^2]	0.127	0.0052	0.0046	–	0.063	0.05	0.0068
StartUp	3 cyc.	3.6 μs	1 cyc.	150 μs	–	4 μs @1MHz	1.24 μs (2 Cyc)[3]
Temp. [°C]	-40/ 125	-20/ 120	-40/ 85	-40/ 125	–	-20/ 125	-40/ 125

9. Conclusions and Future Work

9.1. Conclusions

The development of this degree work has allowed for the consolidation of the design of a reference oscillator for low-power embedded systems. Below, the fulfillment of the proposed objectives is detailed through the obtained technical evidence:

First, the mathematical modeling and simulation of the RC oscillator behavior have been performed, as detailed in Section 3. Through the derivation of analytical frequency equations and the incorporation of non-idealities such as switching delays and on-resistances, it has been possible to predict the circuit's behavior with a model error of less than 1 % validated through simulations with verilog-A as evident in Figure 6. Additionally, the sensitivity analysis presented in Section 3.7 has allowed determining that the passive elements (R and C) and the reference voltage are the critical variables of the system. With this, the first specific objective has been fulfilled, by theoretically validating the circuit dependencies and justifying the need for a calibration mechanism.

[2] This measurement includes the trimming system.

[3] Assuming VREF has been previously established.

Subsequently, the relaxation oscillator has been designed and validated at the transistor level, integrating fundamental blocks such as the static comparator and Schmitt triggers in 28 nm CMOS technology (Sections 5 and 6). The robust validation of the system has been demonstrated in Section 9 through PVT corner simulations and Monte Carlo analysis. The results obtained, outlined in Table 7 and Table 8, indicate that the oscillator achieves the target frequency of 1.048 MHz with a mean error of only 0.9334 % after calibration in typical corner, maintaining an average power consumption of 35.19 μW. Thus, compliance with the second specific objective has been achieved, guaranteeing the circuit's operability under process, voltage, and temperature variations within the design specifications.

Likewise, the physical design (Layout) of the RC oscillator has been developed, applying design for manufacturability (DFM) techniques and latch-up protection described in Section 8. The final design, presented in Figure 17, occupies a total area of $0{,}006874 mm^2$, a value significantly lower than the limit of $0{,}05 mm^2$ established in the initial requirements. With the achievement of a compact design free of design rule check (DRC) errors, the third specific objective has been satisfactorily fulfilled, ensuring the component's manufacturability and integrability into the SoC.

Finally, the successful integration of the analog core with the digital trimming logic (Section 7) has allowed obtaining a self-tuning system capable of dynamically compensating for process deviations. Consequently, the general objective of the project has been fulfilled , delivering a functional relaxation oscillator in 28 nm technology, validated for low-power applications and ready for its integration into the microarchitecture of the OnChip research group.

9.2. Future Work

Although this work has achieved the design and schematic validation of a functional relaxation oscillator in 28 nm technology, several lines of research and development can extend the scope and robustness of this project:

First, it is fundamental to complete the physical verification flow of the design. Layout Versus Schematic (LVS), and, crucially, Parasitic Extraction (PEX). Given that interconnect parasitic effects have a significant impact in advanced 28 nm nodes, post-layout simulations must be performed to quantify frequency degradation and power consumption, adjusting the design to compensate for these deviations prior to manufacturing.

Regarding the architecture, it is proposed to modify the passive element banks (resistors and capacitors) to enable an extended multi-mode operating range. The goal is for the oscillator not only to operate at 1.048 MHz but to cover a discrete spectrum from 32.768 kHz to 1.048 MHz, maintaining trimming capability and stability at each operating point. This would increase the block's versatility for different SoC power states.

Additionally, the implementation of programmable precision control logic is suggested. This would involve adding a selector that allows the user or the SoC to dynamically configure the number of clock cycles used by the frequency comparator (integration window). This feature would enable a real-time trade-off between calibration time (for fast wake-up) and frequency accuracy (for high-precision tasks).

Finally, as the definitive step to close the design cycle, the fabrication of the silicon prototype and its experimental characterization are contemplated. This would allow contrasting simulation models with real laboratory measurements, validating the circuit's behavior against real-world interference and its effective integration with the embedded system's bus interface.

References

Anand, S., et al. (2017). A 0.68nW/kHz Supply-Independent Relaxation Oscillator with ±0.49 %/V and 96ppm/°C Stability. *IEEE International Solid-State Circuits Conference (ISSCC)*, 96-98.

Arenas Peñuela, J. A. (2018). An Integrated RC Oscillator with Frequency Trimming to Decrease Impact of Supply Voltage Variations.

Baker, R. J. (2019). *CMOS: Circuit Design, Layout, and Simulation* (4.ª ed.). Wiley.

Gomez, H., Arenas, J., Rojas, C., Reyes, D., Mantilla, A., & Roa, E. (2019). A 68/36ppm/°C TC 32.768kHz-to-1MHz RC-Based Oscillator with 72/6pJ Start-Up Energy. *IEEE Custom Integrated Circuits Conference (CICC)*, 1-4.

Griffith, D., et al. (2014). A 190nW 33kHz RC Oscillator with ±0.21 % Temperature Stability and 4ppm Long-Term Stability. *IEEE International Solid-State Circuits Conference (ISSCC)*, 300-301.

Joint Committee for Guides in Metrology. (2008). *Evaluation of measurement data – Guide to the expression of uncertainty in measurement (JCGM 100:2008)*. ISO.

Jr., C. J. S., Roden, M. S., & Carpenter, G. L. (1992). *Diseño Electrónico: Circuitos y Sistemas* (2.ª ed.). Addison-Wesley Iberoamericana.

Lei, K.-M., Mak, P.-I., & Martins, R. P. (2021). A 0.35-V 5,200-μm^2 2.1-MHz Temperature-Resilient Relaxation Oscillator With 667 fJ/Cycle Energy Efficiency Using an Asymmetric Swing-Boosted RC Network and a Dual-Path Comparator. *IEEE Journal of Solid-State Circuits*, *56*(9), 2701-2710. https://doi.org/10.1109/JSSC.2021.3067051

Liao, F.-W., Tsou, S.-C., & Chao, C.-S. (2023). A 6nW 30.8kHz Relaxation Oscillator with Sampling Bias-Free RC Circuit and Dynamic Power Scaling in a 12nm FinFET. *2023 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, 1-2. https://doi.org/10.23919/VLSITechnologyandCir57934.2023.10185329

Liu, Y., Zhu, Z., Bao, R., Lin, J., Yin, J., Li, Q., Mak, P.-I., & Yang, S. (2024). A Compact Sub-nW/kHz Relaxation Oscillator Using a Negative-Offset Comparator With

Chopping and Piecewise Charge-Acceleration in 28-nm CMOS. *IEEE Transactions on Circuits and Systems I: Regular Papers*, *71*(2), 515-525. https://doi.org/10.1109/TCSI.2023.3326351

Medeiros, W. T., Klimach, H., & Bampi, S. (2020). A 40 nW 32.7 kHz CMOS Relaxation Oscillator with Comparator Offset Cancellation for Ultra-Low Power applications. *2020 IEEE 11th Latin American Symposium on Circuits Systems (LASCAS)*, 1-4. https://doi.org/10.1109/LASCAS45839.2020.9069038

Moreno, A. L. T., & Sepúlveda, S. S. O. (2024). *Optimization of a crystal oscillator design for a 28 nm SoC implementing start-up time reduction* [Bachelor's thesis in electronic engineering]. Universidad Industrial de Santander, Escuela de Ingeniería Eléctrica, Electrónica y de Telecomunicaciones.

National Institute of Standards and Technology. (n.d.). NIST TN 1297 – Appendix A: Law of Propagation of Uncertainty.

Sebastiano, F., et al. (2009). A low-voltage mobility-based frequency reference for crystal-less ULP radios. *IEEE Journal of Solid-State Circuits*, *44*(7), 2002-2009. https://doi.org/10.1109/JSSC.2009.2020195

Sedra, A. S., & Smith, K. C. (2015). *Microelectronic Circuits* (7th). Oxford University Press.

Srivastava, A., Iqbal, S. M., Tripathi, D., & Goyal, S. (2025). Startup Circuit for Relaxation Oscillators with Low Functional Current and Minimal Area. *2025 38th International Conference on VLSI Design and 2024 23rd International Conference on Embedded Systems (VLSID)*, 214-218. https://doi.org/10.1109/VLSID64188.2025.00050

Taylor, B. N., & Kuyatt, C. E. (1994). *Guidelines for Evaluating and Expressing the Uncertainty of NIST Measurement Results* (inf. téc. N.º NIST Technical Note 1297). National Institute of Standards y Technology. Washington, DC, U.S. Govt. Printing Office.