DISEÑO DEL SISTEMA DE CONTROL DE LA BOMBA DE CARGA DE UN CONVERTIDOR DC-DC DE CAPACITORES CONMUTADOS

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A I.O. y a mí.

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A todos y a cada uno.

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RESUMEN

TÍTULO: DISEÑO DEL SISTEMA DE CONTROL DE LA BOMBA DE CARGA DE UN CONVERTIDOR DC-DC DE CAPACITORES CONMUTADOS*

AUTORES: Wilmer Alexis Rueda Arias **

PALABRAS CLAVE: Bomba de carga, convertidor DC-DC, capacitores conmutados

DESCRIPCIÓN: En este trabajo se presenta el producto de la investigación en el campo de la administración de potencia para sistemas integrados en un chip. Tomando como referencia tecnologías desarrolladas para la administración de altas cantidades de potencia, un convertidor DC-DC de capacitores conmutados basado en la topología de la bomba de carga de Dickson y su sistema de control es diseñado para producir un voltaje mayor que V_{DD}. Los diseños del sistema son realizados con una tecnología standard CMOS de 0.13[µm] para el sistema de administración de una memoria EEPROM. La bomba de carga se compone de un capacitor, un transistor de transferencia principal y un par de transistores auxiliares por cada etapa de conversión, a su vez compuesta por dos etapas de conversión. En el sistema de control el dispositivo que actúa como controlador es un comparador y el actuador se diseña a partir de configuraciones de inversores CMOS. El sistema alcanza un valor promedio de 2.398[V] en el voltaje de salida en estado estable para un voltaje de entrada de 1.2 [V]. El rizado en el voltaje de salida alcanza cerca de 116 [mV] para una frecuencia de conmutación de 100 [MHz]. Las simulaciones de MonteCarlo permiten calcular una desviación standard de 27.9 [mV] en el voltaje de salida esperado.

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*Trabajo de Grado.

** Facultad de Ingenierías Físico-Mecánicas. Escuela de Ingeniería Eléctrica, Electrónica y de Telecomunicaciones. Director: M.Sc. Andrés Felipe Amaya Beltrán.

ABSTRACT

TITTLE:DESIGN OF A CHARGE PUMP CONTROL SYSTEM TO A SWITCHED CAPACITOR DC-DC CONVERTER*

AUTHORS: Wilmer Alexis Rueda Arias**

KEYWORDS: Boost charge pump, switched capacitor, DC-DC converter.

DESCRIPTION: In this work is presented the investigation product about the power management to integrated systems. Based on technology developed to high power management systems a switched capacitor DC-DC converter based on Dickson charge pump topology and its control system is designed to produce a voltage higher than VDD. System designs are realized with a Standard CMOS 0.13[µm] technology for a EEPROM memory power management system. The charge pump is composed of a capacitor, a charge transfer mosfet and two auxiliary mosfet by stage. The system have two conversion stages In the control system is used a comparator as controlator and a driver to transfer the charge to the charge pump. The system achieves an average value of 2.398[V] in the output voltage at steady state for an input voltage of 1.2[V]. The output voltage ripple reach about 116[mV] for a switching frequency of 100[MHz]. Monte Carlo sampling simulations allows to calculate a standard deviation of 27.9[mV] in the expected output voltage.

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*DegreeWork.

**Faculty of PhysicMechanicalEngineering.School of Electric, Electronic and Telecomunications. Director: M.Sc. Andrés Felipe Amaya Beltrán.

INTRODUCTION

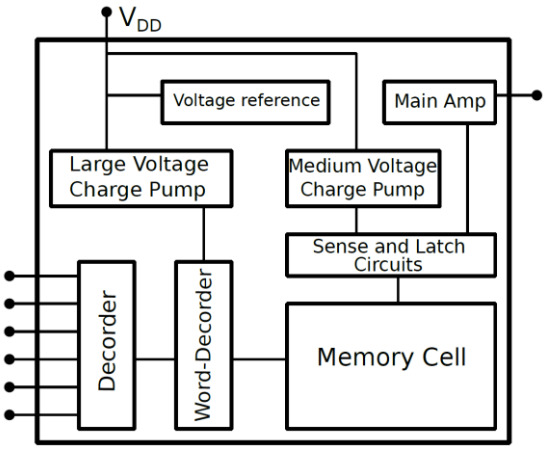
Development on chip's fabrication over discrete devices on Printed Circuits Boards (PCB) has reduced circuit's cost and size. CMOS technology has played a fundamental role in this process and circuits ever larger can be fabricated in the same area. Power management architectures are required in many devices connected to a battery, a DC voltage or a loosely regulated supply because of the need to have a better supply that improve the efficiency of the even more complex CI's. [1] [2]

To provide a regulated medium voltage for a Electrical Erasable Programmable Read Only Memory (EEPROM) power management system is the aim of this work.

The DC-DC converters are building blocks that convert a supply voltage into voltages according to the specifications of the circuit. The DC-DC conversion is done actually by some switching voltage regulators fabricated externally that supply different voltages to the CI; or by providing a voltage to the chip which is converted as specified by integrated linear regulators. Discrete regulators case implies disadvantages like more pines on the chip and an increment in area consumption as well as a limited efficiency.y. [3]

There are two types of DC-DC converters, inductive regulators that use both inductance and capacitance for its operation and capacitive converters which use only capacitance. On integrated case switching capacitor (SC) DC-DC converters are more viable due to the poor quality of the integrated inductance. [1]. To appreciate the SC DC-DC converters importance in the memory power management system the scheme in Figure 1 allows view usage of a charge pump to supply a regulated DC voltage.

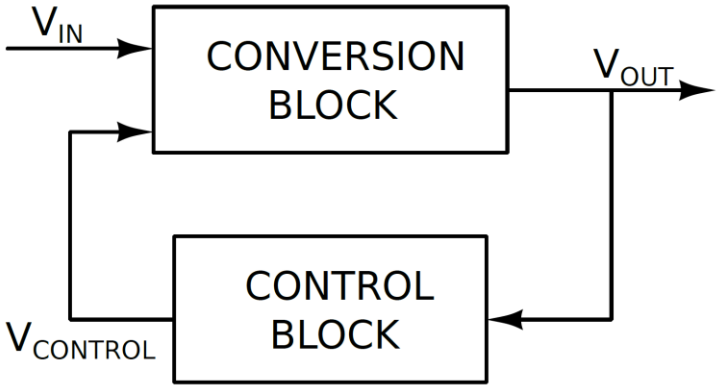
Figure 1. A common flash EEPROM.



1. SWITCHING CAPACITOR DC-DC CONVERTERS

As shown in Figure 2 the SC DC-DC converter is composed by two fundamentals blocks(conversion and control). The conversion from an in voltage to an output voltage is done in the conversion block who represent the low impendance circuit section. The circuit specifications are achieved using the control block and differs in its nature respect to the conversion block cause implies the introduction of high circuit impedances. [5]

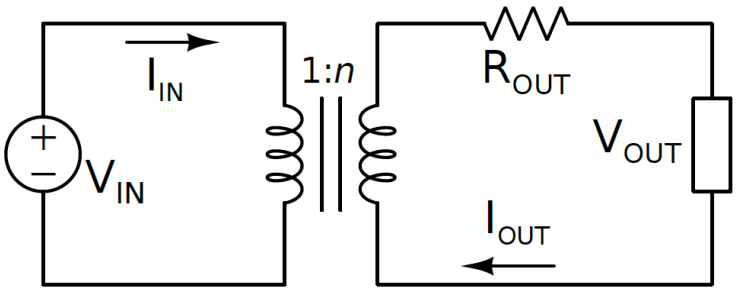
Figure 2: Simplified scheme to the DC-DC converter.



The concepts below are explain to analyze the circuit operation:

- Static characteristics These characteristics are linked to the converter nature, between these are: the voltage conversion ratio (VCR), the noise (due to the non ideals connections in the conversion block), efficiency, power density and accuracy of the circuit.
- Dynamic characteristics Both system control and conversion block circuits affect the dynamic characteristics. Line and Charge Regulation are the circuit capacity to lead with in voltage (R_{line})and with charge current changes (R_{load}), respectively, are measures needed to probe the circuit robustness. Bandwidth are related to control signals and the output voltage ripple can be tuned to a specific value by the system control. [1]

Figure 3: Idealized scheme of a charge pump



A charge pump idealized scheme is shown in Figure 3, the converter operation is domain by the resistance switches conduction and capacitors commutation modeled as output resistance (R_{OUT}). The output resistance depends on two operation modes, slow and fast switching limit (SSL and FSL). Operating on SSL the output resistance is associated to the charge transferred to the capacitors, on the other hand when operates on FSL the losses are related to the switch conduction, principally.

On SSL switching period is large, there are losses depending on switching frequency (f_{SW}) and transistors size. R_{SSL}, is given by:

$$R_{SSL} = \sum_{i \in caps} \sum_{j=1}^{n} \frac{(a_{c,i})^2}{2 f_{SW} C_i} \quad (1)$$

Where f_{SW} y C_i represent switching frequency and the capacitance of each capacitor, respectively. Multiplier $a_{c,i}$ is the relationship between the charge flow per period in C_i and the total output flow per period in steady state.

On FSL the dominant variable in the output resistance $R_{FSL}$is the losses when transistors are on, modeled by R_i . To analyze the circuit on this operation mode is necessary to define a converter duty cycle D_j in the j phase of a $n - phase$ converter. Besides, this output resistance depends on the multiplier $a_{r,i}^{j}$, to quantify the charge flow on i switch in operation phase j. In this way, R_{FSL} can be expressed as:

$$R_{FSL} = \sum_{i \in caps} \sum_{j=1}^{n} \frac{R_i}{D_j} \left(a_{r,i}^{j}\right)^2 \quad (2)$$

To have an optimized charge pump efficiency the converter duty cycle may be the 50% of the period switching, the equations 1 and 2 are rewritten like is shown in equations 3 y 4. The output total resistance product of the two operation modes is modeled in the equation II.5.

$$R_{SSL} = \sum_{i \in caps} \frac{(a_{c,i})^2}{f_{SW} C_i} \quad (3)$$

$$R_{FSL} = \sum_{i \in caps} R_i \left(a_{r,i}^{j}\right)^2 \quad (4)$$

$$R_{OUT} = \sqrt{{R_{SSL}}^2 + {R_{FSL}}^2} \quad (5)$$

On account of the large number of possible converter topologies, components and variables the charge pump control can be realized by different ways. Some straightforward methods are through output resistance (R_{OUT}) regulation and voltage conversion ratio (VCR) variation. Given the model of R_{OUT} a signal-processing block control method uses variations on the converter parameters to

achieve the specifications of the circuit. In [6]- [7] are presented various control methodologies, from the simple linear regulation to a complex variation on the charge pump topology.

On SSL mode the control is usually implemented by skip clock pulse or PWM method, as observed in [6] and [8], in both cases is presented a frequency regulation. In the skip clock pulse case the main advantage is the possibility to control the quiescent current of the converter, this method is used at light loads because the voltage output ripple at V_{IN-max} and $I_{OUT-max}$ is higher than the achieved by other methods. In the PWM case the most important characteristic is the use of a comparator which is faster than operational amplifiers but a wide current load range is not supported and the time constants introduced implies the utilization of large capacitors.

On FSL mode a simple linear regulation can be implemented as explained in [6] and [9]. Where the output voltage is compared with a voltage reference to produce an error signal who is amplified by an operational amplifier regulating the losses of the switching transistors $\sum_n^i R_{Mi}$.

The voltage ratio conversion technique as is done in [10] and [7] achieve a good behavior in the SC DC-DC converter by implementing a sophisticated control methodology but it can lead to a more complex circuit and it is not always necessary.

2. SYSTEM DESIGN

2.1. CHARGE PUMP TOPOLOGY

In this case a boost converter is necessary to achieve the required circuit specification shown in Table I.

A common and straightforward based diode boost charge pump topology was proposed by Dickson in [11].

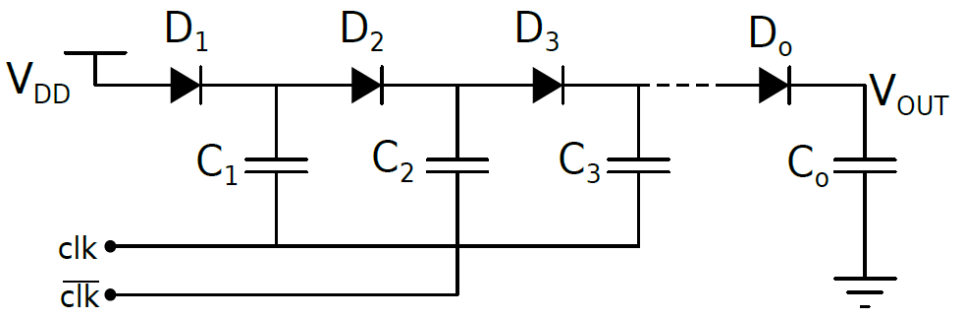
Based on Figure 4 a basic analysis of the based diode charge pump behavior can explain the main disadvantages of the topology:

$$V_{OUT} = (V_{DD} - V_t) * N + V_{DD} \quad (6)$$

Tabla I: Design specifications.

Specification	Value
V_{in}	1.2 [V]
C_L	500 [pF]
f_{sw}	100 [MHz]
Ideal Conversion Ratio	1:2

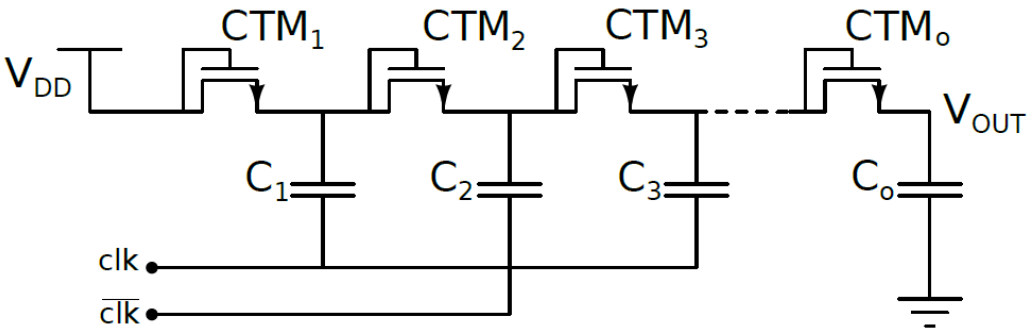
Figure 4: Theorical Dickson charge pump.



In equation 6 V_{DD}, N and V_t are the supply unregulated voltage, the number of stages and the voltage drop in the diode, respectively. The use of a diode-connected MOS transistor implies an increment in V_t, as the number of stages

becomes larger due to the body effect in CTM and it leads to a reduced efficiency, i.e. Dickson charge pump has an output voltage saturation level. [12].

Figure 5: Practical Dickson charge pump.



As shown in Figure 5 a charge transfer MOSFET (CTM) chain is wired two clocks in anti phase, pumping charge to an output capacitor by charging and discharging the coupling capacitors. Several attempts have been made to improve Dickson charge pump characteristics trying to avoid the body voltage degradation problem, both in process technology as in circuit topology. Some results are showed in Table II.

Tabla II: Dickson charge pump improves.

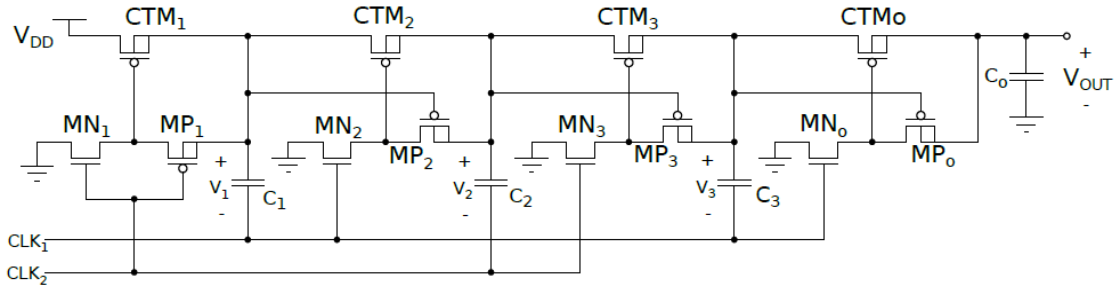
	Circuit Topology					
	Dickson [1976]	ABV [2000]	ABDGV [2007]	PGI-1 [2007]	PGI-2 [2007]	PGI-3 [2007]
V_{DD} [V]	15-19	1.8	1.2	1.5	1.5	1.5
V_{OUT} [V]	48-54	5	5	6	4	6
f_{sw} [MHz]	1	3	100	2	2	2
Load	1 [nF]	-	100 [kΩ]	100 [pF]	100 [pF]	100 [PF]
Stage number	7	4	4	4	4	3
Process Technology [μm]	-	1.5	0.130	0.35	0.35	0.35*
*PGI-3 was fabricated in mixed 0.35 [μm] technology.						

On Adaptive Body Voltage technique (ABV) two auxiliary MOSFET are introduced in the charge transfer block to avoid degradation in threshold voltage, using the body as an active terminal. ABV method can be combined with a Dynamic Gate Voltage control(ABGV), to implement it an inverter is added to the circuit topology connecting its output to the CTM gate terminal. [12] [13].

In [4] are proposed three Pumping Gain Increase(PGI) circuit topologies called PGI-1, PGI-2 and PGI-3. The first and the second PGI circuits are based on a dynamic gate voltages control method. The difference between PGI-1 and PGI-2 is the use of a more complex output stage on the first while PGI-2 use only a PMOS output transistor. PGI- 3 topology achieve the best results, using a

PMOS transistor as CTM and an inverter connected to the gate CTM terminal, as shown in Figure 6.

Figure 6: Charge pump circuit topology.



The use of PMOS transistors reduce the voltage threshold degradation because the body and the source terminals are connected to a terminal becoming more positive than V_{DD} each switching period of the charge pump operation until reaching the steady state. PGI-3 has two operation phases, on the first time CLK_1 is low and CLK_2 is high, this results in turning on MN_1 and MN_3 causing CTM_1 and CTM_3 operate in triode region allowing a charge flow through C_1 and C_3. On the second phase CLK_1 is high and CLK_2 is low turning on CTM_2 and CTM_o charging C_2 and C_o The circuit analysis results are shown as follow:

$$V_1 = V_{DD} \tag{7}$$

$$V_2 = V_{CLK} + V_1 = V_{CLK} + V_{DD} \tag{8}$$

$$V_3 = V_{CLK} + V_2 = 2V_{CLK} + V_{DD} \tag{9}$$

$$V_{OUT} = V_{CLK} + V_3 = 3V_{CLK} + V_{DD} \tag{10}$$

2.2. SYSTEM CONTROL

A skip clock pulse method have been designed, in Figure 7 is shown a scheme of the methodology.A comparator is used to generate the control signal CLKC. A comparison between the reference and the voltage divider terminal V_d allows to regulate the charge injected to the conversion block by skipping CLKC pulses when V_d is higher than V_{REF}. The use of a driver block is necessary to lead whit the large capacitance present in the charge pump block.

As shown in Figure 8 a double tail sense amplifier latch type is designed to compare the signals $In+$ and $In-$. Comparator topology are composed by the input stage and the latching stage, the first one is responsible to receive the signals to be amplified at D_i nodes and the second one based on the differential

voltage ΔV_{Di} regenerate the signals to have an output differential voltage dependent on the difference between $In+$ and $In-$.

Figure 7: System control scheme.

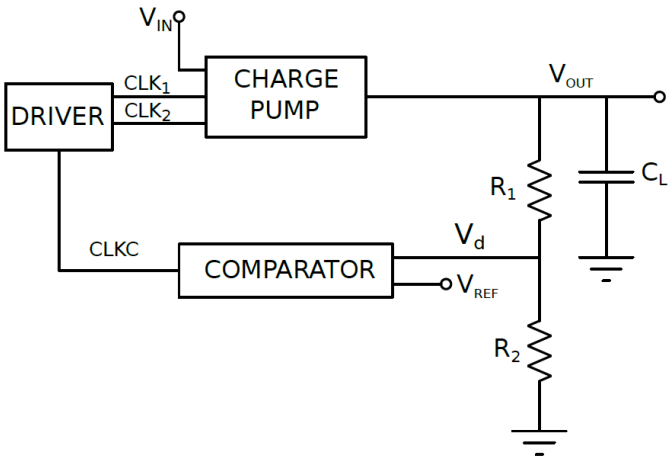
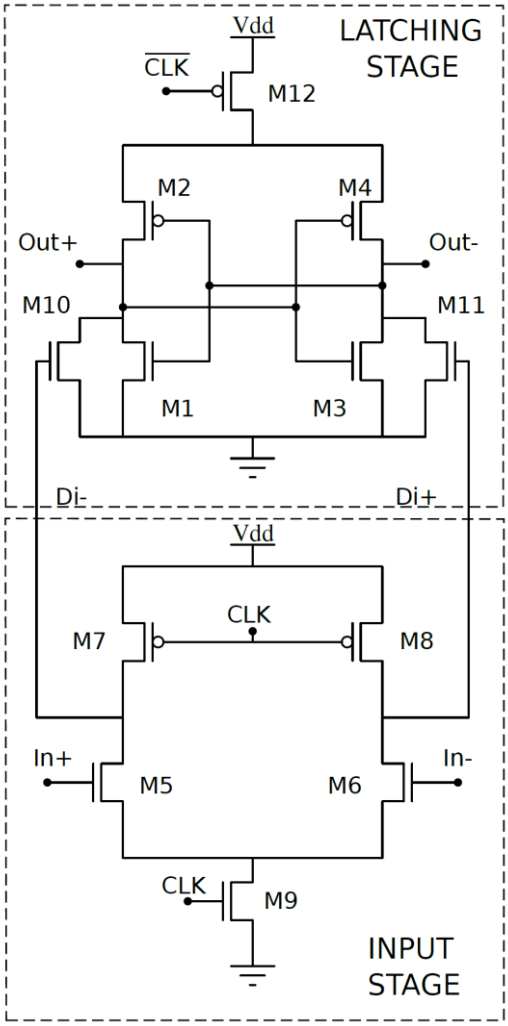


Figure 8: Comparator topology.



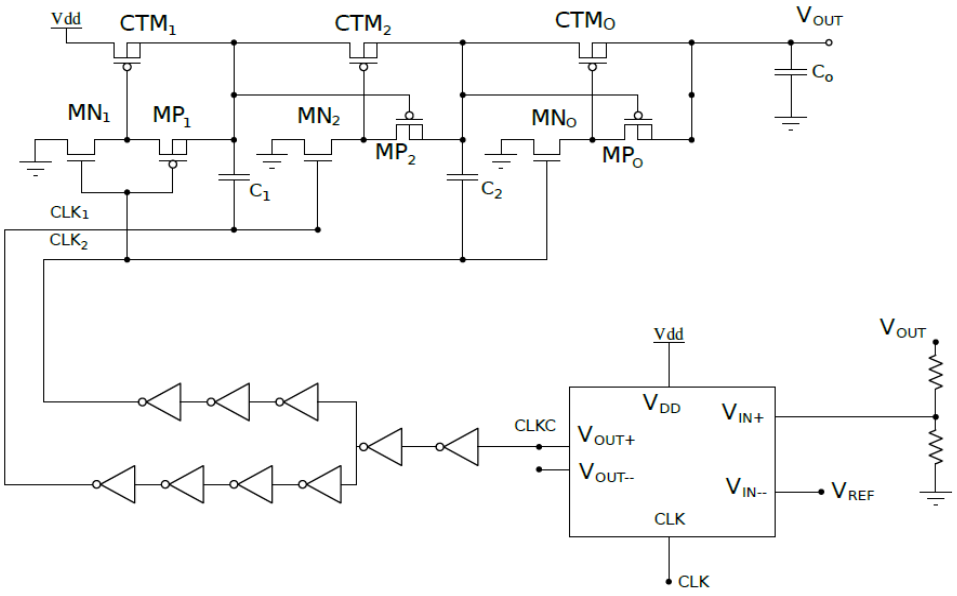
Comparator operation consists on two phases, as explained in [14], on the reset phase (CLK=0) transistors M7 and M8 charge the D_i nodes to V_{DD}, turning on the transistor M10 and M11 to discharge the output nodes to ground. The second one called comparison phase (CLK=V_{DD}) change the operation point of the transistor M9 and M12 activating the two stages of the comparator. The input stage trough the transistors M5 and M6 and based on the difference between signals $In+$ and $In-$ build on D_i nodes a common mode (V_{cm}) and a ifferential voltage (ΔV_{Di}). The signals at D_i nodes are passed to the latching stage by the transistors M10 and M11 where two inverter will regenerate it and put at Out nodes a signal dependent on the ΔV_{Di}.

At this point is necessary that V_{cm} at D_i nodes is no longer high enough for M10 and M11 to connect outputs to ground.

2.3. GENERAL TOPOLOGY

In Figure 9 is presented the general topology of the SC DCDC converter. The comparator into the control system acts like a control block (as mentioned in Section 3.3) and to operate it an external clock signal is connected to CLK nodes of the comparator, the $In+$ terminal are connected to a V_{REF} with the aim of set a reference point to the system, a voltage divider used to sense the output voltage is coupled to $In-$ and only one differential output are used and wired to the driver circuit. As explained in Chapter 11 of [15] is possible to use and inverter string like a buffer connecting circuits to a large capacitive load. The driver design in this case allows to generate two signals in antiphase connecting it two the charge pump block.

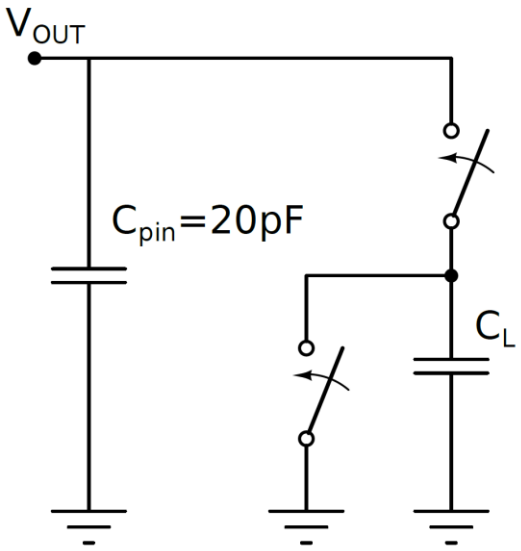
Figure 9: SC DC-DC Converter general topology.



3. SYSTEM SIMULATIONS

Simulations are presented to show the circuit operation at the design specifications and to probe circuit robustness when V_{in} and C_L present changes as well as observe the results of the Monte Carlo sampling method applied to the system. To model the memory as the converter load (C_L) and the output pin (Cpin), the connection on Figure 10 is used only for simulations purpose.

Figure 10: Memory and pin model for simulation purpose.



In Figure 11 are shown the results of the system simulation and some conditions operations, as observed the Output voltage achieves the steady state of operation approximately at 0.2 [µs].

To calculate the average output voltage is used the signal data into the steady state: V_{OUT} = 2.3984. The charge pump due to its capacitive nature present a ripple in the output signal, a section of the data in the steady state of the system are shown in Figure 12. The maximum ripple present in the steady state of the system is $V_{ripple} = 116[mV]$.

The histogram on Figure 13 shows the results of Monte Carlo simulation. Standard deviation, i.e. the expected variation on the output voltage calculated from the data results is σ = 27.9[mV].

To probe the circuit when there are abrupt variations on VIN, the simulation of Figure 14 compare the output voltage signal with the input voltage, in the figure the regulation of the system is observed when there is a change in the supply unregulated voltage. The average output voltage value at VIN = 1.2[V] and VIN = 900[mV] are VOUT = 2.398 and VOUT = 2.364, respectively.

A measure of the VIN regulation can be founded with the expression:

$$\%\mathrm{Rline} = (\Delta\mathrm{VOUT}) \,/\, (\Delta\mathrm{VIN}) * 100\% \qquad (11)$$

$$\%\text{Rline} = (2.398 - 2.364) \,/\, (1.2 - 0.9) * 100\% = 11.2\% \quad (12)$$

Figure 11: SC DC-DC output signal.

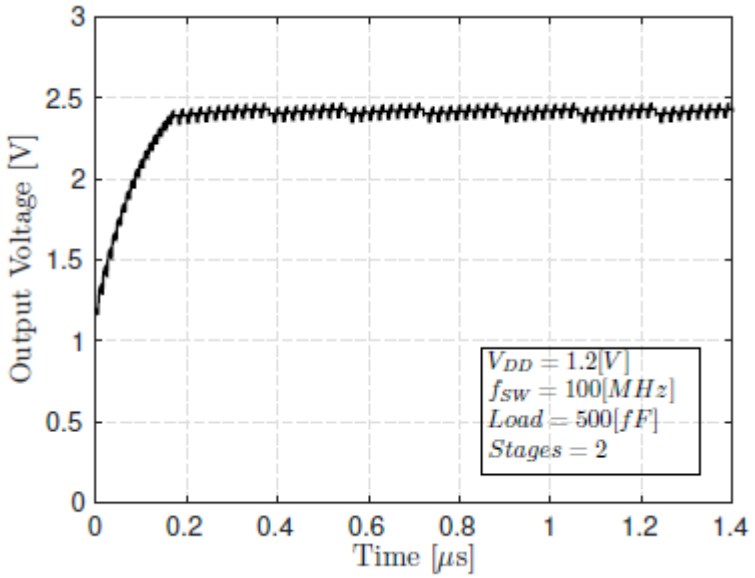


Figure 12: Output voltage ripple.

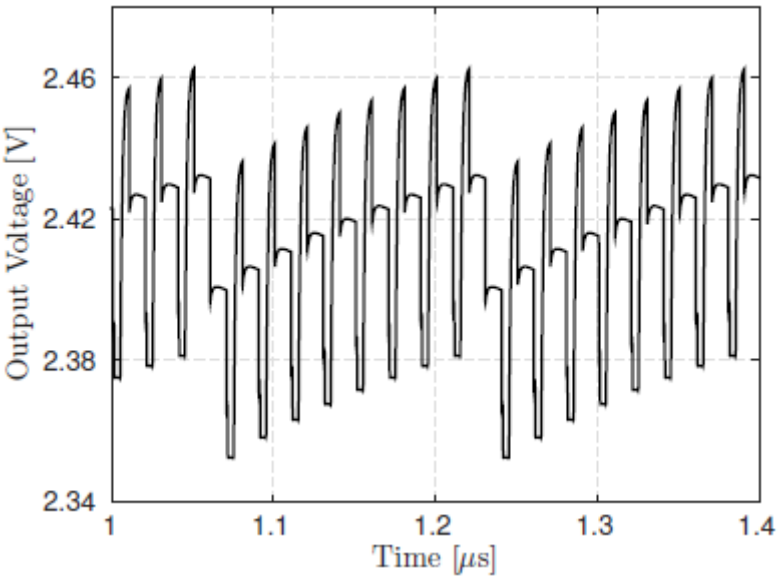
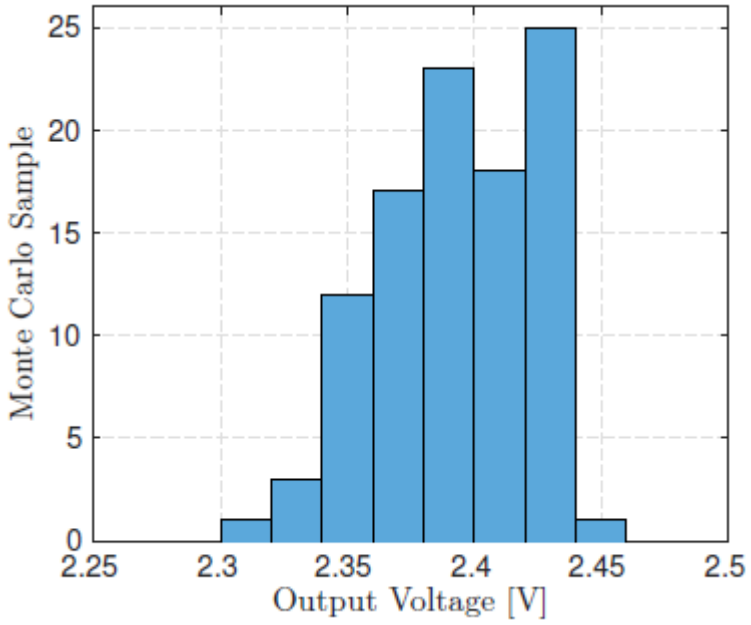
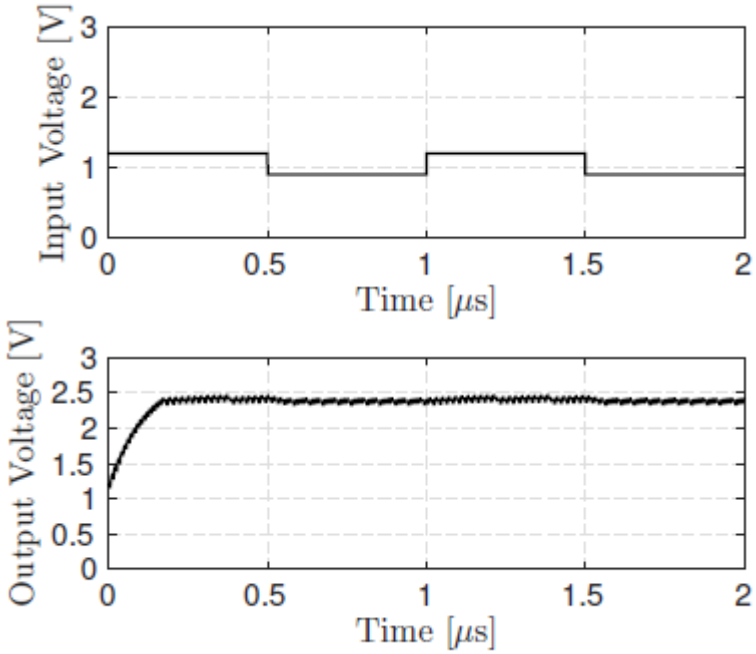


Figure 13: Monte Carlo Simulation Histogram



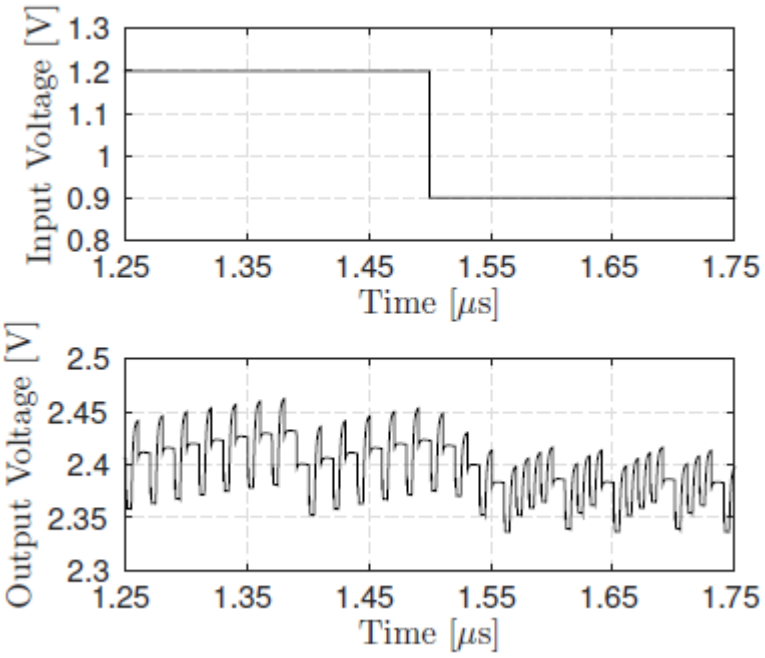
A decrease in the input voltage implies in VOUT a reduction equivalent to 11.2% of the input voltage variation.

Figure 14: Line regulation results on abrupt input changes.



In Figure 15 is shown the variation on the Vripple when the input voltage suffers changes.

Figure 15: Voltage Output Ripple View on Line Regulation



The control action to regulate the system and the signal on the output of the buffer is presented in Figure 16.

As observed, when the Input Voltage decreases the control system injects more pulses increasing the charge supplied to the converter.

Another simulation necessary to measure the line regulation and robustness of the system to the input voltage changes is shown in Figure 17. Under a change in the input voltage of 1 [V] the corresponding VOUT and Vripple variation are:

$$\Delta VOUT = 19.6[mV\ ]$$

$$\Delta Vripple = 56[mV\ ]$$

The percentage of line regulation achieved can be expressed as:

$$\%Rline = 1.96\%.$$

The increase in the average value of VOUT reach only a 1.96% of the variation in the unregulated supply.

On 18 are presented a comparison of the CLK1 and VOUTsignals in the limits of the input voltage variation.

The results of the variations in the load capacitance value are synthesized on Figure 19-20. On the first is observed the transitory behavior of VOUT and on the second is presented the relationship of the average output voltage and the load capacitance variation.

Figure 16: Control Signal and charge pump clk input comparison.

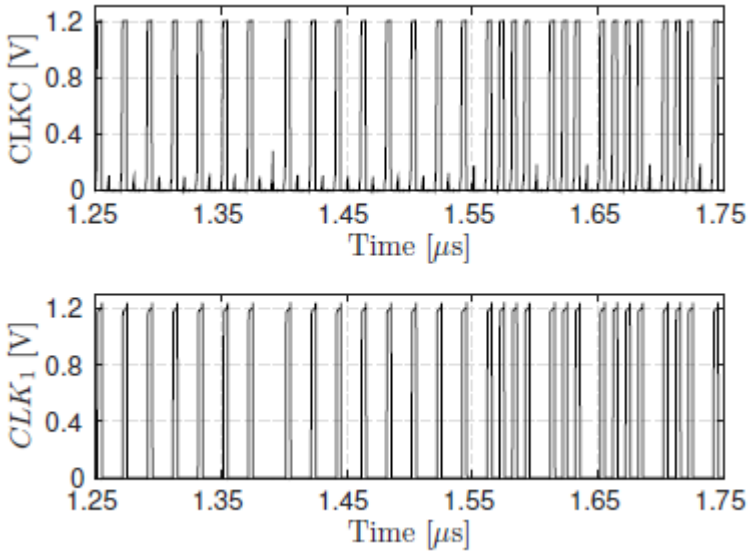


Figure 17: Line Regulation on smooth input changes

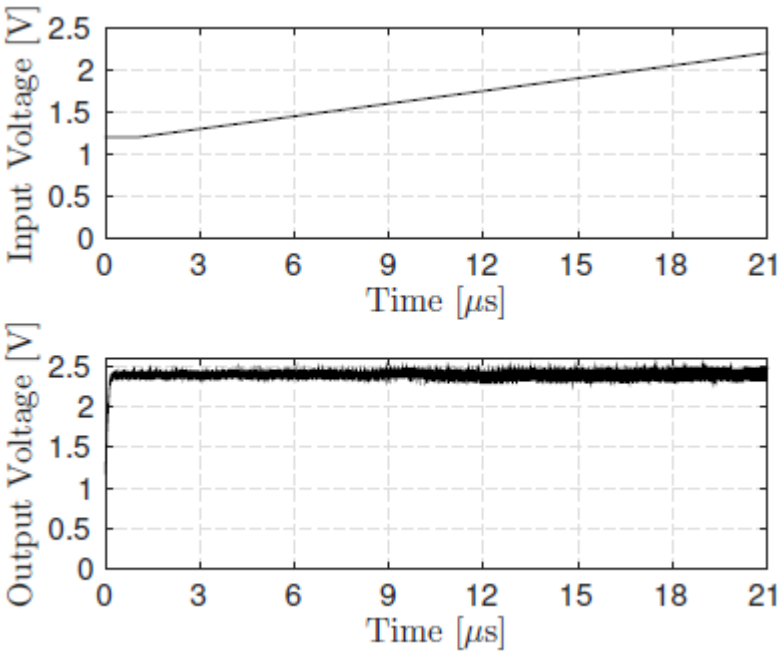


Figure 18: Charge pump input clk comparison on line regulation.

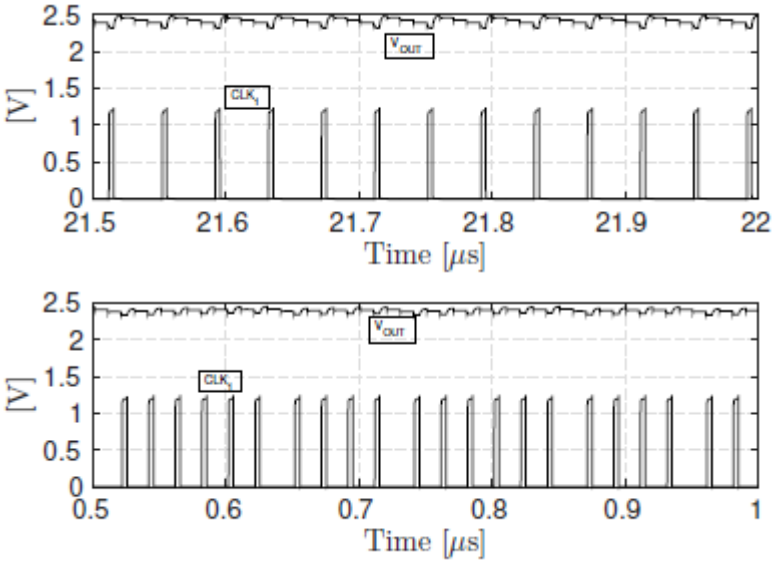
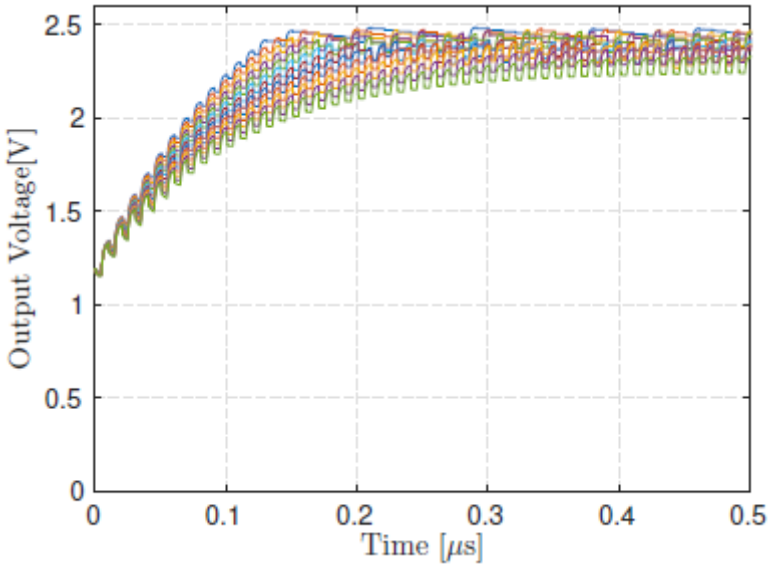
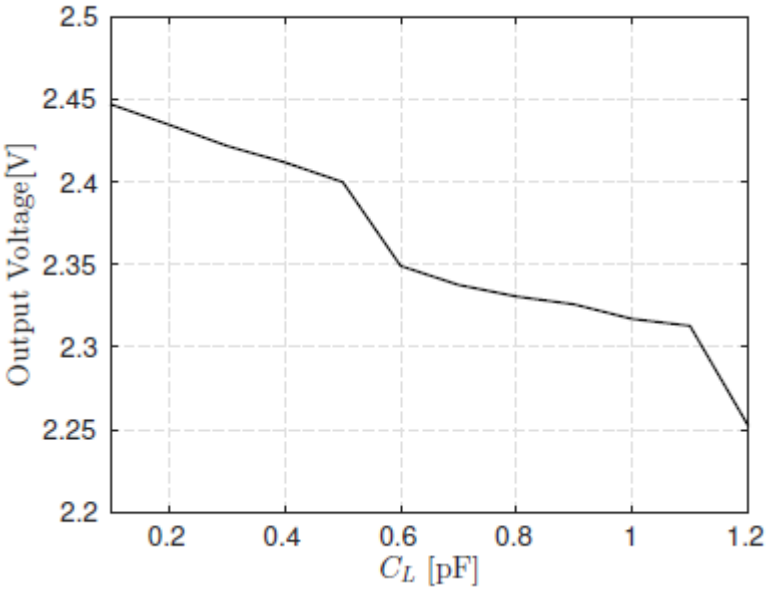


Figure 19: VOUT variations to changes on



CL

Figure 20: VOUT vs CL.



4. CONCLUSIONS

A two stages SC DC-DC converter system has been designed and simulated at fSW = 100[MHz], VDD = 1.2[V] and CL = 500[fF] reaching an output voltage of 3.984[V] and the output voltage ripple achieves a value of 116[mV].

Results of Monte Carlo Sampling simulation shows a standard deviation of 27.9[mV].

Simulation of line regulation shows the system robustness to VIN variations.When the unregulated supply descend 300[mV], the output voltage variation is about 33.7[mV]. An increase in the input voltage of 1[V] implies in the output voltage a variation of 19.6[mV].

The efficiency of the voltage conversion ratio descends to 93.5% for a load of CL = 2.4 [pF].

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