STUDY OF ELECTROMIGRATION AND IR-DROP EFFECTS FOR CHIP RELIABILITY

JUAN PABLO LOZANO CARVAJAL

UNIVERSIDAD INDUSTRIAL DE SANTANDER
FACULTAD DE INGENIERÍAS FÍSICO-MECÁNICAS
ESCUELA DE INGENIERÍAS ELÉCTRICA, ELECTRÓNICA Y DE TELECOMUNICACIONES
BUCARAMANGA
2016

STUDY OF ELECTROMIGRATION AND IR-DROP EFFECTS FOR CHIP RELIABILITY

JUAN PABLO LOZANO CARVAJAL

Trabajo de Grado para optar al título de
Ingeniero Electrónico

Director
HUGO DANIEL HERNANDEZ HERRERA
Ingeniero Electrónico, Ph.D

Co-Director
ELKIM F. ROA.
Ingeniero Electricista, Ph.D

UNIVERSIDAD INDUSTRIAL DE SANTANDER
FACULTAD DE INGENIERÍAS FÍSICO-MECÁNICAS
ESCUELA DE INGENIERÍAS ELÉCTRICA, ELECTRÓNICA Y DE TELECOMUNICACIONES
BUCARAMANGA
2016

Quiero empezar por agradecer a Dios por la salud, la guía y la sabiduría brindada.

A mis papás, Carlos Raúl Lozano y Maria Elena Carvajal, quienes siempre me han brindado su apoyo, su amor, su tiempo y esfuerzo, que me han formado para ser la persona con valores que soy hoy en día, todo por medio de su guía y ejemplo. A mis hermanos, que también me ha acompañado durante todo este proceso. A todos mis familiares, quienes también me han acompañado durante toda mi formación y en especial a mis tíos y tías, que han compartido cada logro como si fuera propio.

A mis amigos y compañeros, que son bastantes para mencionar pero que el apoyo y la compañía de cada uno han sido muy importantes ya que ellos también ayudaron a definir la persona que soy.
A mis compañeros y tutores de CIDIC, quienes me han enseñado y aportado en gran medida. Por último quiero agradecer a los profesores Hugo Hernandez y Elkim Roa, quienes pusieron su confianza en mis capacidades y me guiaron para lograr grandes cosas.

Juan Pablo Lozano Carvajal

CONTENTS

Page

INTRODUCTION 11

1. METHODOLOGY 13

1.1. METHODOLOGY DESCRIPTION 14

2. CIRCUIT ANALYSIS RESULTS: 18

2.1. CHARGE SENSITIVE AMPLIFIER (CSA) 18

2.2. SLVS DRIVER CIRCUIT 18

2.3. PHASE-MIXER CIRCUIT 18

3. CONCLUSIONS 25

BIBLIOGRAFY 26

LIST OF FIGURES

Page

Figure 1 EAD flow 17

Figure 2 CSA testbench 19

Figure 3 SLVS testbench 20

Figure 4 Phase mixer testbench.. 20

Figure 5 CSA Layout 20

Figure 6 CSA layout closer look 21

Figure 7 TX Layout 21

Figure 8 RX layout.. 22

Figure 9 Phase mixer layout 22

LIST OF TABLES

Page

Table 1 Color scale used for EM analysis.. 14

Table 2 EM CHECK RESULTS IN THE CSA CIRCUIT.. 23

Table 3 EM CHECK RESULTS IN THE Tx CIRCUIT 23

Table 4 EM CHECK RESULTS IN THE Rx CIRCUIT.. 24

Table 5 EM CHECK RESULTS IN THE PHASE MIXER CIRCUIT 24

RESUMEN

Titulo	ESTUDIO DE LOS EFECTOS DE LA ELECTROMIGRACION Y EL IR-DROP EN LA CONFIABILIDAD DE LOS CIRCUITOS INTEGRADOS*
Autores	JUAN PABLO LOZANO CARVAJAL**
Palabras Clave	130nm, CMOS, Electromigracion, IR-drop, Confiabilidad, Microelectronica.

DESCRIPCIÓN

Una metodología para analizar los efectos generados por la Electromigración (EM) y el IR-drop en tecnología CMOS 130nm TSMC se llevó a cabo en este trabajo. La metodología implementada evita el sobredimensionamiento de la vista layout en los circuitos diseñados y reduce el tiempo de trabajo utilizado para arreglar sus defectos. Circuitos analógicos, digitales y de señal mezclada fueron analizados mostrando en el layout las estructuras del circuito donde los defectos por EM y IR-drop son críticos. Entre las soluciones más comunes utilizadas en este trabajo para solucionar los defectos encontrados en la vista layout de los circuitos analizados están. La modificación de la geometría de las interconexiones con niveles de densidad de corriente superiores a los permitidos por el Foundry; La reducción en las tensiones de alimentación para evitar niveles elevados de densidad de corriente sacrificando rendimiento del circuito y la reducción en la frecuencia de operación de los circuitos electrónicos que no permiten modificar la geometría de las interconexiones por falta de espacio libre y/o por incumplimiento de las reglas de diseño. Los resultados presentados indican que la metodología implementada es muy eficiente detectando los cuellos de botella con defectos, garantizando la integridad eléctrica del chip producido durante largo tiempo de operación y un amplio uso.

---

* Trabajo de grado

** Facultad de Ingenierías Fisico-Mecánicas. Escuela de Ingeniería Eléctrica, Electrónica y Telecomunicaciones. Director: Hugo Daniel Hernandez Herrera. Codirector: Elkim F. Roa.

ABSTRACT

Title STUDY OF ELECTROMIGRATION AND IR-DROP EFFECTS FOR CHIP RELIABILITY *

Authors JUAN PABLO LOZANO CARVAJAL**

Keywords 130nm, CMOS, Electromigration, IR-drop, Reliability, Microelectronics.

DESCRIPTION

A methodology to analyze Electromigration (EM) and IR-drop effects in TSMC 130nm CMOS technology was implemented in this work. The implemented methodology avoids oversizing of the designed circuit layout and reduces the working time used to fix them. Analog, mixed-signal and digital circuits (amplifiers, comparators, filters, phase mixers, ADCs, bandgap voltage reference, charge pumps) were analyzed showing on the layout the circuit structures where EM and IR-drop effect are critical. Among the most common solutions used in this paper to solve the defects found in the layout view of the circuits analyzed are. The modification of the geometry of the interconnection layers with current density levels higher than allowed by the company that produces the integrated circuits (Foundry); The reduction in the supply voltages to avoid high levels of current densities sacrificing circuit performance and reduction in the operating frequency of electronic circuits that do not allow to modify the geometry of the interconnections layers by lack of free space and / or failure of the layout design rules (DRC).
The presented results indicate that the implemented methodology is very efficient detecting bottleneck regions, which guarantees the electrical integrity of the produced chip during long operation time and extensive use.

---

* Bachelor degree

** Faculty of Physico-Mechanical Engineering. School of Electronics and Electrical engineering telecommunications. Director Hugo Daniel Hernandez Herrera. Codirector: ELKIM F. ROA.

INTRODUCTION

The integrated circuits have driven the technological advances in the last decades. Small electronic products with high throughput are possible today due to the integrated circuits. The high integration levels of the new generation of integrated circuits have led to that Electromigration (EM) and IR-drop fails have become serious reliability issues.

The progressive displacement in the conductors atoms generated by collisions with electrons flowing through of the material is recognized as the Electromigration (EM) phenomenon. The company that produces the integrated circuit (Foundry) sets some current density limits, for the different technology layers which compose the available devices to be used by the IC designers. During the layout phase of the simulated circuit, the interconnection metal paths and the technology devices must be dimensioned to support the current expected in a specific circuit node, according to the current density limits defined by the foundry. If the current density rules have not been attended during the layout phase, the produced chip will have a reduced lifetime.

The IR-drop is an unwanted voltage drop generated by the electrons flow resistance of the conductive material, which can affect the functionality or the expected specifications of the considered circuit. EM and IR-drop fails are detected more frequently on power nets (VDD and GND) because through these nets circulate the DC and AC current consumed by the circuit.

The IC layout designer must know the current density of each conductive layer for manually set the interconnection path dimensions which are sensitive to human error. The EM and IR-drop study on the circuit layout of Ultra-large-scale integration (ULSI) chips is a complex process due to the number of nets and metal structures that compose the chip.

Manual analysis of probable electrical or physic fails of the designed circuit during the layout phase is impossible when the circuit is composed of Millions or Billions of transistors.

The automatic analysis is possible by using professional EDA tools which integrate the current profiles of the studied circuit obtained from electrical simulations of the schematic or netlist view, with the current densities supported by the devices and interconnection materials available for the used IC technology.

To perform EM and IR-drop analysis is decisive for the IC companies because the electronic consumers want better products with higher capabilities and smaller sizes without electrical fails.

This work presents an EM and IR-drop methodology analysis implemented on the Cadence design flow in TSMC 130nm CMOs technology. The considered methodology allows detecting probable EM and IR-drop problems directly on the layout view of the designed circuit.

This work includes the experimental results produced by the implementation of an analysis methodology in a TSMC 130nm CMOS technology for (EM) and IR-drop. The proposed methodology reduces both the over-design of the electronic circuits and the time used to fix them.

1. METHODOLOGY

The new generation of EDA tools incorporate the schematic or netlist view of the circuit, the layout view of the designed circuit and the extracted view which it is a circuit netlist including parasitic capacitances and resistances introduced from the layout. Basically, to perform an EM and IR-drop analysis, the commercial EDA tools uses the electrical simulation of the schematic for tracing a current profile of each circuit node. The current density information obtained from simulation is utilized to determine if the interconnections and devices connected to a specific node satisfy the reliability rules defined by the foundry. This analysis flow can also incorporate the extraction view which requires a Layout Versus Schematic (LVS) check. There are several EDA tools companies presented on the market among which can be highlighted: Cadence, Mentor Graphics and Synopsys.

Currently, the Cadence EDA tools are the most popular and they are used for academic and industrial applications.

TSMC 130nm CMOS technology has available design kits for Cadence and Synopsys in OpenAccess database. The Cadence VIRTUOSO Layout Suite for Electrically Aware Design (EAD) tool was selected to implement the EM and IR-drop analysis flow in this work.

Cadence VIRTUOSO integrates all the required tools of analysis and verification with the design and simulation tools in the same platform, accelerating the electrical circuit specification, problems solution and the physical verification of the chip to be produced.

Cadence VIRTUOSO allows calculating the highest voltage drop in every net of the proposed circuit layout. Those values are given back to the layout designer to improve this specification when it is significant. A value up to 5\% from Supply voltage is permitted, it is 60mV for TSMC 130nm CMOS technology with a nominal supply voltage of 1.2V. The circuit performance degradation due to this voltage drop can be evaluated by post-layout simulations of the designed layout, but determinate, where the bottleneck path is placed on the circuit layout, is an intensive labor if it is performed manually. This justifies using an automatic flow to analyze the IR-drop effect directly during the layout phase before the post-layout simulation phase, reducing the total design time and avoiding over-design. Therefore, to introduce automatic IR-drop analysis in the IC traditional design flow will represent time and fabrication cost reductions.

Cadence VIRTUOSO permits to make an interactive signal analysis, highlighting EM violations on the layout using a color map. The tool will place a colorful flag on the circuit layout if an EM rule is violated or close to being violated in a specific net. A colors scale is defined by the percentage of the current density from the limit, according to the technology EM rules.

The color coding is fully customizable so it can be configured to see how far the designer is from violating the maximum current density permitted in a specific interconnection.

Table 1 presents the color scale used in this work for the EM analysis.

Table 1 Color scale used for EM analysis

% of limit	Color
25	Green
50	Yellow
75	Orange
100	Red

1.1. METHODOLOGY DESCRIPTION

In this section, a detailed description of the methodology is presented. The understanding of the theoretical basis behind (EM) and IR-drop phenomena allows the correct configuration and application of this methodology leading to a successful analysis.

As described in Figure 1 the first step of the methodology is to make the schematic view of the proposed circuit and to perform the requested electrical simulations. The IC designer should adjust the devices dimension and parameters so that it achieves the desired specifications.

When the specifications are met, a simulation testbench is configured to save the currents (average, peak & RMS) that the designer will use for EM checking in the VIRTUOSO layout EDA tool.

The results of the EM and IR-drop analysis are strongly correlated to the configuration of the simulation testbench.

When assessing the reliability of interconnection layers in a chip, there are no testing settings by default, a common practice was the usage of accelerated stress test conditions (high temperature and high current densities) which accelerate the failure mechanisms that are expected to occur under normal operational conditions.

To accelerate the failure mechanisms that are expected to occur under normal operational conditions, a common practice stresses the circuit in the corner conditions of voltage supply and temperature. These simulations on stress conditions were performed configuring the VIRTUOSO simulation tool (ADE XL /GXL), defining a high-temperature value (i.e., 110 C) and building a testbench where the maximum current flows through the circuit. This condition is obtained using the highest allowed supply voltage or operational frequency of the circuit for the related technology. The circuit under test must be working properly as designed during the testbench simulation.

Once the testbench simulation is done, the results are saved in a data set which contains all the currents values in every net of the circuit under test. The ADE XL/GXL menu includes several options to save all values from the circuit or select some nets of interest, whether if they are saved in the hard disk drive for future use or temporarily saved in memory. Also, a dynamic selection of data results from simulation in a particular time gap is available reducing the saving time of a large amount of data in the largest simulations.

The correct usage of the simulation tools is a key issue in the analysis of the circuits under test, depending on whether the circuit is analog, mixed-signal or digital, a particular setup generates more or fewer data (more or less accurate). In the majority of tests, the simulator used was Spectre.

In some digital circuits, Ultra-sim simulator was used looking for feasible simulation times due to the big size of those circuits. It is recommended to look for more instructions (advanced settings) within the simulation tools available.

EM depends on various factors, such as the local current density, homogeneity of the current flow through a region and so forth. All these factors are captured for different conductor layers and vias as rules in technology files (tech files, ICT files or EMdata files) for each process technology specification.

The tech file and ICT files are provided by the foundry. Inside there are layer definitions, tech layer properties, layer rules, Via definitions, routing specs and so forth. The ICT file contains additional information related to the fabrication technologies developed by the foundry such as WEE (wire edge enlargement) and erosion tables for example.

The EMdata file contains the information to calculate the current densities (Avg, RMS, Peak) of all layers and the maximum current density allowed. Sometimes the EMdata file is inside the tech file or ICT file, sometimes it does not even exist, then it has to be created. Based on the documents provided by the foundry the EMdata file was created this time.

Before the EM check, a setup in the layout EAD tool was required. Process, extraction, environment and electromigration options were set in the EAD setup window (based on the information available in the technology files). These settings are used during EM checking.

The layout EAD tool is where data sets (currents saved) and process technology files (tech file, ICT and EMdata) are used for EM checking.

As long as the layout is created or modified, the Layout EAD tool extracts and shows the resistance values in every net. When the EM check is performed, the actual current data and the standard EM limits specified in the technology files (EMdata file) are compared. The Layout EAD tool can be configured to dynamically run EM checks as the layout is modified.

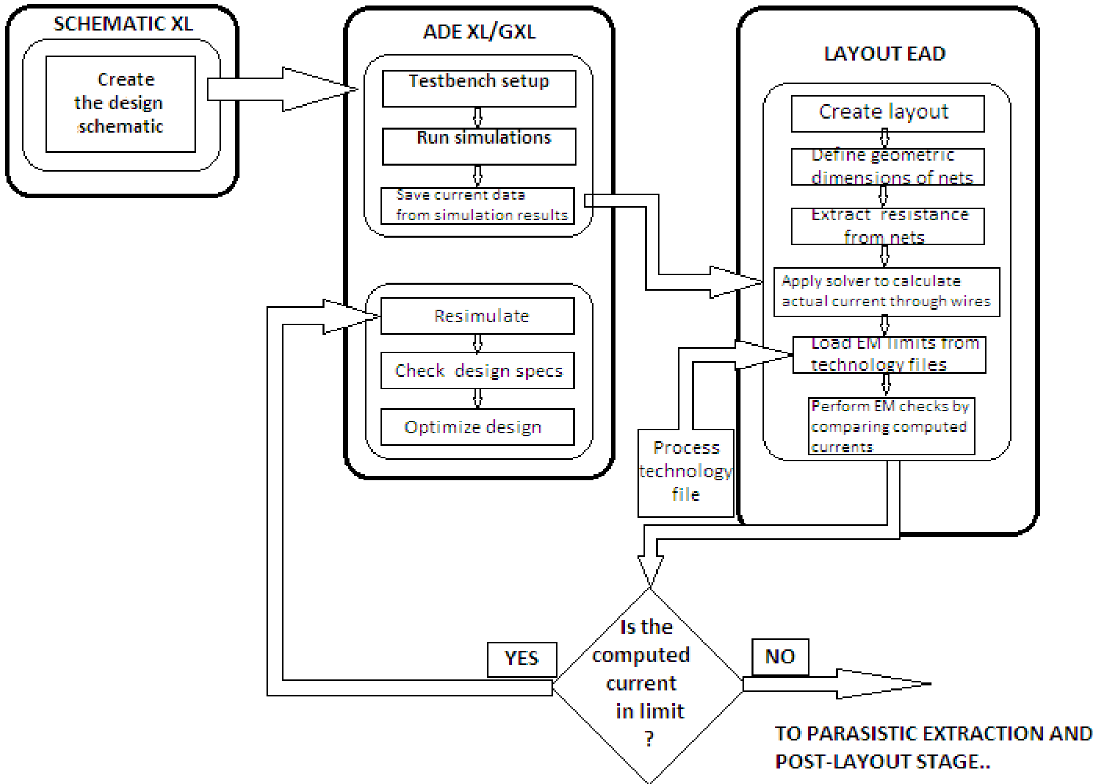
The results of EM checks are displayed in charts, indicating if the specific net passed or not the testing. The reported EM violations can be fixed by modifying the placement and routing of components in the layout or by changing the geometric properties of the nets, and then re-running the EM checks to verify the results.

The most common ways to solve the EM and IR-drop violations in this project were:

- The widening of the interconnection layers to reduce the current density inside.
- The reduction in the operational frequency of the circuit.
- The lowering in the supply voltage of the circuit.

The widening of interconnection layers took benefit from the availability of “free-space” to re-route and modify the geometric properties of the nets, then becoming the first choice to solve the EM violations. In a different scenario with limited silicon “area” or budget, the reduction and lowering of the operational frequency and supply voltage gains a higher interest.

Figure 1 EAD flow



2. CIRCUIT ANALYSIS RESULTS

The methodology is meant to be used on analog, mixed-signal and digital circuits. In this section, is shown the experimental results in a variety of electronic circuits.

Analog circuits such as low/high pass filters, nauta OTAs, charge pumps, bandgap voltage reference circuits among others, were tested following the methodology described above.

2.1. Charge sensitive amplifier (CSA)

A Charge Sensitive Amplifier (CSA) part of a gaseous detector readout front-end sensor is one of the analog circuits under test.\cite{c6} The testbench used, shown in Figure 2 resembles the actual operational conditions in the Time Projection Chamber (TPC). Where the particles (charge signal) impacting the sensor inputs are represented by a pulsed current source, then the signal is integrated and filtered by a low and high pass filters respectively, generating a Semi-Gaussian pulse as output. This pulse is converted from analog to digital domain subsequently and digitally processed in the next stages.

The analysis results show that some EM violations exist in some nets in the circuit.

All the voltage drops in nets are reported to the designer besides EM violations.

Mixed-signal circuits such as phase mixers, comparators, ADCs among others, were tested following the methodology described above.

2.2. SLVS driver circuit

The increasing processing speeds developed on the actual devices such as microprocessors, optical transmission links and routers by the actually integrated technologies, push the off-chip data rates into a whole new level. Circuits such as (Low-voltage differential signaling) are a key part of transmission systems carrying a high volume of data.

One of the mixed-signal circuits under test is an SLVS driver circuit, composed of the (TX) transmitter and (Rx) receiver. The testbench used, connects the transmitter (TX) and receiver (RX) through a channel modeled by capacitors and inductors as shown in Figure 3.

The analysis results show that some EM violations exist in some nets in the circuit. All the voltage drops in nets are reported to the designer besides the EM violations.

2.3. Phase-mixer circuit

A Phase mixer is one of the mixed-signal circuits under test. Particularly useful in high-speed serial interfaces where high-speed serial data streams are common, and the receiver needs to recover the clock in order to sample the data. The testbench used is shown in Figure 4.

The analysis results show that some EM violations exist in some nets in the circuit. All the voltage drops in nets are reported to the designer besides the EM violations.

With the digital circuits, the analysis was more challenging. The simulation using a testbench was successfully done and the corresponding data sets were created, but warning messages are displayed when the EM check is run.

Due to some inherent limitations and incompatibilities between the routing grids of the interconnection layers and the track patterns at the layout view, the successful analysis of digital circuits was not possible. The automated layout generated in digital circuits can't be analyzed with this EDA tool.

Alternative procedures were planned to solve this issue such as:

- The manual inspection of data results from simulation, aiming to save just the representative values.
- The manual verification of the layout interconnection layers, calculation of the actual current density and IR-drop value.

The latter attempts were not profitable, due to the huge number of data to handle and the absence of a clear correspondence between the net's names inside the simulation tool and the layout tool.

Figure 2 CSA testbench

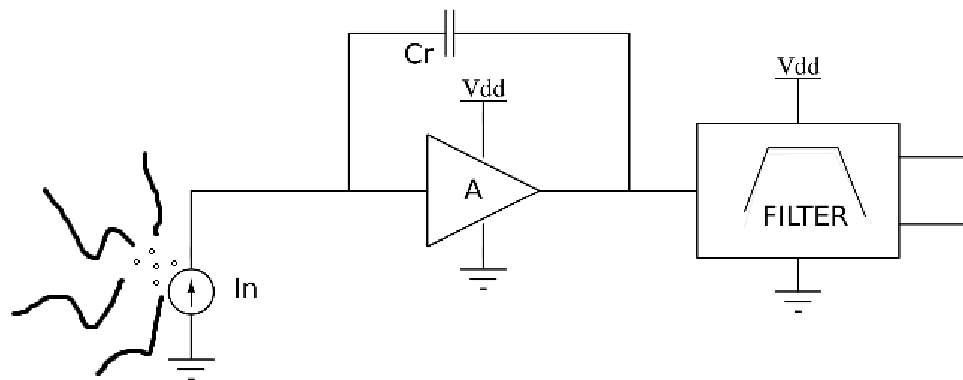


Figure 3 SLVS testbench

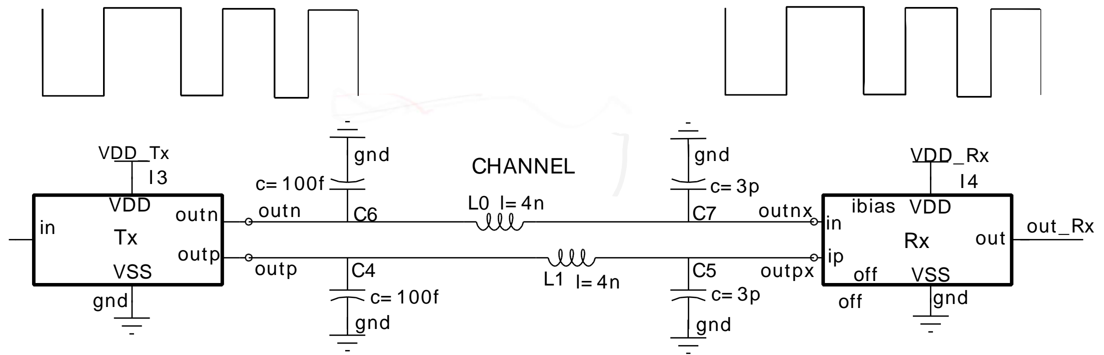


Figure 4 Phase mixer testbench

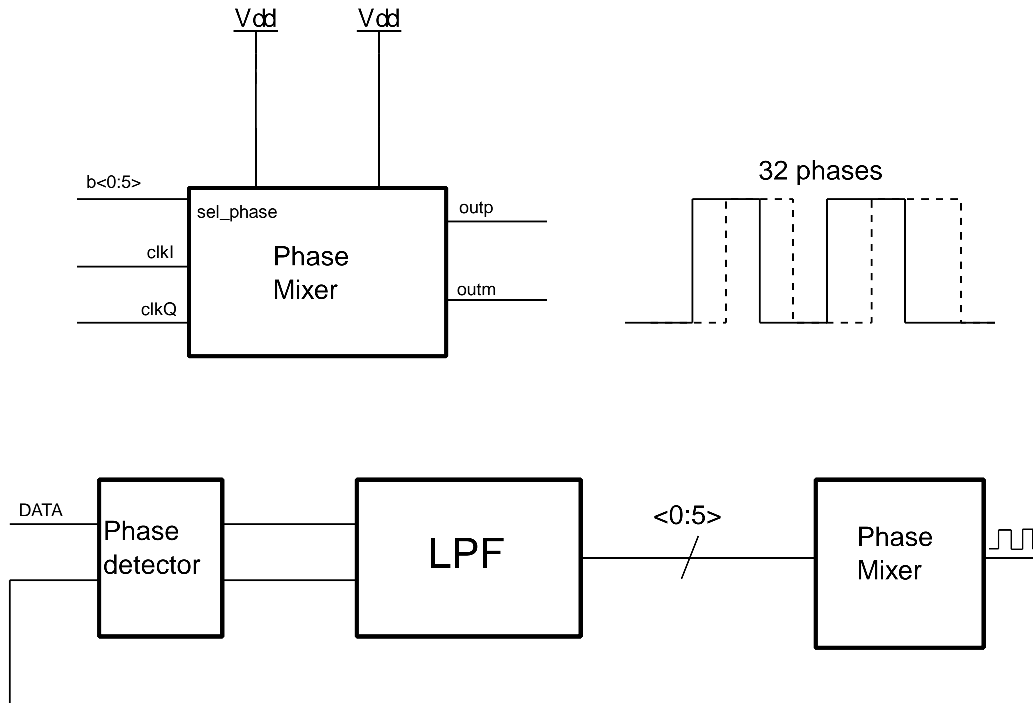


Figure 5 CSA Layout

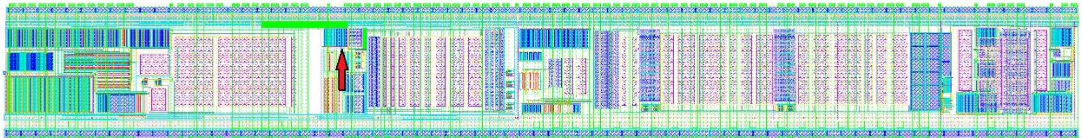


Figure 6 CSA layout closer look

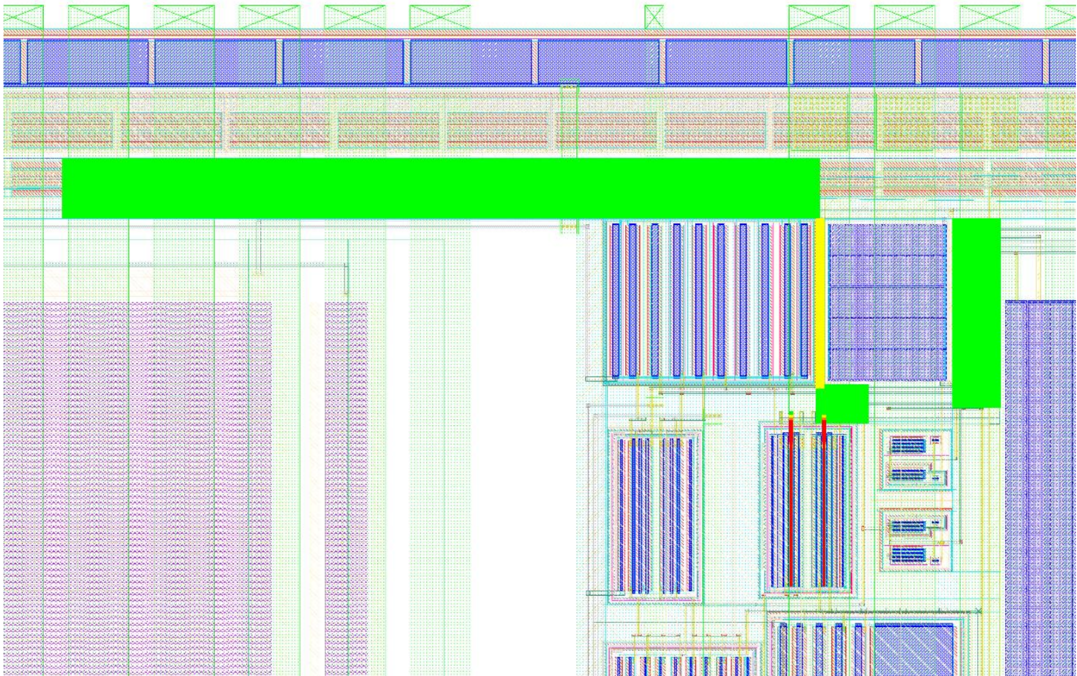


Figure 7 TX Layout

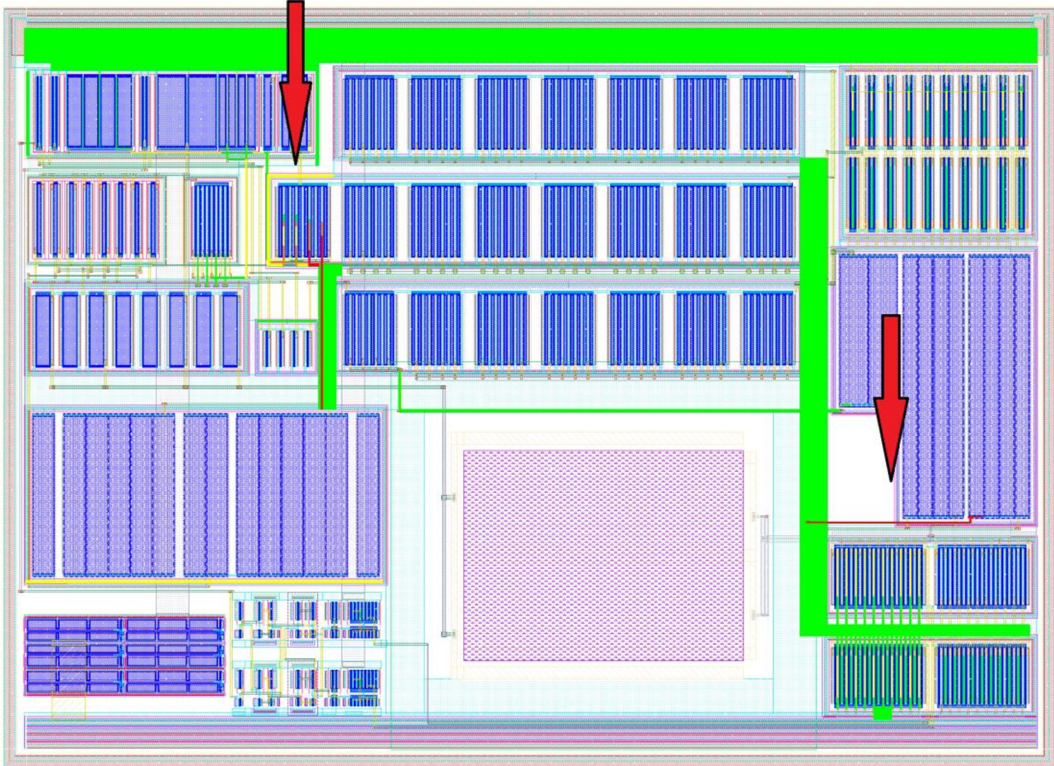


Figure 8 RX layout

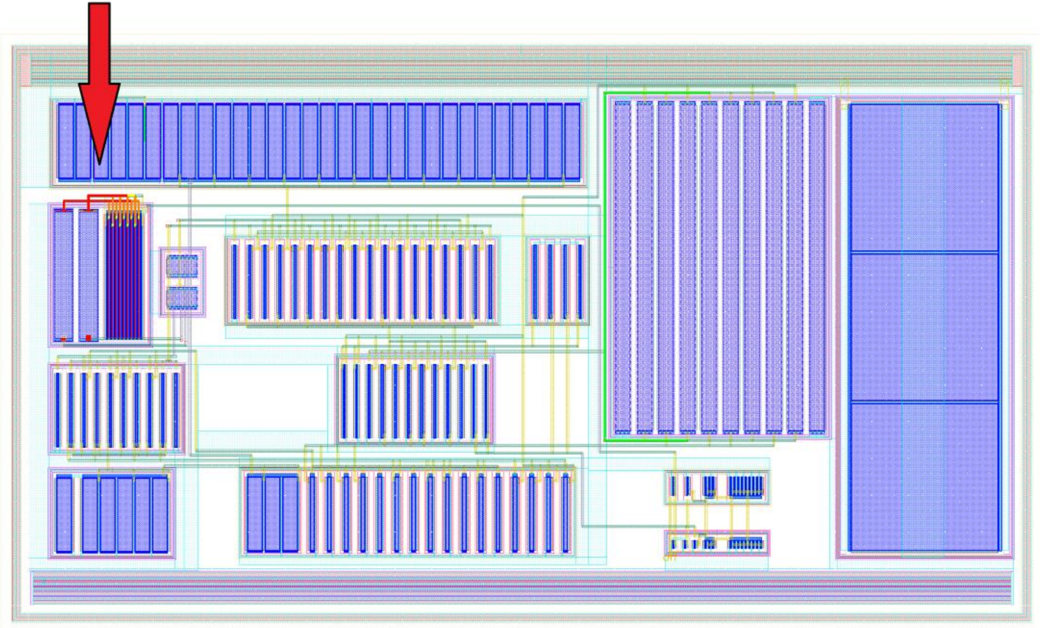


Figure 9 Phase mixer layout

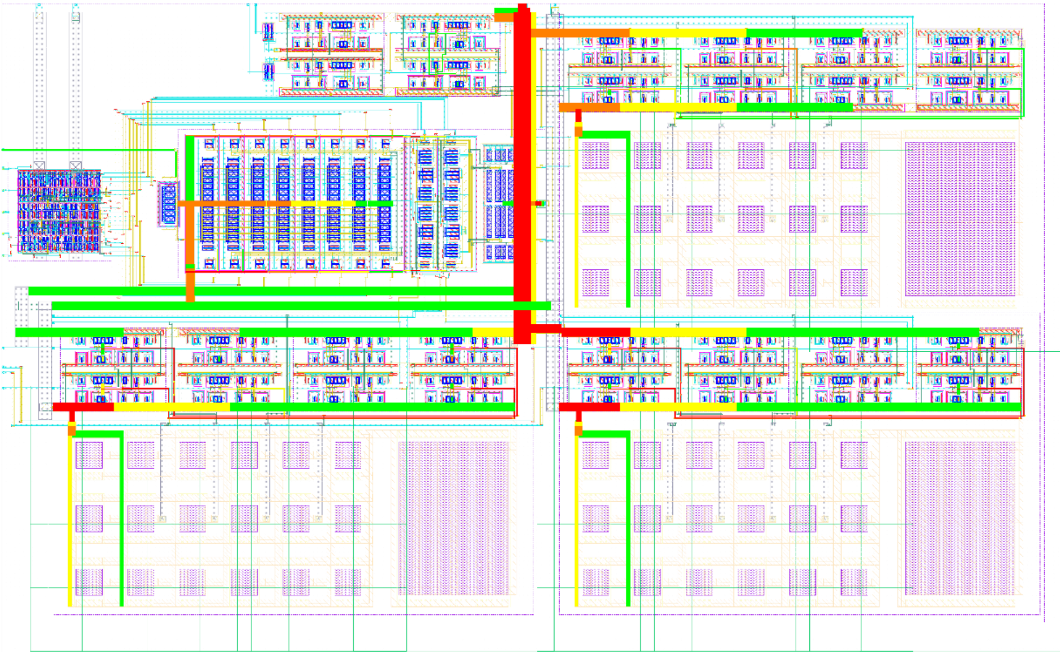


Table 2 EM CHECK RESULTS IN THE CSA CIRCUIT

Net	Total R	EM Viol	J/Jmax	Max Drop
|I27/net0	6.62E+03	102	2.142	7.66E-02
VDD	2.52E+03	32	6.24	2.41E-02
|I27/net0	1.75E+03	72	1.774	6.34E-02
out_f2p	2.01E+03	76	1.751	3.97E-02
out_f2n	1.65E+03	76	1.748	4.86E-02
|I27/inpx	2.40E+03	0	6.74E-02	5.28E-04
|I28/net5	95.79	0	5.86E-02	6.26E-05
|I28/net6	95.16	0	5.58E-02	5.96E-05
out_f1n	4.91E+03	0	1.13E-02	2.33E-04
|I28/net0	224.7	0	3.34E-03	8.04E-06

Table 3 EM CHECK RESULTS IN THE Tx CIRCUIT

Net	Total R	EM Viol	J/Jmax	Max Drop
|I0/nn	655.1	18	8.909	1.95E-02
VSS	5.22E+04	21	1.591	2.97E-03
|I0/net02	1.61E+04	0	6.10E-01	2.33E-03
VDD	303.9	0	5.98E-01	7.37E-03
outp	156.4	0	5.41E-01	1.84E-03
|I0/vbp	1.02E+03	0	5.38E-01	3.20E-03
|I0/net04	486.1	0	4.06E-01	8.04E-03
vin	2.76E+04	0	3.85E-01	3.08E-04
vip	2.76E+04	0	3.82E-01	3.06E-04
|I0/net07	1.14E+03	0	2.37E-01	3.37E-03

Table 4 EM CHECK RESULTS IN THE Rx CIRCUIT

Net	Total R	EM Viol	J/Jmax	Max Drop
net029	155.8	22	4.24	9.03E-02
net033	164.9	17	2.673	5.98E-02
in	18.46	1	2.257	7.14E-05
ip	155.5	1	2.217	9.22E-05
net013	2.44E+03	0	3.45E-01	8.84E-03
ibias	3.22E+03	0	2.70E-01	3.04E-04
VDD	4.24E+03	0	2.05E-01	9.17E-04
out	23.47	0	8.29E-02	9.79E-05
VSS	1.31E+04	0	7.07E-02	1.27E-04
net028	1.92E+03	0	5.32E-02	5.89E-05

Table 5 EM CHECK RESULTS IN THE PHASE MIXER CIRCUIT

Net	Total R	EM Viol	J/Jmax	Max Drop
agnd	1.23E+04	32	2.634	3.22E-02
avdd	2.19E+03	21	4.211	2.28E-02
|FilterOut	5.37E+03	10	1.258	1.25E-02
|FilterOut	5.36E+03	9	1.347	1.00E-02
ain_ckIpm	3.80E+03	0	2.22E-01	3.00E-04
ain_ckIpm	3.79E+03	0	2.07E-01	2.86E-04
ain_ckQpr	3.81E+03	0	2.13E-01	4.09E-04
ain_ckQpr	3.80E+03	0	2.09E-01	2.93E-04
aout_naut	645.8	0	1.30E-02	7.96E-06
aout_naut	641.2	0	3.52E-02	2.13E-05

3. CONCLUSIONS

In this paper, an Electromigration and IR-drop analysis methodology implementation was presented. A detailed description of analysis results after the methodology application in Analog and Mixed-signal circuits were also discussed. The implemented methodology reduces both the over-design of the electronic circuits and the time used to fix them, in the same way, it allows to analyze, verify and correct in real time the created layout view. In spite of the circuits under analysis were designed and they will be fabricated in a 130nm TSMC CMOS technology, this methodology is independent of the considered process technology. This characteristic is the most salient advantage of the implemented methodology.

For future work, the usage of this methodology in combination with another tool specialized in the analysis of digital circuits will allow a complete inspection of the design integrity issues not only at the circuit level but at the full chip level too.

BIBLIOGRAFY

ALPHA AND OMEGA SEMICONDUCTOR, Power Semiconductor Reliability Handbook. [Online] Alpha and Omega Semiconductor. [Sunnyvale. CA U.S.A], 2010. [Cited 30 Oct 2015] Available From The Internet: http://www.aosmd.com/media/reliability-handbook.pdf

CADENCE DESIGN SYSTEMS, Cadence Virtuoso Layout Suite for Electrically Aware Design. [Online] Cadence Virtuoso. [San Jose. CA U.S.A] Cadence Design Systems, 2013. [Cited 30 Oct 2015] Available From The Internet: http://www.cadence.com/rl/Resources/datasheets/electrically_aware_design_ds.pdf

HERNANDEZ Hugo, VAN NOIJE Wilhelmus, Noise reduction of a Charge Sensitive Amplifier for gaseous detector readout front-ends, 2015. [Online] 2015 IEEE International Symposium on Circuits and Systems (ISCAS), May 2015 [Cited 30 Oct 2015], pp. 1058 – 1061. Available from IEEE Xplore digital library.

KING-NING Tu. Solder Joint Technology Materials, Properties, and Reliability. Los Angeles: Springer Science+Business Media LLC, 2007.

LIMING XIU. VLSI Circuit Design Methodology Demystified A Conceptual Taxonomy. Piscataway, NJ: John Wiley & Sons, Inc., 2008.

ON SEMICONDUCTOR, Quality and Reliability Handbook. [Online] Literature Distribution Center for ON Semiconductor. [Phoenix, AZ U.S.A], 2014. [Cited 30 Oct 2015] Available From The Internet: http://www.onsemi.com/pub_link/Collateral/HBD851-D.PDF