# DESIGN OF ENERGY-EFFICIENT VOLTAGE COMPARATORS FOR A SYSTEM-ON-CHIP USING A CMOS TECHNOLOGY NODE OF 28NM

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**Degree work presented as a requirement to qualify for the title of Electronic Engineer**

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# RESUMEN

**TÍTULO:** DISEÑO DE COMPARADORES DE VOLTAGE ENERGETICAMENTE EFICIENTES PARA UN SISTEMA EN CHIP EN UNA TECNOLOGIA CMOS DE 28NM [*]

**AUTORES:** DANIEL FELIPE BARRIOS RUEDA
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**PALABRAS CLAVE:** Comparadores, Offset, Latch, Histeresis, Efectos de Retroalimentacion

**DESCRIPCIÓN:**

En respuesta a los recientes avances tecnológicos que exigen sistemas en chip (SoC) más pequeños y rápidos para cumplir con las necesidades computacionales, minimizando el consumo energético, el grupo de investigación en microelectrónica OnChip tomó la iniciativa de desarrollar un nuevo microcontrolador de baja potencia utilizando una tecnología CMOS de 28 nm, dentro del cual, uno de los bloques es el centro de este proyecto, el cual se basa en diseñar dos comparadores energéticamente eficientes: un comparador estático (tiempo continuo) y un comparador dinámico (con reloj).

Diferentes retos surgen durante el diseño debido a las restricciones en el consumo de corriente, el tiempo de respuesta y el offset referido a la entrada. De la misma forma, la tecnología de 28nm también presenta un conjunto de retos que implican pronunciadas variaciones e inconsistencias en el rendimiento de los dispositivos después de la fabricación, causado por las reducidas dimensiones físicas, como lo son, la corriente de fuga (leakage), desigualdades entre transistores, y elementos parásitos.

Este trabajo detalla el funcionamiento de los comparadores y las decisiones de diseño consideradas para entender el diseño final, el cual es presentado como esquemático y layout.

Por último, este diseño se valida mediante simulación, que incluye extremos estadísticos de proceso, tensión y temperatura (PVT), así como variaciones de Monte Carlo de parámetros y la extracción de efectos parásitos (resistencias y capacitancias) post-layout.

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[*] Trabajo de Grado

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# ABSTRACT

**TITLE:** DESIGN OF ENERGY-EFFICIENT VOLTAGE COMPARATORS FOR A SYSTEM-ON-CHIP USING A CMOS TECHNOLOGY NODE OF 28NM [*]

**AUTHORS:** DANIEL FELIPE BARRIOS RUEDA
NESTOR IVAN MATAJIRA ORTIZ [**]

**KEYWORDS:** Comparators, Offset, Latch, Hysteresis, Feedback Effects

**DESCRIPTION:**

In response to the recent technological advancements that necessitate smaller and faster systems-on-chip (SoC) to meet computational power demands while minimizing power consumption, the microelectronics research group OnChip has taken a proactive approach by developing a new low-power microcontroller using a 28nm CMOS technology node, inside of which, one of the blocks in this is the focus of this work, which involves designing two energy-efficient voltage comparators: a static (continuous time) comparator and a dynamic (clocked) comparator.

Different challenges arise in the design due to restrictions on current consumption, time delay, and input referred offset. The 28nm technology also presents another set of challenges involving pronounced variations and inconsistencies in device performance after fabrication caused by the smaller physical dimensions, such as current leakage, mismatches, and parasitics. Furthermore, the research involves conducting additional measurements to characterize the comparators, including the input common-mode range (ICMR), input referred noise, slew rate, and other relevant parameters.

This work contains the comparator's functioning and the design decisions made to comprehend the final design, presented in schematic and layout forms.

Finally, the design undergoes validation through simulation, encompassing statistical corners of process, voltage, and temperature (PVT), as well as Monte Carlo variation of parameters and post-layout parasitic (resistances and capacitances) extraction.

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[*] BSc Thesis

[**] Facultad de Ingenierías Físico-Mecánicas. Escuela de Ingenierías Eléctrica, Electrónica y de Telecomunicaciones. Advisor: JAVIER FERNEY ARDILA OCHOA

# INTRODUCTION

Inside the incredibly complex system of a microcontroller, there are many different blocks, each with its purpose to achieve the desired functionality. One of these blocks, and the main component of many of the systems, such as regulators, converters, and modulators inside the chip, is the comparator. Comparators play the essential role as decision-making devices, comparing two analog voltage inputs and producing a digital output based on their relative magnitudes. This digital output triggers specific actions or adjustments within the microcontroller, enabling precise regulation and response to changing conditions inputs.

The microelectronics research group OnChip is developing a new microcontroller composed of multiple blocks that enable its operation, including the processor, power management units, oscillators, analog to digital converters, and others. The project aims to develop general-purpose voltage comparators with minimal power consumption while maintaining a high-speed response.

To carry out the project, it required understanding the circuit's topology and the parameters affecting the characteristics and performance of the comparators. This thesis presents the design process and the information considered in decision-making.

Consequently, the order is as follows: The first and second chapters present detailed information about the comparator, then chapter three examines the characteristics of the comparator and the factors influencing the design process, and finally, the results of the schematic simulations and final layout, along with conclusions and recommendations for future work.

# 1. PROJECT OVERVIEW

## 1.1. MOTIVATION AND OBJECTIVES

A comparator stands as one of the fundamental building blocks within integrated circuits, serving as the foundation for various functionalities such as analog-to-digital converters (ADCs), zero-crossing detectors, and voltage monitors like brown-out detectors (BOD) and power-on-reset (POR) modules. Some authors have asserted that comparators are perhaps the second most prevalent analog building block after operational amplifiers (OP Amps) [1]. With this assertion in mind, the primary motivation behind this project is to gain practical experience in microelectronics and analog circuit design, thereby honing circuit analysis and problem-solving skills.

The project aims to design energy-efficient dynamic and static comparators for a System-On-Chip utilizing a 28nm technology node and meet specifications including response times, power consumption, and addressing non-idealities such as offset and gain. Subsequently, the next phase will entail executing the layout design while adhering to best practices to ensure that the post-layout simulations validate the specifications, preparing the circuit for fabrication.

## 1.2. COMPARATOR OPERATION

A comparator functions as a non-linear circuit, comparing an analog input with another analog input or a fixed reference, providing a binary output based on the comparison. This component finds widespread application in voltage regulation, zero-crossing detection, analog-to-digital conversion, among others.

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[1] Tony CHAN, David JOHNS, and Martin KENNETH. *Analog Integrated Circuits Desing*. 2nd. John Wiley Sons, Inc, 2012.

Figure 1 depicts the symbol of a comparator, while Figure 2 illustrates its ideal transfer characteristic. In the perfect scenario, the output is high when the difference between the inputs ($V_p$ and $V_n$) is positive and low when the difference is negative.

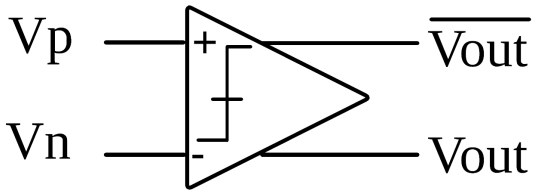


**Figure 1.** *Comparator Block.*

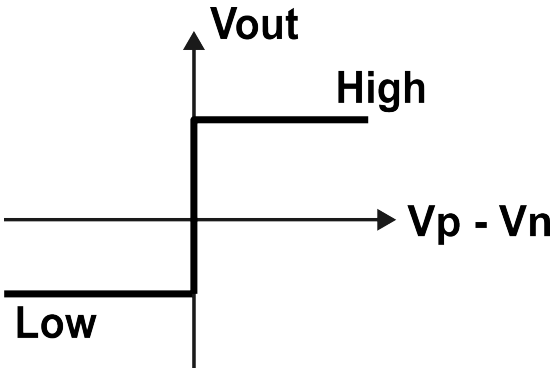


**Figure 2.** *Ideal transfer curve of a comparator.*

All comparators adhere to the block diagram in Figure 3. They typically comprise three stages: preamplification, decision, and post-amplification. While in some instances , each stage may output single-ended signals, a differential output can reduce asymmetry-related issues such as offset [2]. The preamplification stage encompasses a low-gain, high-speed amplifier that amplifies the small differential input values to levels suitable for subsequent processing. Subsequently, the decision stage, as implied by its name, determines the output state, primarily through positive feedback or high-gain

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[2] Phillip ALLEN and Douglas HOLBERG. *CMOS Analog Circuit Design*. 3rd. Oxford University Press, 2012.

mechanisms. Finally, the output connects to the post-amplification stage, where it interfaces with driving stages such as inverters or buffers to enhance speed and signal integrity.

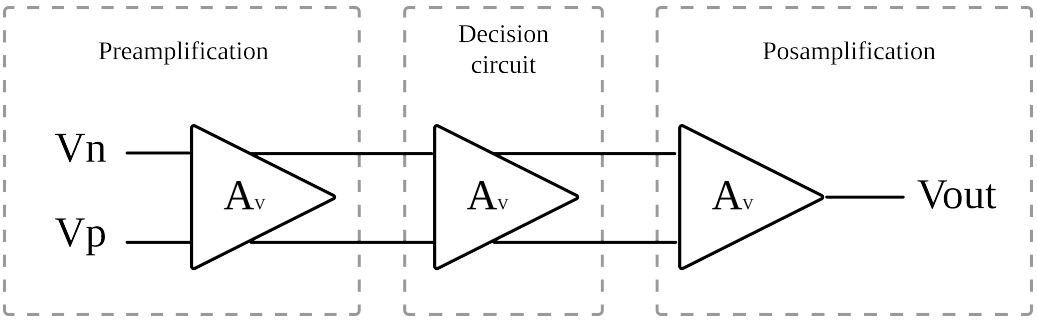


**Figure 3.** *General comparator block diagram.*

Comparators fall into two general categories, static and dynamic, depending on their use of a clock signal [3]. Below are described the advantages and disadvantages of each category.

**Static Comparator** A static comparator functions as a high-resolution, high-speed open-loop amplifier that typically lacks compensation due to its tendency to introduce undesirable delays and because stability concerns are minimal. Figure 4 illustrates an elementary static comparator, where both signals undergo comparison within the differential pair, and subsequently, an inverter drives the output to achieve a rail-to-rail value.

Some topologies utilize positive feedback, such as cross-coupled transistors or unbalanced differential pairs [4] , in order to improve the transient response, as well as the gain [3].

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[3] Bernhard GOLL and Horst ZIMMERMAN. *Comparators in Nanometer CMOS Technology*. Springer, 2016.

[4] José MOUTINHO. “Automatic sizing of continous-time comparators using a generic cell library”. In: (2016).

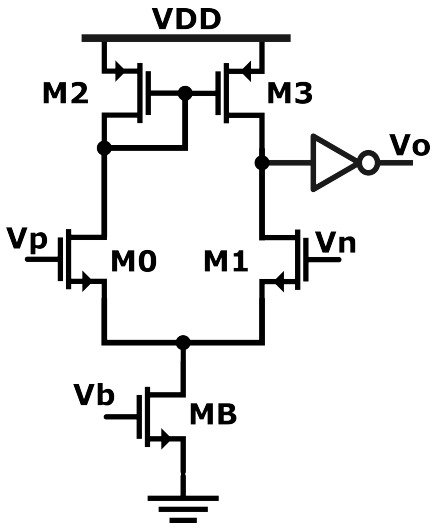


**Figure 4.** *Example schematic of a static comparator.*

**Dynamic Comparator** A dynamic comparator, as depicted in Figure 5, comprises inputs and a clock signal, which activates the transistors for comparison. Most topologies use a simple preamplifier stage, such as a differential pair, and employ a clocked latch as the decision stage. For instance, a StrongARM latch reduces the gain requirements in the preamplification stage and outputs rail-to-rail voltages, albeit with invalid responses for half a clock cycle [3]. Dynamic comparators offer the advantage of power consumption only during clock transitions.

### 1.2.1. COMPARATOR MEASUREMENTS

Below are the main electrical performance parameters of the comparators:

**Propagation Delay.** The propagation delay represents the time it takes for a change in the input to manifest as a change in the output. Usually, this duration is measured

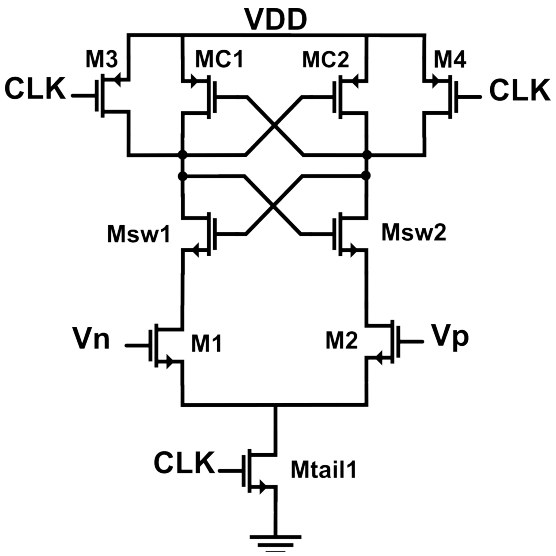


**Figure 5.** *Example schematic of a dynamic comparator.*

from a 50% transition at the input to a 50% transition at the output. In the case of a static comparator, the delay from the clock signal to the output is also quantified. This value is dependent on the difference between inputs. The units of this parameter are seconds.

**Bandwidth.** Bandwidth is defined as the maximum switching frequency of the inputs that achieves the desired specifications. Measured in Hertz.

**Sensitivity.** Sensitivity refers to the minimum differential voltage input required for the comparator to generate a consistent output. In this case, it represents the minimum input difference necessary to achieve the specified propagation delay[5]. The units of this parameter are volts.

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[5] Franco MALOBERTI. *Analog design for CMOS VLSI systems*. 1st. Kluwer Academic, 2001.

**Input Referred Offset.** The voltage required at the input to obtain the crossing point between low and high logic levels reflects the effect of mismatches and asymmetries among the components in the signal's path[3]. The units of this parameter are Volts.

**Current Consumption.** The circuit's current consumption indicates the amount of current it utilizes. This consumption comprises static consumption, occurring when the circuit reaches a stable state, and dynamic consumption, which represents the average current during switching, primarily depends on the clock frequency and capacitances. The units are Amperes.

**Gain.** A measure of the increase in magnitude at the output relative to the input is utilized, particularly in comparators where open-loop gain is employed. Figure 6 shows the transfer curve of a comparator with finite gain and offset. The units of this parameter are decibels (dB) or volts per volt (Volts/Volts).

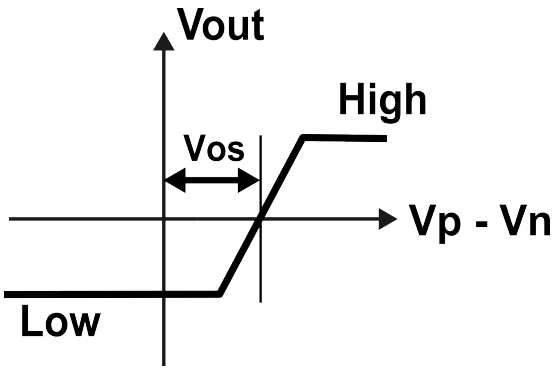


**Figure 6.** *Transfer curve of a non-ideal comparator.*

**Input Common Mode Range (ICMR).** The range encompasses the minimum and maximum values required to meet the desired specifications. In the context of a comparator, this range corresponds to only one of the inputs. The units of this parameter are volts.

**Power Supply Rejection (PSR).** It represents the circuit's ability to reject signals originating from the power supply sources. Similar to gain, the units of this parameter are decibels (dB) or volts per volt (Volts/Volts) [6].

**Hysteresis.** Hysteresis quantifies the voltage disparity between the rising and falling thresholds in the comparator. This feature aids in mitigating rapid oscillation or false triggering induced by noise or input voltage fluctuations around the threshold level [7], Figure 7 illustrates the transfer curve of a comparator exhibiting hysteresis. The units of this parameter are volts.

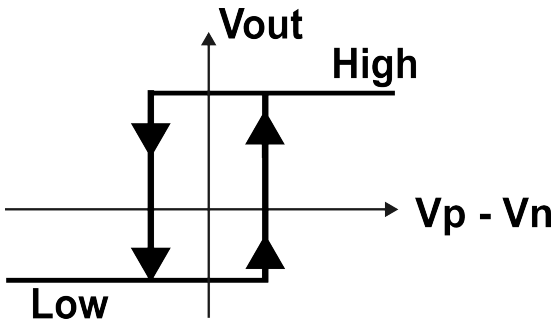


**Figure 7.** *Transfer curve of a comparator with hysteresis.*

**Input Referred Noise.** Noise, a random phenomenon, remains unpredictable even when all previous conditions and time values are known. Instead, researchers can define a statistical model using the signal's spectral density. From this model, one can derive an average power and RMS value of the noise[6], which may represent a random voltage source at one of the inputs. In a comparator, noise may alter decision-making and result in constant undesired switching. The units of this parameter are RMS volts.

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[6] Behzad RAZAVI. *Design of Analog CMOS Integrated Circuits*. 2nd. McGraw-Hill Education, 2017.

[7] Behzad RAZAVI. *Fundamentals of Microelectronics*. John Wiley and Sons, Inc., 2014.

**Offset Voltage Drift.** Due to the influence of temperature on semiconductor device operation, variations in asymmetry change with temperature fluctuations, also affecting offset. Therefore, temperature stability is a critical factor in the performance of the comparator. The units of this parameter are microvolts per degree Celsius ($\mu$V/C)[8].

## 1.3. STATE OF THE ART

Many different topologies exist thanks to newly proposed ideas that achieve the desired behavior. Below are described the advantages and disadvantages of the most relevant comparators' designs from papers and books.

### 1.3.1. STATIC COMPARATOR

Non-clocked comparators fall under different names, such as continuous-time comparators (CT), static comparators, and time-domain comparators. The following are some of the most popular topologies.

#### Open-loop Comparator

A simple open-loop comparator, shown in Figure 8, works similarly to an OPAMP with rail-to-rail output provided by an inverter. This circuit is fast due to only having two poles and is very simple, reducing the complexity of layout placement and routing. The drawback of this topology comes from its only stage that sacrifices low gain for high speed, resulting in metastable response for low differential input signals.

#### General Purpose Comparator

This topology seen in Figure 9 adds one extra stage of positive feedback, the cross-coupled transistors, which achieve high speeds without sacrificing gain. This topology

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[8] Peter WILSON. *The Circuit Designer's Companion*. 1st. Elsevier, 2012.

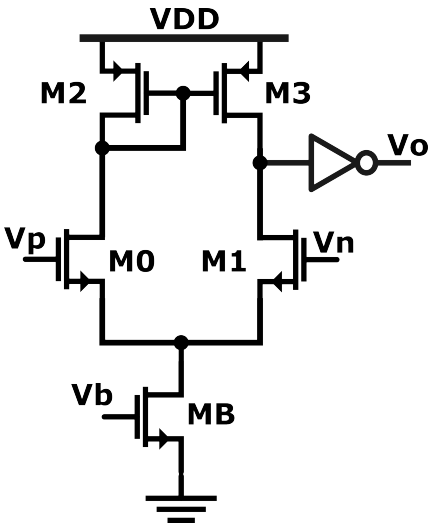


**Figure 8.** *Open-loop Comparator.*

requires four total stages to maintain the expected response, meaning high static current overall and extra matching transistors, which can cause offset.

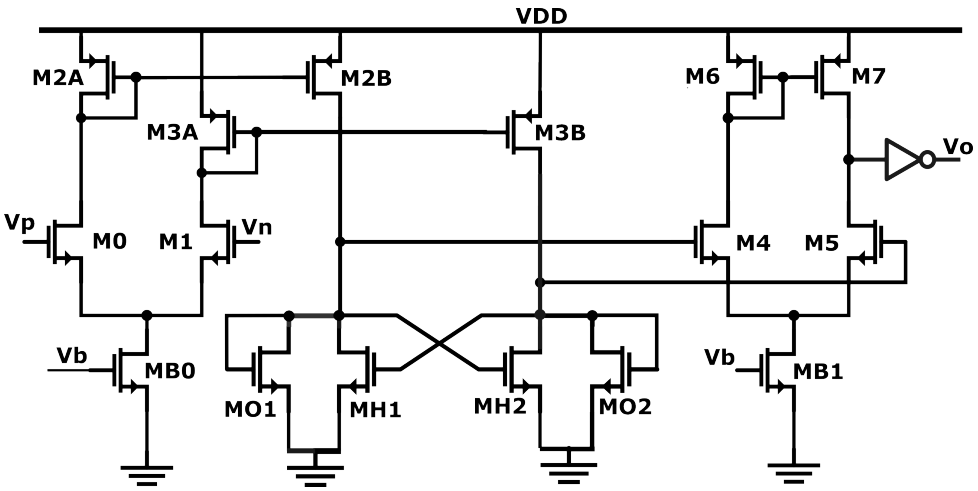


**Figure 9.** *General Purpose Comparator.*

### Park Comparator

The topology seen in Figure 10 consists of a dual PMOS and NMOS input pair with added diode-connected pairs on each side, providing a rail-to-rail differential input,

with extra DC gain near $V_{DD}$ or $V_{SS}$ reference values [9]. For analog to digital converters and zero-crossing detectors, this topology works excellently. Nonetheless, due to the nature of the topology, non-fixed references can have low-speed outputs and be very susceptible to mismatch.

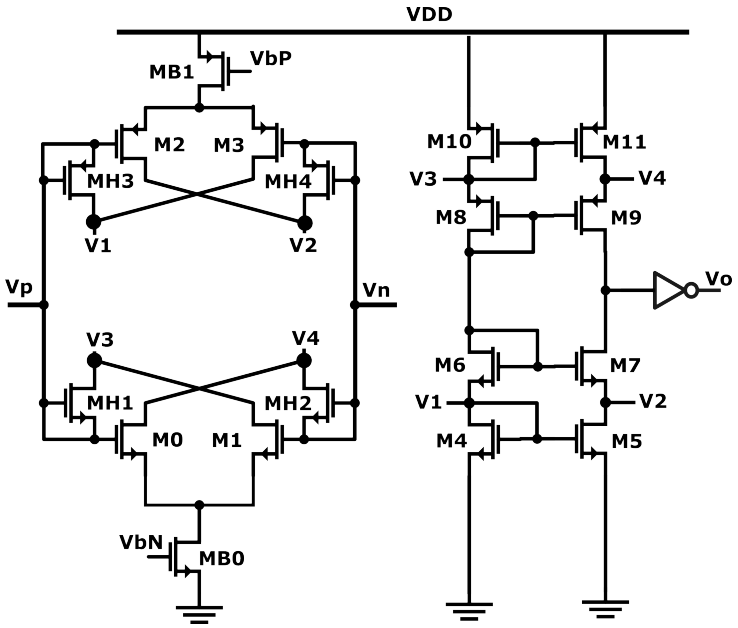


**Figure 10.** *Park's Comparator.*

### Chu Comparator

Lastly, the topology shown in Figure 11, similarly to the previous comparator, adds another input and decision stage for rail-to-rail input realization and uses a switch to control the desired output. The main issue with this topology is the loading of the secondary PMOS stage, which leads to slow output times and a possible cross-over

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[9] Park SANGBEOM, E.W. GREENEICH, and T.A. DEMASSA. "Low-power transistor-string and new rail-to-rail comparator in A/D converter". In: *42nd Midwest Symposium on Circuits and Systems (Cat. No.99CH36356)*. Vol. 1. 1999, 194–197 vol. 1. DOI: 10.1109/MWSCAS.1999.867241.

current if the switches are not properly turned off [10].

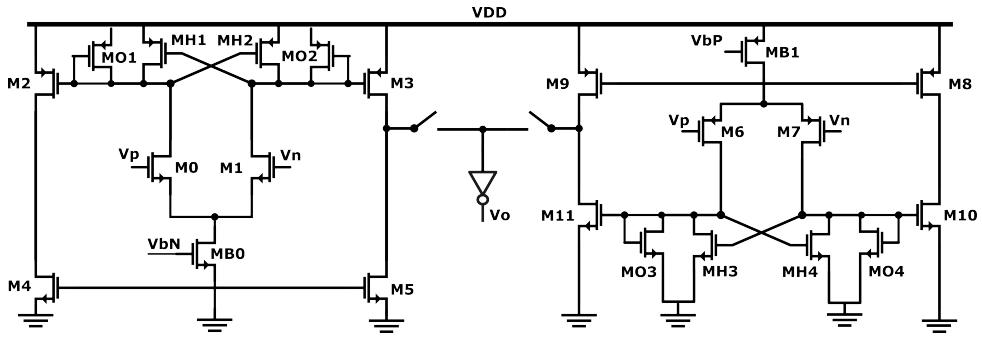


**Figure 11.** *Chu's Comparator.*

### 1.3.2. DYNAMIC COMPARATOR

After reviewing the literature, the two most common topologies are StrongARM and the double tail. The paper [11] introduced a third version, which is a combination of the previously mentioned. Below is the description of each of them.

#### Conventional Dynamic Comparator or StrongARM

Figure 12 shows the classic dynamic comparator, also called StrongARM. This topology has high input impedance, rail-to-rail output swing, and no static power consumption. The behavior is the following. During the reset phase ($CLK = 0$), $M_{tail}$ is off, and the transistors $M_3$ and $M_4$ pull the nodes $Out_N$ and $Out_P$ to $V_{DD}$, and in the decision phase ($CLK = V_{DD}$) transistors $M_3$ and $M_4$ are off, $M_{tail}$ is on and the nodes $Out_N$ and $Out_P$ start to discharge from $V_{DD}$ with different speed depending of $INN$

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[10] Chu WEI-SHANG and K.W. CURRENT. "A rail-to-rail input-range CMOS voltage comparator". In: *Proceedings of 40th Midwest Symposium on Circuits and Systems. Dedicated to the Memory of Professor Mac Van Valkenburg*. Vol. 1. 1997, 160–163 vol.1. DOI: 10.1109/MWSCAS.1997.666058.

[11] Samaneh BABAYAN-MASHHADI and Reza LOTFI. "Analysis and Design of a Low-Voltage Low-Power Double-Tail Comparator". In: *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 22.2 (2014), pp. 343–352. DOI: 10.1109/TVLSI.2013.2241799.

and $INP$. Assuming that $INN > INP$, $Out_P$ discharges slower than $Out_N$, therefore when $Out_N$ falls to $VDD - |V_{thp}|$ the PMOS transistor ($M_{C2}$) turns on initiating the latch regeneration causing $Out_N$ to discharge to $V_{SS}$ and $Out_P$ to increase to $V_{DD}$.

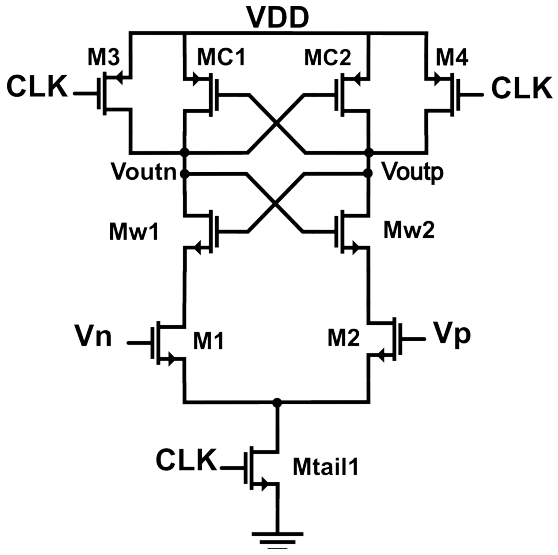


**Figure 12.** *Conventional Dynamic Comparator or StrongARM.*

### Conventional Double-Tail Dynamic Comparator

Figure 13 shows the schematic of a conventional double-tail comparator. This topology has less stacking and can work at lower supply voltages when compared to the StrongARM. This topology has two phases. The first one is known as reset, which begins when the CLK is low, thus causing transistors $M_{tail1}$ and $M_{tail2}$ to be off, and the nodes $f_P$ and $f_N$ are precharged to $V_{DD}$, making transistors $M_{R1}$ and $M_{R2}$ discharge the outputs. The second is the decision phase, which occurs when CLK is high. Here, $M_{tail1}$ and $M_{tail2}$ turn on, making the voltages at nodes $f_P$ and $f_N$ fall with a rate defined by $INN$ and $INP$. Then, the voltage difference $\Delta V_{fn(p)}$ passes from $M_{R1}$ and $M_{R2}$ to the cross-coupled inverters, and similar to the StrongARM topology, it initiates latch regeneration.

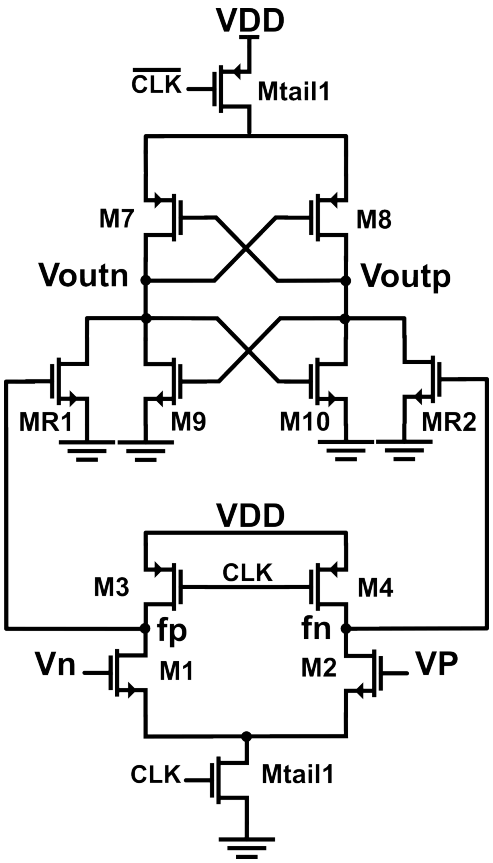


**Figure 13.** *Conventional Double-Tail Dynamic Comparator.*

**Proposed Double-Tail Dynamic Comparator** Figure 14 shows the circuit's schematic. This topology presents a combination of StrongARM and conventional Double-Tail, and the operation is the same. The objective of this comparator is a better performance of double-tail in low-voltage applications. The main idea is to increase $\Delta V_{fn/fp}$ to obtain more speed.

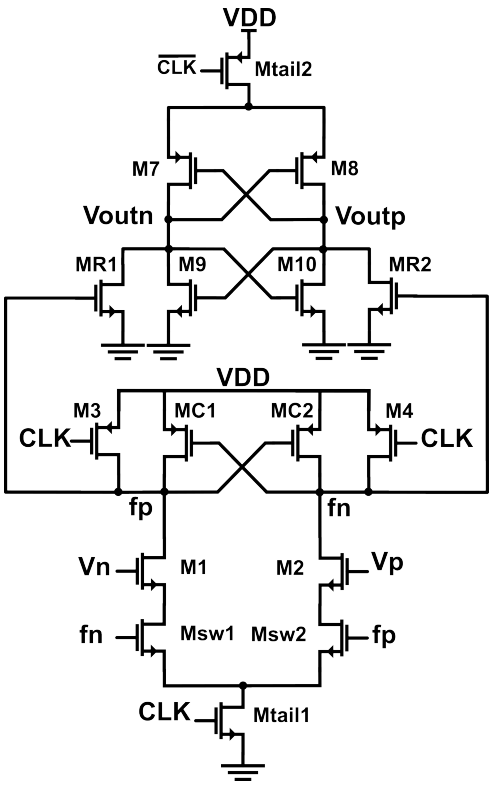


**Figure 14.** *Proposed Double-Tail Dynamic Comparator.*

### 1.4. DESIGN SPECIFICATIONS

The Table 1 lists the key design specifications for each of the comparators. These specifications form the basis of the design process and the decisions to obtain the best results.

#### 1.4.1. STATIC COMPARATOR

Considering the electrical specifications, the chosen topology for the static comparator is the one shown in Figure 9, as there is no explicit application and, although it is not the fastest nor the least consuming, it can achieve most parameters without sacrificing others.

**Table 1.** *Requirements for design for the static comparator.*

| Parameters | Units | Design Target | | |
|---|---|---|---|---|
| | | $Min$ | $Typ$ | $Max$ |
| Current Consumption | uA | - | - | 25 |
| ICMR | V | TBS* | - | TBS* |
| Slew Rate | V/ns | - | TBS* | - |
| Bandwidth | MHz | 5 | - | - |
| Propagation Delay (in-out) | ns | - | - | 50 |
| Input Referred Noise | V/Hz | - | TBS* | - |
| Sensitivity | mV | - | TBS* | - |
| Offset Voltage | mV | -5 | - | 5 |
| Offset Voltage Drift | uV/℃ | - | TBS* | - |
| PSR | dB | - | TBS* | - |
| DC Gain | dB | - | TBS* | - |
| Hysteresis | V | - | TBS* | - |

*TBS: To be simulated.

### 1.4.2. DYNAMIC COMPARATOR

Considering the specifications shown in the Table 2, the chosen topology for the dynamic comparator is the StrongARM Comparator, illustrated in Figure 12. The main reason for making this choice is that since the StrongARM is a single-stage comparator, it has less power consumption, which is the principal aim of the project.

**Table 2.** *Requirements for design for the dynamic comparator.*

| Parameters | Units | Design Target | | |
|---|---|---|---|---|
| | | $Min$ | $Typ$ | $Max$ |
| Static Consumption | nA | - | - | 5 |
| Dynamic Consumption @ 10MHz | uA | - | - | 25 |
| Slew Rate | V/ns | - | TBS* | - |
| Bandwidth | MHz | 5 | - | - |
| Propagation Delay (in-out) | ns | - | 50 | - |
| Propagation Delay (clk-out) | ns | - | 50 | - |
| Input Referred Noise | V/Hz | - | TBS* | - |
| Offset Voltage | mV | -20 | - | 20 |
| Sensitivity | mV | - | TBS* | - |
| Offset Voltage Drift | uV/℃ | - | TBS* | - |

*TBS: To be simulated.

# 2. COMPARATOR CORE

## 2.1. STATIC COMPARATOR

As previously discussed, a comparator contains three stages: pre-amplification, decision, and post-amplification. This section explains each stage to understand how the comparator works. The topology analyzed is from Figure 9.

**2.1.1. Pre-amplification Stage** The first stage, shown in Figure 15, consists of a differential amplifier using diode-connected loads. This stage aims to convert $V_p$ and $V_n$ into high enough signals detectable by the decision stage.

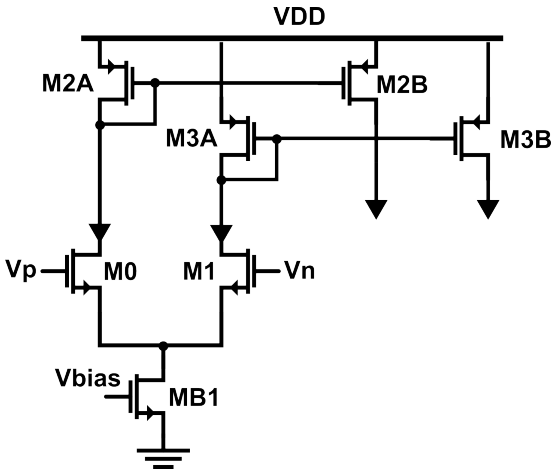


**Figure 15.** *Preamplification Stage for the Static Comparator.*

By assuming that $MB1$ sets a current $I_{ss}$ and the difference between $V_p$ and $V_n$ is low enough for small signal analysis to be valid, then the current going through M0 is equal to $I_1 = \frac{I_{ss}}{2} + \frac{g_m}{2}(V_p - V_n)$ and similarly through $M1$ the current is $I_2 = \frac{I_{ss}}{2} + \frac{g_m}{2}(V_n - V_p)$. Via these equations, one can see that the max current is $I_{ss}$ and, by increasing $V_p$, current through $M0$ increases while current in $M1$ decreases. Thus, as long as $M2$ and $M3$ are in strong-saturation acting as current mirrors, the gain of the first stage is $gm$

and only depends on the input pair. This current then passes onto the next stage.

**2.1.2. Decision Stage** This stage, from Figure 16, controls whether the output should be high or low by using positive feedback and obtaining voltages slightly higher than $V_{t_H}$ on one node and lower than $V_{t_H}$ in the other.

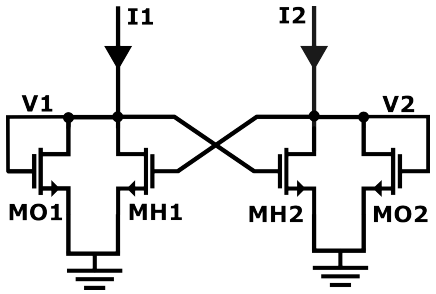


**Figure 16.** *Decision Stage for the Static Comparator.*

This is achieved thanks to transistors $M_{H1}$ and $M_{H2}$ which are cross-coupled while transistors $M_{O1}$ and $M_{O2}$ set the maximum and minimum values.
To analyze this stage, first assume $V_1 >> V_{t_H}$ and $V_2 << V_{t_H}$ and $I_1 > I_2$. In this case $M_{O1}$ is in strong saturation, while $M_{H2}$ is in triode, while $M_{O2}$ and $M_{H1}$ are turned off. In this state, all the current $I_1$ is going through $M_{O1}$ and all of $I_2$ goes through $M_{H2}$. Then, by making $V_p$ lower, $I_1$ starts decreasing, which means $I_2$ starts increasing as well, and by using equations 1 and 2, one can find the new values for $V_1$ and $V_2$. For all equations assume long channel, where $\beta = \mu_n C_{OX}(\frac{W}{L})$.

$$V_1 = \sqrt{\frac{2I_1}{\beta_O}} + V_{t_H} \tag{1}$$

$$V_2 = (V_1 - V_{t_H}) \mp \sqrt{(V_1 - V_{t_H})^2 + \frac{2I_1}{\beta_O}} \tag{2}$$

These equations explain that $V_1$ is determined by $M_{O1}$, and by decreasing $I_1$, $V_1$ should

also decrease, causing the $V_{GS}$ of $M_{H2}$ to decrease. To maintain the same current $I_2$, then $V_2$ increases and, remembering that decreasing $I_1$ also increases $I_2$, $V_2$ goes even higher.

If $V_2$ keeps increasing there is a point where $V_2 > V_{t_H}$, causing $M_{O2}$ to turn on and, considering $M_{O1} = M_{O2} = M_{H1} = M_{H2}$ then $V_1 < V_{t_H}$, so $M_{O1}$ turns off. In this case, then $M_{O2}$ sets the value for $V_2$ while $M_{H1}$ sets $V_1$.

Considering weak inversion currents, the increase of $V_2$ also increases the current going through $M_{H1}$ and no longer passes through $M_{O1}$, decreasing $V_1$. This effect is known as positive feedback, as decreasing $V_1$ by decreasing $I_1$ causes a further decrease in $V_1$.

This change of decision only occurs when $V_p = V_n$ if all transistors are equal. In the case where $\beta_H > \beta_O$, we can infer that it is easier to drive more current through the cross-coupled pair, meaning $V_{DS}$ does not need to increase as much, thus, to reach $V_1 > V_{t_H}$ or $V_2 > V_{t_H}$ more current is required, causing what is known as hysteresis. The equation for hysteresis is as follows. [12]

$$S_{PH} = V_p - V_n = \frac{I_{SS}}{gm} * \frac{\frac{\beta_H}{\beta_O} - 1}{\frac{\beta_H}{\beta_O} + 1}, \qquad S_{PN} = -S_{PH} \tag{3}$$

In the case of $\beta_H < \beta_O$, an inverse effect of hysteresis occurs, in which transistors $M_{O1}$ and $M_{O2}$ turn on before the other node reaches $< V_{t_H}$ causing a metastable region where both outputs are high. And due to the topology of the buffer, no $V_{DD}$ or $V_{SS}$ output is reached.

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[12] Jacob BAKER. *CMOS Circuit Design, Layout and Simulation*. 3rd. John Wiley Sons, Inc, 2010.

**2.1.3. Post-amplification Stage** This last stage consists of a differential to a single-ended amplifier connected to a sink/source inverter, as seen in Figure 17.

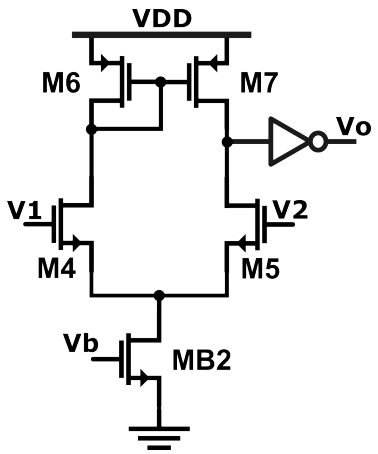


**Figure 17.** *Post-amplification Stage for the Static Comparator.*

To analyze this stage, consider the possible inputs from the previous stage. Choosing $V_1 > V_{t_H}$ and $V_2 << V_{t_H}$, $M_5$ is assumed to be turned off so that $I_{M5} = I_{M7} \approx 0$. Then, $I_{M4} \approx I_{B2}$, causing $M_6$ to saturate and set $V_{G_{M6}} = V_{DD} - V_{DSAT}$. As $M_7$ tries to sink nearly zero current, while its $V_{SG} \neq 0$, its $V_{SD}$ then tends to zero. Finally, $V_{D_{M7}} = V_{DD}$ and $V_{OUT} = V_{SS}$.

After switching occurs in the decision stage, $V_2 > V_{t_H}$ and $V_1 << V_{t_H}$, causing$I_{M4} = I_{M6} \approx 0$. In this state, $V_{SGM6} \approx 0$. Now, while $M_7$ tries to sink all of $I_{B2}$ with a low $V_{SG}$, its $V_{SD}$ increases, resulting in $V_{D_{M7}} = V_{SS}$ and $V_{OUT} = V_{DD}$. As $M_4$, $M_6$, and $M_7$ are off, one can see that no current path exists, decreasing the current consumption to nearly zero in this state and making rising and falling delays unequal.

Finally, we can say that $V_p > V_n$ causes $V_{OUT} = V_{SS}$ and $V_p < V_n$ causes $V_{OUT} = V_{DD}$. To make this comparator noninverting, one can swap the inputs from $M_4$ and $M_5$.

## 2.2. DYNAMIC COMPARATOR

In the same way as the static comparator described above, the dynamic comparator is also composed of a pre-amplification, decision, and post-amplification stage. This section describes each part of the circuit and the different phases in the comparison process to understand the operation of the dynamic comparator.

**2.2.1. Pre-amplification and Decision Stage** The operation of the conventional dynamic comparator or StrongARM, shown in Figure 12, can be separated into phases controlled by the clock signal. The first phase is called reset, and it occurs when the clock is logic low, Figure 18 shows the equivalent circuit, where $M_3$ and $M_4$ are on, and the transistors $M_{tail}$, $M_{C1}$, and $M_{C2}$ are off, this charges the equivalent capacitors at nodes F and H to $V_{DD}$.

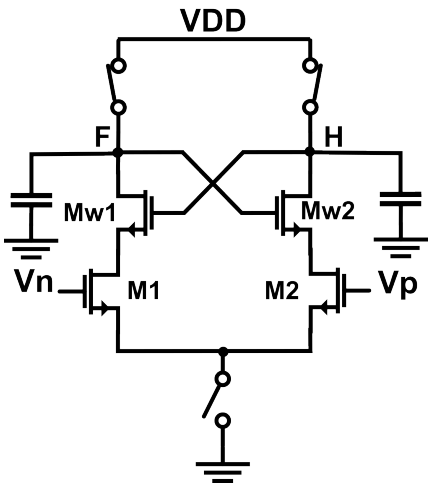


**Figure 18.** *Precharge.*

The second phase is amplification, which begins when the clock goes from low to high, causing $M_3$ and $M_4$ to turn off and $M_{tail}$, $M_1$, and $M_2$ to turn on. Figure 19 illustrates the circuit in this phase. The voltages at nodes F and H begin to drop from $V_{DD}$ to $V_{SS}$ with different rates according to $V_n$ and $V_p$. Assuming $V_p$ is lower than $V_n$, the voltage at node F discharges faster than the voltage at node H. Figure 20 shows the behavior

of the node's voltage where the voltage at node F falls faster.

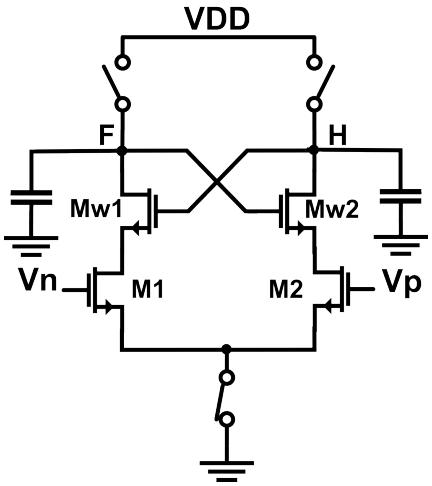


**Figure 19.** *Amplification.*

The next phase starts when the voltage at node F falls to $VDD - |V_{thp}|$ when transistor $M_{C2}$ turns on, beginning the regeneration phase of the cross couple. Due to the positive feedback, the voltage at node F goes high, and the voltage at F continues to ground or zero. The waveforms of the voltage at nodes F and H are illustrated in Figure 20.

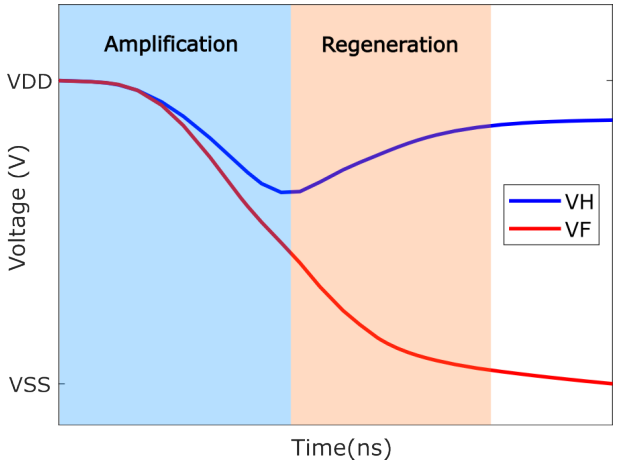


**Figure 20.** *Operation phases for the StrongARM latch comparator.*

**2.2.2. Post-amplification Stage** The circuit described above can act as a post-amplifier or output stage but can't drive high capacitances. Therefore, it is necessary to add an output stage. The proposed circuit is shown in Figure 21. After each output node of the StrongARM latch, there are two inverters whose function is to adapt the signal to the NAND latch.

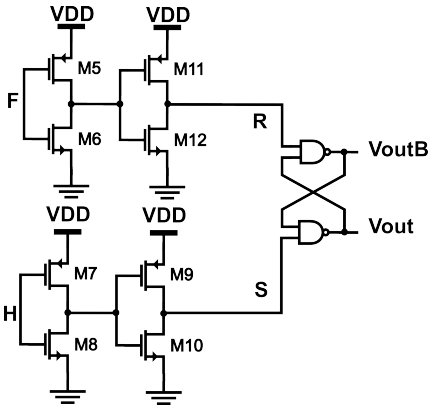


**Figure 21.** *Proposed output stage.*

Continuing with the example from the previous stage where $V_p$ is lower than $V_n$, the StrongARM output signal serves as the input for the inverters. Since the two inverters function as a buffer, the output is the same as the input. This behavior is illustrated in Figure 22.

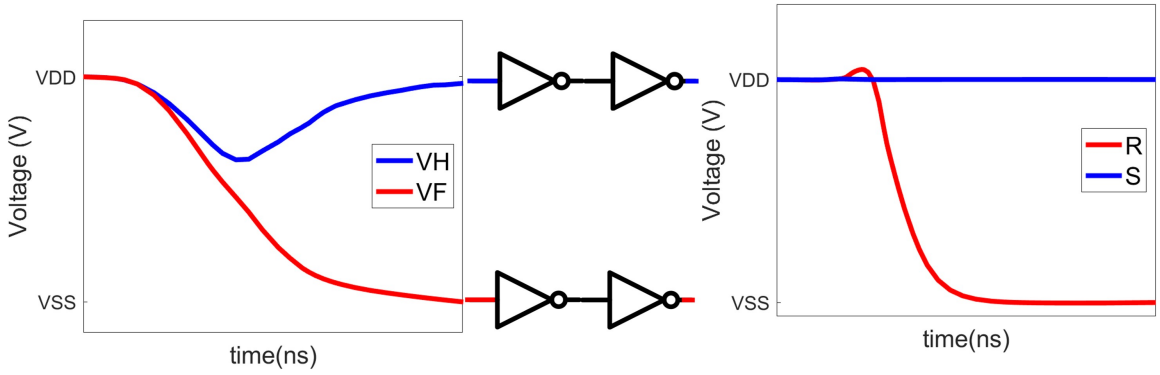


**Figure 22.** *Operation of the inverters.*

Finally, the inputs of the latch are $Reset = 0$ and $Set = 1$, and according to Table 3 that

**Table 3.** *Truth table of NAND latch.*

| Set | Reset | Vout | VoutB |
|---|---|---|---|
| 1 | 1 | No change | No change |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 0 | 0 | Invalid | Invalid |

shows the truth table of the latch, the output is $V_{OUT} = 0$ and $V_{OUTB} = 1$.

# 3. CIRCUIT IMPLEMENTATION

This chapter encompasses all aspects of the design process and outlines the considerations undertaken to fulfill each of the specifications outlined in section 1.4.

## 3.1. STATIC COMPARATOR

Considering the specifications and restrictions, the sizing of each transistor accounts for the effect on the comparator's electrical characteristics, which will be explained throughout this chapter. The diagram in Figure 23 shows a general idea of the flow in the design process for the static comparator.

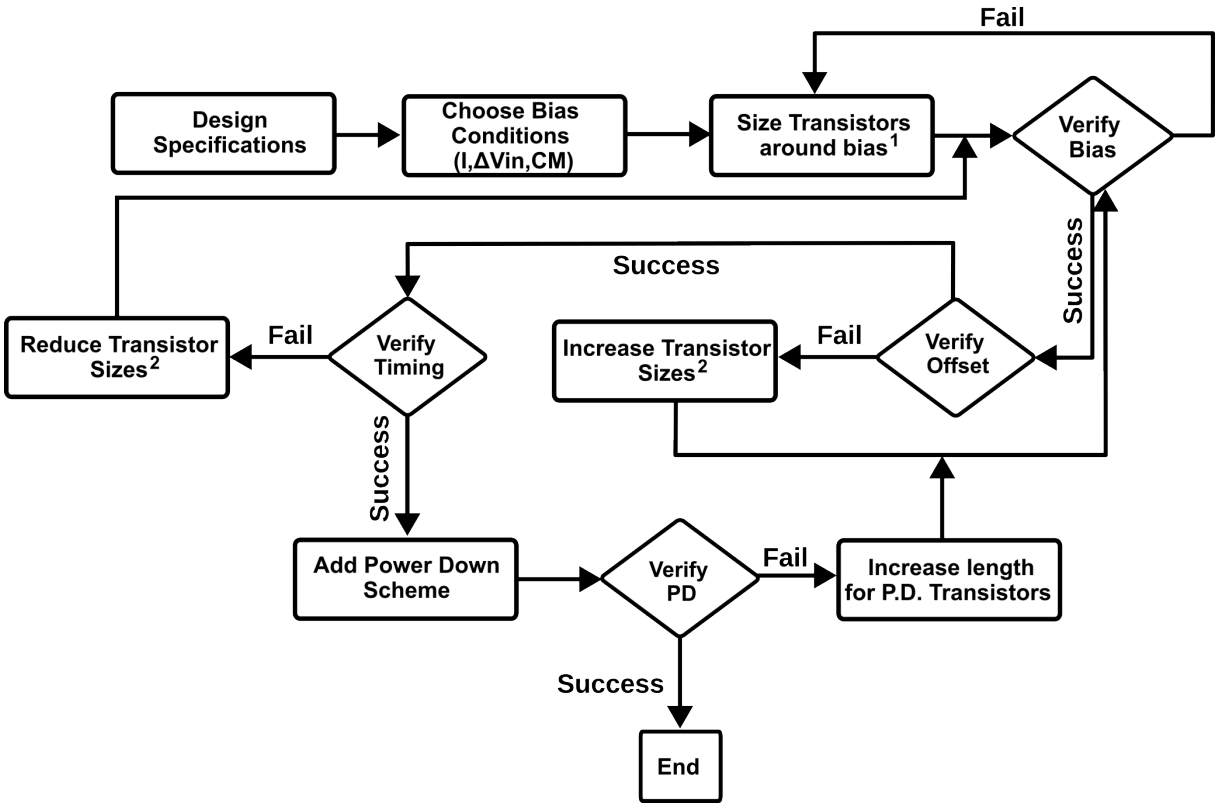


**Figure 23.** *Design Process Methodology for the Static Comparator.*

The following list provides recommendations during the design process.

1. For the initial sizes, a length of 5-10 times the minimum is recommended.
2. Consider increasing length in non-signal path transistors first.
3. Consider reducing length in signal path transistors first.

**3.1.1. Bias and Static Current** Due to the nature of the static comparator, both the preamplifier stage and decision stage will consume current constantly, and to meet the specification of $25$ [$\mu A$], one can set a limit of $10$ [$\mu A$] per stage, leaving $5$ [$\mu A$] for the reference current and the post-amplifier.

Because the reference current comes from another circuit, the value is already set, in this case, $1$ [$\mu A$]. The post-amplifier uses a current copy of $1$ [$\mu A$], such that $3$ [$\mu A$] will be a budget considering PVT variations.

Then, referring back to the bias points, one of the inputs was selected as $VDD/2 = 900$ [mV], a common bias point for most applications. Also a differential input of $5$ [mV] is used, meaning there is an output high and an output low bias point.

Transistors $M_{B0}$, $M_{B1}$, $M_2$, and $M_3$ behave as current mirror, then, it is desired to operate them in strong inversion and have long channels to minimize short channel effects, such as channel length modulation. To achieve maximum gain in the preamplifier, transistors $M_0$ and $M_1$ are expected to be saturated while in weak inversion. This property can be seen by the $gm/Id$ graph from Figure 24, allowing for maximum gain without increasing current. This also improves the offset performance.

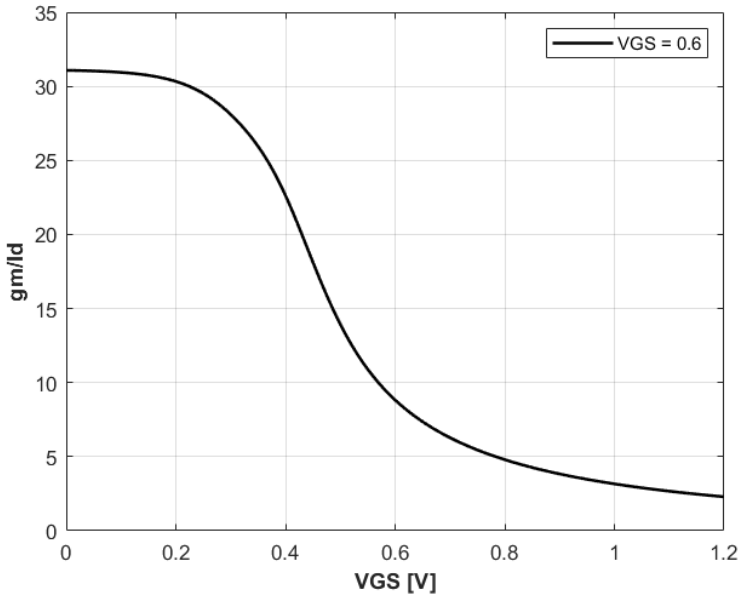


**Figure 24.** $gm/Id$ *vs* $V_{GS}$.

Transistors $M_{H1}$, $M_{H2}$, $M_{O1}$, and $M_{O2}$ are biased using the operation seen in subsection 2.1.2. While $V_p > V_n$, $M_{O1}$ is in strong inversion and saturated, $M_{H2}$ is in triode, $M_{H1}$ is in weak inversion, and $M_{O2}$ is off. While $V_p < V_n$, the conditions swap between $M_{O1}$ and $M_{O2}$, also $M_{H1}$ with $M_{H2}$.

Finally, following the operation described in subsection 2.1.3, to ensure that the output is either $V_{DD}$ or $V_{SS}$, the bias points are as follows. If $V_p > V_n$, then $M_4$ and $M_5$ are saturated in weak inversion, $M_{B2}$ and $M_6$ are in strong inversion and saturated, and $M_7$ is in triode. Then, if $V_p < V_n$, due to the reduction in current explained in the previous chapter, $M_{B2}$, and $M_5$ are in triode, $M_4$ and $M_7$ are in saturated weak inversion, and $M_6$ is off.

**3.1.2. Timing considerations** To characterize how fast or slow a change in the input is reflected in the output, one can use a $\tau = RC$ equivalent of the signal nodes, such as the drains of $M_0$ and $M_1$, the positive feedback node, the drains of $M_4$ and $M_5$,

and the output of the inverter. In each of these nodes, an equal capacitance is found by adding every parasitic capacitance from the MOSFETs that can be seen in Figure 25, which are directly related to the total area of the device, meaning that to minimize the capacitance, area should be minimum too.

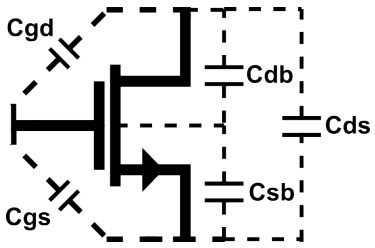


**Figure 25.** *MOSFET parasitic capacitances.*

Then, for the equivalent resistances, each node has to be analyzed separately using a small signal equivalent. For the node in the drain of $M_0$ and $M_1$, the resistance is approximately equal to $\frac{1}{gm_{2,3}}$, which generally is a very low impedance.
For the drains of $M_4$ and $M_5$, the resistance is $r_{O_7}$, which can be either low or high depending on the channel length. In this node, a short channel device is desirable.

For the hysteresis pair, the sum of the capacitance can be seen in Figure 26

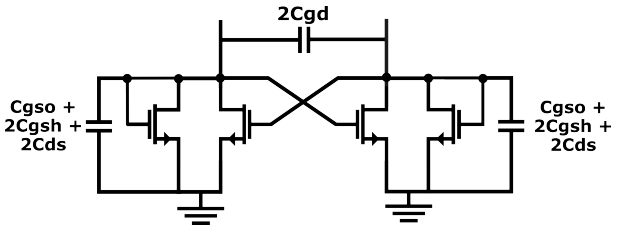


**Figure 26.** *Decision circuit with parasitics.*

Calculation using small signal analysis to find the equivalent resistance to the nodes leads to a resistance equal to:

$$R_{eq} = \frac{1}{g_{mh} - (g_{mo} + 1/r_O)} \tag{4}$$

Because the sizes of all four transistors are the same, $g_{mh} \approx g_{mo}$, and from Equation 4, the resistance tends to be $r_O$ which is high for long channel devices, and leads to a high $RC$ constant.

Lastly, to find the propagation delay for an inverter, a first-order analysis is done by integrating the capacitive load over the current that gets sunk into it[13]. This results in a RC equivalent which is dependent on the on-resistance of the transistors and expressed as:

$$t_p = 0.69 R_{eq} C_L \tag{5}$$

$$R_{eq}HL \approx r_{on} \quad R_{eq}LH \approx r_{op} \tag{6}$$

In summary, to minimize propagation delay, minimum-length devices are desired, mainly for the inverter and decision stage, as their capacitive load is high.

**3.1.3. Matching and Offset** Due to the nature of the comparator's topology, differences through the signal path are present, mainly in the buffer, as the loading effect caused by the inverter in the drain of $M_4$ is different from the drain of $M_5$. This leads to an asymmetrical response[6], named systematic offset, as it is present even if all transistors match each other. Another cause of offset comes from the manufacturing process in which all transistors can suffer from variations of their width or length, as well as

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[13] Rabaey JAN, Chandrakasan ANANTHA, and Nikolic BORIVOJE. *Digital Integrated Circuits: A Design Perspective*. 1st. Pearson Education, 2003.

doping and temperature variations throughout the wafer[14].

An accepted representation of the mismatch for each transistor is presented in Equation 7 relating the variation of the threshold voltage of the transistor to the sizing (WL) and spacing (D) between the matched transistors[3], with $A_v$ and $S_{V_t}$ being factory-dependent constants.

$$\sigma^2(V_{t_H}) \approx \frac{A_v}{\sqrt{WL}} + {S_{V_t}}^2 D^2 \tag{7}$$

This variation can be referred back to the input of the comparator by using the gain of each stage and modeled as a voltage source, as shown in Figure 27.

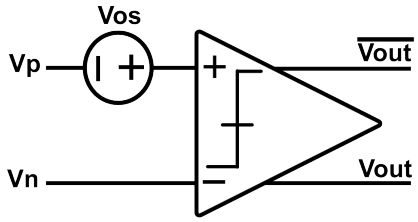


**Figure 27.** *Input Referred Offset.*

Here, it causes a problematic effect on the comparator, as a low differential output can lead to wrong decisions and metastable states, and affects the propagation delay, as it is directly dependent on the difference between inputs[3], as the positive feedback delay also depends on the initial state of the nodes.

For the static comparator, all the bias currents $M_{B0}$, $M_{B1}$, and $M_{B2}$ match each other to minimize variations in the overall current and bias points. The current mirrors $M_2$ and $M_3$ should match between them to not affect the decision stage. Input transistors

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[14] Kumar LAKSHMIKUMAR, R.A. HADAWAY, and M.A. COPELAND. "Characterisation and modeling of mismatch in MOS transistors for precision analog design". In: *Solid-State Circuits, IEEE Journal of* 21 (Jan. 1987), pp. 1057–1066. DOI: 10.1109/JSSC.1986.1052648.

$M_0$ and $M_1$ also match for the differential input. For the buffer, the same effect of the preamplifier is present, meaning $M_4$ and $M_5$ match, and $M_6$ and $M_7$ too. Finally, the most important matching occurs in the decision stage, where $M_{O1}$, $M_{H1}$, $M_{H2}$, and $M_{O2}$ all match to minimize incorrect decisions and reduce hysteresis (if not desired) and metastable regions, as mentioned in Chapter 2.

In summary, making transistors big is desired, as random variations are less detrimental to the comparator's performance. However, this leads to the well known trade-off of wanting large transistors for their matching properties but smaller transistors to minimize capacitances for faster responses and reduced area consumption.

**3.1.4. Power Down** To reduce the current consumption of the circuit while not in use, a couple of transistors are added to disconnect the bias current and bias the transistors such that no current goes through them. Figure 28 shows the first version of this scheme, where the added transistors are in red, and the signal PD is a new input.

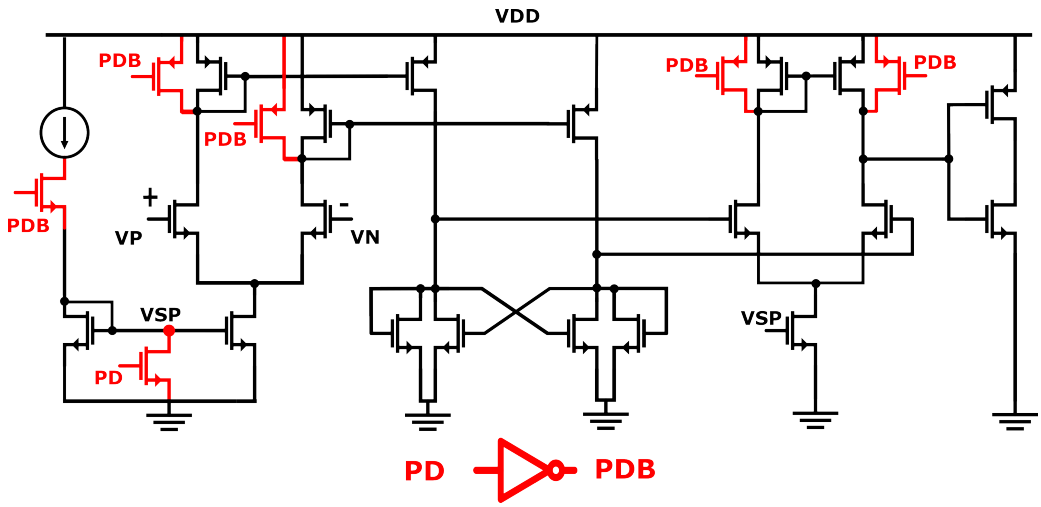


**Figure 28.** *Original Power Down Scheme for the Static Comparator.*

In this scenario, we can see that the transistor under the bias current prevents any

current from going through, and the transistor under $V_{SP}$ forces the node to $V_{SS}$, thus forcing $M_{B1}$ and $M_{B2}$ to stop sourcing current. Then, the current mirror transistors in the preamplifier and buffer force the nodes to $V_{DD}$, forcing the decision stage and inverter to not let any current through. This scheme results in the current consumed while in power down to be $\approx 24.04[nA]$ in the worst corner. Nonetheless, this is almost five times higher than desired, as the specification for the dynamic comparator is less than $5[nA]$.

In this case, although there are various sources of leakage current, the most relevant can be seen in Figure 29 and are explained as follows.

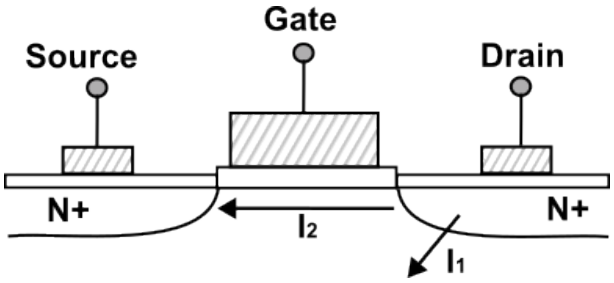


**Figure 29.** *Summary of static current.*

**PN Junction Reverse-Bias Current (I1)** The connections between the drain and well, or source and well, are typically reverse-biased, resulting in a pn-pn junction leakage current. The current $I1$ depicted in Figure 29 consists of two components: the first involves minority carrier diffusion/drift near the edge of the depletion region, while the second results from electron-hole pair generation in the depletion region of the reverse-biased junction [15].

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[15] K. ROY, S. MUKHOPADHYAY, and H. MAHMOODI-MEIMAND. “Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits”. In: *Proceedings of the IEEE* 91.2 (2003), pp. 305–327. DOI: 10.1109/JPROC.2002.808156.

**Subthreshold Leakage (I2)** Subthreshold current, or weak-inversion conduction current, flows between the drain and source when the gate-to-source voltage is smaller than the threshold voltage ($V_{th}$). This occurs because the channel is not completely cut-off.

By analyzing the current paths, we found that most of the current was coming through the power-down transistors and sinking to $V_{SS}$ through the bulk connection of the input pair due to the width of $M_0$ and $M_1$. The problematic current paths can be seen in Figure 30 highlighted in red.

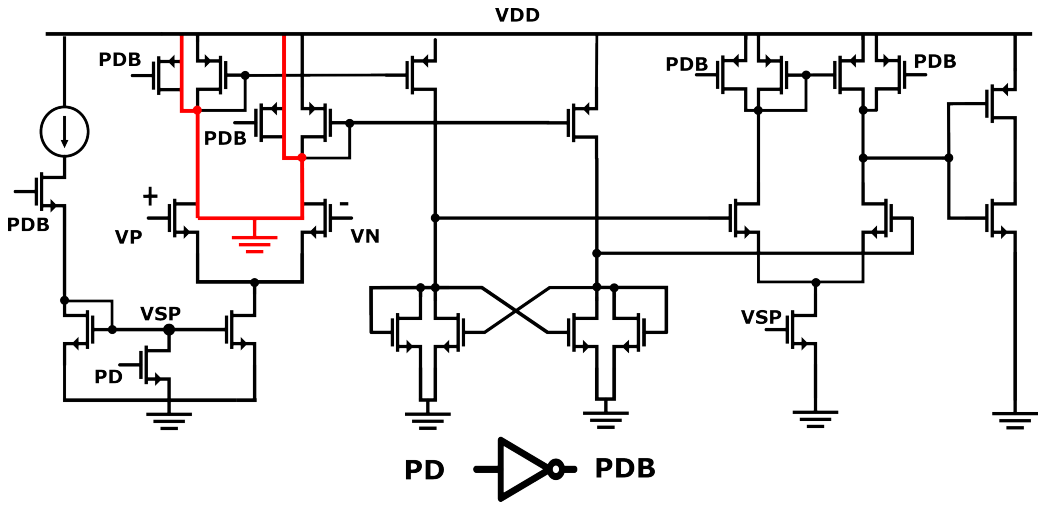


**Figure 30.** *Problematic Power Down current paths.*

To mitigate this issue, the power-down transistors are moved on top of the current mirrors $M_2$ and $M_3$, reducing the overall power down current at the cost of adding loads in both the preamplifier and the decision stages. Figure 31 shows the resulting schematic.

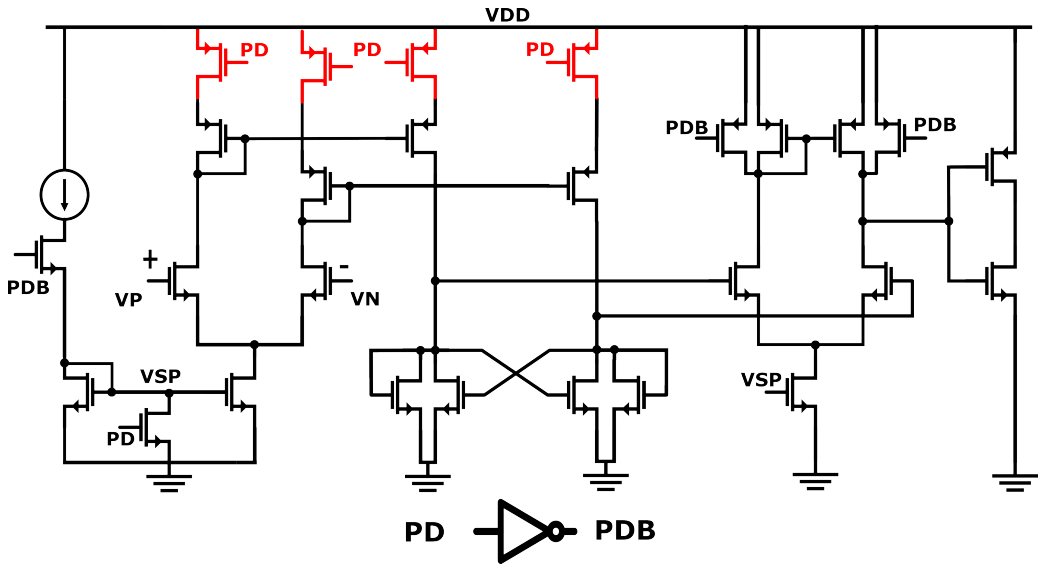


**Figure 31.** *Fixed Power Down Scheme for the Static Comparator.*

### 3.2. DYNAMIC COMPARATOR

The diagram in Figure 32 shows a general idea of the flow in the design process for the dynamic comparator.
It is important to note that when following the design diagram of Figure 32, the increase of the W/L ratio when timing fails, only applies to the input pair transistors and in the NAND Gate, due to reasons that will be explained throughout this chapter.

Below are the main characteristics and factors that affect the performance of the dynamic comparator.

**3.2.1. Static current** It is the current flowing through the circuit in clock or input inactivity. In the selected topology, the primary source of static consumption arises from leakage current occurring when the transistor should be in the off state. The most relevant were described previously in subsection 3.1.4.
There are four principal techniques to reduce leakage current: transistor stacking, mul-

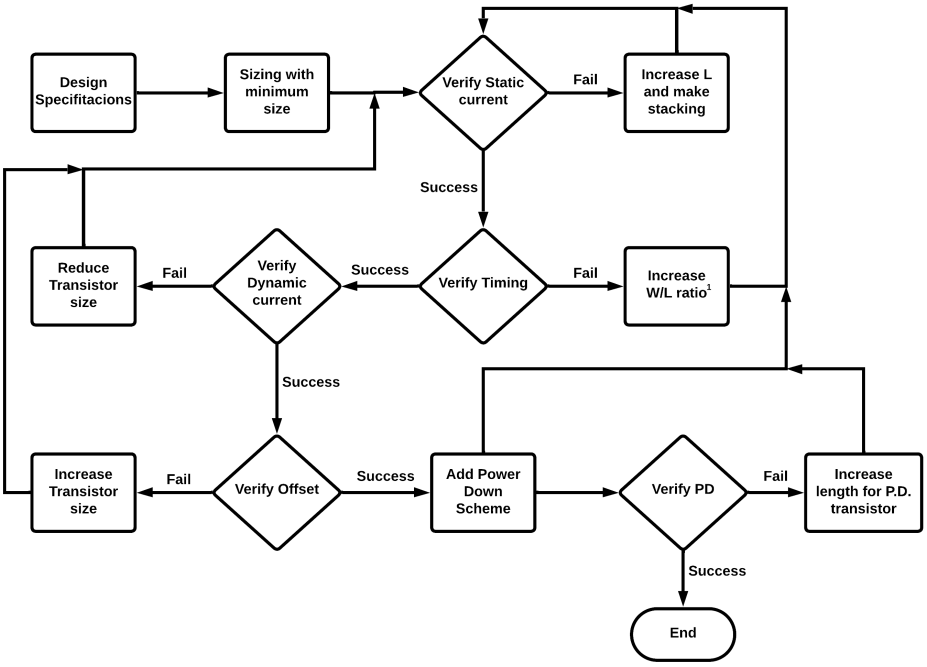


**Figure 32.** *Design Process Methodology for the Dynamic Comparator.*

tiple threshold voltages ($V_{th}$), dynamic threshold voltages ($V_{th}$), and supply voltage scaling[15]. The design process utilizes transistor stacking and increasing the length (L), which has proven effective. Other methods for reducing static current were not considered in this work because they require alterations to the physical structure of the transistor or the use of multiple types of transistors, which could increase the cost of the fabrication process.

The first step in reducing static current involves identifying the transistors responsible for the current. Given that the behavior of the transistors differs depending on the state of the clock (CLK) and the output, it is essential to conduct the analysis when the clock (CLK) is both high and low.

**CLK High** Figure 33 highlights the transistors that should be in the off state when the input $V_n$ is smaller than $V_p$.

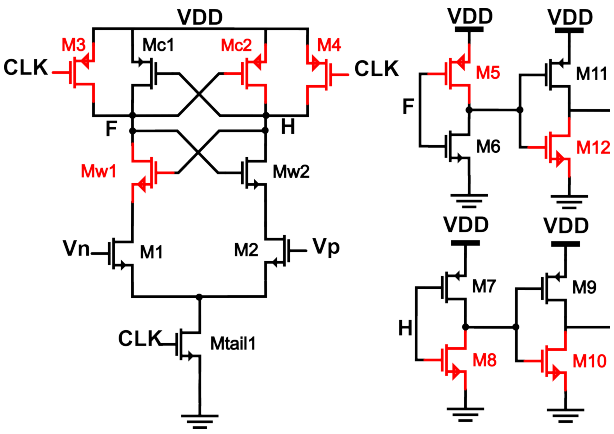


**Figure 33.** *The transistors highlighted in red are the ones relevant to static current when CLK is high and $V_n < V_p$ in the StrongARM and inverters.*

It is crucial to simultaneously apply the same changes to each transistor and its symmetrical counterpart. For example, modifying transistor $Mw1$ is necessary to replicate these changes in transistor $Mw2$.

For the latch stage, Figure 34 illustrates the transistors that should be in the off state. Similar to the previous stage, suppose a specific scenario to facilitate the analysis. At this stage, assume R and S as high and low, respectively, resulting in $Vout$ being high and $VoutB$ being low.

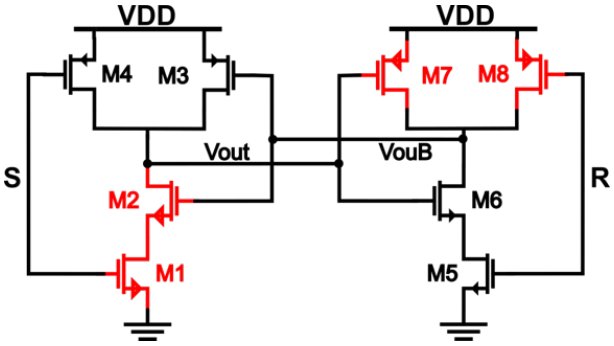


**Figure 34.** *The transistors highlighted in red are the ones relevant to static current when CLK is high and $V_n < V_p$ in the Latch.*

**CLK LOW** When the CLK is LOW, the red transistors of the Figure 35 are the ones that are off.

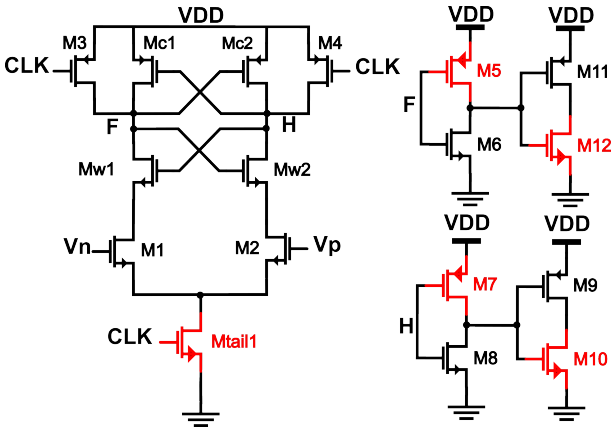


**Figure 35.** *The transistors highlighted in red are the ones relevant to static current when CLK is low and $V_n < V_p$ in the StrongARM and inverters.*

When the CLK transitions from high to low, the Set (S) and Reset (R) inputs go high, causing the latch to retain the previous stage, with $Vout$set to high and $VoutB$ equal to low. Under these conditions, Figure 36 shows the transistors off.

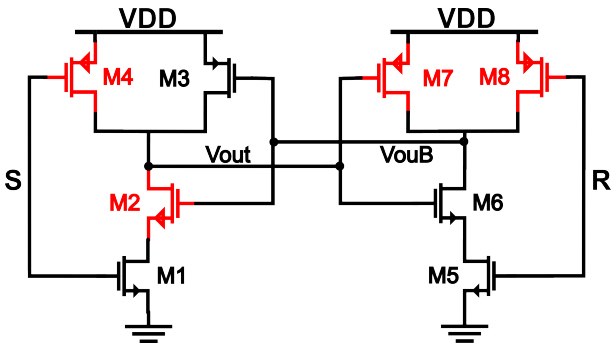


**Figure 36.** *The transistors highlighted in red are the ones relevant to static current when CLK is low and $V_n < V_p$ in the Latch.*

**3.2.2. Timing considerations** The delay in the StrongARM has two components, namely $t_0$ and $t_{latch}$. The fisrt one, $t_0$, represents the time required to discharge nodes F and H to $VDD - |V_{thp}|$, assuming $Vp > Vn$ (Figure 35). Since the current through

M2 is greater than the current through M1, the voltage at node H discharges more rapidly. Therefore, the delay time $t_0$ is given by:

$$t_0 = \frac{C_L|V_{thp}|}{I_2} \tag{8}$$

And now $I_2 = I_{tail}/2 + \Delta I_{in} = I_{tail}/2 + gm_{1,2}\Delta V_{in}$ and with small $\Delta V_{IN}$ the current $I_2$ can be approximated to $I_{tail}/2$

The second term, $t_{latch}$, represents the delay in the regeneration phase at the cross-coupled stage. Assuming a voltage variation of $VDD/2$ at the output from a minor difference $V_0$, this delay is given by:

$$t_{latch} = \frac{C_L}{gm_{eff}} ln(\frac{Vout}{V_0}) \tag{9}$$

$$t_{latch} = \frac{C_L}{gm_{eff}} ln(\frac{Vout/2}{V_0}) \tag{10}$$

Where $gm_{eff}$ represents the transconductance of each inverter [1], considering the previously mentioned, the method to decrease the delay involves augmenting the $Itail$ current, which entails increasing the width-to-length ratio $W/L$ of the $Mtail$ transistor. On the other hand, to enhance the voltage difference $V_0$ at nodes F and H, it is necessary to increase the $W/L$ ratio of $M1,2$.

The delay analysis of the inverters, which constitutes the subsequent stage, was conducted in Section 3.1.2.

The delay of the latch has two phases: Low to High and High to Low. To analyze the timing of the latch, we assume $Vout$ to be high and $VoutB$ to be low. Figure 36 illustrates the transistors in the off state in red and those in the on state in black when the clock is 0. When Reset (R) transitions from high to low, $VoutB$ charges because transistor $M8$ turns on. Since $Vout$was assumed to be high, transistor $M7$ remains off. Therefore, the delay from low to high is given by:

$$t_{LH} = 0.69 R_{eqp} C_L \tag{11}$$

Where $R_{eqp}$ represents the equivalent on-resistance of the pMOS transistor[13]. The equation is identical to that of the inverter."

Transistors M2 and M3 function as an inverter. Thus, when $VoutB$ surpasses VDD/2, $Vout$transitions from 1 to 0 [13]. Therefore, the delay from high to low is given by:

$$t_{HL} = t_{LH} + 0.69 \cdot 2R_{eqn} \cdot C_L \tag{12}$$

Where $R_{eqn}$ represents the equivalent on-resistance of the pMOS transistor. To minimize the delay in the latch, it is essential to decrease the on-resistance, increasing the width-to-length (W/L) ratio.

**3.2.3. Matching and Offset** The mismatch in the dynamic comparator resembles that addressed in the static comparator, as explained in Section 3.1.3. Therefore, similarly, large transistors are also sought. The preamplification and decision stages do not exhibit systematic offsets because the circuit is ideally symmetric. However, regarding random offset, the transistors in the StrongARM that require matching are $M1 - M2$, $M_{sw1} - M_{sw2}$ and finally $M_{C1} - M_{C2}$ [16]. Among these, the transistors $M_1 - M_2$ have the most significant impact because the mismatches in the $M_{sw1} - M_{sw2}$ transistors are typically divided by a factor of four, and in the $M_{C1} - M_{C2}$ transistors, by a factor of ten. Offset simulations use a slow input ramp and a fast clock.

**3.2.4. Power down** Transistor $Mena$ enables the comparator, as depicted in Figure 37. The red transistor prevents the capacitors from discharging, thereby preventing the

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[16] Behzad RAZAVI. "The Design of a Comparator [The Analog Mind]". In: *IEEE Solid-State Circuits Magazine* 12.4 (2020), pp. 8–14. DOI: 10.1109/MSSC.2020.3021865.

comparison. Due to nodes F and H remaining unchanged in the subsequent digital stages, the power consumption is negligible.

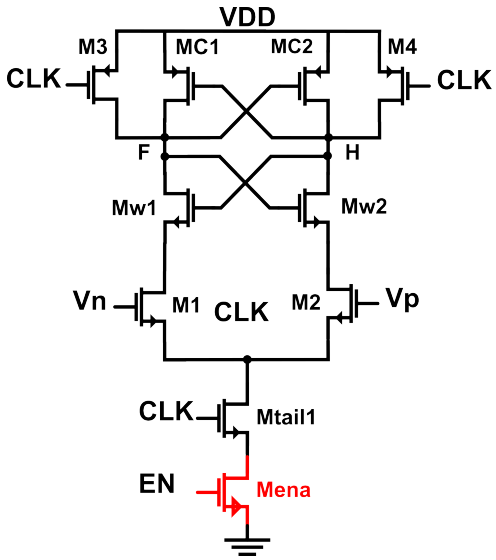


**Figure 37.** *Dinamic comparator with power down.*

**3.2.5. Dynamic current** The dynamic current is the current consumed by the circuit during operation. This consumption consists of two components: the first arises from the short circuit between VDD and VSS when the circuit is switching, and the second is due to charging capacitances. Figure 38 illustrates the capacitors in the StrongARM. Considering these factors, the dynamic current in the StrongARM is given by:

$$I_{StrongARM} = f_{CLK}(2C_{eq1,2} + C_{F,H})VDD \tag{13}$$

Similarly to the StrongARM, the inverters also exhibit dynamic current due to the presence of capacitors. In this case, Figure 39 shows the capacitances. This Figure shows only one pair of inverters. Hence, the total current consumption is given by:

$$I_{Inv} = f_{CLK}C_{tot}VDD \tag{14}$$

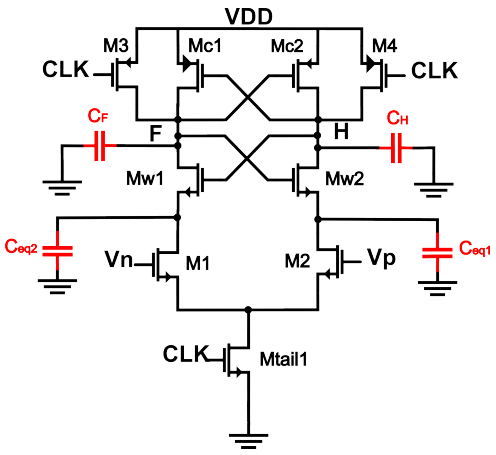


**Figure 38.** *capacitors in the StrongARM.*

$$I_{Total-Inv} = 2f_{CLK}C_{tot}VDD \tag{15}$$

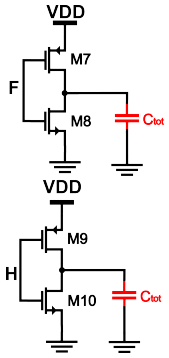


**Figure 39.** *Capacitors in the Inverters.*

The capacitances mentioned above are parasitic capacitors. Finally, the total current consumption of the latch is given by:

$$I_{Latch} = 2f_{CLK}C_{L}VDD \tag{16}$$

The total dynamic current is given by:

$$I_{total} = I_{StrongARM} + I_{Latch} + I_{Total-Inv} \tag{17}$$

# 4. RESULTS

## 4.1. DEVICE SIZING

In this section, the final dimensions of both circuits are shown. The technology used for this process was TSMC's $28[nm]$ CMOS using the $1.8[V]$ standard transistors.

### 4.1.1. Static Comparator

Figure 40 shows the final schematic with each transistor in the static comparator and their names. Table 4 shows the values of the W/L of the transistors in micrometers. The column P refers to how many parallel transistors were used, including fingers, and column S is for in-series devices. As previously mentioned, the sizing was done according to the diagram from Figure 23.

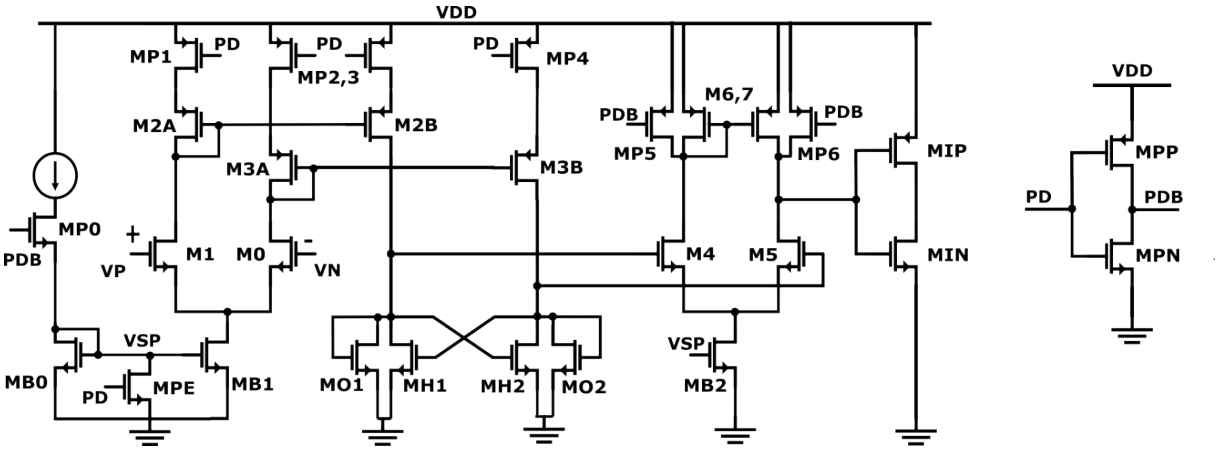


**Figure 40.** *Final Schematic of the Static Comparator.*

**Table 4.** *Final dimensions for the Static Comparator without hysteresis.*

| Name | W/L [um/um] | P | S | Name | W/L [um/um] | P | S |
|---|---|---|---|---|---|---|---|
| $M_{0,1}$ | 0.5/2 | 96 | 1 | $M_{B0}$ | 0.27/2 | 1 | 1 |
| $M_{2,3}$ | 0.27/1.6 | 6 | 1 | $M_{B1}$ | 1.1/2 | 3 | 1 |
| $M_{O1,O2}$ | 0.8/1.2 | 1 | 2 | $M_{B2}$ | 0.6/2 | 1 | 1 |
| $M_{H1,H2}$ | 0.78/1.2 | 1 | 2 | $M_{P1,2,3,4}$ | 0.27/0.5 | 1 | 1 |
| $M_{4,5}$ | 0.6/0.3 | 2 | 1 | $M_{P5,6}$ | 0.27/2 | 1 | 1 |
| $M_{6,7}$ | 0.27/1 | 1 | 1 | $M_{P0}$ | 0.27/0.15 | 1 | 1 |
| $M_{IN}$ | 1.3/0.15 | 1 | 1 | $M_{PE}$ | 0.27/2 | 1 | 1 |
| $M_{IP}$ | 1.1/0.3 | 2 | 1 | $M_{PP}$ | 0.27/2 | 1 | 1 |
| $M_{PN}$ | 0.65/2 | 4 | 1 | - | - | - | - |

As an addition to the project, a slightly altered sizing is presented which achieves hysteresis under all PVT variations while increasing the minimum differential input to $10$ [mV]. Table 5 shows the sizes that were changed to achieve this.

**Table 5.** *Final dimensions for the Static Comparator with hysteresis.*

| Name | W/L [um/um] | P | S | Name | W/L [um/um] | P | S |
|---|---|---|---|---|---|---|---|
| $M_{2,3}$ | 0.35/1.6 | 6 | 1 | $M_{B1}$ | 1.05/2 | 3 | 1 |
| $M_{H1,H2}$ | 0.88/1.2 | 1 | 2 | $M_{B2}$ | 0.5/2 | 1 | 1 |

### 4.1.2. Dynamic Comparator

Figure 41 shows the final schematic with each transistor in the dynamic comparator and their names. Table 6 shows the values of the W/L of the transistors in the StrongARM latch and the inverters in micrometers. The column P refers to how many parallel

transistors were used, including fingers, and column S is for in-series devices. Once again, the sizing was done according to the diagram from Figure 32.

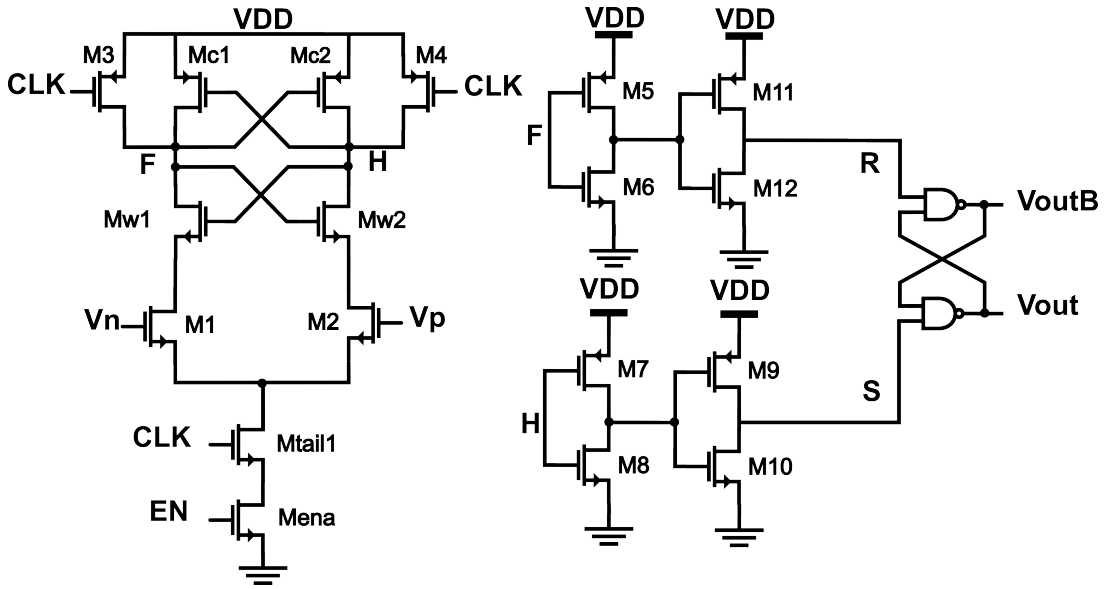


**Figure 41.** *Final Schematic of the Dynamic Comparator.*

**Table 6.** *Final dimensions for the Dynamic Comparator.*

| Name | W/L [um/um] | P | S |
|---|---|---|---|
| $M_{1,2}$ | 1.335/2 | 3 | 1 |
| $M_{sw1,2}$ | 0.5/1 | 1 | 1 |
| $M_{C1,2}$ | 0.27/0.5 | 1 | 1 |
| $M_{tail1}$ | 1.2/1.2 | 1 | 3 |
| $M_{ena}$ | 1.2/0.9 | 1 | 1 |
| $M_{3,4}$ | 0.27/1 | 1 | 1 |
| $M_{5,7}$ | 0.27/1 | 1 | 1 |
| $M_{6,8}$ | 0.27/2 | 1 | 1 |
| $M_{9,11}$ | 0.27/0.5 | 1 | 2 |
| $M_{10,12}$ | 0.27/1 | 1 | 3 |

Figure 42 shows the final schematic of the NAND latch and the transistor's names. Table 7 shows the transistor dimension information with the same columns as Table 6.

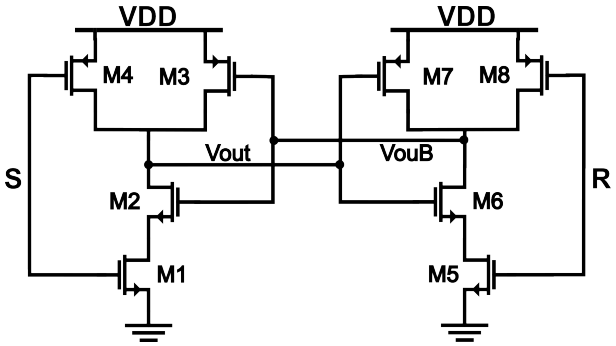


**Figure 42.** *Final Schematic of the NAND latch.*

**Table 7.** *Final dimensions for the Dynamic Comparator.*

| Name | W/L [um/um] | P | S |
|---|---|---|---|
| $M_{3,4,7,8}$ | 1.3/0.73 | 2 | 1 |
| $M_{2,6}$ | 1.3/0.9 | 1 | 2 |
| $M_{1,5}$ | 0.27/0.9 | 1 | 1 |

## 4.2. SCHEMATIC RESULTS

In order to verify and validate the performance of the comparators, different simulations were carried out using Cadence Virtuoso and Spectre.

**4.2.1. Static Comparator** Table 8 shows the results of PVT corners and Monte Carlo simulations for all of the specifications and restrictions of the Static Comparator obtained after carrying out the design process.

**Table 8.** *Results for the Static Comparator's Schematic without hysteresis.*

| Parameter | Condition | Units | Target | PVT | | | MC | |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Mean | $3\sigma$ |
| Static Current | Out High Vinn = 900mV | uA | $<$25 | 16.72 | 18.98 | 21.32 | 19.01 | 2.85 |
| | Out Low Vinn = 900mV | uA | $<$25 | 18.1 | 20.48 | 22.5 | 20.48 | 2.97 |
| Propagation Delay | $\Delta$Vin = 5 mV High to Low | ns | $<$50 | 21.32 | 24.88 | 31.93 | 25.3 | 12.39 |
| | $\Delta$Vin = 5 mV Low to High | ns | $<$50 | 22.6 | 26.8 | 34.71 | 27.78 | 13.8 |
| Bandwidth | - | MHz | 5 | 11.2 | 13.6 | 22.5 | - | - |
| Offset | - | mV | ±5 | - | - | - | 0.08 | 3.54 |
| PD Current | | nA | $<$5 | 0.039 | 0.072 | 4.59 | - | - |
| Input Range | | V | - | 0.5 | - | 1 | - | - |
| Slew Rate | $\Delta$Vin = 5 mV High to Low | V/us | - | 361.3 | 539.6 | 685.6 | 533.1 | 105.51 |
| | $\Delta$Vin = 5 mV Low to High | V/us | - | 170.4 | 301.4 | 406.5 | 298.5 | 38.52 |
| Sensitivity | - | mV | - | 0.16 | 0.44 | 1.1 | - | - |
| DC Gain | - | dB | - | 67.04 | 75.80 | 79.08 | - | - |
| PSR | - | dB | - | -77.16 | -74.81 | -53.4 | - | - |
| Input Noise | RMS | uV | | 40.35 | 56.98 | 113.1 | - | - |
| Offset Drift | -40 to 125 | uV/C | | - | 1.17 | - | - | - |

From the results, we can see that almost every parameter is not only affected by PVT variations but by mismatches between transistors. This happens as the current will vary due to the variation of $V_{GS}$ and $V_{tH}$ in PVT corners, and the current being copied by $M_{B1}$, $M_{B2}$, $M_2$, and $M_3$ will increase or decrease depending on their mismatches, which are seen in the Montecarlo results.

This change in current also represents a change in delay, as the current being sunk

into each node differs, which also leads to the expected change in slew rate. Figure 43 shows the output of the fastest, slowest, and nominal corners.

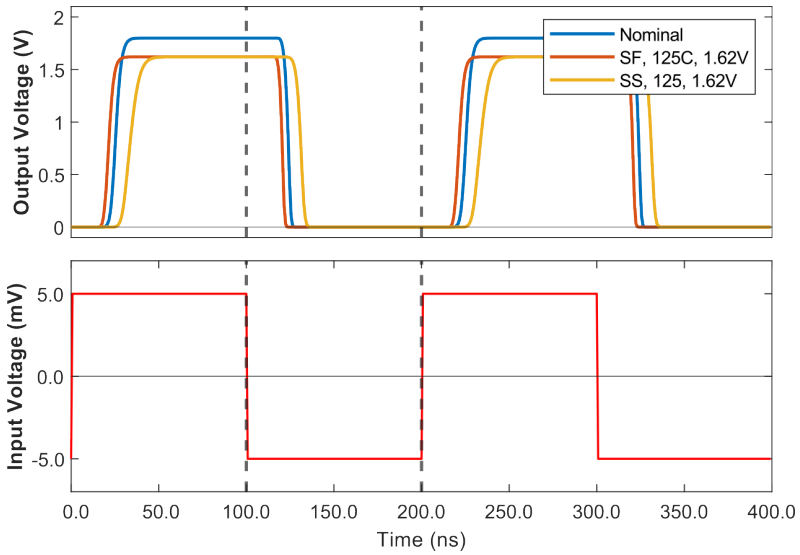


**Figure 43.** *Nominal, fastest and slowest output in the static comparator without hysteresis.*

The value of offset in the comparators mostly changes when there is a mismatch between transistors, and for this reason, no PVT variations were considered. From the results, we can see that there are $80$ [$\mu$V] of systematic offset caused by the post-amplifier stage. Also, the biggest contributor to offset variability is the decision stage with nearly $40\%$ of the total coming from $M_{O1,2}$ and $M_{H1,2}$ mismatches. This value also changes with temperature to a max of $3\sigma$ of $3.8$ [mV] represented in the offset drift value. Figure 44 shows the histogram of the offset.

From the remaining results, we can see that the power-down current is low but near the self-imposed limit of $5$ [nA], reaching $4.5$ [nA] in high-temperature corners.
The input range of the comparator goes from $0.5$ [V], where $M_{B0}$ is no longer saturated, causing a very slow response, to $1$ [V], where $M_{2,3}$ turn off.
Sensitivity is a strong point of the design, where the worst corner needs a $1.1$ [mV]

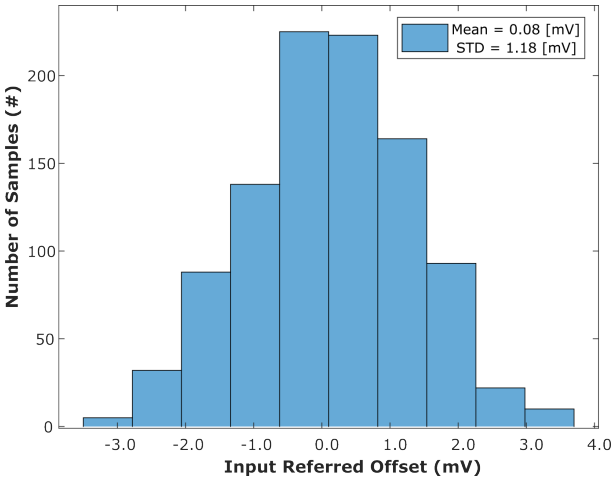


**Figure 44.** *Offset histogram of the static comparator without hysteresis.*

guaranteed differential input to achieve all required specifications.

For the Input Referred Noise, whenever the $\Delta V_{in} < 113$ [$\mu$V], then the response will be completely dominated by the internal noise.

The design successfully meets all requirements with high margins for propagation delays ($\approx 10$ [ns]) and offset ($\approx \pm 1.4$ [mV]). Nonetheless, it is important to remember that in cases where the offset is positive, the propagation delay increases for the low-to-high response and decreases for a high-to-low response, and, when the offset is negative, the relation is reversed. Then, maintaining offset as low as possible also benefits a stable propagation delay.

Table 9 contains the results of PVT corners and MonteCarlo simulations for the schematic of the static comparator including hysteresis.

**Table 9.** *Results for the Static Comparator's Schematic with hysteresis.*

| Parameter | Condition | Units | Target | PVT | | | MC | |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Mean | $3\sigma$ |
| Static Current | Out High Vinn = 900mV | uA | $<$25 | 15.51 | 17.52 | 20.8 | 17.52 | 2.4 |
| | Out Low Vinn = 900mV | uA | $<$25 | 16.88 | 19.03 | 20.8 | 19.05 | 2.57 |
| Propagation Delay | $\Delta$Vin = 10 mV High to Low | ns | $<$50 | 19.92 | 24.32 | 30.09 | 23.93 | 7.29 |
| | $\Delta$Vin = 10 mV Low to High | ns | $<$50 | 21.19 | 24.96 | 31.88 | 25.04 | 6.51 |
| Bandwidth | - | MHz | 5 | 11.7 | 15.15 | 17.4 | - | - |
| Offset | - | mV | ±5 | - | - | - | 0.012 | 3.82 |
| Hysteresis | - | mV | - | - | - | - | 5.46 | 4.68 |
| PD Current | | nA | $<$5 | 0.03 | 0.08 | 4.26 | - | - |
| Input Range | | V | - | 0.51 | - | 0.99 | - | - |
| Slew Rate | $\Delta$Vin = 10 mV High to Low | V/us | - | 405.8 | 529.3 | 641.2 | 529.5 | 70.38 |
| | $\Delta$Vin = 10 mV Low to High | V/us | - | 198.7 | 301.4 | 365.1 | 299.9 | 25.2 |
| Sensitivity | - | mV | - | 3.7 | 4.4 | 6.3 | - | - |
| DC Gain | - | dB | - | 68.1 | 77.11 | 82.67 | - | - |
| PSR | - | dB | - | -73.01 | -69.06 | -48.99 | - | - |
| Input Noise | RMS | uV | | 35.8 | 58.33 | 203.1 | - | - |
| Offset Drift | -40 to 125 | uV/C | | - | 1.19 | - | - | - |

In this case, the comparator does not require as much current as the design without hysteresis, as a result of the increase in the differential input, which, as was previously explained, causes faster responses and is also reflected in the bandwidth as it is slightly higher. Figure 45 shows the fastest, slowest, and typical simulations for the comparator with hysteresis. For Montecarlo simulations, the standard deviation is halved due to the increase in the input differential voltage.

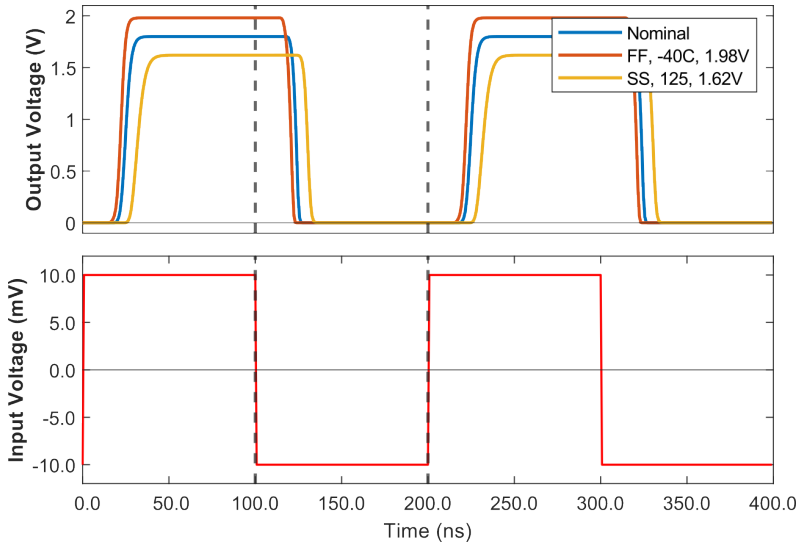


**Figure 45.** *Nominal, fastest and slowest output in the static comparator with hysteresis.*

Most importantly the hysteresis of the design varies from up to $\approx 9.4$ [mV] down to $\approx 0.98$ [mV]. This is caused due to mismatches between the $M_{O1,2}$ and $M_{H1,2}$ transistors. This became the focus going into the placement and routing of the layout, as maintaining hysteresis is the focus of this design. Doing this also helps mitigate offset, which is shown in Figure 46.

The rest of the measurements had no significant change.

**4.2.2. Dynamic Comparator** Table 10 shows the results in corners and Monte Carlo simulations obtained after carrying out the design process for the dynamic comparator.

In the dynamic comparator, almost every parameter is only affected by PVT variations due to much of the circuit being logic, making it very robust against Monte Carlo variations.

Higher currents occur at high-temperature corners, specifically at 125℃. This is be-

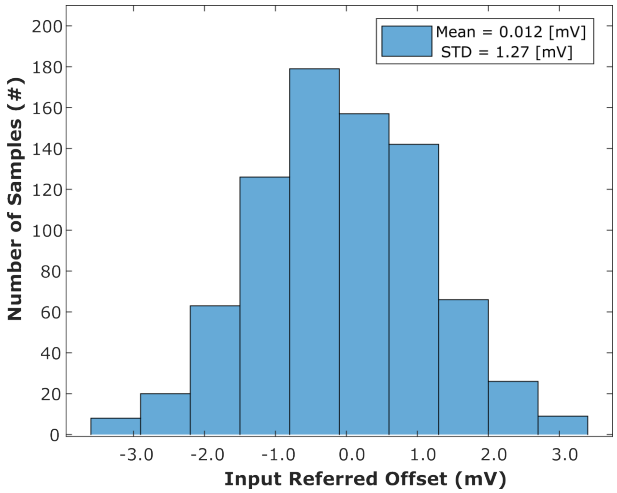


**Figure 46.** *Offset histogram of the static comparator with hysteresis.*

cause, as the temperature rises, the voltage threshold and mobility decrease. However, at lower Vgs, the dominant effect on current is Vth [12].

The low-to-high delay differs from the high-to-low delay due to variations in the transistor distribution utilized for charging and discharging. This also causes the slew rate from high to low to be lower than low to high in all cases. Additionally, the high-to-low process initiates when the negated output surpasses $VDD/2$. On the other hand, the most significant delay occurs in the output stage due to the presence of the load capacitance, which is the largest in the circuit.

Higher dynamic currents occur at high-temperature corners, that is to say, 2V. This is due to the broader voltage range, leading to an increase in voltage across most nodes. As a result, $Vgs$ and $Vds$ (for n-type transistors) and $Vsg$ and $Vsd$ (for p-type transistors) increase, consequently elevating the currents.

From the other results we can see that the power down current is relatively low, this current is greater than the static current since the transistor used is not as large as those used to limit the static current. On the other hand, the greatest current is found in the high temperature corners, same as the static current.

Now, as for the common mode voltage, the lower limit is determined by the delay, since

**Table 10.** *Results for the Dynamic Comparator's Schematic.*

| Parameter | Condition | Units | Target | Min | Typ | Max |
|---|---|---|---|---|---|---|
| Static current | CLK HIGH | nA | $<5$ | 0.016 | 0.039 | 4.773 |
| | CLK LOW | ns | $<5$ | 0.035 | 0.80 | 4.78 |
| Propagation Delay | Low-High $\Delta$Vin=5m | nA | $<50$ | 6.889 | 9.82 | 14.97 |
| | High- Low $\Delta$Vin=5m | nA | $<50$ | 12.27 | 18.6 | 30.39 |
| Dynamic current | $\Delta$Vin=300m | $\mu$A | $<25$ | 17.92 | 20.67 | 23.8 |
| Bandwidth | $\Delta$Vin=5m | MHz | $>5$ | 10 | 26 | 36 |
| PD Current | $\Delta$VIN Switching | nA | - | 0.675 | 1.3 | 7.484 |
| | VIN stable | nA | - | 0.522 | 0.68 | 6.625 |
| Input Range | | V | - | 0.532 | | 1.52 |
| Slew Rate | Low-High $\Delta$Vin=5m | V/$\mu$s | - | 111 | 190 | 303 |
| | High-Low $\Delta$Vin=5m | V/$\mu$s | - | 62 | 119 | 211 |
| Input Noise | | $\mu$V | - | 280 | 540 | 660 |
| Offset Drift | -40 to 125 | uV/C | | - | 2.8 | - |
| **Parameter** | **Condition** | **Units** | **Target** | - | **Mean** | $\sigma$ |
| Offset | TCLK 500n Trise=600u | mV | $\pm$ 20 | - | 0.07 | 2.143 |

having low voltage at the input, the currents will be low, increasing the delay of the regeneration process. Meanwhile, the upper limit is determined by a single corner (125℃ 2V ff) where If one were to use a reference voltage of 1.8, the dynamic current is 25.33 [$\mu$A]. Taking into account that corners are extreme statistical cases then it is likely that most of the fabricated devices will reach 1.8V at their input without consuming 25[$\mu$A].

After measuring the minimum $\Delta V_{in}$ at which the comparator responds while meeting all specifications, it was found that this value is less than the noise level. Therefore, the

noise level determines the sensibility.

Finally there is the offset, which is determined by the mismatch between transistors, so the measurement is carried out simulating Monte Carlo. This result is the one with the greatest margin among all the measurements since $3\sigma$ is equal to 6.429.

### 4.3. LAYOUT CONSIDERATIONS

The common centroid and interdigitated techniques were employed to enhance matching among critical transistors, aiming to minimize offset, particularly in components like the input pair or the current mirrors. Another crucial consideration was implementing symmetric placement and routing to alleviate discrepancies in metal routes and minimize parasitic effects on the comparators. One example that highlights the use us symmetry, common centroid and dummies can be seen in Figure 47 for the static comparator and in Figure 48 for the dynamic comparator.

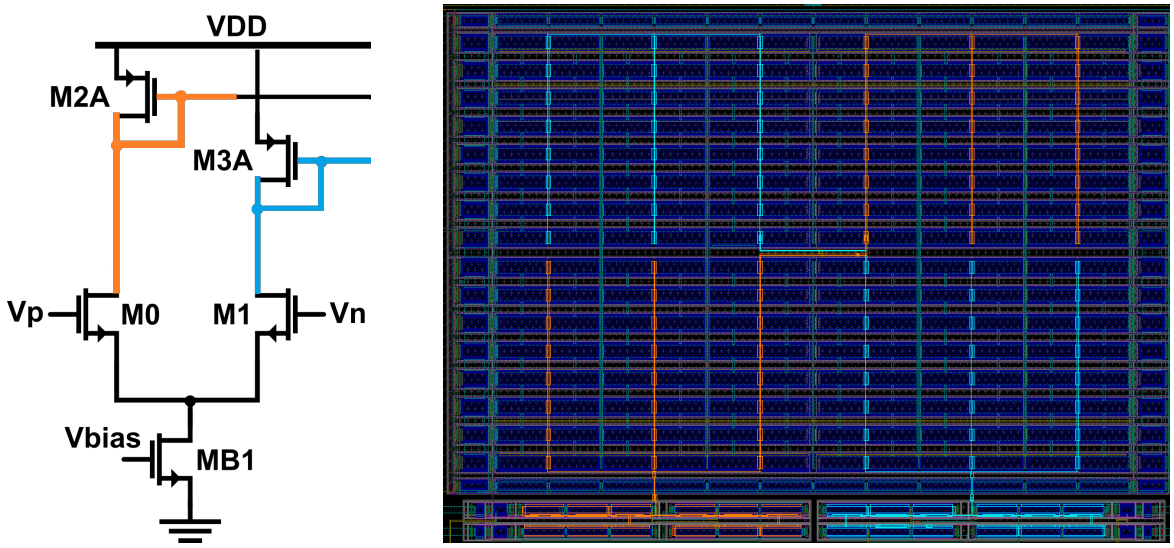


**Figure 47.** *Symmetrical Layout structure of the preamplifier stage in the static comparator.*

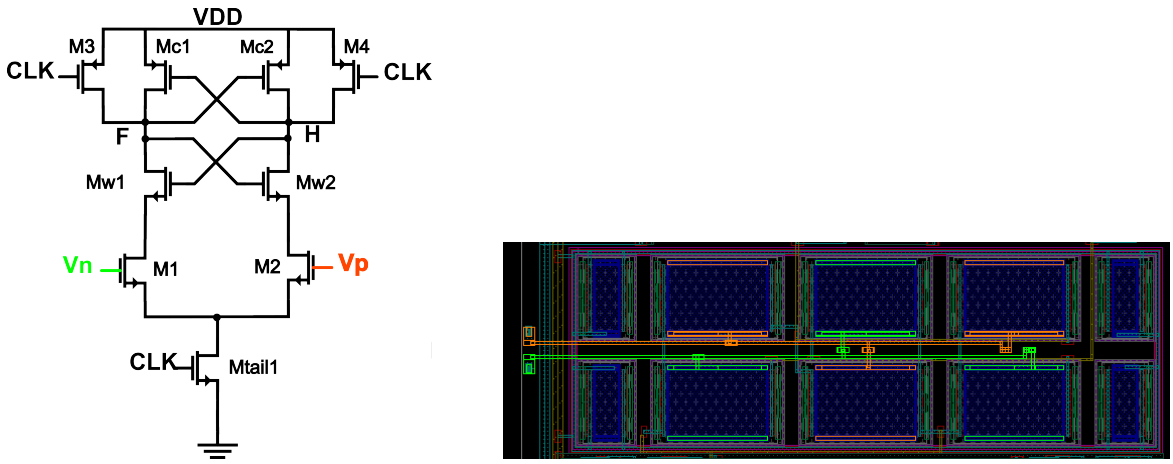


**Figure 48.** *Symmetrical Layout structure of the StrongARM stage in the Dynamic comparator.*

## 4.4. LAYOUT RESULTS

**4.4.1. Static Comparator** The layout of the static comparator is seen in Figure 49. With a total area of $29[\mu m]$ x $30[\mu m]$. The layout passes DRC (Design Rule Checks) and LVS (Layout v Schematic). Then, a parasitic extraction (R+C+CC) was done in order to verify the performance of the comparator to be ready for fabrication. The results of the post-layout simulations can be seen in Tables 11 and 12.

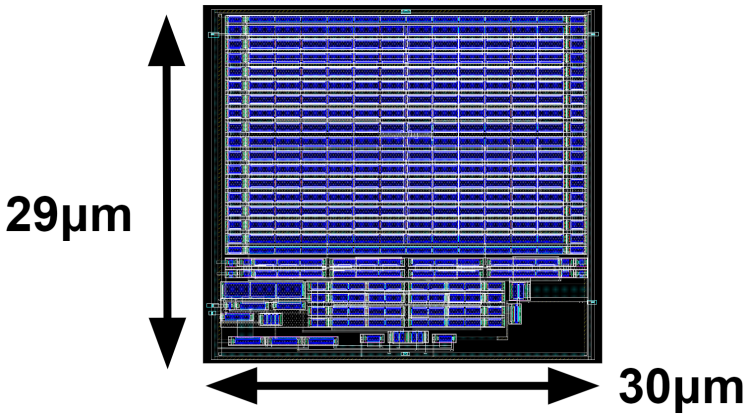


**Figure 49.** *Final layout of the static comparator.*

**Table 11.** *Results for the Static Comparator's Layout without hysteresis.*

| Parameter | Condition | Units | Target | PVT | | | MC | |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Mean | $3\sigma$ |
| Static Current | Out High Vinn = 900mV | uA | $<$25 | 18.77 | 20.77 | 24.1 | 20.74 | 2.49 |
| | Out Low Vinn = 900mV | uA | $<$25 | 20.41 | 22.49 | 24.34 | 22.29 | 2.61 |
| Propagation Delay | $\Delta$Vin = 5 mV High to Low | ns | $<$50 | 26.02 | 30.55 | 37.02 | 30.92 | 18.39 |
| | $\Delta$Vin = 5 mV Low to High | ns | $<$50 | 25.27 | 29.39 | 37.37 | 29.55 | 15.66 |
| Bandwidth | - | MHz | 5 | 10.2 | 13 | 14.84 | - | - |
| Offset | - | mV | ±5 | - | - | - | -0.25 | 3.6 |
| PD Current | | nA | $<$5 | 0.09 | 0.13 | 4.6 | - | - |
| Input Range | | V | - | 0.51 | - | 0.98 | - | - |
| Slew Rate | $\Delta$Vin = 5 mV High to Low | V/us | - | 228.4 | 422.7 | 533.3 | 413.6 | 90.57 |
| | $\Delta$Vin = 5 mV Low to High | V/us | - | 134.5 | 259.4 | 337.3 | 256.5 | 27.84 |
| Sensitivity | - | mV | - | 0.38 | 0.9 | 1.84 | - | - |
| DC Gain | - | dB | - | 59.5 | 69.58 | 74.61 | - | - |
| PSR | - | dB | - | -47.21 | -33.31 | -26.25 | - | - |
| Input Noise | RMS | uV | | 67.51 | 82.63 | 311.5 | - | - |
| Offset Drift | -40 to 125 | uV/C | | - | 1.21 | - | - | - |

Analyzing these results, the design meets all requirements, even with the added parasitic capacitances, resistors, and variations due to layout-dependent effects.

Both propagation delay and current ended up as marginal values for Montecarlo simulations. This means that if the circuit needs to be faster, either the conditions of differential input must increase or the restrictions must be lowered.

It is important to note that the significant increase in propagation delay was primarily

caused by parasitic capacitors, especially in the decision stage, where a total of $7$ [fF] in each node increased the delay by $\approx 5$ [ns]. Figure 50 shows the resulting slowest, fastest and nominal response of the extracted view.

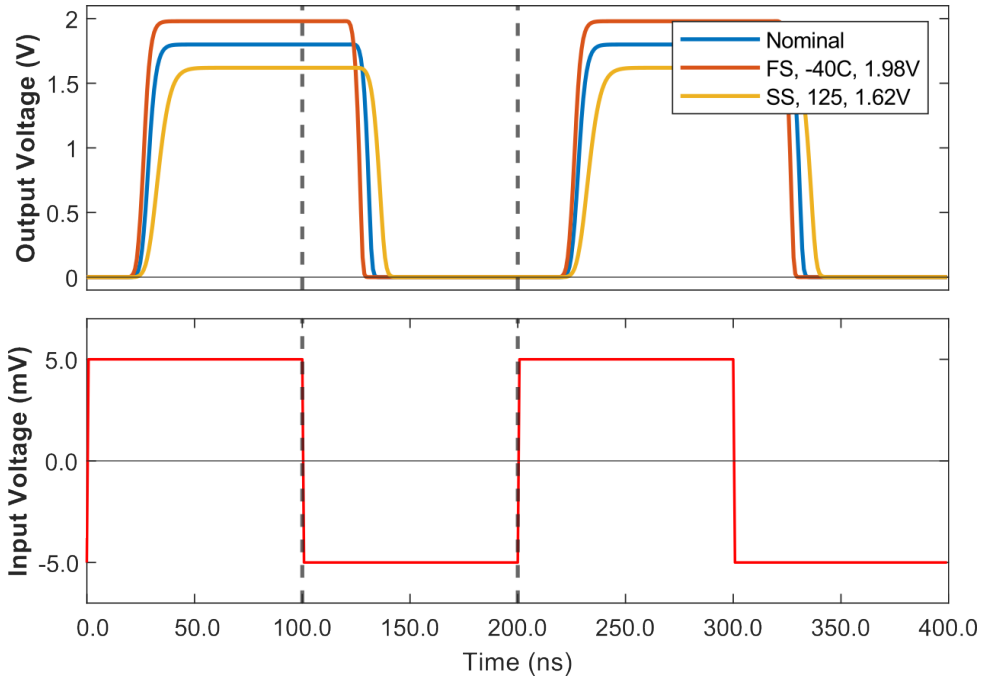


**Figure 50.** *Nominal, fastest and slowest output in the static comparator without hysteresis after parasitic extraction.*

Thanks to symmetrical placement and routing, together with the addition of dummies, the offset didn't present a significant increase other than in the mean value where the long cables going to the output had the highest effect. A histogram with the offset simulation can be seen in Figure 51

Finally, observing the Power Down current had a minor increase, which is still lower than the desired amount of $5$ [nA]. This is mostly thanks to the parasitic resistances which lowered the current going through each transistor.
Now, for the comparator with hysteresis, the results can be seen in Table 12.

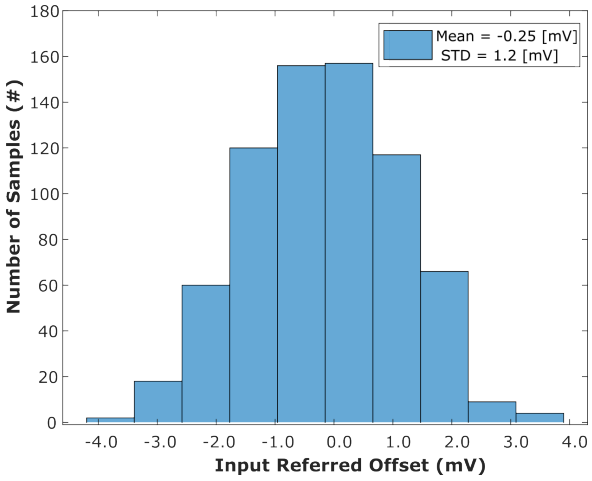


**Figure 51.** *Offset histogram of the static comparator without hysteresis after parasitic extraction.*

For this design, the propagation delay increased significantly, crossing $40$ [ns] in PVT corners and slightly increasing the standard deviation. Figure 52 shows the response of the slowest, fastest, and nominal corners.

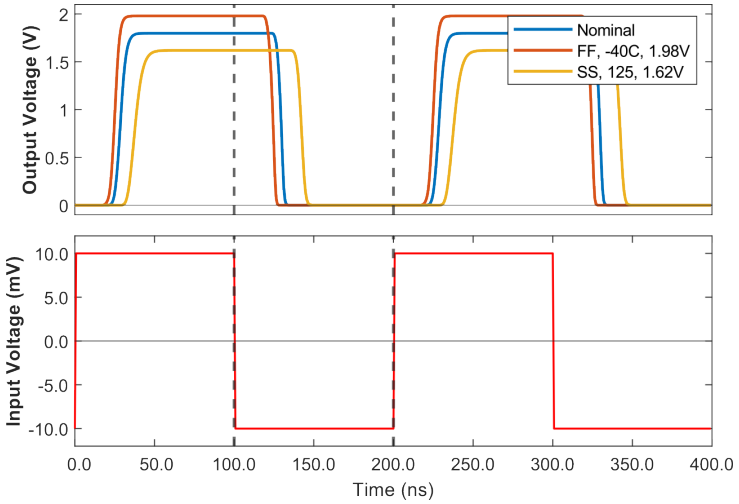


**Figure 52.** *Nominal, fastest and slowest output in the static comparator with hysteresis after parasitic extraction.*

**Table 12.** *Results for the Static Comparator's Layout with hysteresis.*

| Parameter | Condition | Units | Target | PVT | | | MC | |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Mean | $3\sigma$ |
| Static Current | Out High Vinn = 900mV | uA | $<$25 | 18.34 | 19.93 | 21.66 | 20.05 | 2.52 |
| | Out Low Vinn = 900mV | uA | $<$25 | 19.96 | 21.64 | 23.46 | 21.77 | 2.7 |
| Propagation Delay | $\Delta$Vin = 10 mV High to Low | ns | $<$50 | 23.98 | 29.3 | 42.12 | 29.56 | 8.34 |
| | $\Delta$Vin = 10 mV Low to High | ns | $<$50 | 24.48 | 28.67 | 37.67 | 29 | 6.6 |
| Bandwidth | - | MHz | 5 | 9.8 | 13.1 | 15.3 | - | - |
| Offset | - | mV | ±5 | - | - | - | -0.66 | 3.54 |
| Hysteresis | - | mV | - | - | - | - | 1.51 | 2.64 |
| PD Current | | nA | $<$5 | 0.03 | 0.08 | 4.26 | - | - |
| Input Range | | V | - | 0.52 | - | 0.95 | - | - |
| Slew Rate | $\Delta$Vin = 10 mV High to Low | V/us | - | 323.5 | 458.8 | 546 | 458 | 41.13 |
| | $\Delta$Vin = 10 mV Low to High | V/us | - | 177.9 | 266.4 | 344 | 267.5 | 24.87 |
| Sensitivity | - | mV | - | 2.8 | 4 | 6.8 | - | - |
| DC Gain | - | dB | - | 70.52 | 77.93 | 82 | - | - |
| PSR | - | dB | - | -43.37 | -31.14 | -21.62 | - | - |
| Input Noise | RMS | uV | | 78.14 | 98.15 | 156.29 | - | - |
| Offset Drift | -40 to 125 | uV/C | | - | 1.27 | - | - | - |

For the offset results, the mean value significantly increased to $-660$ [$\mu$V] mainly due to the sum of asymmetries throughout the whole layout, mainly near the gates of transistors in the decision stage as the routing had to be modified to fit the wider transistors. The offset variation was almost the same as in the schematic. The results can be seen in Figure 53.

The rest of the measurements remained similar.

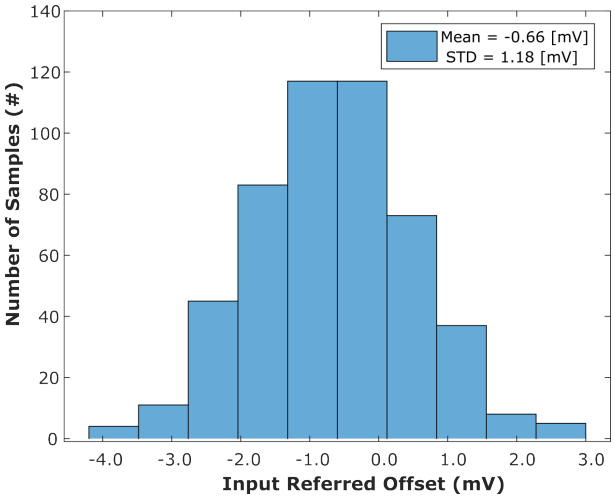


**Figure 53.** *Offset histogram of the static comparator with hysteresis after parasitic extraction.*

**4.4.2. Dynamic Comparator** The layout of the dynamic comparator is seen in Figure 54. With a total area of $13.4[\mu m]$ x $13[\mu m]$. Similarly to the static the layout of the static comparator, the layout of the dynamic comparator passes successfully DRC and LVS. After carrying out the parasitic extraction (R+C+CC), the Table 13 shows the obtained results.

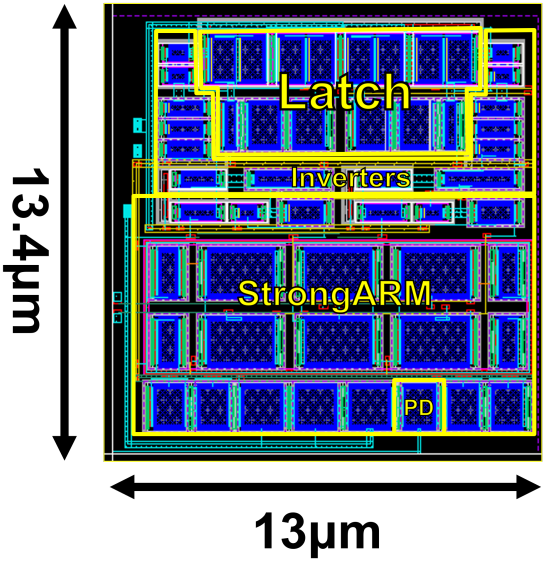


**Figure 54.** *Final layout of the dynamic comparator.*

**Table 13.** *Results for the Dynamic Comparator's Layout.*

| Parameter | Condition | Units | Target | Min | Typ | Max |
|---|---|---|---|---|---|---|
| Static current | CLK HIGH | nA | $<5$ | 0.020 | 0.041 | 2.529 |
| | CLK LOW | nA | $<5$ | 0.058 | 0.107 | 3.359 |
| Propagation Delay | Low-High $\Delta$Vin=5m | nA | $<50$ | 7.738 | 11.01 | 16.83 |
| | High- Low $\Delta$Vin=5m | nA | $<50$ | 13.87 | 21.02 | 34.5 |
| Dynamic current | $\Delta$Vin=300m | $\mu$A | $<25$ | 18.11 | 20.9 | 24.04 |
| Bandwidth | $\Delta$Vin=5m | MHz | $>5$ | 10 | 26 | 36 |
| PD Current | $\Delta$VIN Switching | nA | - | -0.104 | -0.082 | 3.512 |
| | VIN stable | nA | - | -0.12 | -0.037 | 2.933 |
| Input Range | | V | - | 0.519 | | 1.498 |
| Slew Rate | Low-High $\Delta$Vin=5m | V/$\mu$s | - | 110.1 | 188.9 | 301 |
| | High-Low $\Delta$Vin=5m | V/$\mu$s | - | 54.34 | 107.6 | 188 |
| Input Noise | | $\mu$V | - | 310 | 425 | 660 |
| **Parameter** | **Condition** | **Units** | **Target** | - | **Mean** | $\sigma$ |
| Offset | TCLK 500n Trise=600u | mV | $\pm$ 20 | | 0.37 | 1.97 |

In this table, the measurement for Offset Drift is not presented due to hardware and time limitations, as this value was expected to take around 3 days to measure using 1000 Montecarlo samples. It is also noted that offset in a typical temperature did not change significantly between schematic and post-layout, which leads us to believe that these changes due to temperature should be around the same as in the schematic.

### 4.5. COMPARISON WITH OTHER PROJECTS

To compare this project with other state-of-the-art comparators, Tables 14 and 15 were created, highlighting the main results found in the papers. It is important to note that

not every paper presented conditions used for verification, nor expanded which corners results are presented, or if Montecarlo simulations were used. In these cases, We assumed typical corners results and $3\sigma$ results for offset.

**Table 14.** *Comparison of Static comparators.*

| Parameter | Our Work (1) | Our Work (2) | Paper 1[17] | Paper 2[18] | Paper 3[19] |
|---|---|---|---|---|---|
| Technology | 28nm | 28nm | 90nm | 130nm | 150nm |
| $\Delta V_{in}$ [mV] | 5 | 10 | 1300 | 300 | 0.2 |
| Delay [ns] | 24.2 | 39.89 | 0.168 | 300 | 36.7 |
| Power [$\mu$W] | 38.95 | 42.28 | 103.4 | 1.05 | 227.7 |
| Offset [mV] | 3.6 | 3.54 | 186 | 2.055 | 15.5 |
| Area [$\mu m^2$] | 882 | 882 | 197.1 | N/A | N/A |
| PD Current [nA] | 4.6 | 4.26 | N/A | N/A | N/A |
| Extras | Power Down | Power Down | N/A | Latched | AIDA-C |

First, our designs are beaten in propagation delay by paper 1, which uses more than twice the power and uses digital 1s and 0s as its inputs. In terms of power, both designs are second to paper 2, which is designed for extra low-power energy harvesting chips at the cost of speed, being the slowest by far. In offset, the designs place second and third behind paper 2. In terms of area, our designs proved to be the biggest, but it is not clear in papers 2 and 3 whether a layout was made, implying that both of these works present schematic results. Finally, only our work presents results for power-down currents, although paper 3 adds a scheme, its current consumption is not specified in any results.

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[17] Satyabrata NANDA and Avipsa S. PANDA. “Design of conventional three-stage CMOS comparator in 90-nm CMOS technology and comparative analysis with its counterparts”. In: 2015

[18] Lukas NAGY et al. “Low-Power Rail-to-Rail Comparator in 130 nm CMOS Technology”. In: 2022

[19] Jose CACHACO et al. “Automatic technology migration of analog IC designs using generic cell libraries”. In: 2017

**Table 15.** *Comparison of Dynamic comparators.*

| Parameter | Our Work | Paper 1 [20] | Paper 2[21] | Paper 3[22] |
|---|---|---|---|---|
| Technology | 28nm | 130nm | 130nm | 90nm |
| Delay [ns] | 16.01 | 0.453 | 0.462 | 60.6 |
| Dynamic power[$\mu$W] | 37.62@10M | - | 104@200M | - |
| Static Power [nW] | 0.148 | 1.8 | - | 0.546 |
| Offset [mV] | 1.97 | - | 4.36 | - |
| PD Current [nA] | 3.51 | N/A | N/A | N/A |
| Extras | Power Down | - | - | - |

The delay in our work is the second slowest, although no author specifies the capacitance value they use for testing, and for paper 2 it is assumed that they do not use load capacitance, given the low delay and low power. In terms of dynamic power, our work consumes more power than paper three, but given the previous argument, it is not completely certain which consumes more power. On the other hand, in static current, our work has the lowest current of all, also achieving a lower offset than paper 3. Finally, our work is the only one to implement a power-down scheme.

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[20] N Gowtham KUMAR and B SRINIVAS. "Design of Low Power High Speed Dynamic Comparator". In: (2017)

[21] K. SWETHA et al. "Analysis and Simulation of Single Tail and Double Tail Circuits". In: 2019

[22] Jewel Mercy FERNANDES, Mahaveera K, and Soorya KRISHNA K. "Design of Double-tail Dynamic Latch Comparator for Low Power Application". In: 2019

# 5. CONCLUSIONS AND FUTURE WORK

## 5.1. Conclusions

After carrying out the design of the comparators, the following conclusions are reached.

- Two energy-efficient comparators were successfully designed within the desired specifications, using a 28 [nm] CMOS technology, validated through simulation, and presented in layout, achieving no errors in DRC and LVS. A parasitic extraction was used to re-verify the layout including undesired capacitances, resistances and layout dependent effects. Both comparators meet all design restrictions.

- Due to the need of non-latching positive feedback for the static comparator, which is achieved by adding diode-connected transistors in the decision stage, this stage ends up highly-loaded, resulting in a slower response than the dynamic comparator. These added transistors also have to match with the positive feedback transistors, increasing overall mismatch.

- Implementing a power down scheme comes with different problems, in this project, by adding parallel transistors a new path of leakage current is enabled causing a relatively high power down current even with large transistors. But, using stacked transistors result in an increase in load and reduced signal swings but with low leakage with small area.

- When performing the post-layout simulation, it is observed that the static comparator is more sensitive to capacitance variations, mainly in the decision stage,

which is highly sensitive to capacitive loads. On the contrary, the dynamic comparator is robust to variations in resistance and capacitance, even benefiting its performance thanks to these parasitic elements, such as the leakage current being lowered overall.

- At the time to compare different designs it was found that comparators vary considerably depending on their specific application, for example, a comparator designed for a SAR ADC is vastly different than a comparator in a PWM module. As such, other works often omit measurements as they are not relevant for that use scenario, making it almost impossible to create a universal figure of merit.

## 5.2. Future Work

Below are some recommendations to improve the implementation of the circuit and thus its performance for future proyects.

- Implement an offset compensation scheme such as output or input offset cancellation for both comparators.
- Implement a hysteresis control scheme for the static comparator to reduce variability for PVT corners and Montecarlo simulations.
- Verify the performance on the comparators using non-ideal biasing components by replacing the power supply by a 1.8[V] LDO and the current source by the 1 [$\mu$A] current reference circuit, both of which also include the BGR.

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