Conception and Modeling of a Low-Voltage DC/DC Power Supply in Multiphase Buck-Converter Topology (Board Layout, Measurements and Simulation)

By

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Abstract

This work is mainly focused on the development of a simplified simulation model for a multiphase Buck converter, based on a real circuit, which uses a PWM controller. The circuit is implemented on a board and has the main requirements of a dc/dc converter for PC applications. It uses passive components in the input and output filters; drivers and power MOSFETs in the conversion stage and a PWM Multiphase Buck controller (ADP3168) programmable through capacitors and resistors. The Controller regulates the output voltage of the circuit using PWM pulses to change the duty cycle of the power MOSFETs.

The simulation model was built using ideal and behavioral Pspice® components like operational amplifiers, resistors, capacitors, etc. and it is formed by two main stages: a power stage and a control stage. The power stage replaces all passive components by equivalents plus main parasitic resistances; for instance, a capacitance and a series resistance represent the output capacitors. The PWM controller model that was created using the datasheet and the compensation network form the control stage. It implements a voltage mode control loop and a Current Balancing circuit. Secondary security functionalities were omitted.

DC and transient measurements were carried out on the real circuit in order to make adjustments to the simulation model. On DC measurements, the most important achievement is the implementation of a dynamic output voltage depending on the total output current. Current sharing and output voltage versus input voltage also have a similar behavior to measurements. On transient measurements, comparison between the waveforms of the simulation and real circuit are mainly similar, but small parameters like Overshoot, Undershoot, etc. could not be matched.

Detailed transient analysis cannot be carried out using this model since the accuracy of the results cannot be granted. Nevertheless, it is possible to use the model to analyze the behavior of the control stages in a multiphase buck converter versus high and low currents, input voltage, frequency of operation, etc.

Resumen

Este trabajo está enfocado principalmente en el desarollo de un modelo de simulación simplificado para un Convertidor Multifase de Buck, basado en un circuito real. El circuito fue implementado en una tarjeta y cumple con los principales requerimientos de un convertidor dc/dc usado en aplicaciones para PC. Se usaron elementos pasivos para los filtros de entrada y salida, así como "drivers" y MOSFETS de potencia en la etapa de conversión, además de un controlador PWM (ADP3168) programable a través de condensadores y resistencias. El controlador regula la tensión de salida del circuito cambiando el ciclo de trabajo de los transistores.

El modelo de simulación está formado por componentes ideales y programables (.abm) en Pspice®, tales como resistencias, amplificadores operacionales, etc. Se pueden diferenciar dos etapas principales: una etapa de potencia y una etapa de control. En la etapa de potencia se reemplazaron los componentes pasivos por sus equivalentes ideales y las resistencias parásitas mas importantes. Por ejemplo, los condensadores fueron reemplazados por un condensador más una resistencia serie. El modelo del controlador PWM que fue creado a partir de la hoja de datos, y la redo de compensación forman la etapa de control. Esta implementa un lazo de control de voltaje y un circuito de balance de corriente. Funciones de seguridad fueron omitidas.

Se realizaron pruebas en DC y transitorios en el circuito real para ajustar el modelo de simulación. En DC o estado estable el logro más importante fue la implementación de la pendiente dinámica en la tension de salida, que es proporcional a la corriente total de salida. Se logró un comportamiento similar en el balanceo de corriente entre las fases y la tensión de salida ante cambios en la tensión de entrada. En las medidas

transitorias, se compararon las formas de onda y se obsevó un comportamiento similar aunque parámetros específicos como sobrepaso, tiempo de subida, etc. no pudieron ser totalmente ajustados. Este modelo es útil para estudiar el comportamiento del circuito en estado estable. Debido a la falta de fidelidad en respuesta transitoria, no es recomendable realizar análisis transitorios; para tal fin se requiere de un nivel de descripción más detallado dentro del modelo de simulación.

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Chapter 1
INTRODUCTION

Since the early 80's, the computer industry has undergone great expansion. Processors are becoming faster and more powerful, thanks to the increasing number of transistors per unit area. In order to limit the associated increase in power losses, the voltage level required by the transistors underlying the microprocessors has decreased continuously, approaching 1V. On the other hand, the relative voltage tolerances for steady state and transients of the processor input voltage remain constant or smaller leading to a decreasing absolute voltage tolerance. Since the power consumption of the processor is growing, currents of 100A and higher will be required by the processor in the near future.

The current slew rate ($di/dt \approx 200A/\mu s$) caused by rapid load changes of the microprocessor requires a fast response of the voltage regulator, therefore the transient response of the voltage converter becomes of major importance to maintain an accurate voltage regulation. The need for a fast transient response and the continuously decreasing voltage tolerance droveg up the switching frequency of the voltage regulator to frequencies of around 150 to 500 kHz in Year 2002.

In order to keep up with these requirements, the computer power supplies need to be constantly improved although when the required current and power increase, the available board space remains constant or gets even smaller. This work focuses on the system's dc/dc power supply that is either implemented on-board which is in the case for most motherboards or in the form of Voltage Regulator Modules (VRMs). Latter are used in high-end computer systems, requiring better performance. The standard topology for dc/dc core supplies is the multiphase synchronous buck topology. Figure

1.1 shows a typical two-phase converter section on a motherboard. Each phase consists of one high-side and two low-side MOSFETs in parallel as well as several passive components such as output capacitors and chokes. The dc/dc converter section of today's motherboards usually consists of two to three phases. In future, increasing processor load currents will drive up the need for more phases.

Basically, A multiphase buck converter is in charge of the power conversion to supply the microprocessor. Its input is a 12 V silverbox DC output voltage and its output is a DC voltage between the 1 and 1.5 V. as mentioned, the increasing power leads to higher output currents and small voltage tolerances (output voltage ripple ≈ 10mV).

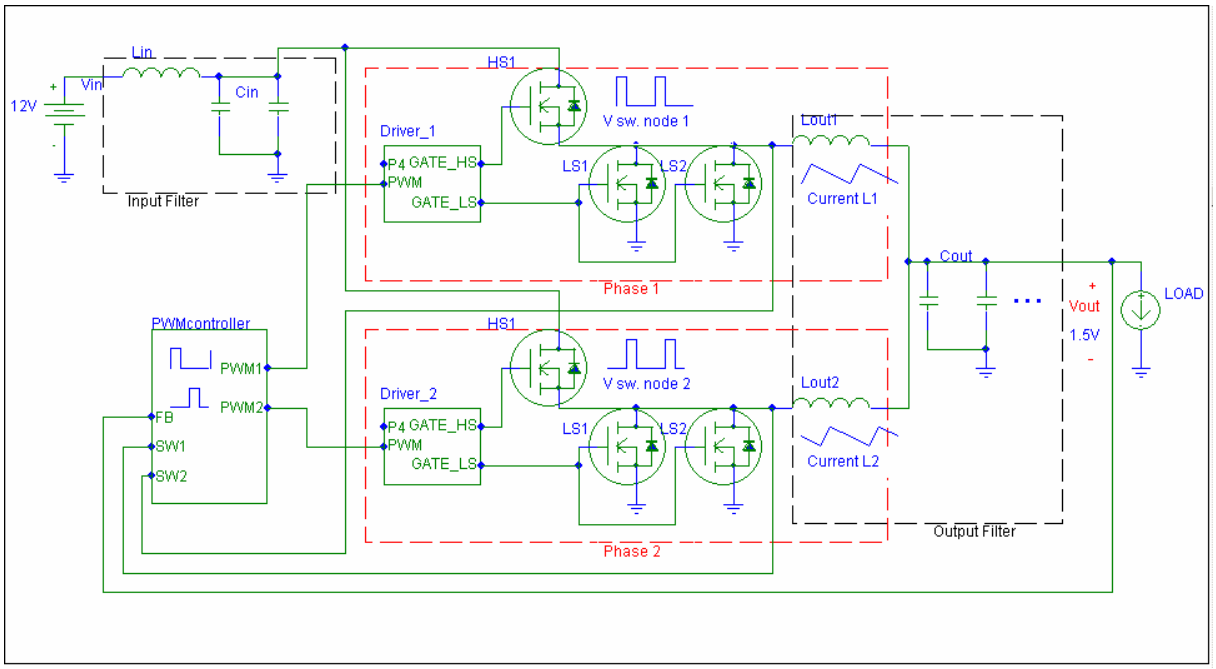

Figure 1.1 Scheme of 2-phase buck converter topology

Author's design

1.1 OBJECTIVES

The purpose of this work is to develop a dc/c multiphase buck converter board and a simulation model of that board mainly focused on a PWM controller model plus a compensation network. The board has to respond to the trends for next generation microprocessors. Lately, the evolution of microprocessors demands a better performance in terms of power management and thermal behavior for desktop and notebook applications. Searching these goals, it is important to know in details the behavior of each stage of a commonly used power supply, such a multiphase dc-dc buck converter.

The achievement of this main goal assumes:

- It is important to know in details the behavior of the power stages and mainly of the control stage in the multiphase dc-dc Buck converter. Therefore, a board with multiple points of test is required, in order to measure specific signals that will help to understand the behavior of the total system.

- Selection and put into operation of a proper Synchronous Buck controller, selecting additional components for its proper operation.

- Development of an approximated simulation model for the PWM controller, plus a simplified model for power stages to form an entire dc/dc converter that would help to evaluate the performance of the circuit versus load currents, input and output voltages, etc.

- Compare simulated waveforms to measurements in order to verify the proper implementation of the controller functions in the simulation model.

- Analysis of the transient response, high and low load, high and low input voltage, operation of the controller, balancing of the phase currents, dynamic output droop, component tolerances, etc. in the converter operation.

1.2 Principle of operation of a Multiphase Buck Converter

Let us consider the operation of the buck converter shown in Figure 1.2

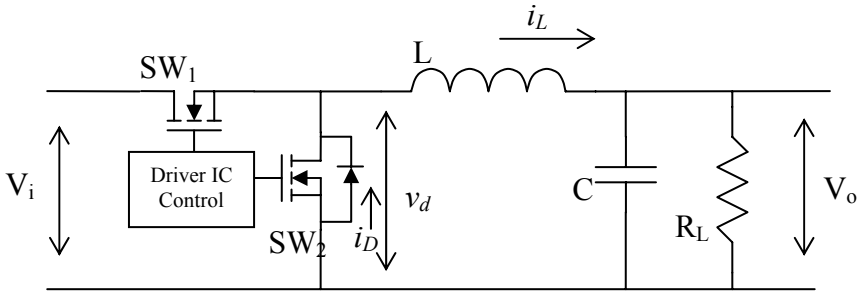

Figure 1.2 Basic Buck Converter Circuit

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When controlled by the signal of a pulse-width modulator (PWM), its dc input voltage V_i is converted to a regulated dc output voltage V_0. During normal operation, the electronic switches of the buck converter are turned on and off, driven by a PWM controller (and a gate driver) at a high switching frequency (typically 100KHz - 500KHz). Thereby both switches are never ON at the same time in order to avoid a short-circuit from the input-voltage source to ground. The state of the electronic switches and the waveforms of i_L, i_{sw1}, i_{sw2}, v_{sw1} and v_{sw2} are shown in Figure 1.3. In the waveform diagram, the following assumptions have been made:

- The switching action of the converter has reached steady state.
- The percentage of time during which the high side switch is turned on is defined as the duty cycle D:

$$t_{on} = DT \qquad \textbf{Eq. 1.1}$$

where 1/T is the switching frequency.

- The inductance L is so large that the inductor current i_L will not decay to zero during the time the switch is turned off (continuous-mode operation).
- The output filtering capacitor C is so large that within a switching cycle the change in V_0 is very small.
- Parasitics, such as stray inductances and resistances due to the board layout and packages are neglected.

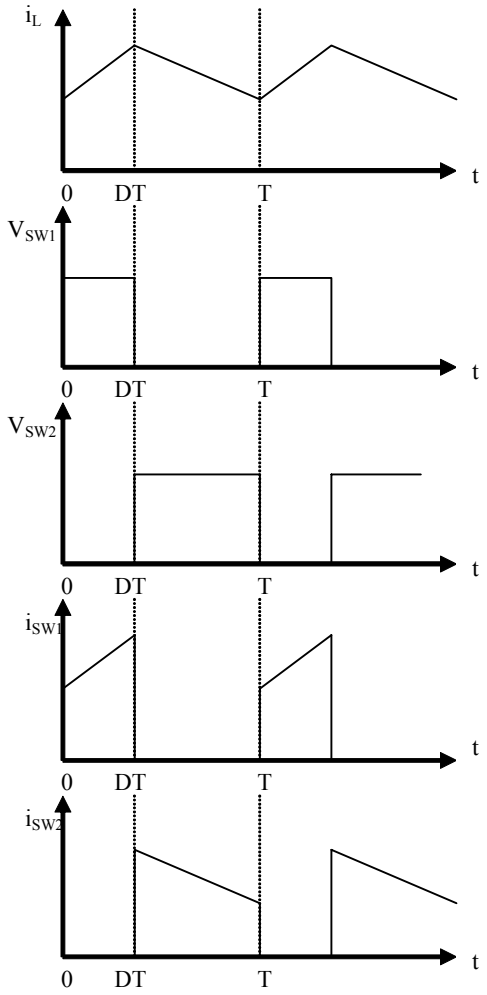

Figure 1.3 Ideal current and voltage waveforms of a buck converter.

Author's design

Having made above assumptions, the examination of the operation of the converter can be derived step by step. At t = 0, the switch SW_1 is turned on, and the inductor current i_L builds up. This current increases linearly, and the current i_D at this time is zero, because the switch SW_2 is in the OFF state. For $0 < t < DT$, the switch SW_1 is maintained in the ON state, and at t = DT, it is turned off, and SW_2 is turned on; consequently, the way of the inductive current i_L is now forced to pass through SW_2. During the small transition time before SW2 is ON, the current flows through the intrinsic diode of SW2. For $DT < t < T$, SW_1 remains OFF, and SW_2 ON. The inductor current i_L continues to flow through SW_2, while its amplitude decreases. At t = T, SW_1 is turned on again while SW_2 is turned off, and a new cycle starts.

The waveform of v_D in Figure 1.4 shows that within each cycle we have

$$v_D = V_i \quad \text{for } 0 < t < DT \qquad \textbf{Eq. 1.2}$$

$$v_D = 0 \quad \text{for } DT < t < T \qquad \textbf{Eq. 1.3}$$

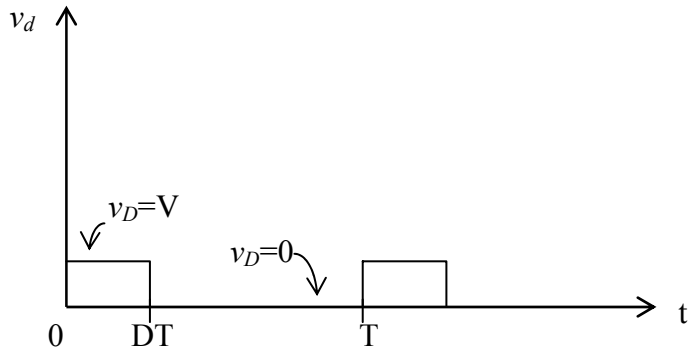

Figure 1.4 Voltage V_D waveform

Author's design

The average value of v_D is therefore equal to DV_i. If it is assumed that the filtering circuit (L and C) allows only the dc component of V_D to appear at the output we obtain:

$$V_0 = \text{average value of } V_D = DV_i \qquad \textbf{Eq. 1.4}$$

The output voltage V_0 can therefore be controlled by varying the duty cycle D of the driving pulses applied to the switching transistors according to feedback signals such as the output voltage. This method is called “Pulse Width Modulation”, or briefly, “PWM”.

There are basic two types of buck converters, depending on the switches used: The high side switch can be a MOSFET and the low-side switch a diode. In this case the converter is called “Asynchronous Buck Converter”. When the high-side MOSFET is ON, the current through the diode is zero because Vi reversely biases it, and when the MOSFET is turned off, the inductor current is forced to pass through the diode, biasing it forwardly.

In striving for maximum efficiency, one of the largest power-loss factors to consider is that through the diode. The power dissipated in the low-side switch is simply the diode’s forward voltage drop multiplied by the current through it. To minimize this loss, most DC-DC switching regulator circuits use Schottky-type diodes whose relatively low forward voltage drop and high speed minimize losses. However, for maximum efficiency, another MOSFET instead of a diode, can be used as low-side switch. This is known as "synchronous rectification" and the associated type of converter is called “synchronous buck”. The synchronous rectifier switch (SW_2) is open when the main switch (SW_1) is closed, and vice versa. To prevent cross conduction in case both switches are closed at the same time, the switching scheme must be “break-before-make”. Consequently, the diode is still required to conduct the current during the so-called dead time between the opening of the main switch and the closing of the synchronous rectifier switch. In most cases the MOSFET’s (intrinsic) body diode is utilized during the dead time. Some MOSFET technologies

implement Schottky diodes directly or chip-by chip in the package. In other cases, additional discrete Schottky diodes are used in parallel to the low-side MOSFET.

If for the design of a high current supply a normal regulator is used, this current flow will increase the thermal stress on the individual power components, dissipating a big amount of power and also reducing these components life. The solution for this problem is using a multiphase converter, this means, paralleling several power regulators, such that they share the amount of current that is flowing into the circuit.

In effect, a multiphase converter interleaves the clock signal of the paralleled power stages, reducing input and output ripple current, without increasing the switching frequency. The usual way of interleaving the regulator clock signals is separating them 360°/m, being m the number of phases.

In Figure 1.5 it is shown a scheme for a 2-phases converter, and the typical waveforms for the current through the different output inductors.
The use of more than one phase for high current purposes leads to several advantages, as:

- Since the output current is shared by the different phases, its ripple is less than the one obtained when having only one phase.
- The size and cost of the capacitors are reduced, as well as the inductor values, which means at the same time better dynamic response to load transients.
- The power losses in the circuit also decrease, helping achieve high efficiency.
- Better thermal behavior due to the distribution of the heat over the PCB area, beause it is concentrated at more components, reducing overheating and extending life times of components.

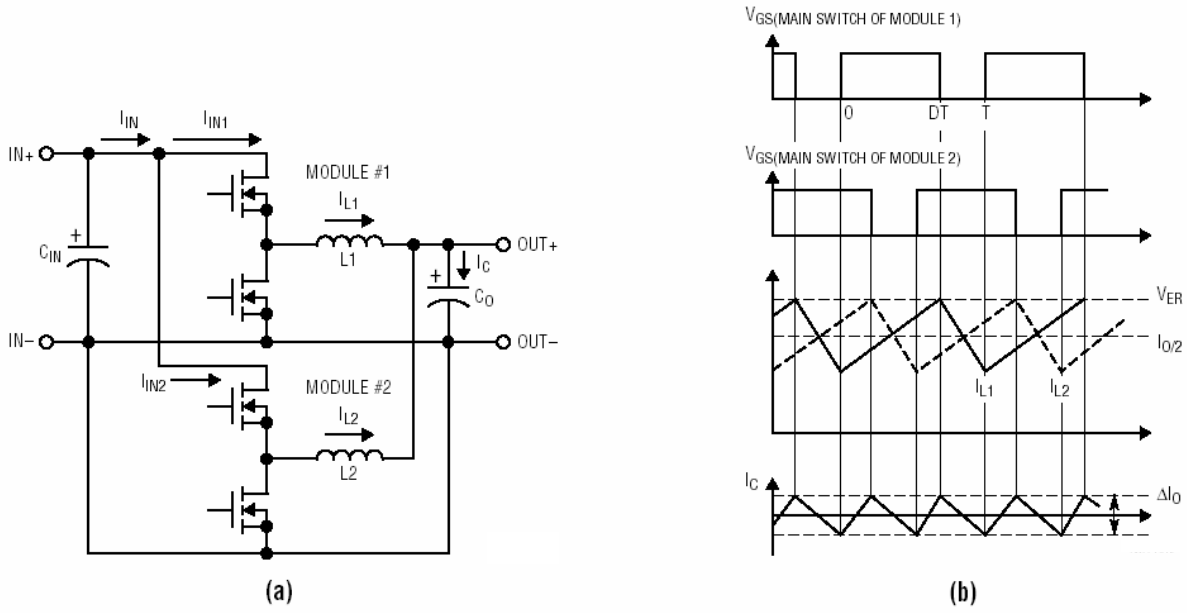

Figure 1.5 2-Phases Converter. (a) Schematic (b) Typical waveforms

Author's design

Chapter 2

TEST BOARD 1.0

2.1 Purpose

Measuring on a real circuit is the best way to confirm simulations and theoretical results. Consequently, the conception of a board implementing the circuit under study becomes of major importance in order to have better reference data to compare simulation results.

The most challenging application of the Multiphase Synchronous Buck Converter topology is the conversion from a 12 V "Silverbox" output voltage to the level required by a microprocessor, and the main parameters of this conversion for proper processor operation are specified by the most important microprocessor manufacturer, Intel. The latest version of this specification is the VRD10, for next microprocessor generation. Thus, this board will carry out the same main requirements:

- Input Voltage (V_{IN}) = 12 V
- VID Setting Voltage (V_{VID}) = 1,5 V (programmable through VID* Code)
- Nominal Output Voltage at No load (V_{ONL}) = 1,480 V
- Nominal Output Voltage at Full Load (V_{OFL}) = 1,3256 V
- Load Line (R_O) = 2,375 mΩ (Depending on series resistance of bulk output capacitors)
- Maximum Output Current (I_O) = 65 A
- Number of phases (n) = 3 (2)*
- Switching Frequency per Phase (f_{SW}) = 267 kHz (100-600KHz)**

2.2 General Description

Based on their functions, it is possible to distinguish two different stages: a power or conversion stage, formed by the input and output filter and power MOSFET's; and a control stage, in this case, a multiphase synchronous Buck controller, compensation components and external circuitry of the controller. Drivers for the transistor are in charge of the switching control, over-temperature and short-through protection of the transistors, thus they could be in either group. For this study, drivers will be included on the power stage.

* 6-bit Voltage Identification Code
* For an ease and more detailed study of the PWM Microcontroller behavior, the frequency and the number of phases will be selectable, and the previous values will be used for the calculation of components around the Microcontroller.

2.2.1 Power Stages

2.2.1.1 Input and Output Filters

The output and input filters are formed by passive components L and C as shown in Figure 2.1. In the input, an inductor followed by a bulk capacitor bank are placed between the primary power supply Vcc and High Side transistors, in order to prevent large voltage transients and to reduce the input current *di/dt* due to the switching action of the MOSFET's. The location of some ceramic capacitors near components like drivers and the Microcontroller is recommended due to its low series resistance (ESR) and series inductance (ESL), reducing the effects of parasitic ESL of bulk capacitors. In this case, the inductor value selected is L_{IN} = 1μH with a series dc resistance (DCR) of 1mΩ. The bulk capacitor bank is formed by six 100μF 20V capacitors (C_{IN} = 600μF), and there are also 2 ceramic capacitors of 4,7μF near each switching node.

An inductor connected between the switching node and a capacitor bank form the output filter. The choice of inductance for the inductor determines the ripple current in the inductor. Less inductance leads to more ripple current which increases the output ripple voltage and losses in the MOSFET's but allows using smaller inductors and, for a specified peak-to-peak transient deviation, less total output capacitance.

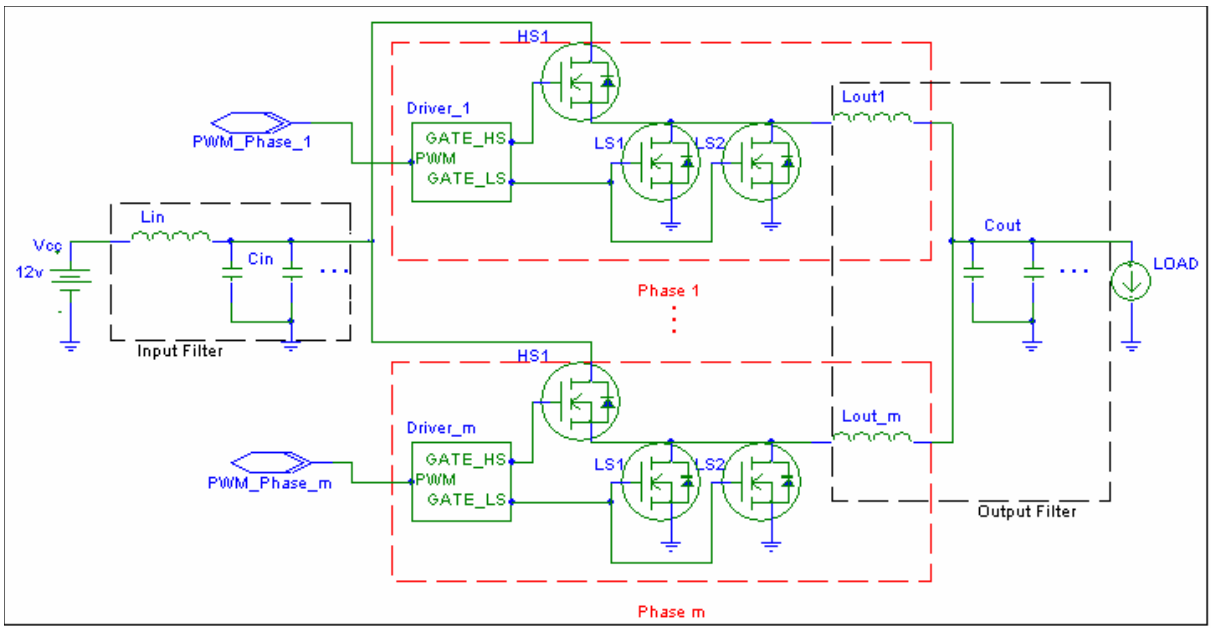

Figure 2.1 Power Stages in a multiphase Buck converter.

Author's design

Conversely, a higher inductance means lower ripple current and reduced losses in the MOSFETS but requires larger inductors and more output capacitance for the same peak-to-peak transient deviation. The selected value for the output inductance is L_{OUT} = 600nH with a DCR of R_L = 1mΩ. Another important issue when selecting an inductance is the availability of the values; therefore it is better, first to choose commercial values for inductance, and next, finding values of capacitors and resistors in order to match the specifications.

The output decoupling capacitors bank is formed by both, bulk and ceramic capacitors, and their values must be adapted to accomplish the transient response requirements. For a maximum load step ΔI_O it is possible to find a lower value limit for capacitance, given by:

$$C_{X(MIN)} \geq \left(\frac{L \times \Delta I_O}{n \times R_O \times V_{VID}} - C_Z \right) \qquad \textbf{Eq 2.1}$$

where C_Z is the total ceramic capacitance which must be placed inside the microprocessor socket cavity and along the outer edge as well. Having several capacitors placed in parallel will reduced the ESR, ESL and consequently the output voltage ripple. The selected values are C_X = 8000µF (8 Rubikom capacitors 1000µF 16V) for a total ESR of R_X = 2,375mΩ (19mΩ each) and C_Z = 70,5µF (15 ceramic capacitors 4,7µF).

2.2.1.2 Power MOSFETs

The transistors in buck converters need to be able to switch high currents at high frequencies and to fulfill additional requirements. Since conventional transistors are not suitable for this task, special MOSFETs such as Power MOSFETs are needed. Over the time, the technology that underlies power MOSFETs has been continuously improved. The two most important technologies are planar and trench technologies. For this project, Infineon's OptiMOS®2 technology is used, which is based on a trench technology.

OptiMOS®2 is a Power MOSFET which characteristics are shown in figure2.2 In this section, an overview of the trench technology will be given with its most important characteristics.

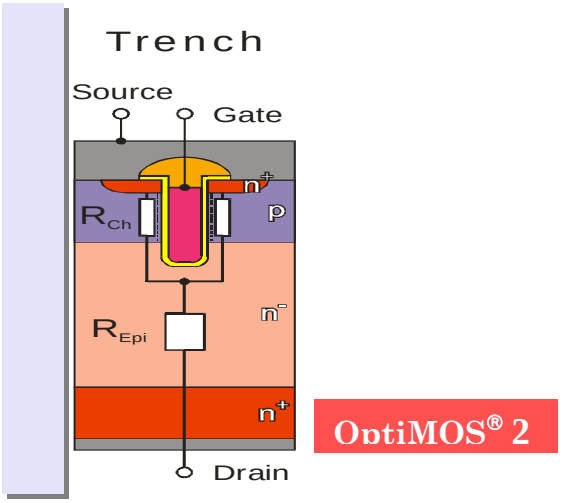

Figure 2.2 OptiMOS®2 technology

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The Figure of Merit (FOM) of a power transistor is a measure of performance for a given MOSFET technology. It is commonly defined as the product of the on-state resistance $R_{ds(on)}$ and the gate charge Q_g, i.e. FOM = $R_{DS(on)}$*Q_g. When increasing the size of a chip, $R_{DS(on)}$ decreases which is an advantage since a small resistance is needed when a high current is flowing. However, this increases also the gate charge Q_g. A higher gate charge leads to higher switching and driver losses. In case of the High-Side MOSFETs (HSMOS), it is reasonable to use a smaller Q_g even though the $R_{DS(on)}$ is higher. This is because the time during which the HSMOS is conducting is only around 15% of the total cycle. Thus, the losses due to conduction are not significant as compared to the switching losses.

For the case of Low-Side MOSFETs (LSMOS), the opposite applies. This transistor is turned on approximately 85% of a cycle and consequently, the losses due to commutation are small compared to the DC losses. Therefore, this device should have an $R_{DS(on)}$ value as small as possible.

Another technology parameter to consider is related to the chip area of the MOSFET. A bigger area means fewer MOSFETs on the same wafer. Consequently, this results in increased costs per MOSFET.

Trench technologies avoid the JFET resistance, thus reducing the $R_{DS(on)}$ value. Furthermore, this technology allows more cells to be allocated in a given area, which reduces the $R_{DS(on)}$ per area further. OptiMOS®2 reaches a particularly low FOM as shown in the comparison in Table 1.

OptiMOS®2		OptiMOS®	
Device	FOM($\div 10^{-10}$) (nC · mΩ)	Device	FOM($\div 10^{-10}$) (nC · mΩ)
IPD06N03LA	0,912	IPD06N03L	1,6198

Table 1 F.O.M. Comparison

The MOSFETs used in a multiphase buck converter are "Power MOSFETs". They support high currents and are based on the technology explained above.

One of the characteristics of Power MOSFETs is that they use the whole thickness of a wafer. This technique is called "Vertical Channel Design". The drain and source are placed on the opposite sides of a wafer. This is suitable for power devices, as more space can be used as source. Moreover, as the length between the source and drain is reduced, it is possible to increase the drain-to-source current rating.

2.2.1.3 Gate Drivers

The gate driver is one of the most important devices in a synchronous buck converter. It has two basic tasks. It amplifies the signals coming from the PWM controller and it protects the Power MOSFETs. For this thesis, the Infineon's gate driver TDA21101G is used. Its features that are also typical for other gate drivers are outlined in the following. Due to its fast rise and fall times, the TDA21101G has the capability to work with switching frequencies of up to 2 MHz. It is further capable of driving a gate peak current of up to 4A. The general function of the driver is to amplify the logic signal from the PWM controller, which is fed into the MOSFET gate. While the gate driver charges the gate of a MOSFET, the MOSFET's $R_{DS(on)}$ resistance decreases. For the LSMOS, it is desirable to apply the maximum available gate voltage of 12V. For the HSMOS, the TDA21101G allows the gate voltage to be adjusted by means of an input called PVCC. This pin is a high-impedance input used

only for this purpose. A bootstrap diode is integrated into the gate driver. This diode is used to assure that the voltage at the gate of the HSMOS is larger than the input voltage. It must be ensured that both transistors are not conducting at the same time. This is accomplished by the driver's adaptive gate drive control.

2.2.1.4 Current Sense Resistors

Sense Resistors are placed in each phase, in series with the output inductors, in order to measure the phase current which must be shared uniformly between the phases, otherwise one or two phases could be too hot, resulting on possible damages and bad thermal behavior. These resistors have a value around 1mΩ and they are designed to dissipate a maximum power of 2 W. The voltage drop measured on the resistor will be proportional to the current flowing through it, following the Ohm law.
i.e. $i_{phase} = V/R$
These sense resistors are just for measure purposes in order to compare the model with the board, and are not used in "real" motherboards because of their high costs. The controller implements another methods to measure the current per phase.

2.2.2 Control Stage

The most important component in the control stage is the controller in charge of regulating the output voltage and responding to transient changes via using the Pulse Width Modulation (PWM) plus safety functions like Current limit, short circuit and latch-off protection, etc.

Nowadays, there are several multiphase synchronous Buck controllers in the market. For this study, the ADP3168 was selected because its features respond to the actual requirements, as well as its good technical datasheet and easy implementation. The

ADP3168 was design to control 2, 3 or 4 phase Synchronous Buck converter with frequency of operation up to 1MHz per phase and 6-Bit digitally programmable (VID) range from 0,8375V to 1,6V output voltage.

In order to program the Output Voltage, frequency of operation, and all features, the ADP3168 controller needs an external circuitry formed by resistors and capacitors which selection criteria is based on the datasheet and application information using operation parameters (output and input voltage, maximum output current, switching frequency, number of phases, etc.) and values of power components (input and output filter components, MOSFET's $R_{DS(ON)}$, etc.). Equations were used to find the component values as follows:

The resistor R_T is use to set the internal clock frequency, and they have the relation,

$$R_T = \frac{1}{\left(n \times f_{SW} \times 5{,}83pF\right) - \frac{1}{1{,}5M\Omega}} \qquad \text{Eq. 2.2}$$

where 5,84 pF and 1,5 MΩ are internal controller components. Solving for a range of frequency from 150 kHz to 600 kHz per phase and 2 or 3 phases it is obtained R_{TMIN}= 102 kΩ (3 phases at 600 kHz)and R_{TMAX}= 943kΩ (2 phases at 150 kHz).

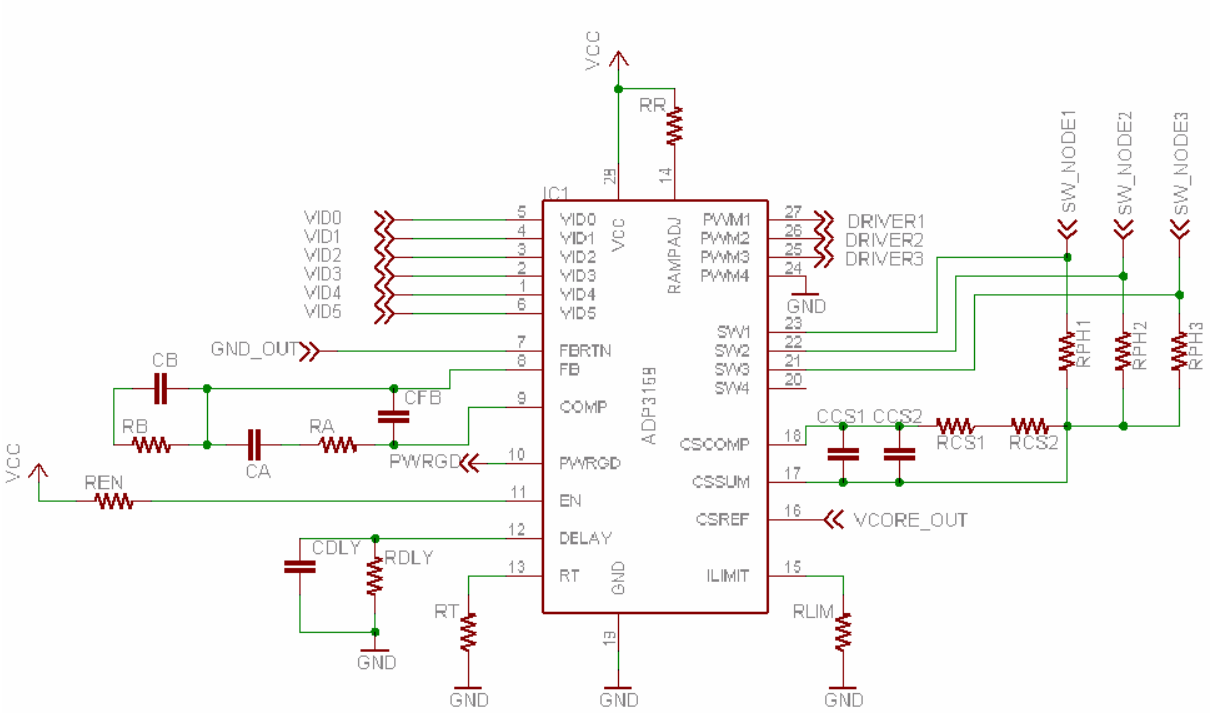


Figure 2.3 ADP3168 and external components

Author's design

The controller measures the total output current by summing together the phase currents. This is done by taking the voltage across each output inductor and passing the signal through a low-pass filter. This summer filter is the operational amplifier CSA configured with resistors $R_{PH(X)}$ (summers) tied to the non-inverting input (pin CSSUM), and R_{CS} and C_{CS} (filter) placed between the CSA output (pin CSSCOMP) and the non-inverting input.

$$R_{PH(X)} = \frac{R_L}{R_O} \times R_{CS} \qquad \text{Eq 2.3}$$

setting R_{CS} =100 kΩ and solving $R_{PH(X)}$ = 88,42kΩ (91kΩ standard value)

$$C_{CS} = \frac{L_{OUT}}{R_L \times R_{CS}} \qquad \text{Eq. 2.4}$$

and then solve for C_{CS} = 3,24nF (3,3nF standard value).

Intel's specification requires that at no load the nominal output voltage of the regulator be offset to a lower value (V_{ONL}) than the nominal voltage corresponding to the VID code. This can be accomplish setting the value of R_B

$$R_B = \frac{V_{VID} - V_{ONL}}{I_{FB}} \qquad \text{Eq. 2.5}$$

where I_{FB} = 15μA is the current flowing out of the pin FB. In this case, R_B = 1,33 kΩ (1,3 kΩ standard value).

To select the current limit set point is necessary to choose the value of R_{LIM} using the following expression

$$R_{LIM} = \frac{A_{LIM} \times V_{LIM}}{I_{LIM} \times R_O} \qquad \text{Eq. 2.6}$$

where V_{LIM} is a 3V source across R_{LIM} with a gain of 10,4mV/μA and replacing with these values, R_{LIM} = 109,5 kΩ (110kΩ).

The regulation voltage is compare with an internal ramp that can be set with R_R, to produce the PWM modulation.

$$R_R = \frac{A_R \times L}{3 \times A_D \times R_{DS} \times C_R} \qquad \text{Eq. 2.7}$$

where A_R = 0,2 is the internal ramp amplifier gain, A_D =5 is the current balancing amplifier gain, R_{DS} is the total low-side MOSFET ON resistance and C_R = 5 pF is the internal ramp capacitor value. The internal ramp amplitude can be calculated using

$$V_R = \frac{A_R \times (1-D) \times V_{VID}}{R_R \times C_R \times f_{SW}} \qquad \text{Eq. 2.8}$$

having as result V_R = 0,385V, where D is the duty cycle (V_{VID} / V_{IN}).

The compensation network of the ADP3168 is formed by the resistors R_A, R_B and the capacitors C_{FB}, C_A, C_B as a type three compensator on the voltage feedback, being adequate for the proper compensation of the output filter. Following the expressions given by the fabricant for an optimal voltage positioning, it is necessary to compute the time constants for all the poles and zeros of the system:

$$R_E = n \times R_O + A_D \times R_{DS} + \frac{R_L \times V_{RT}}{V_{VID}} + \frac{2 \times L \times (1 - n \times D) \times V_{RT}}{n \times C_X \times R_O \times V_{VID}} \qquad \text{Eq. 2.9}$$

$$T_A = C_X \times (R_O - R') + \frac{L_X}{R_O} \times \frac{R_O - R'}{R_X} \qquad \text{Eq. 2.10}$$

$$T_B = (R_X + R' - R_O) \times C_X \qquad \text{Eq. 2.11}$$

$$T_C = \frac{V_{RT} \times (L - \frac{A_D \times R_{DS}}{2 \times f_{SW}})}{V_{VID} \times R_E} \qquad \text{Eq. 2.12}$$

$$T_D = \frac{C_X \times C_Z \times R_O{}^2}{C_X \times (R_O - R') + C_Z \times R_O} \qquad \text{Eq. 2.13}$$

where R'= 0,6 mΩ aprox. is the PCB resistance from the bulk capacitors to the ceramic (in a 4-layer board), R_{DS} is the total low side MOSFET ON resistance per phase, A_D = 5 is the current balancing amplifier gain, L_X is the total ESL of the bulk output capacitors and V_{RT} is the ramp amplitude on the COMP pin added to the internal ramp, which can be calculated using

$$V_{RT} = \frac{V_R}{\left(1 - \frac{2 \times (1 - n \times D)}{n \times f_{SW} \times C_X \times R_O}\right)} \quad \text{Eq. 2.14}$$

getting as result in this case V_{RT} = 0,42V.

The results for the constant times are: R_E = 29,4mΩ, T_A = 14,32µs, T_B = 4,8µs, T_C = 6,48µs, T_D = 221,42ns and the compensation values can then be solved using the following equations:

$$C_A = \frac{n \times R_O \times T_A}{R_E \times R_B} \quad \text{Eq. 2.15}$$

$$R_A = \frac{T_C}{C_A} \quad \text{Eq. 2.16}$$

$$C_B = \frac{T_B}{R_B} \quad \text{Eq. 2.17}$$

$$C_{FB} = \frac{T_D}{R_A} \quad \text{Eq. 2.18}$$

having as results C_A = 2,6nF, R_A = 2,49kΩ (2,4 kΩ standard value), C_B = 3,6nF (3,9nF standard value), C_{FB} = 88,97 pF (82 pF standard value).

There are other less relevant components in the control stage. For information about selection of any other component of external controller circuitry, please check the Appendix B (ADP3168 datasheet).

2.3 Testability

The board includes a socket for a 478 pin microprocessor which VID output pins are tied to the controller trough jumpers, so that the output voltage could be set manually or the processor can request different output voltages during operation (on-the-fly). These jumpers (VID0-VID5) have also a connection to ground in order to change the output voltage of the converter manually.

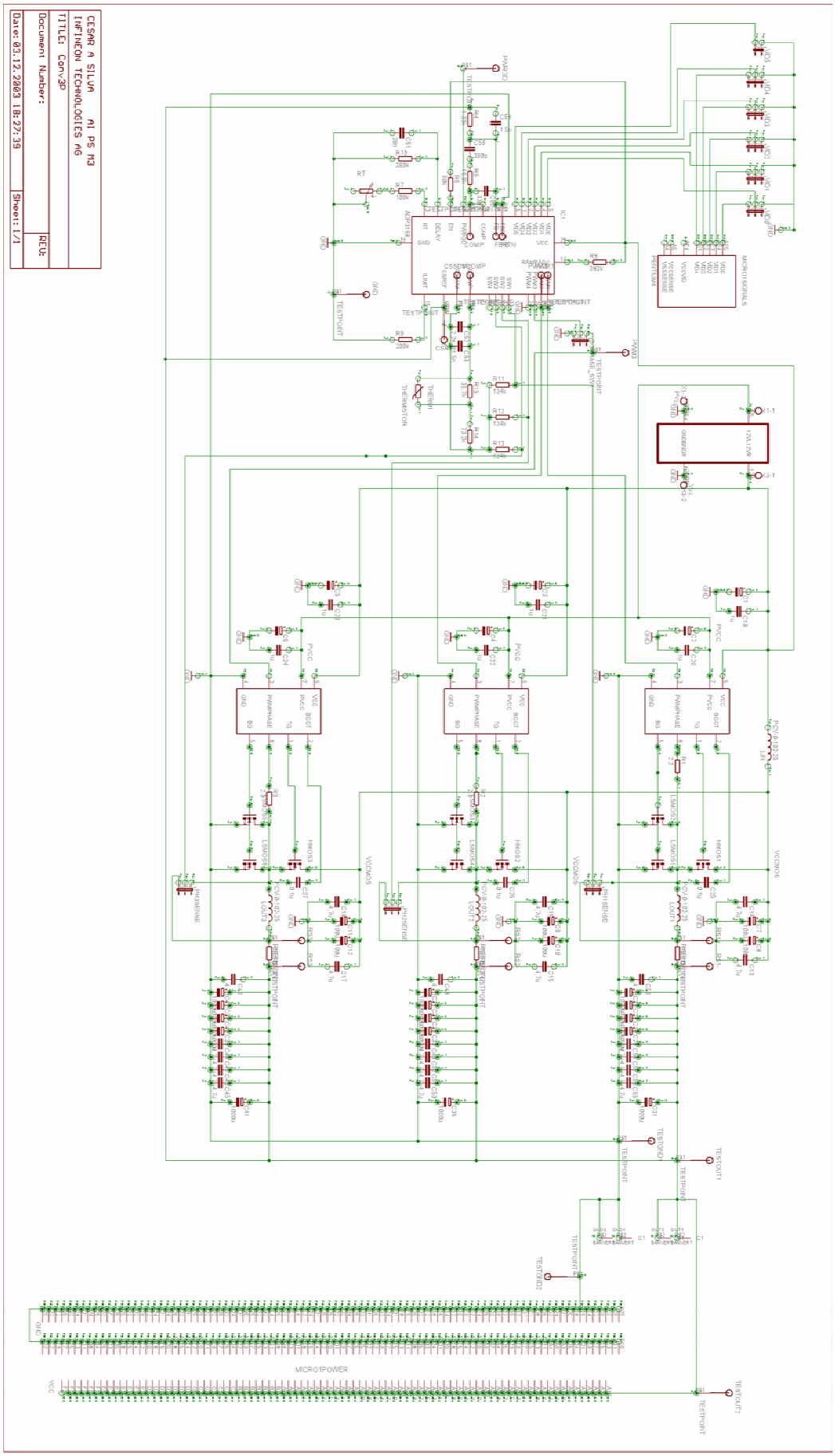
The operation frequency can be modified thanks to a 1MΩ potentiometer R_T starting from 100 KHz to 600 KHz per phase. Moreover, the number of phases can be modified changing the position of jumpers "2-3PHASE_SW1" and "PH3SENSE".
Several test points were introduced in the layout at the power stage and around the controller to have easy access to signals such as currents in each phase, CSCOMP, COMP, FB, etc.

The circuit can be connected to a "Silverbox" or a laboratory power supply using two different kinds of connectors at the input. An electronic DC load can be employed between the "Banvert" connectors and an AC load can be placed on the 478 pin socket. It was already mentioned that the sense resistors are for measuring the phase current only.

2.4 Bill of Materials

REFERENCE	DESCRIPTION	CASE/ FOOTPRINT	MANUF.	QTY.
X1,X3	Connector WAGO	W237-102	WAGO	2
SILVERBOX	4 pin Mini fit Jr.		Molex	1
C1,2	OSCON electrolytic capacitors 270µF, 16V	10 x 10.5	Sanyo	2
C7,8,9	OSCON electrolytic capacitors 100µF, 20V	10 x 10.5	Sanyo	3
C13-18,43-57	4.7µF Ceramic capacitor	1206	EPCOS	21
C19-24	1µF Ceramic capacitor	1210	EPCOS	6
C25-27	0.1µF Ceramic capacitor	0805	EPCOS	3
C30-37	Rubycon electrolytic capacitors 1000µF,16V	10 x 16	Rubycon	8
C58	3.9nF Ceramic capacitor	1206	S+M	1
C59	2.7nF Ceramic capacitor	0805	EPCOS	1
C60	82pF Ceramic capacitor	0805	S+M	1
C61	39nF Ceramic capacitor	1206	EPCOS	1
C62	1.5nF Ceramic capacitor	1206	EPCOS	1
HSMOS1,2,3	IPD09N03LA Power-MOSFET	P-TO252-3-1	Infineon Tech.	3
LSMOS1-6	IPD06N03LA Power-MOSFET	P-TO252-3-1	Infineon Tech.	6
D1-3	TDA21101 High Speed Driver	P-DSO-8	Infineon Tech.	3
Lin	1µH Inductor			1
Lout1-3	680nH Inductor	11 x 18		3
R1-3	2.2Ω SMD Resistor	2512	Any	3
R4	1.3kΩ Resistor 1%	1206	EPCOS	1
R5	2.4kΩ Resistor 1%	1206	EPCOS	1
R6	51kΩ Resistor 1%	1206	EPCOS	1
R7	100kΩ Resistor 1%	1206	EPCOS	1
R8	510kΩ Resistor 1%	1206	EPCOS	1
R9	110kΩ Resistor 1%	1206	EPCOS	1
R10	390kΩ Resistor 1%	1206	EPCOS	1
R11,12,13	180kΩ Resistor 1%	1206	EPCOS	3
R14	75kΩ Resistor 1%	1206	EPCOS	1
R15	36kΩ Resistor 1%	1206	EPCOS	1
RT	1MΩ SMD trimmer	3004W	Any	1
Rsense1-3	1mΩ Resistor 1% 2W	7520W	Cyntec	3
IC1	ADP3168 2-,3-,4-Phase Synchronous Buck Controller	TSSOP-28	Analog Devices	1
Out1,2,GND1,2	Banana connector			4
MICRO1	478pin PGA socket	PGA478		1
PH1-3SENSE VID0-5	3-way jumper 2mm	2mm spacing	Berg	9
TESTGND1,2 TESTOUT1,2 FBRTN, FB, PWRGD,RS1-3	Test points	P1-13	Williams Hughes	17

2.5 Schematic


CESAR A SILVA AI PS M3
INFINEON TECHNOLOGIES AG
TITLE: Conv3P
Document Number:
REV:
Date: 03.12.2003 18:27:39
Sheet: 1/1

2.6 Layout

The layout of the circuit was carried out in 4 layers with EAGLE® software. In the top layer (LT) are placed most of the tracks and signals from the controller to the different parts, the controller itself and the parts around the controller as they are SMD type. In the two inner layers, there is one for ground (LG) and one for 12V (LV). The bottom layer (LB) was used to route some other signals coming out and in the controller, and to reflect the signals from the top layer, improving the thermal dissipation in some key areas like the switching nodes and output voltage, and to limit DC losses in the high current paths. Pursuing this, some vias were placed all around the layout, in the switching nodes, besides the MOSFET's, sense resistors, in the output and input node, etc. The final layout and board are shown in Appendix C.

Chapter 3
CIRCUIT MODELING IN PSPICE

3.1 Purpose

The increasing computational power in the last decade has led into the development of simulation as a powerful tool in Engineering. In this particular case, simulation offers the possibility to make variations or add tolerances to the components easily, as well as to access more data than in the real circuit. All these features are useful for a better understanding of the application. The use of ideal and behavioral components has as final purpose, to have an more accurate and relatively fast simulation model.

Some of the functionalities of the real controller were omitted in the simulation because they are not relevant for the study of the PWM controller behavior, for instance the “Soft start”, “Current limit, short circuit and latch-off protection”, “Power good monitoring” and “Output enable” as described in the “theory of operation” section of the ADP3168 datasheet (see appendix B) are all protective or security functionalities which are not required when simulating the normal operation.

3.2 Power Stage Model

In the power stage, as already mentioned in the description of the board, there are input and output filters, MOSFET’s and drivers. The input and output filters are

represented in the simulation model by analog components “C” and “L” as well as some of the most important parasitic resistances of the real components like ESR in the case of capacitors and DCR in inductances, as shown in the figure 3.1.

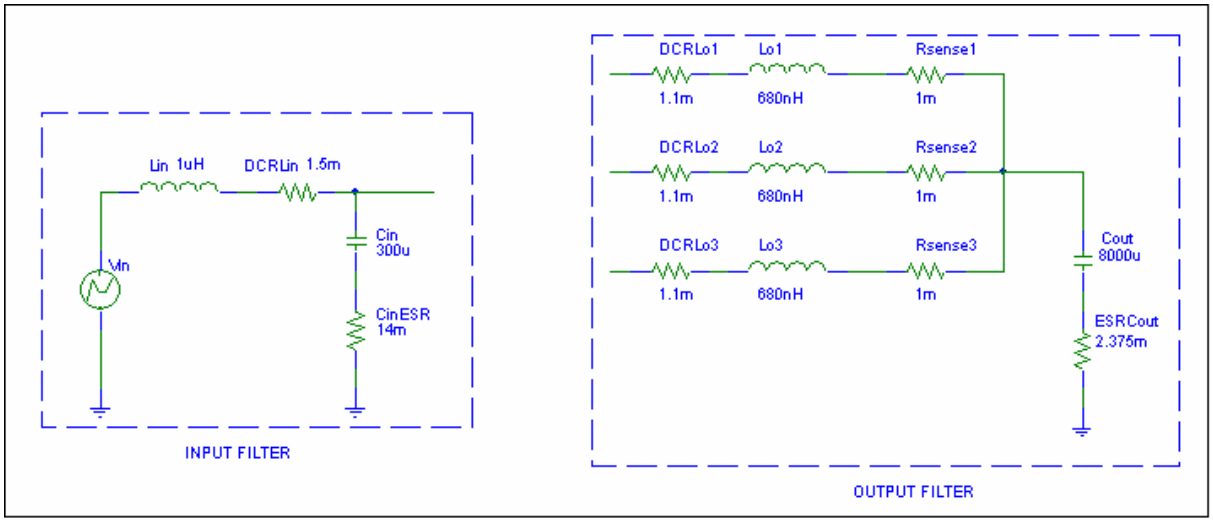


Figure 3.1 Models of Input and Output Filters

Author’s design

Although Infineon MOSFET’s and driver models for Pspice® are available, it would require a lot of processing time without adding useful information for the study of the control behavior. it would make the simulation impractical and much more complex since it would be necessary to add 9 transistors and 3 drivers. Instead of these, ideal components such as controlled voltage switches were placed, one for each High Side phase and one for each Low Side phase (see figure 3.2). The value of internal resistance of the switches is a changeable attribute in Pspice® called RON, therefore the values of the real MOSFET’s $R_{DS(ON)}$ can be introduced in the corresponding phase, for instance RON = $R_{DS(ON)}$ = 9mΩ in the High Side switches and RON = $R_{DS(ON)}$ = 3mΩ in the Low Side switches (2 MOSFETs with $R_{DS(ON)}$ = 6mΩ in parallel). These values were taken from the datasheets of the MOSFETs used on the board.

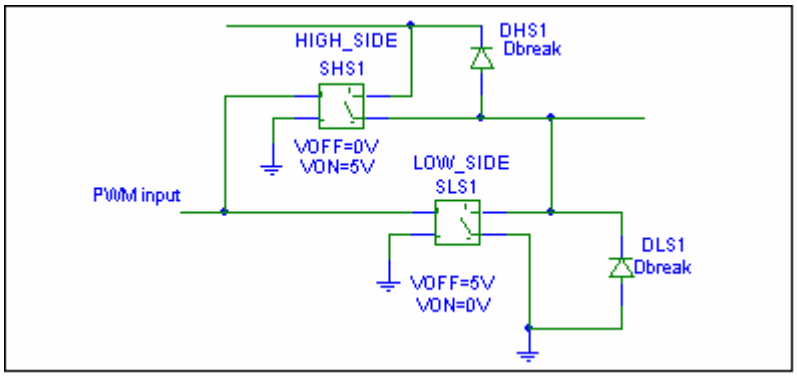


Figure 3.2 High Side and Low Side Switches

Author's design

The driver was omitted because the switches can be controlled by the same PWM signal coming out of the controller directly. It is necessary just to invert the voltage values of VON and VOFF. Diodes "Dbreak" were placed in parallel to the switches in order to allow reverse currents to flow during the OFF time of the switches, replacing the intrinsic body diode of the MOSFETs.

3.3 Control Stage Model

The models of the controller (see figure 3.3) and the control stage were developed based on the block description, "theory of operation" and "Application information" sections of the ADP3168 datasheet.

Firstly, the voltage mode control loop was analyzed and modeled by two ideal operational amplifiers, or "OPAMP": the Current Sense Amplifier (CSA) and the Internal Error Amplifier (IEA).

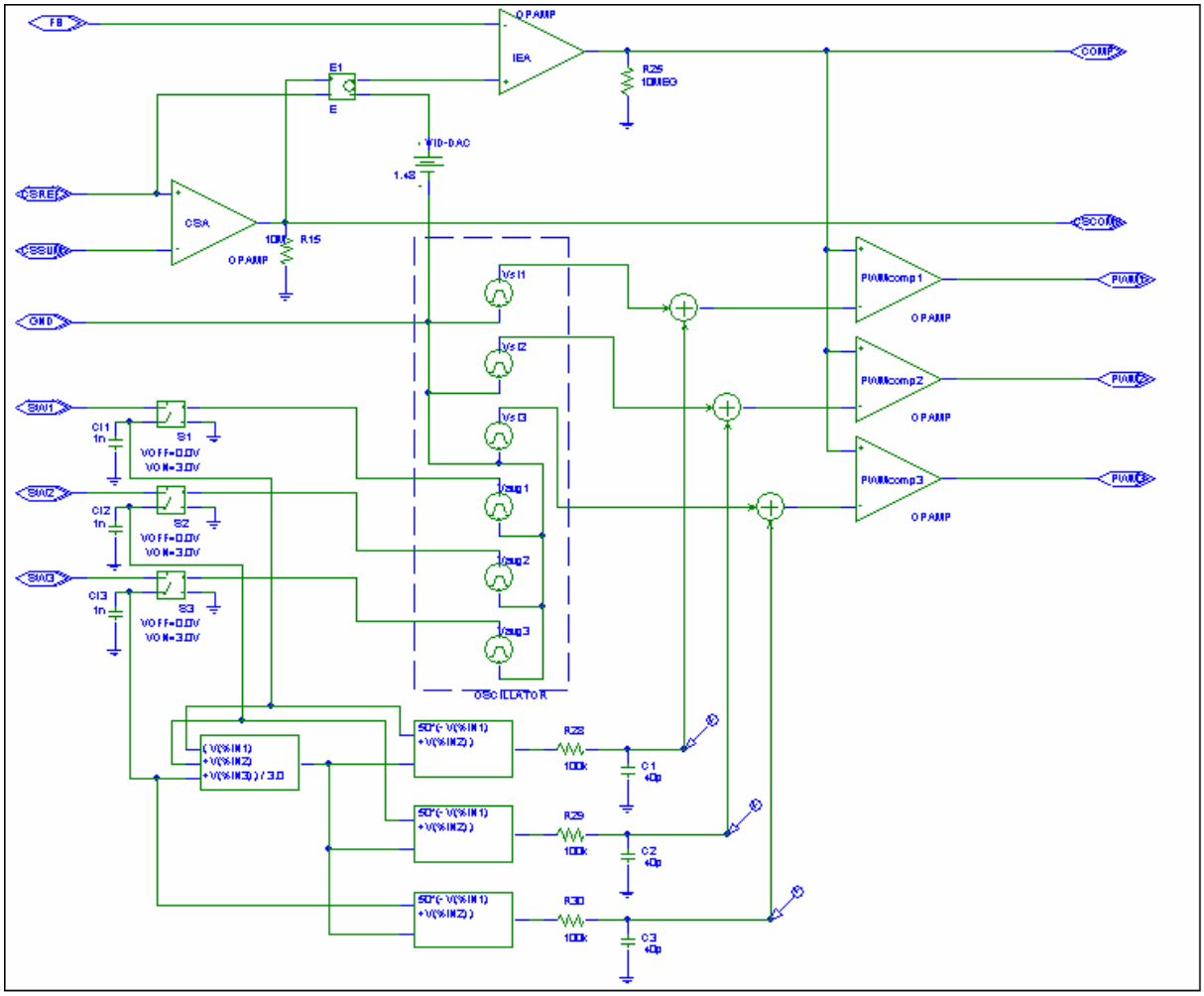


Figure 3.3 Controller simulation model

Author's design

3.3.1 Dynamic Droop (Output Load Line)

The CSA has its inverting input tied to the CSSUM pin, the non-inverting tied to the CSREF pin, and the output to the CSCOMP pin. This operational amplifier is in charge of calculating the dynamic output voltage droop. It sums the phase currents giving as result a voltage proportional (*Vdroop*) to the total output current at CSCOMP pin. This voltage represents the load line of the output voltage, since:

$$Vo = VIDsetting - nlo - Vdroop \quad \textbf{Eq 3.1}$$

where *nlo* : No-load offset, in this case *nlo* = 20 mV.

From Eq. 3.1 it is clear that the output voltage is a function of the output current,

$$Vo = f(Io) \quad \textbf{Eq 3.2}$$

The resistors R_{PH1}, R_{PH2}, $R_{PH3,}$ R_{CS} and the capacitor C_{CS}, which are tied to the input and output pins of the CSA, were replaced simply by "R" and "C" components. The simulation attributes of the CSA are: VNEG= 0, VPOS= 3.3, following the specifications given on the ADP 3168 datasheet (Output voltage Range: Min 0.05 V; Max 3.3 V) and GAIN= 1E3 which represents a typical value for an operational amplifier implemented on an integrated circuit.

3.3.2 Voltage Mode Control

The Internal Error Amplifier has only its inverting input and output connected to the FB and COMP pins respectively. The compensation network is between these two pins and it is formed by RA, CA, RB, CB, CFB, also represented by "C" and "R" with same values to the real components. Simulation attributes of the IEA are VNEG= 0, VPOS= 3.5V due to the values found on the specification (Output voltage Range: Min 0.5 V; Max 3.5 V) for the ADP3168. The non-inverting input of the IEA is connected to a Voltage controlled Voltage Source "E" (E1), with an internal gain of 1. This voltage source is reducing the reference voltage, which is set through an ideal DC voltage source (VDC in Pspice) called VID-DAC because it replaces the Digital-Analog converter that changes the VID code into an analog voltage in the real integrated circuit.

Finally, the PWM signals are generated thanks to the comparison between the compensation voltage (output IEA) and a saw-tooth signal coming from the "oscillator". Depending on the number of phases, the oscillator shifts the saw-tooth signals by 360°/m, where m is the number of phases. In this case, the oscillator

functions are carried out by ideal "VPULSE" Voltage sources (Vst1-Vst3) which are programmed to have the required time shift.

The models of the controller (see figure 3.3) and the control stage were developed based on the block description, "theory of operation" and "Application information" sections of the ADP3168 datasheet. Firstly, the voltage mode control loop was analyzed and modeled by two ideal operational amplifiers, or "OPAMP": the Current Sense Amplifier (CSA) and the Internal Error Amplifier (IEA).
here is one ideal "OPAMP" per phase, working as comparator. The attributes of these "PWMcompX" are: VNEG= 0 V, VPOS= 5 V; due to the voltage range of the PWM signals going out of the real controller; GAIN = 1E6 in order to minimize the falling and rising time in the simulation.

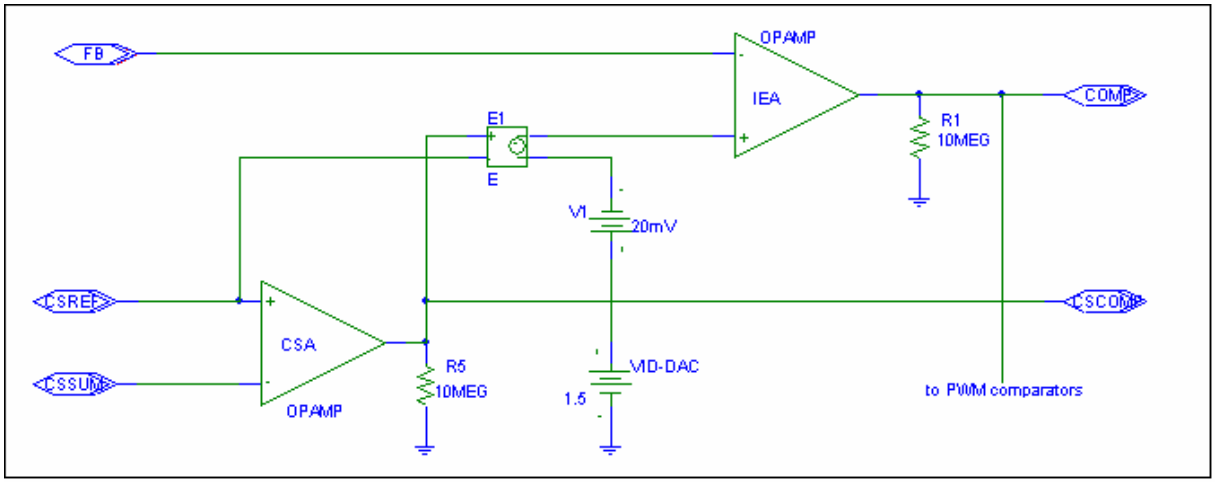


Figure 3.4 Voltage control mode Components.

Author's design

3.3.3 Balancing Circuit

The model for the "Current Balancing circuit" of the ADP3168 was developed using analog components "R" and "C" and "behavioral" (.abm) blocks as follows: the current in each phase is sensed by looking at the $R_{DS(ON)}$ voltage in each low side

MOSFET. This information is stored periodically through a “sample and hold” circuit per phase, here implemented by a Pulse Voltage Source “VPULSE” (VavgX) which drives a switch “S” connected between the “SWx” pin of the controller and a capacitor. Each Switching node is tied to one of the “SWx” inputs,

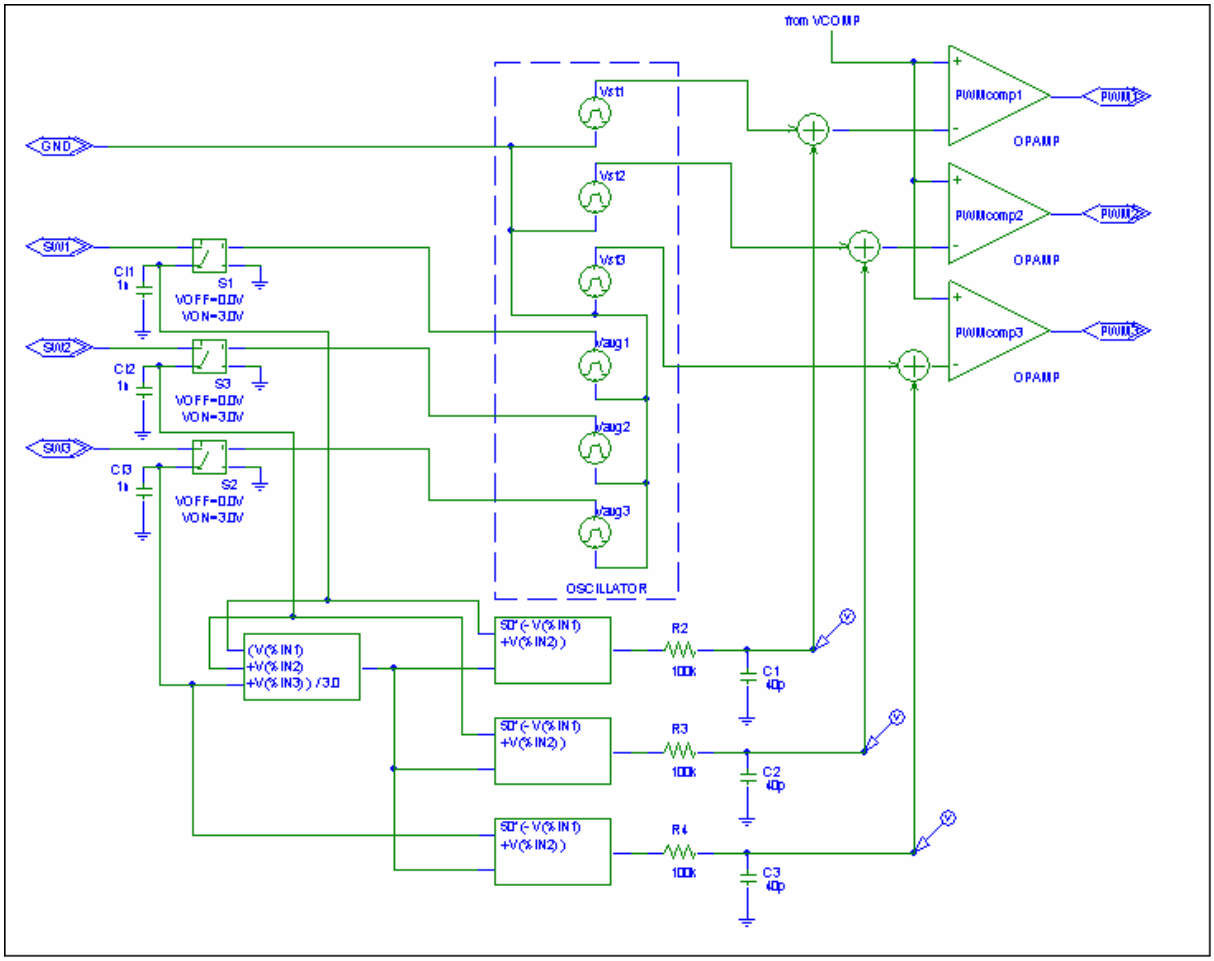


Figure 3.5 Current Balancing Circuit components

Author’s design

Afterwards, the values of the current phases (voltage in the capacitors) are summed together and divided by the number of phases to calculate an average current per phase, used to obtain the current error signal making the difference between average current and the current in each phase. An RC net filters this information to obtain a smooth value of voltage, used to change the width of the PWM pulse in the

corresponding phase. The correction is made by the addition of this voltage to the ramp of each phase, forcing the current error signal toward zero. Current Balancing loop is presented in figure 3.5

3.4 Converter Model

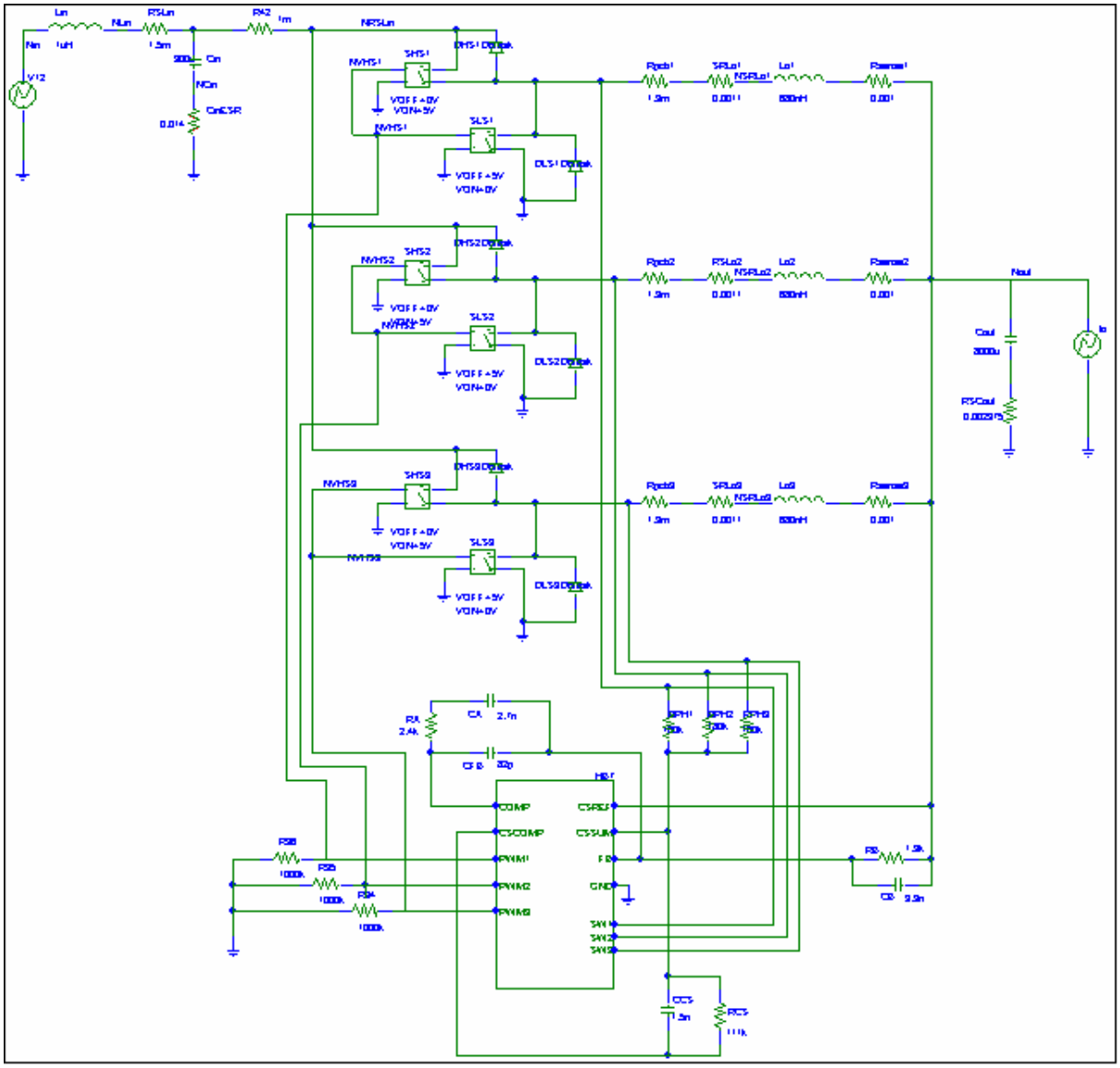


Figure 3.6 Global model

Author's design

The whole model, presented in figure 3.6, is formed by the power stage, control stage, an ideal voltage source “VPWL” as input voltage source and a Load represented by an ideal “IPWL” current source. In the final Schematic, the controller is represented by only one block with its respective pins connected to other parts in the circuit and linked to the schematic of the controller in a lower level. Some resistors were added in order to facilitate the bias point calculation and to reduce the probability of non-convergence errors, for ex: R34= R35= R36= 1 MΩ; R42= 1mΩ; and R25= R15= 10MΩ.

Simulations were done as similar as possible to measurements. Although Pspice® presents some limitations when simulating fast current and voltage changes which are usual in power electronics, most of these problems can be solved changing some simulation parameters. In this case, the parameters that differ from the default values are (default values are in
parenthesis):

ABSTOL = 1000pA (1pA)
CHGTOL = 0,1pC (0,01pC)
ITL4 = 100 (10)
RELTOL = 0,01 (0,001)

Chapter 4
MEASUREMENTS vs. SIMULATION

There are 2 types of measurements that can be performed: DC measurements, which mean no changes in the load while taking the measurement; and AC measurements, which mean transient response of the circuit when having current load steps.

It is necessary to have adequate equipment to carry out the measurements: a DC load, Oscilloscope, probes, voltage source and multimeters for DC measurements. And additional Voltage Transient Test (VTT) Tool is required in order to perform AC measurements.

4.1. DC Behavior

4.1.1. Output voltage load line:

As already mentioned in chapter 2 and 3, the output voltage of the DC/DC converter has a droop or load line. For each value in the output current there is a corresponding output voltage, representing an output resistance that can be theoretically calculated as:

$$R_O = \frac{V_{ONL} - V_{OFL}}{I_O} \qquad \textbf{Eq 4.1}$$

And using the values of Chapter 2 R_O = 2.375 mΩ.

In this measurement, the electronic load was connected to the output of the circuit; the VID code was set to 101110 (VID5-VID0) representing 1.5V output voltage. Two multimeters, in the output and input voltages, were used. Output current was increased in steps of 10A. The configuration is represented in figure 4.1 and the results are show in table 4.1 and figure 4.2. "Board" trace.

Io (A)	0	10	20	30	40	50
Vout (V)	1,4743	1,4526	1,4317	1,41	1,3881	1,366

Table 4.1 Output Voltage (Board) vs. Output current

Several simulations, with different output currents, show the behavior of the dynamic output voltage before any change was done to the circuit. Simulation results are shown in table 4.2 and figure 4.2 as "No Rth".

Io (A)	0	10	20	30	40	50
Vout (V)	1,48	1,463	1,45	1,436	1,417	1,408

Table 4.2 Output load line (simulation without matching)

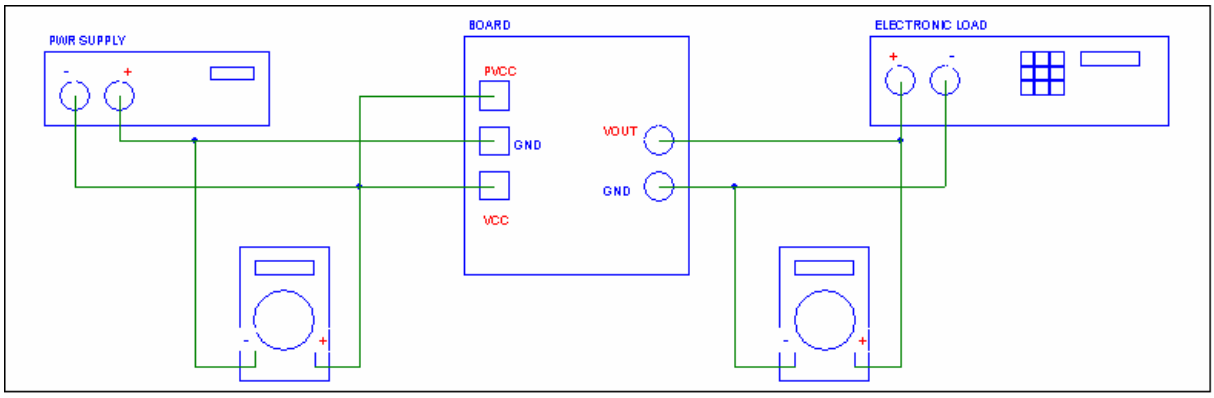


Figure 4.1 Measure Elements in DC

Author's design

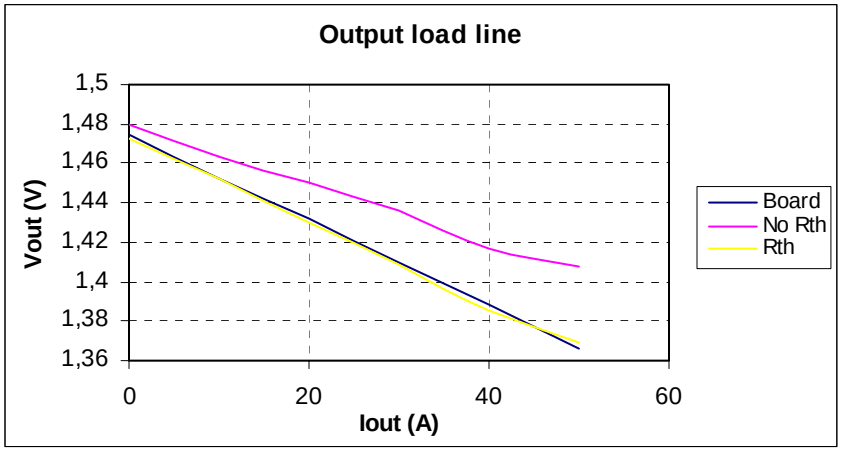


Figure 4.2 Output voltage loadline

Author's design

As it is possible to observe when comparing the traces "Board" and "No Rth" in figure 4.2, there is a higher slope in the output voltage load line of the measurements than in the simulation results that could be due to a wrong value of the voltage controlled voltage source "E1" or to a mismatch in the sense element. In this case, the resistance DCR of output inductors are been used as sense elements in order to have a voltage proportional to the output current, and since the measurements were taken "in hot"* it is possible to conclude that due to the positive temperature coefficient on of copper (TC) of 39%/°C and, therefore a higher DCR, the real controller supposes that the phase current flowing is higher. In order to have the same behavior in the simulation model, it is necessary to calculate the additional resistance to be added in series to the DCR in the simulation model. After comparing between the input and output voltages of the CSA it is possible to calculate the error in the closed loop Gain of the CSA and consenquently the additional resistance, for instance:

Experimental (I out = 50A):

VCSCOMP = 1,225V; VCSREF = 1,35V; difference V(CSREF-CSCOMP) = 0,125V.

Vout = 1,366V. Gain CSA (meausured) = 0,001874 (Close loop).

Simulation Pspice® (Iout = 50A):

* The circuit is ON approx. 10 minutes before measuring.

VCSCOMP = 1,3123V; VCSREF = 1,372V; difference V(CSREF-CSCOMP) = 0,0597V.

Vout = 1,372V. Gain CSA (simulation) = 0,001166 (Close loop).

factor Gain CSA Measured/simulation = 1,6072

new DCR = old DCR * factor Gain = 3,4 mΩ.

Then, the resistor to be added has a value of 1,3mΩ. After adding this resistor under the name of Rth the load line was very similar to the experimental one, as it is possible to observe in figure 4.2 when comparing "Rth" and "Board" traces.

4.1.2. Output voltage vs. Input voltage

The controller should grant independence between the output and input voltage. Here, the input voltage was changed in steps of 0.25V, from 11V to 13V at different load currents, from 0A to 50A in steps of 10A. The implementation in figure 4.1 is used here, but changing the input voltage. It is important to mention that this measurement were carried out "in hot" and the VID code was set to 1,55V output voltage. The results are shown in table 4.3 and figure 4.3.

Vin (V)	Io (A)	0	10	20	30	40	50
11	Vo(V)	1,5238	1,5025	1,4807	1,4595	1,437	1,4142
11,25		1,5237	1,5024	1,4807	1,4596	1,4371	1,4144
11,5		1,5236	1,5022	1,4807	1,4597	1,4372	1,4146
11,75		1,5234	1,5022	1,4806	1,4598	1,4372	1,4146
12		1,5233	1,5018	1,4805	1,4598	1,4372	1,4147
12,25		1,5233	1,5018	1,4802	1,4597	1,4372	1,4139
12,5		1,5233	1,5015	1,4798	1,4595	1,436	1,4121
12,75		1,5233	1,5012	1,4794	1,4586	1,4341	1,4107
13		1,5231	1,501	1,4791	1,4576	1,4326	1,4098

Table 4.3 Output Voltage vs. Input Voltage

Several simulations, with different output currents, show the behavior of the dynamic output voltage without any change to the circuit. Simulation results are shown in table 4.3.

In these simulations, the results (see table 4.4) are similar to those obtained in the experimental measurements; therefore, no changes are necessary regarding this characteristic.

Vin (V)	Io (A)	0	10	20	30	40	50
11	Vo(V)	1,523	1,502	1,481	1,459	1,438	1,417
11,5		1,524	1,504	1,481	1,46	1,438	1,417
12		1,523	1,503	1,482	1,46	1,438	1,416
12,5		1,523	1,503	1,482	1,461	1,439	1,417
13		1,524	1,504	1,483	1,462	1,44	1,418

Table 4.4 Output voltage vs. Input voltage (simulation)

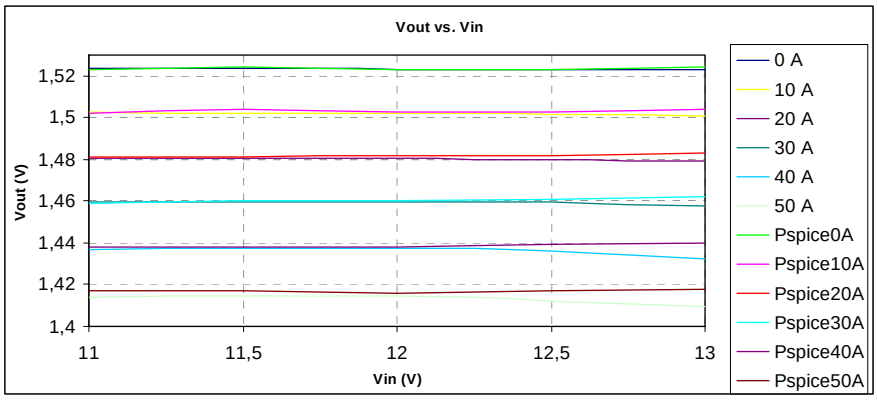


Figure 4.3 Output voltage vs. Input voltage

Author's design

4.1.3. Current Sharing

The current per phase can be measured thanks to the Current sense resistors. Since the voltage on the sense resistors is proportional to the phase current and then, to the output current, it is better to perform measurements with high values of output current

for accuracy. For instance, if we assumed that the phases share the output current uniformly, with a I_O = 15A, the phase current would be I_{phase} = 5A and the differential voltage on the sense resistors V_{avg} = 5mV. Moreover, this voltage is not referenced to ground, thus it could be relatively difficult to have accurate measure when the current flowing through the phases is not higher than 10A per phase.

The measurements of phase current were performed with a differential probe and a differential amplifier in order to have data as accurate as possible. In figure 4.4 is represented the Sharing percentage of each phase versus the output currents. This was calculated adding the mean values of the voltage measured at the Sense resistors and taking this as 100% which could represent the output current, assuming that the current ripple is negligible.

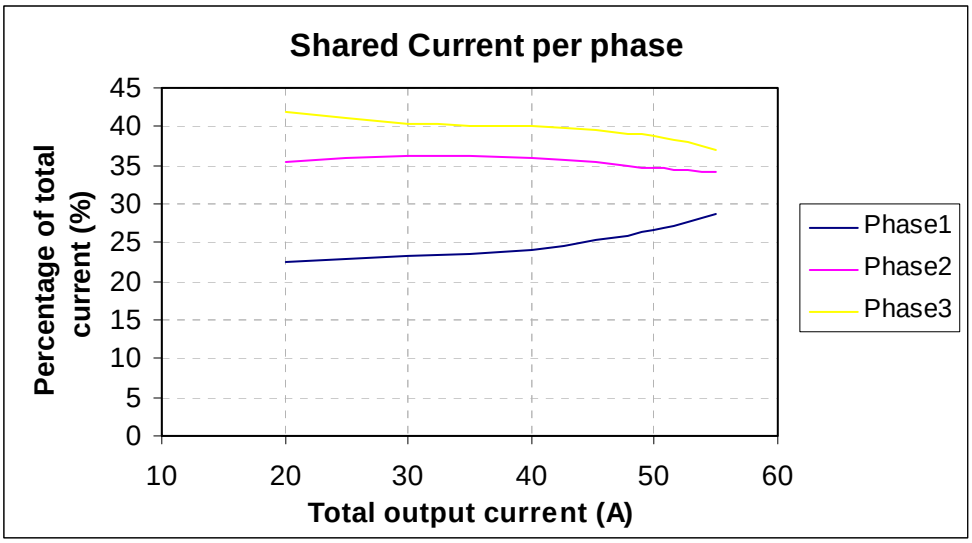


Figure 4.4 Current per phase percentage of the total output current

Author's design

From the graphic it is possible to conclude that the phases 2 and 3 are carrying most of the total output current and through phase 1 flows fewer current. The model should also show this behavior. This can be achieve by placing an additional resistance in series with the $R_{DS(ON)}$ of the low side MOSFETs in phase 1 and phase 2, where the current balancing circuit senses the voltage that represents the current per phase. The

additional resistance necessary to adjust the model was calculated taking the percentages of mismatch multiplied by the total $R_{DS(ON)}$ of the Low Side (3mΩ). The values found here are:

New $R_{DS(ON)}$ phase1 = 4,19mΩ.

New $R_{DS(ON)}$ phase2 = 3,29mΩ.

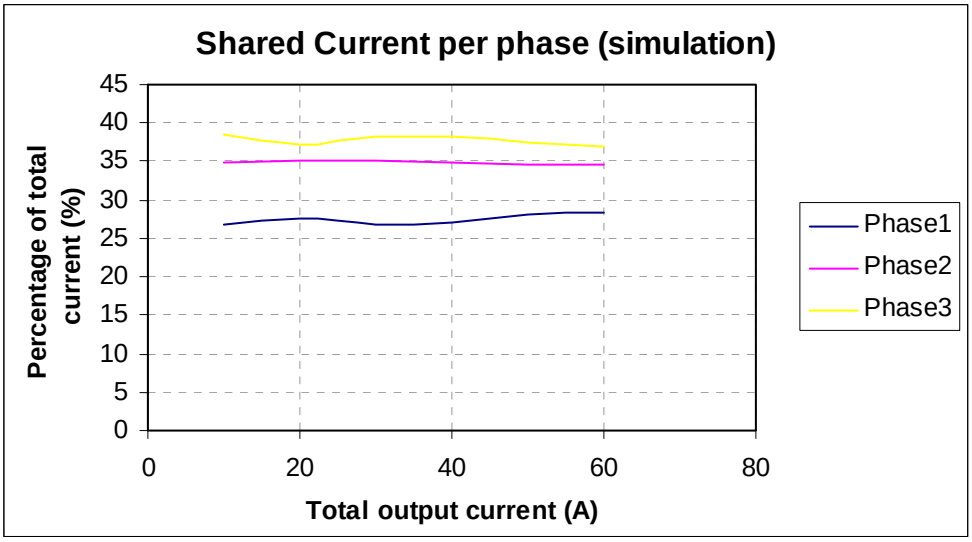


Figure 4.5 Current per phase percentage of the total output current (simulated)

Author's design

Simulation results are represented in figure 4.5. The percentages of current shared are close to the mean of the values in figure 4.4. It is not possible to have a similar behavior in the currents. Before any change in the simulation model the output current was shared uniformly in the phases.

Looking at the layout of the board, it is possible to find the reason of the unbalancing between the phase currents. The element use to get a current phase proportional value is the $R_{DS(ON)}$ of the Low Side MOSFETs. As it is visible on the top layer of the board, in Appendix C, there are tracks coming from each switching node to the controller. In phases 2 and 3, these tracks are tied almost at the same point to the switching nodes, but in phase 1 the copper area between low side MOSFETs drains and the track, is longer than in the other two phases, increasing the resistance used to sense the current flowing on this phase. Although, the differences in the layout are small (mm), there

are great disparities in the phase currents due to the small values of $R_{DS(ON)}$ = 3 mΩ. For instance, an additional 1mΩ resistance in the copper would cause an approx. 30% mismatch in the phase current.

4.2 AC Behavior

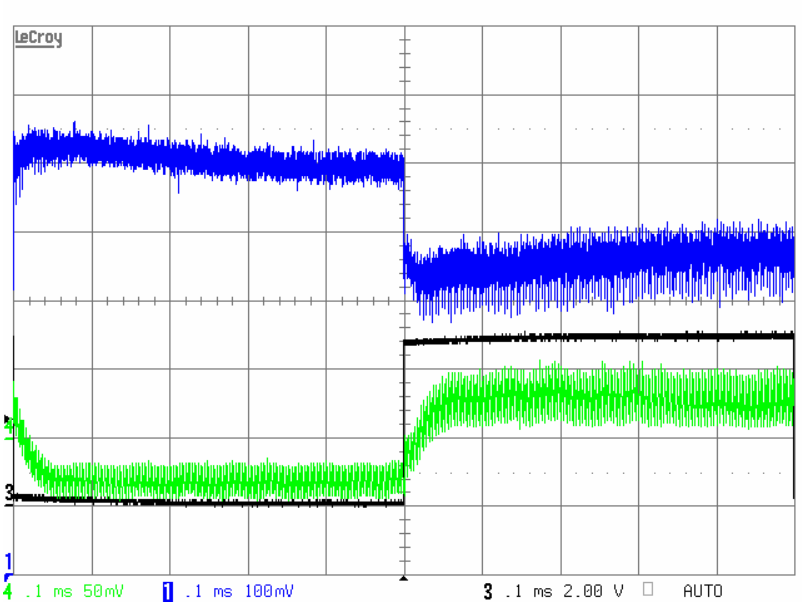


Figure 4.6 Load step current measured. Output voltage (blue); Phase Current (green). *dI/dt* =50A/μs

Some experimental and simulation waveforms are presented in this section, at different rations of load step (*dI/dt*), where I_{min} = 10A and I_{max} = 60A. These measurements were performed thanks to a Voltage Transient Test (VTT) Tool. A differential amplifier and probe were connected to the sense resistor in phase 2 and a normal probe was connected to the output voltage. The comparison is centered on the Output Voltage and Phase Current. The load determines the output current waveform.

From figures 4.6 is visible that the Experimental Output voltage accomplishes the load line after a load step. The Output voltage (in blue) changes about ΔVo = 120 mV,

for load step of ΔIo = 50A, which gives a load line of R_O = 2,4 mΩ, which is close to 2,375 mΩ. In figure 4.7 are shown the results of simulation and calculating the load line: ΔVo = 110 mV, and R_O = 2,2 mΩ. Similar results are obtained for different *dI/dt* as shown in figures 4.8-4.11 for Output Voltages.

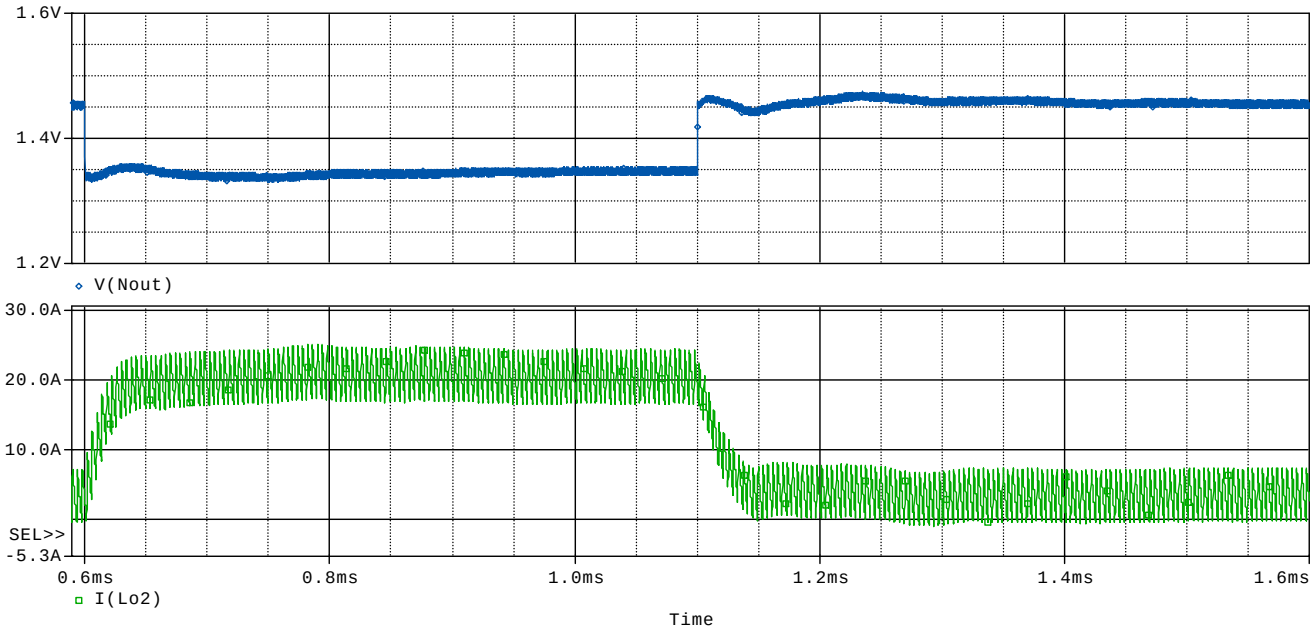


Figure 4.7 Load step current (simulation). Output voltage (blue). Phase Current (green). *dI/dt* = 50A/µs

Phase Current represented on figure 4.10 shows a rising time of 25 µs. And for the simulation in figure 4.11 this time is 30 µs. This comparison shows that the simulation results are not accurate on the worst case (*dI/dt* = 400 A/µs). Unfortunately, comparisons in the transient response parameter like rising time and Overshoot, changes in the simulation model without finding any better performance. For such a purpose, a deeper description level, like transistor level or transfer function level, in order to match experimental and simulation results is recommended. Ideal components are not very useful for such a task.

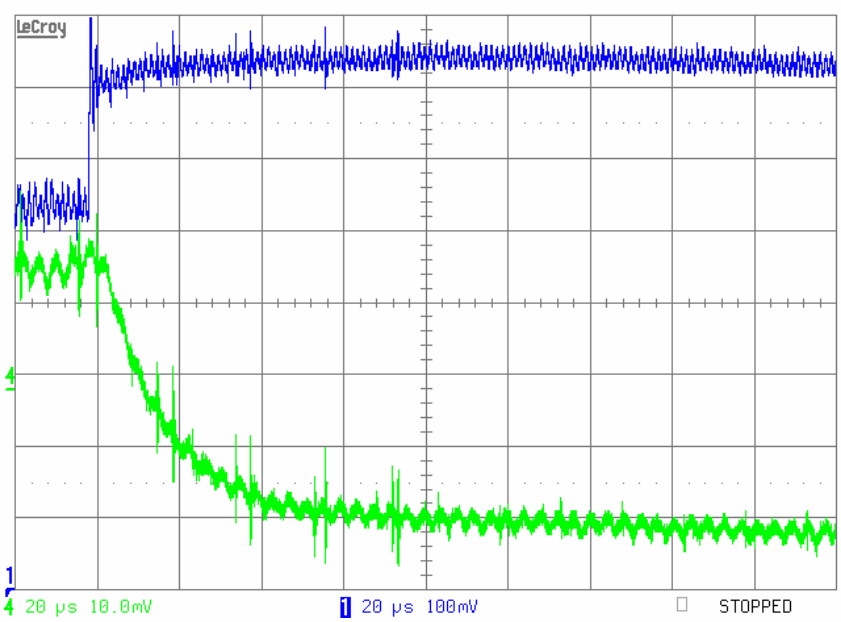


Figure 4.8 Load step current measured. Output voltage (blue); Phase Current (green). *dI/dt* = 100A/µs

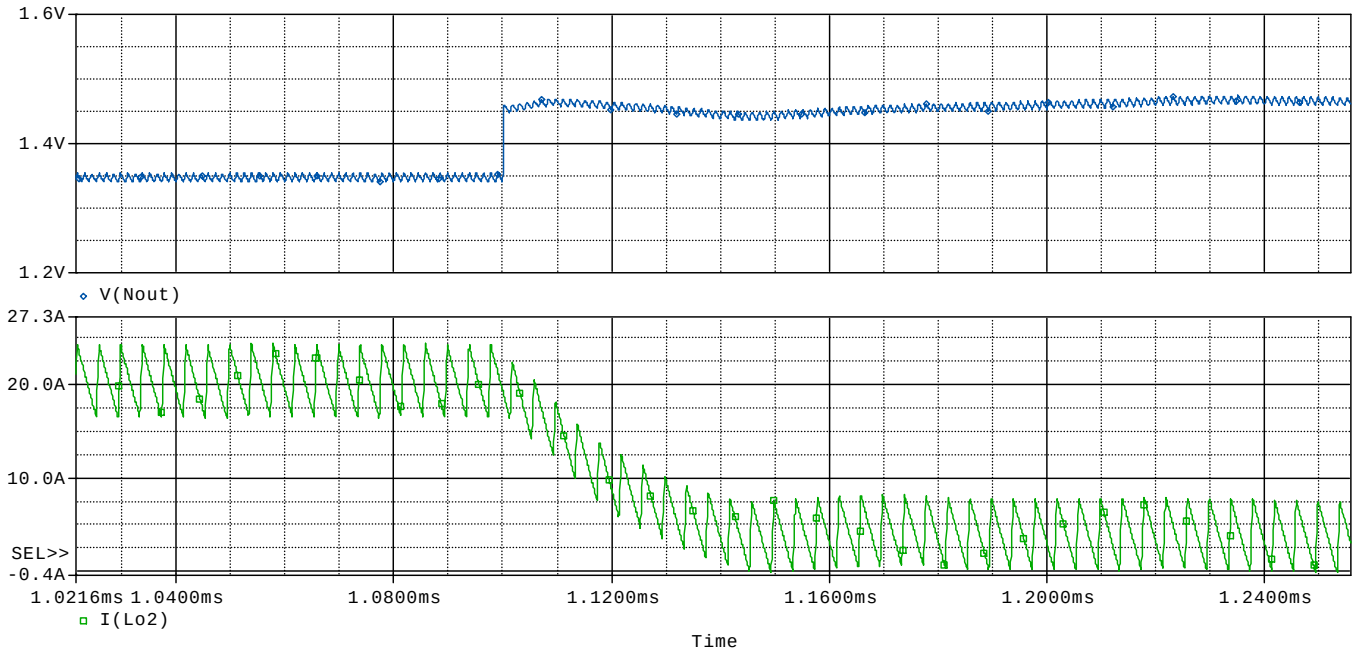


Figure 4.9 Load step current (simulation). Output voltage (blue). Phase Current (green). *dI/dt* = 50A/µs

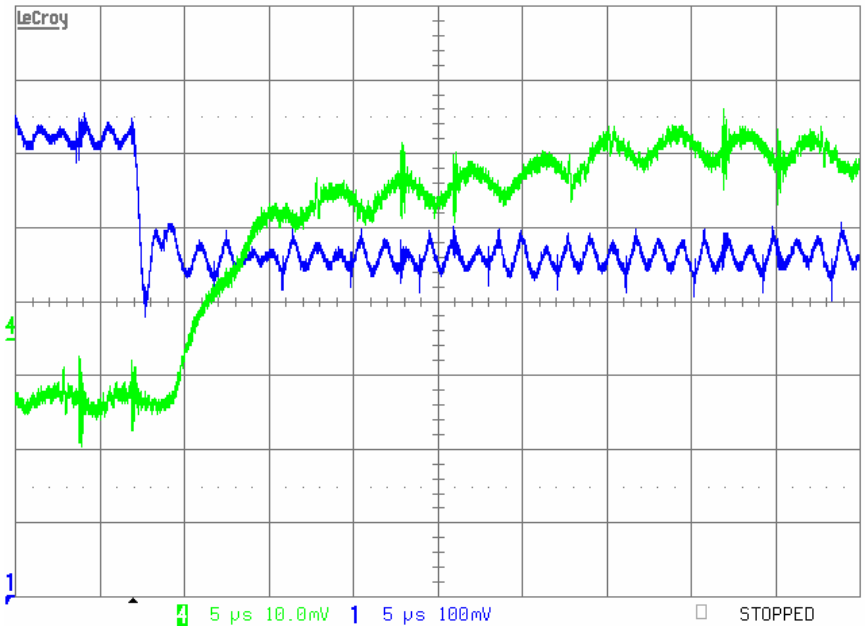


Figure 4.10 Load step current measured. Output voltage (blue); Phase Current (green). *dI/dt* = 400A/µs

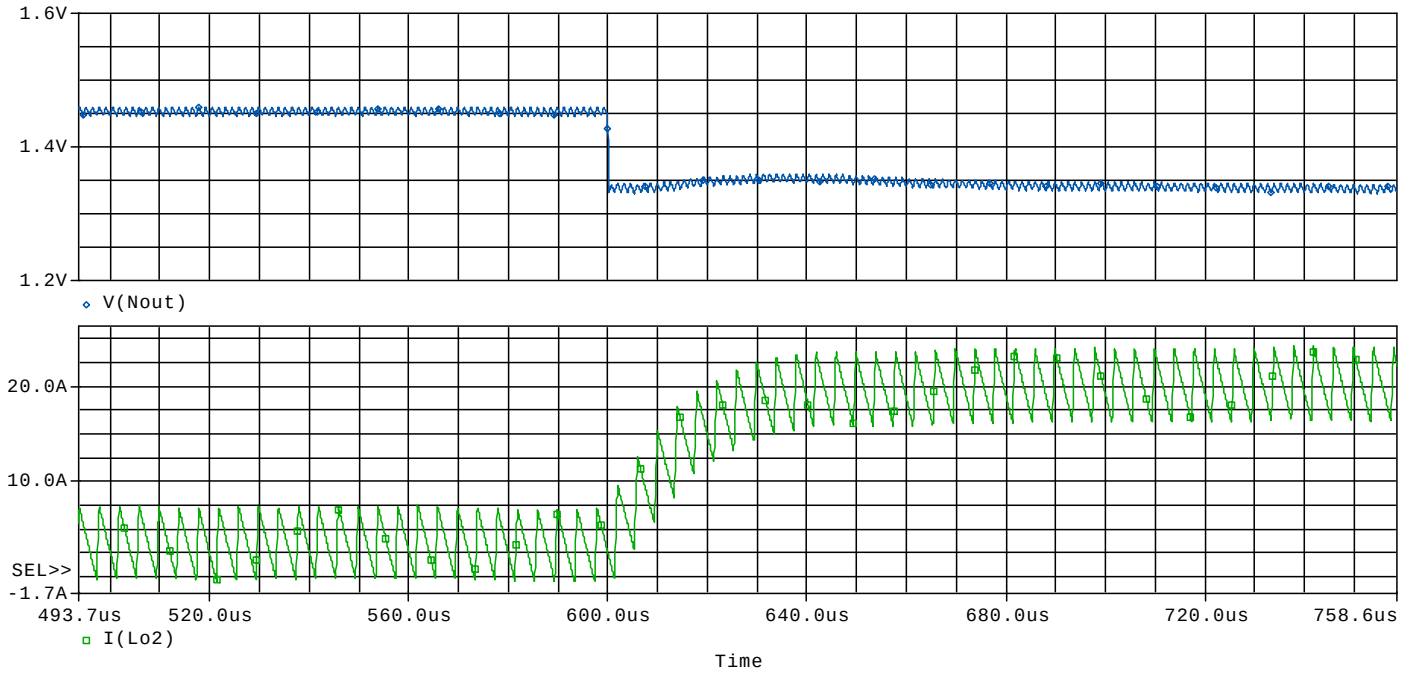


Figure 4.11 Load step current (simulation). Output voltage (blue). Phase Current (green). *dI/dt* = 400A/µs

Chapter 5
CONCLUSIONS

- It is possible to analyze the converter DC behavior using the simulation model developed, since they have similar performances confirmed by the comparison already done.

- Since there are not details about the internal circuitry of the controller, signals like the error voltage on the compensation pin and internal ramp are different in the model. Nevertheless, simulation results are similar to experimental results on the main areas like output voltage load line, output voltages and current sharing.

- A good layout (same in all phases and sense tracks close to sense components) is fundamental for carrying out some controller functionalities like good current sharing in the phases which also leads to a good thermal behaviour

- In spite of the Pspice® limitations, with appropriate adjustments in parameters, it is suitable for simulating low voltage power electronics systems like the multiphase Buck Converter.

Appendix A

Optimos® 2

OptiMOS®2 Power-Transistor

Feature

- Ideal for high-frequency dc/dc converters
- n-Channel
- Logic Level
- Excellent Gate Charge x $R_{DS(on)}$ product (FOM)
- Low On-Resistance $R_{DS(on)}$
- Superior thermal resistance
- 175°C operating temperature
- d*v*/d*t* rated

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Max Continuous Drain Current	I_D		50		A
Gate-Source Voltage					
Operation Temperature	T		-55…+175		°C
Threshold Voltage	$V_{GS(th)}$	1.2	1.6	2	V
Gate Resistance	R_G	-	1	-	Ω
Input Capacitance	C_{iss}	-	1283	1706	pF
Output Capacitance	C_{oss}	-	586	713	pF
Gate Charge Total	Q_G	-	11.3	15	nC
Inverse Diode Forward Voltage	V_{SD}	-	1	1.3	V

For further information please check the datasheet at www.infineon.com

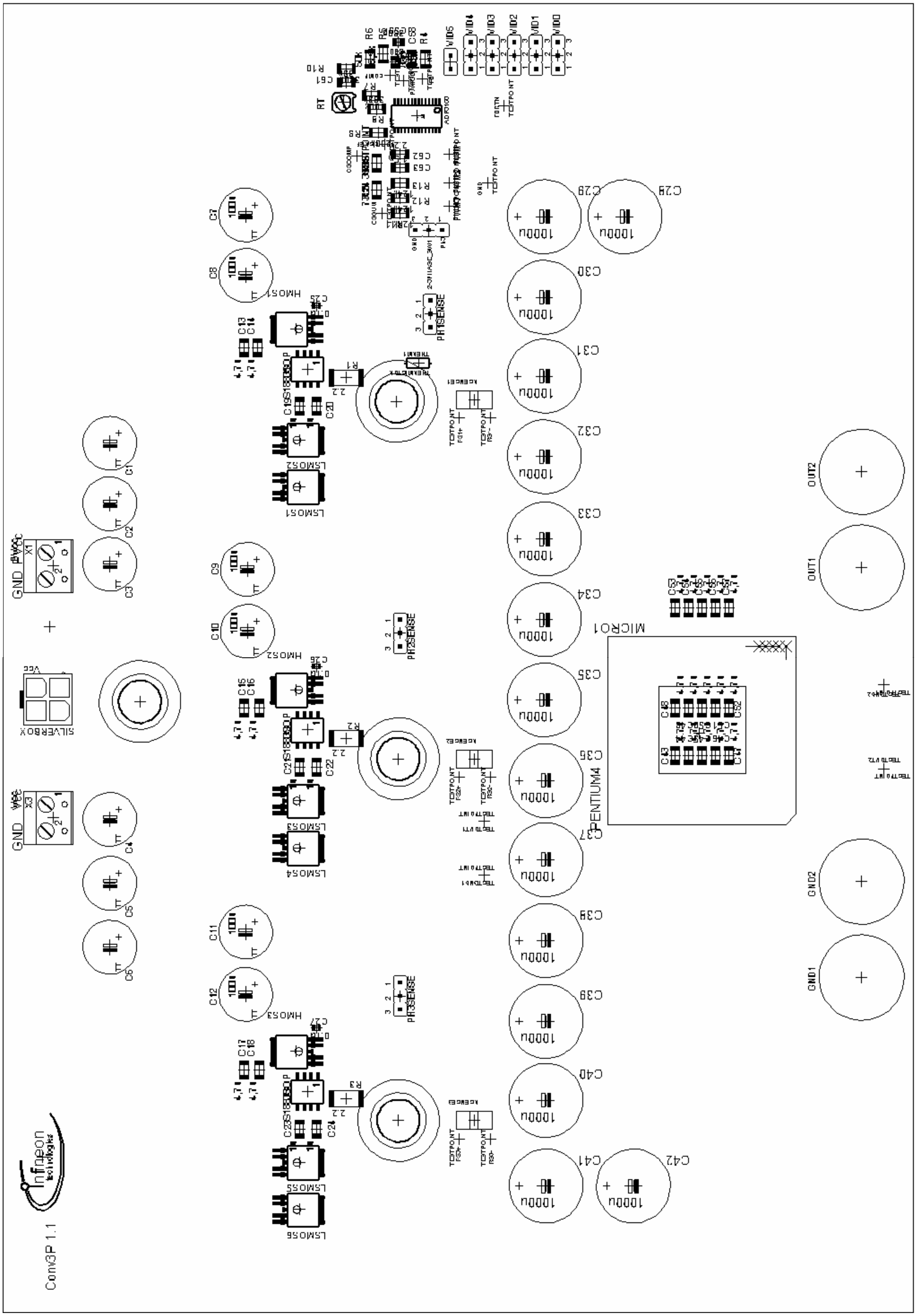
Appendix B

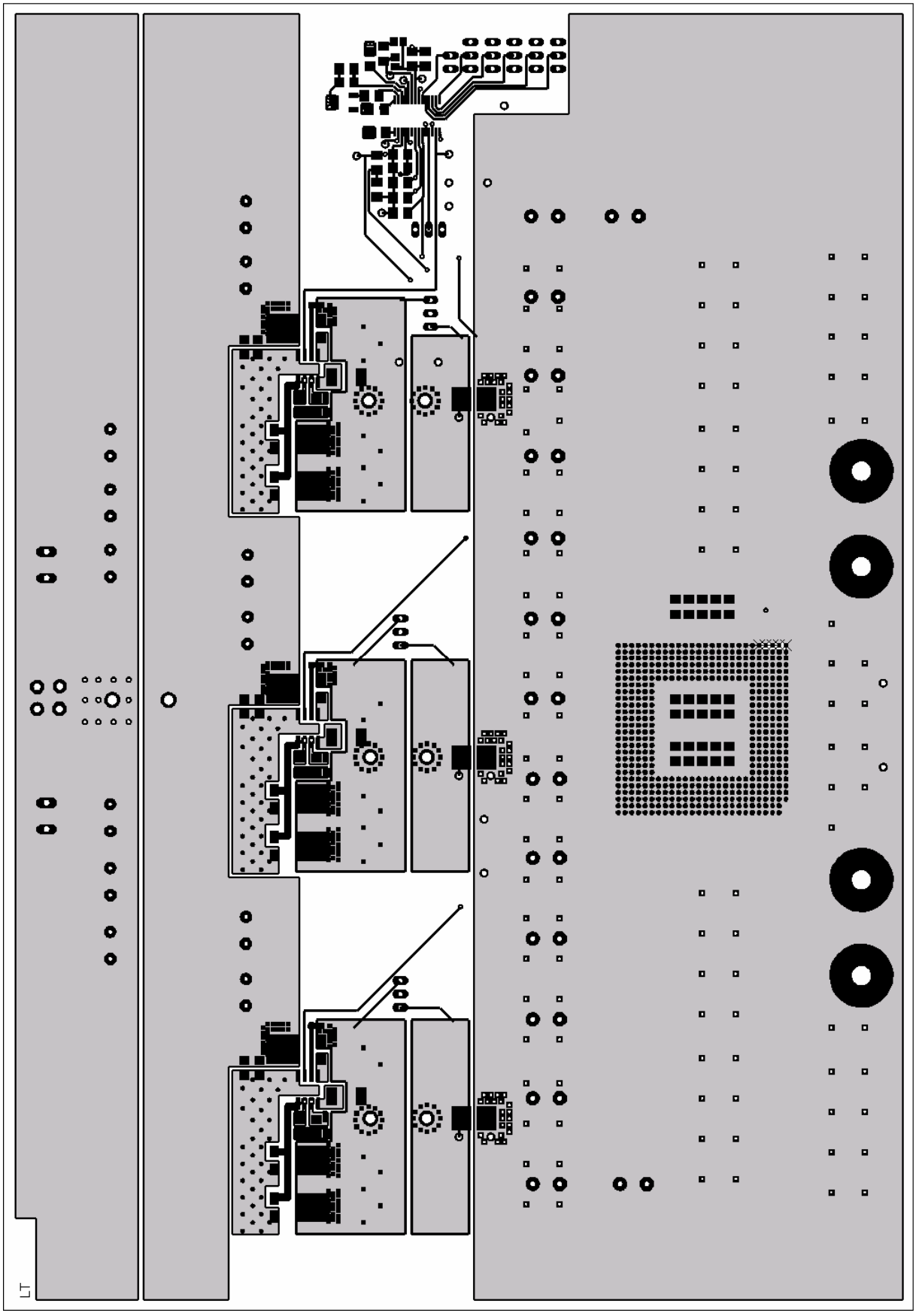
ADP3168 Datasheet

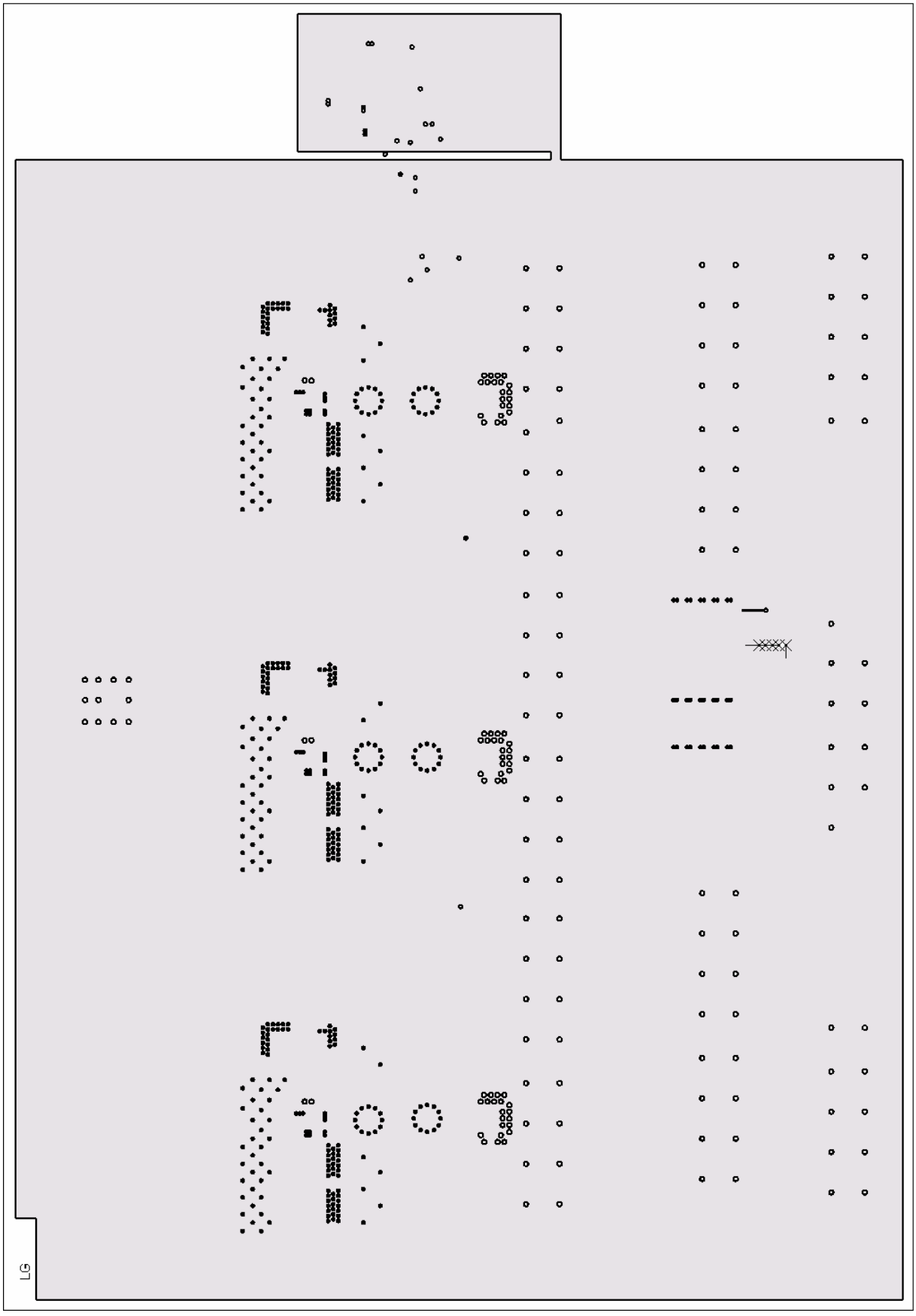
Appendix C

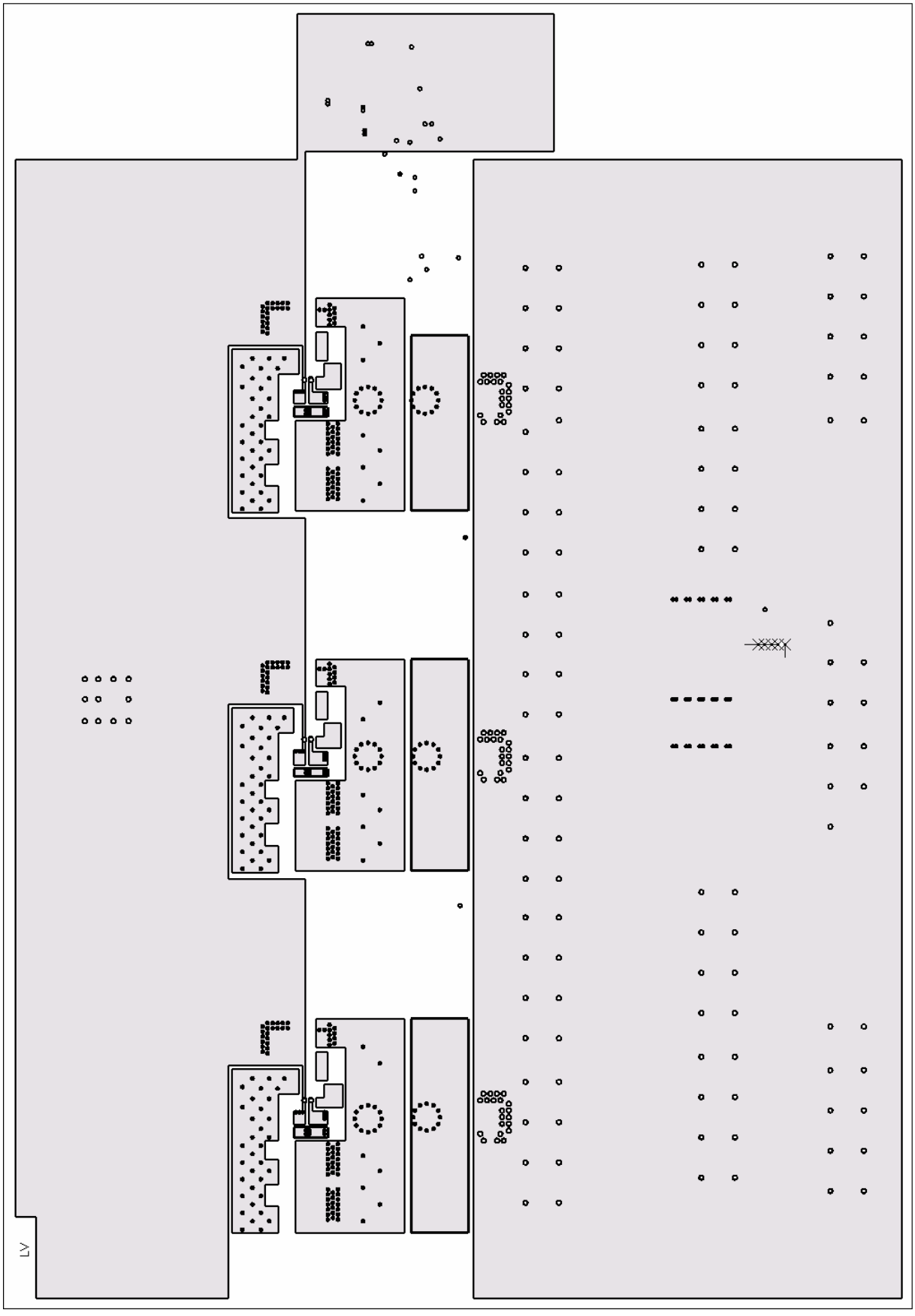
Board Layout

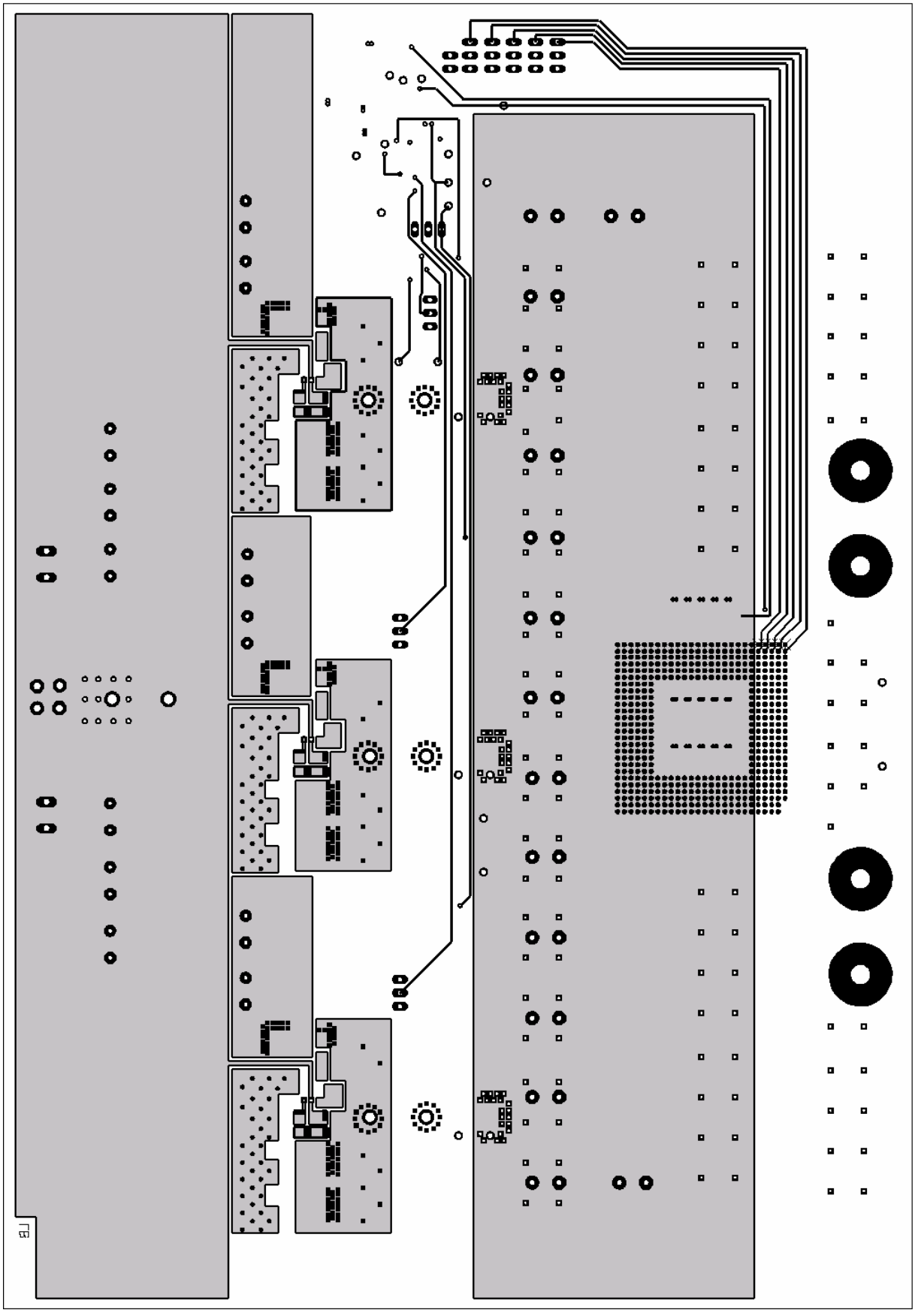
- Silkscreen
- Top Layer
- Inner 1 (Ground) Layer
- Inner 2 (PVcc & Vcc) Layer
- Bottom Layer
- View

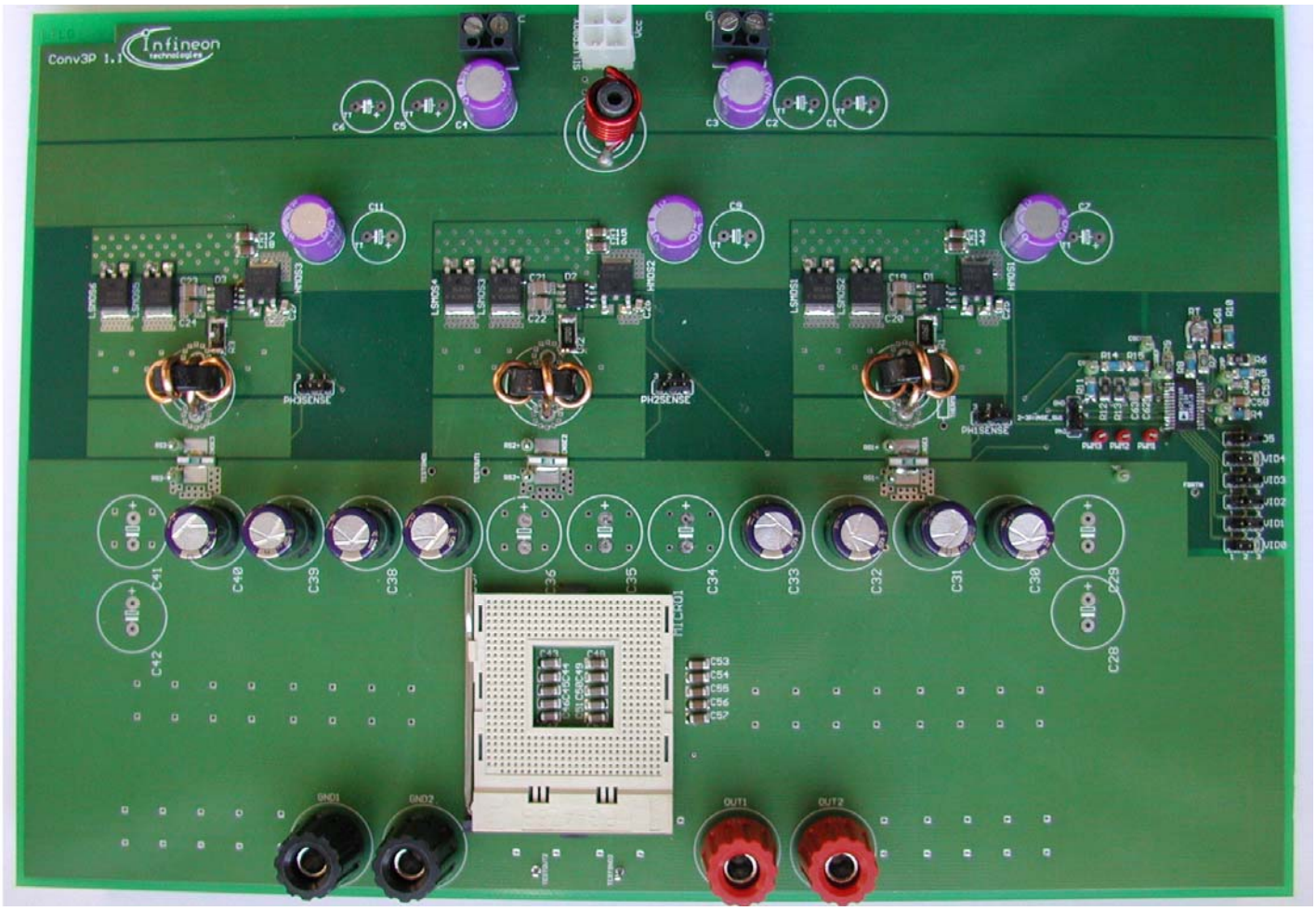

Conv3P 1.1
PENTIUM4
MICRO1
OUT1
OUT2
GND1
GND2
SILVERBOX
PH1SENSE
PH2SENSE
PH3SENSE
LSMOS1
LSMOS2
LSMOS3
LSMOS4
LSMOS5
LSMOS6
HMOS1
HMOS2
HMOS3


LT


LG


LV




Conv3P 1.1
Infineon
technologies
VCC
PH3SENSE
PH2SENSE
PH1SENSE
GND1
GND2
OUT1
OUT2

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