FRONT-END CIRCUIT TECHNIQUES FOR HIGH SPEED INTERFACES

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Resumen

TÍTULO: Técnicas de circuitos de interfaces de alta velocidad. *

AUTOR: CRISTHIAN ROLANDO TORRES DELGADO †

PALABRAS CLAVES: interfaces de alta velocidad, ecualizador lineal, técnicas de circuito.

La demanda por comunicaciones más rápidas en aplicaciones con alto contenido multimedia ha incrementado las velocidades de datos de los circuitos de E / S integrados en los sistemas para centros de datos y productos electrónicos de consumo. Para lograr estas velocidades de datos en dispositivos electrónicos de bajo precio, las interfaces de alta velocidad requieren mejorar su ancho de banda manteniendo el consumo de energía y los costos de producción y desarrollo. La integración de interfaces de alta velocidad utilizando la tecnología CMOS de canal largo contribuye a minimizar los gastos de producción. Sin embargo, la adopción de transistores de canal largo causa capacitancias parásitas grandes, lo que requiere altas corrientes de polarización en el transistor para amplificar a altas frecuencias. Mientras tanto, los costos de desarrollo pueden reducirse reemplazando el trabajo humano con algoritmos y funciones automatizadas realizadas por computadoras. Este trabajo explora tres técnicas de circuito utilizadas en el extremo receptor de las interfaces de alta velocidad destinadas a contribuir

*Trabajo de Investigación.

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a la reducción de los gastos en diseño, caracterización e integración. El primero supera las limitaciones de frecuencia del transistor MOS, manteniendo el consumo de energía en los circuitos de ecualización. El segundo busca reemplazar el equipo de prueba, y el tercero reduce el trabajo humano. Finalmente, las técnicas de circuito se aplican en tres circuitos diseñados e implementados en una interfaz analógica para un receptor estándar compatible con USB 3.0.

Abstract

TITLE: Front-end Circuit Techniques for High-Speed Interfaces [‡]

AUTHOR: CRISTHIAN ROLANDO TORRES DELGADO [§]

KEYWORDS: High-speed interfaces, linear equalizer, circuit techniques.

The demand for faster communications in richer media content applications has increased the data rates of I/O circuits integrated into systems for data centers and consumer electronics. To achieve these data rates in low-priced electronics, the high-speed interfaces require to enhance its bandwidth keeping fair its power consumption and production and development costs. The integration of high-speed interfaces using long-channel CMOS technology contributes to minimizing production expenses. However, the adoption of long-channel transistors causes large parasitic capacitances, requiring high transistor currents to amplify at high-frequencies. Meanwhile, the development costs can be reduced replacing human labor with algorithms and automated functions performed by computers. This work explores three circuit techniques used in the receiver-end of high-speed interfaces aimed to contribute to the reduction of the expenses in design, characterization, and integration. The first overcome the frequency limitations of the MOS transistor, maintaining power consumption in equalization circuits. The second replaces testing equipment, and the third reduces human labor. Finally, the

[‡] Research Work

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techniques are applied in three circuits designed and implemented in an analog front-end for a compliant USB 3.0 standard receiver.

INTRODUCTION

New applications such as telemedicine, streaming videogames, and the multi-end video incorporate rich media content and real-time execution features, expanding data traffic in electronic handheld devices and data centers (2). Demand for data traffic has been partially satisfied by increasing the number of I/O pins per component. However, expanding of I/O pins is not feasible for systems constrained in area and number of pins. Due to this limitation, the new communication standards tend to increase the per-pin data rate, as is shown in Fig.1 (1; 3). To support the increase of data speeds, the I/O circuits require to enhance the pin bandwidth while maintaining its power consumption.

The implementation of high-speed interfaces is a challenge, especially in low-price low-volume electronic devices. Due to a restricted budget, inexpensive elec-

Figure 1. Per-pin data rate evolution for a variety of common standards(1).

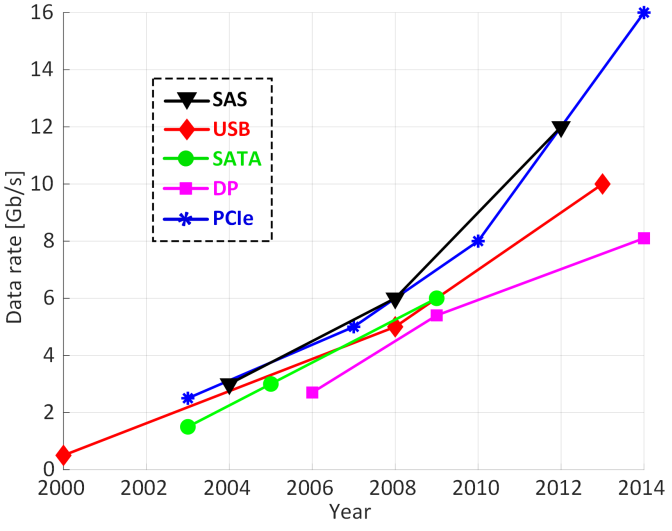
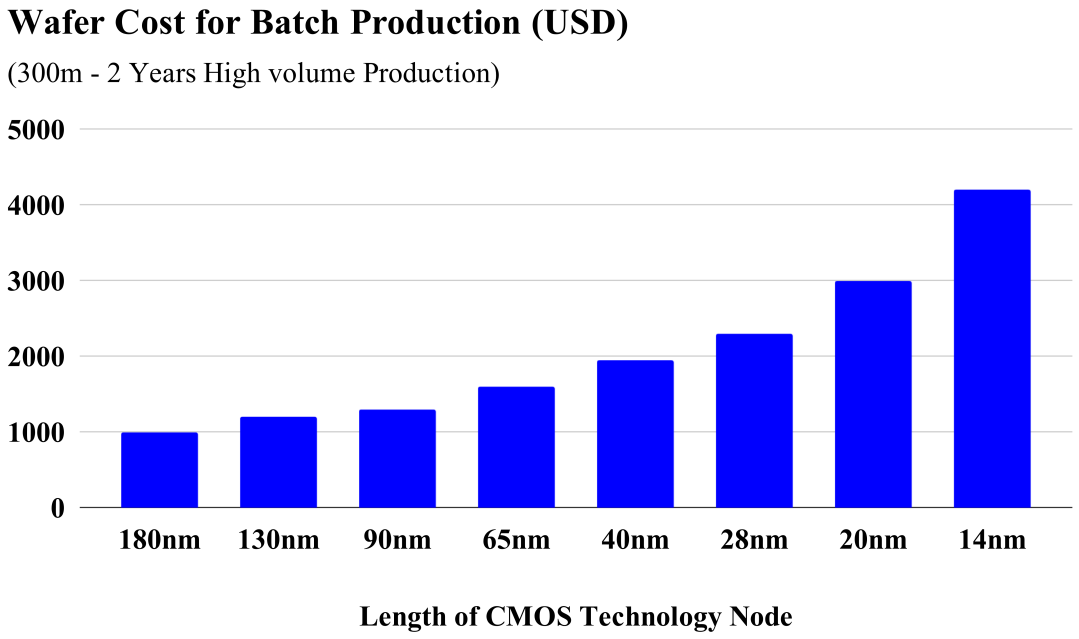


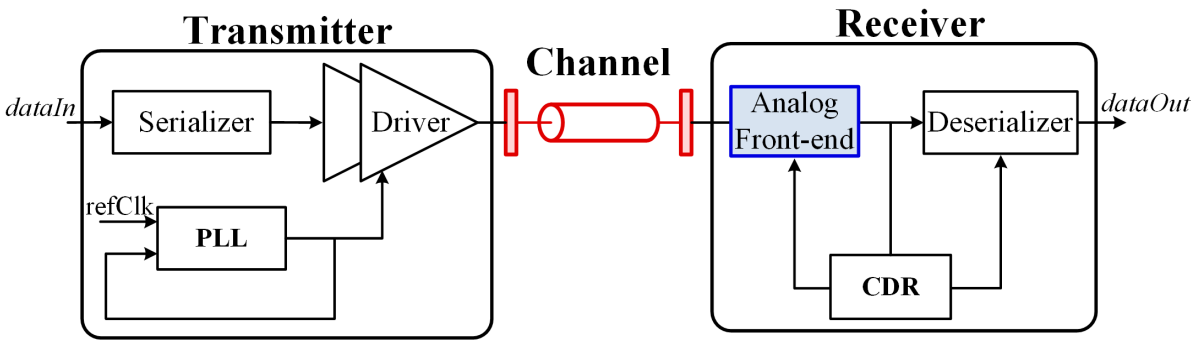
Figure 2. Foundry wafer cost in different CMOS technology nodes(4).



tronic products require to minimize expenses in development, characterization, and implementation. To keep low implementation costs is necessary to reduce the costs of circuit fabrication. As Fig.2 shows the cost of silicon wafers depend on the CMOS fabrication technology. Therefore, the choice of cheaper CMOS technologies implies circuit integration using long channel transistors. The enlarge transistor size causes larger parasitic capacitors. Due to the effect of these capacitances, the transistor behaves as a low-pass filter, making difficult to reach gain in frequencies near to transistor transition frequency (f_T).

A high-speed interface can be modeled as is depicted in Fig.3. At high frequencies, the channel experiences skin effect and dielectric losses. These dispersion losses grow proportionally to the frequency increase. Thus, the communication channel acts as a low-pass filter. This low-pass behavior affects the

Figure 3. Typical transceiver for high-speed interfaces.



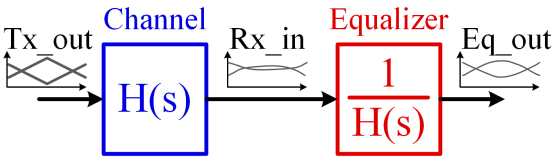
integrity of high-frequency signals causing data corruption and the potential loss of information (5; 6). To overcome these issues and achieve a successful data transmission, the analog front-end needs to boost the gain of high-frequency signal components counteracting the channel attenuation. However, if the receiver circuit is integrated using low-cost CMOS technology, the high-speed I/O design became limited by the underlying technology. Therefore, the integration of high-frequency circuits into low-price CMOS technologies requires the application of broadband circuit techniques. The objective of these techniques is to obtain best performance of the CMOS technology and compensate the signal losses caused by the transmission channel.

As is depicted in Fig.4, the gain losses produced by the channel can be alleviated producing the channel inverse transfer function. The analog front-end block of new high-speed links integrates circuits such as continuous time linear equalizer (CTLE) and variable gain amplifier (VGA) to mitigate the gain losses. The design techniques employed in equalization circuits aim to get the best ratio between gain, bandwidth, and power consumption. To achieve this goal, the majority of the equalizer architectures reported in the literature employ two circuit topologies. The first technique attempts to reduce the effect of the transistor para-

sitic capacitances, and the second aims to increment the transconductance of the amplification stage at higher frequencies. The design techniques used in broadband equalizers comprise the integration of inductances, negative capacitances, and the addition of extra transconductance. Although several works report equalization circuits for a variety of standards and specifications, the literature lacks a work that brings together all the circuit methods employed in linear equalization circuits. The reporting of an equalization topologies summary gives the possibility of compare each technique advantages and issues.

The scale-down of the implementation expenses is not enough to accomplish a remarkable drop in the final cost of electronic components. The leading cause on the high price of chips is the payment of skilled labor needed for the design and testing stages of integrated circuits (4). Accordingly, replacing or decreasing human labor, with algorithms and automated functions performed by computers, it is required to reduce the chip final cost. Reaching to contribute to this approach, this research work presents two circuit solutions to reduce the human time required in circuit design and validation. The first circuit consists of an on-chip eye diagram characterization circuit for high-speed interfaces. The circuit adjusts the phase time and comparison voltage level of a comparator to modify the sampling point. The bit error rate (BER) measurement is employed to determine if each selected sampling is inside or outside the eye diagram. This characterization scheme allows replacing expensive scopes required to validate interfaces in higher frequencies. The second circuit generates the bias current reference of the analog circuits that comprise the analog front-end. The number of required bias current reference depends upon the number of analog circuit blocks, and peripherals vary with each particular integrated system. The bias current reference source implemented in this work is modular. This characteristic allows the

Figure 4. Ideal equalizer transfer function



selection of the number of outputs, and the bias current can be adjusted accordingly with the currents required by the system. The modular feature reduces the designing time and contributes to getting lower chip final costs.

This research work explores multiple circuit techniques applied in the design of VGA and CTLE circuits integrated into high-speed wireline links. As a conclusion of these comparisons, the thesis proposes a circuit design of a VGA with equalization function integrated. The VGA-CTLE circuit achieves the specifications for the USB 3.0 standard, with an operating frequency of 2.5GHz, and it is integrated into a TSMC $0.18\mu m$ CMOS technology. Additionally, the thesis proposes the implementation of a characterization technique to build the eye diagram at the receiver of high-speed links without interruption of the data transmission. The main advantage of the proposed circuit technique is the characterization of eye diagram at the receiver of the high-speed link without any expensive equipment. Finally, the thesis introduces two versions of bias current reference circuit with modular implementation. The current reference circuit has a remarkable performance against process-voltage-temperature (PVT) variations obtaining a maximum error of 0.6% for the current reduced version.

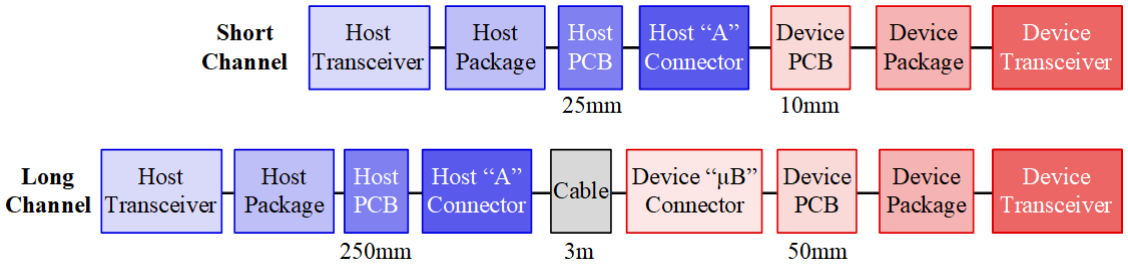
1. VARIABLE GAIN AMPLIFIER WITH LINEAR EQUALIZATION FUNCTION

The speed data transmission scaling requires a proportional increase on I/O circuits bandwidth to support new communication standards. The most popular communication standard is the USB, it is found in all types of devices ranging from high-performance computers, toys, cell phones, and storage devices. The communication channel to link these devices has bandwidth limitations. Thus, the receiver requires a circuit to boost the signal gain at higher frequencies. These circuits must increase the maximum speed of operation keeping low-power consumption, and a low-cost devices. However, obtaining inexpensive interfaces requires the use of long transistors restricting the speed of circuit operation due to the transition frequency. This chapter compares the advantages and limitations of the most common circuit techniques employed in the design of high-speed I/O circuits. These techniques are compared through a design case of the equalization function for the USB 3.0 standard. The conclusions can be extrapolated to the design of other high-speed interfaces.

1.1. BACKGROUND

The universal serial bus (USB) standard has become the most common approach to connectivity and power charging for computers and electronic devices. Since their first versions, USB has been consistent with the speed, dynamic, and power requirements for a variety of peripherals such as laptops, mobile phones, flash memory sticks, and many other devices. The USB 3.0 specification is the version approved in 2008 by the universal serial bus implementation forum (USB-IF). This standard version incorporates previous revisions of the standard and fixes a new

Figure 5. USB interconnection environments (7).



nominal data rate of $5Gb/s$.

Fig.5 shows the two possible channel losses environments initially considered by the USB-IF for two electronic devices interconnected through a USB interface. The short channel takes into account the losses caused by the connection between the die pad to the USB transceiver, the package, the PCB traces, and the connector losses for host and device. Meanwhile, the extended channel model uses the worst possible scenario for PCB traces and includes a three-meter ca-

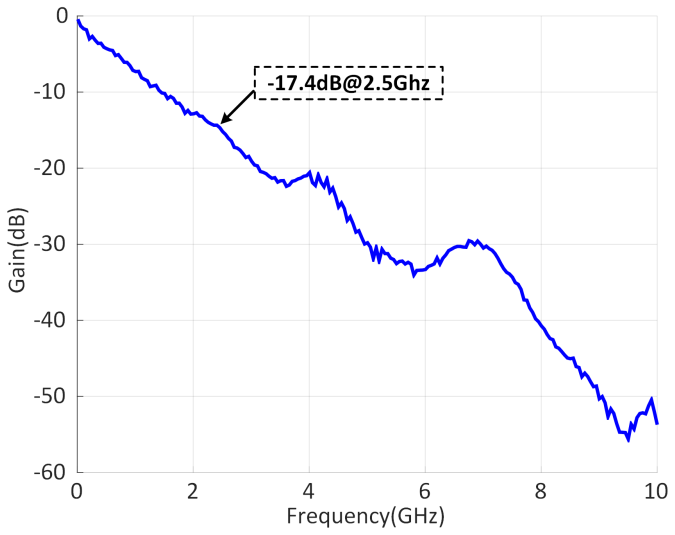
Figure 6. USB 3.0 loss budgets for all legal configurations (8).

ble, the longest length accepted by the standard. Based on these considerations operating at a Nyquist frequency of $2.5GHz$, the first revision of the standard suggested insertion losses around $-20dB$ for the full link (9). However, the rapid expansion of market applications such as smartphones and tablets changed the initial loss requirements, and the power budget has had to be adjusted and distributed, considering the different cables and connectors. Fig.6 shows a summary of the power budget currently established for various connectors. Fig.7 shows the frequency response of the channel model used for the characterization of the long channel case. The S-parameters are published in the USB forum website. Even though there are no model for the short channel scenario, the specifications of the standard fix channel losses between $-4dB$ and $-18dB$ as the general consideration (7).

The USB transceiver must be capable of compensating the losses induced by the transmission channel. This compensation of losses can be distributed between the transmitter and the receiver. The USB standard defines minimum normative specifications for the receiver-end to maintain data signal integrity and warrant a successful data transfer. Although these specifications do not indicate the strict implementation of a linear equalization function in the receiver-end, the budget for channel losses makes this clear (7; 9).

Fig.8 shows a block diagram of a typical analog front-end integrated into the receiver of high-speed interfaces. The termination block involves the impedance matching network and the electrostatic discharge (ESD). Commonly, the VGA and CTLE circuits are performed separately. However, these functions can be integrated into the same circuit block. The purpose of VGA-CTLE is to compensate the channel losses effect and balance the gain of high and low-frequency components. As a result, it is possible to improve the vertical opening of the eye diagram

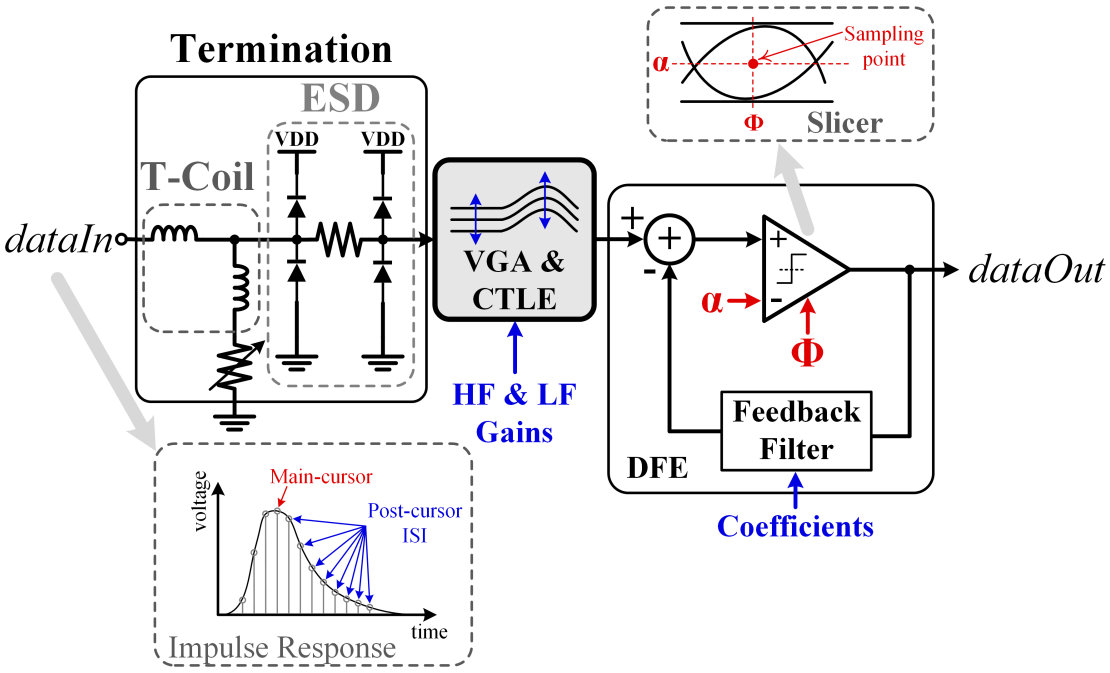
Figure 7. USB 3.0 Full link channel frequency response model.



facilitating the information recovery. The channel conditions change according to the connector and cable characteristics. Then, the equalizer must be capable of adapting the signal in all the possible link environments, even for earlier revisions of the USB standard where the frequency of operation is low, and the equalization function is not required. For this reason, the VGA-CTLE must be adjustable, so that it can behave like a buffer and in other cases produce gain peaking to provide a gain in the nominal frequency of $2.5GHz$.

The implementation of the VGA-CTLE circuit in a long length CMOS transistor node requires the application of circuit techniques to produce gain and force the transistor to operate at the speed limit. This chapter presents the application and comparison of a variety of circuit techniques used in the design of VGA and CTLE circuits to the design of a VGA-CTLE circuit for USB 3.0. The chapter concludes with the circuit design of a VGA-CTLE circuit in a $0.18\mu m$ CMOS standard technology. The proposed circuit complies the specifications for the equalization function

Figure 8. Typical architecture of analog front-end block.



of the USB *SuperSpeed* standard (7) with a low power consumption compared to the reported current designs in the literature. Simulations results prove the robustness for the process-voltage-temperature corners using the ranges commonly considered by the industry.

1.2. COMPARISON OF THE EQUALIZATION CIRCUIT TECHNIQUES FOR VGA AND CTLE CIRCUITS

Considering that the equalizer is one of the dominant power consuming blocks and its power increases with the demand of faster data rate in communication links, circuit designers have widely studied this circuit, to improve its operation without area and power consumption impact. The techniques presented in the circuit implementation are useful for the USB 3.0 analog front-end, also are appropriate in most of the known I/O standards such as peripheral component in-

Table 1. 2018 State of the art CTLE circuits using broadband techniques

Ref.	Circuit technique	CMOS Tech [nm]	Nyquist Freq. [GHz]	HF Peak [dB]	Supply voltage [V]	Power [mW]	Area [mm2]
(10)	CD	28	14	34	1.5	560	3.34
(11)	CD	45	5	7.5	1.1	14.3 CTLE+1-tapDFE	N.A
(12)	IP	180	5	35	1.8	54 VGA+AGC	1.32
(3)	CH	90	2.2	60	1	2.5	0.01
(13)	CD - IP	65	14	8.8	1.2	2.5	N.A
(14)	CD - IP	45	12.5	8	1	2.4	0.01
(15)	CD - IP	65	20	16	1	8	0.36
(16)	CD - IP	28	20	7	0.85	927 Full transceiver	0.81
(17)	CD - IP	180	2.5	11	1.8	18	N/A
(18)	CD	20	28	23	0.9	177 Front-end	0.22
(19)	IP	180	0.9	94.1	1.8	20.5	0.42
(20)	CD	65	7.5	20	1.1	13.9	0.05
(21)	CH - IP	90	2.2	40	1	2.5	0.01
(22)	CD - IP	16	28	12	0.9	60 Front-end	N/A
(23)	CD	28	16	15	0.9	240 Front-end	0.33
(24)	CD	130	2.7	22	1.2	26	0.18
(25)	CD - IP	65	20	22.8	1	97	N/A
(26)	CD - NC	32	6.25	10	1.1	5.25	N/A
(5)	CD - IP - NC	40	10		1.1	25.2	0.13
(27)	CD - IP - CH	130	10	20	1.5	60	0.2
(28)	CD	28	6.5	10	1	32 Front-end	0.226
(29)	CD - IP	65	7.5	11	1.1	39	0.62
(30)	CD - IP	65	10.5	14.4	1.2	34.2 CTLE+1-tapDFE	0.027
(31)	CD - IP	22	16	16	1.07	7.64 Front-end	0.079
(32)	CD - IP	65	14	8.8	1.2	24 CTLE+2-tapDFE	0.72
(33)	CD - IP	40	20	18.6	1.1	43.9 CTLE+DFE	N/A
(34)	CD	28	7	4	0.9	102 Front-end	0.0144
(35)	CD - NC	32	3.5	17	1	7	N/A

terconnect express (PCIe), serial advanced technology attachment (SATA), display port (DP), high definition multimedia interface (HDMI), etc. These standards have different applications and the choice of the equalization function depends on conditions such as channel losses at the Nyquist frequency, technology node of integration, and power budget. The circuit techniques shown in this section are the most commonly used into VGA and CTLE circuits of high-speed receivers. These techniques are based on capacitive degeneration (DC), inductive peaking (IP), include a negative capacitance (NC) and Cherry-Hooper amplifier (CH).

Table 1 shows a summary of the relevant publications that report the implementation of VGA or CTLE circuits in receiver-ends and full transceivers. The table indicates the initials of the technique employed in the circuit and the most relevant parameters to evaluate the performance of an equalizer.

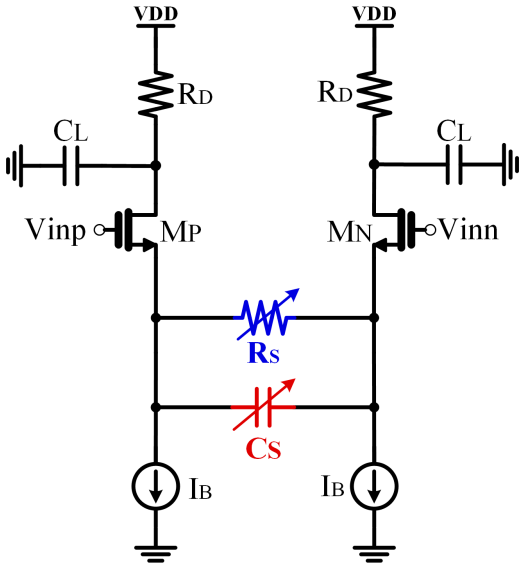
The techniques presented in the table were separately applied in the design of the VGA-CTLE circuit for USB 3.0 interface. The objective of each circuit implementation is to find the advantages and limitations of each circuit technique in the design of an equalizer for USB 3.0 standard. This section shows a comparative analysis of the considerations and results concluded by applying the circuit techniques found in the current literature to generate the frequency boosting required by the equalizer.

The design specifications for the VGA-CTLE circuit are derived from the USB 3.0 specification manual and the equalizer design guidelines, both available on the USB forum website (7; 9). The low-frequency gain (A_{LF}) of the equalizer used as reference display values between $2dB$ when the link is the short channel and $-3dB$ with the long channel link. Furthermore, the gain at the Nyquist frequency ($A_{2.5GHz}$) is varying between $2dB$ when the highest performance of the equalizer is needed, and attenuation when the channel does not enforce larger

Table 2. CTLE design specifications summary.

Parameter	Value	Description
A_{LF}	-3dB to 2dB	low-frequency gain range
$A_{2.5GHz}$	2dB	Minimum gain at 2.5GHz
Peaking	0dB to 6dB	Difference between A_{LF} and $A_{2.5GHz}$
C_L	700pF	Load capacitance

Figure 9. Differential pair with RC degeneration.



losses. The load capacitance of the equalizer is set at $700pF$, considering the full architecture of the receiver. This estimation of the load takes into account the input capacitance of the circuit connected to the equalizer output and the parasitic capacitances produced by routing and physical implementation of the circuit. Table 2 summarizes the equalizer specifications.

1.2.1. Capacitive Degeneration Equalizer The low-pass response of a differential pair results from the output pole caused by the combination of the parasitic capacitance seen at the drain of the amplification transistor and the load capacitor (C_L). The differential pair is degenerated using a capacitor as Fig.9 shows, to create a broadband response and make that the effective transconductance

increases at high frequencies.

The circuit employs both resistive and capacitive source degeneration with the objective of having control of the response at high and low frequency, thus obtaining the CTLE and VGA functions. Fig.10 depicts the half-circuit equivalent of the RC degeneration. The equivalent transconductance is expressed by:

$$G_m = \frac{g_m}{1 + g_m(\frac{R_s}{2}||\frac{1}{2sC_s})} \tag{1.1}$$

$$= \frac{g_m(sR_sC_s + 1)}{sR_sC_s + 1 + g_mR_s/2}. \tag{1.2}$$

In consequence the transconductance G_m contains a zero at $1/(R_sC_s)$ and a pole at $(1 + g_mR_s/2)/(R_sC_s)$. Then G_m will have a frequency response, as shown in Fig. 11a). If the G_m cell is properly designed the zero could cancel the pole (R_DC_L) due to the load capacitance, obtaining the frequency response shown in Fig. 11b), where the bandwidth is extended by a factor $1 + g_mR_s/2$. The consequence of its bandwidth extension is a reduction in the gain that at low frequencies is $A_v = g_mR_D/(1 + g_mR_s/2)$.

Figure 10. Half equivalent circuit with RC degeneration

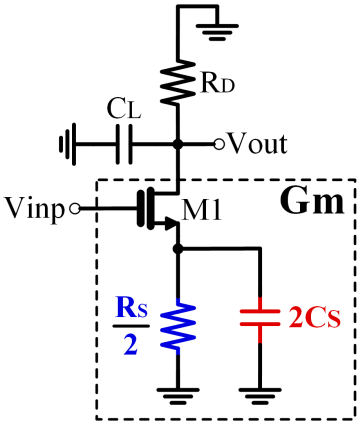
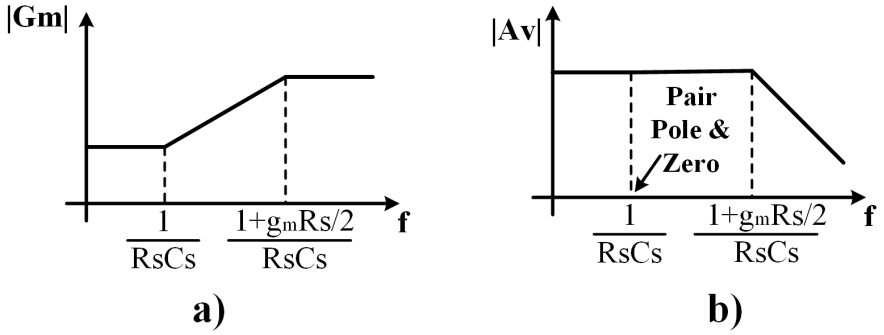


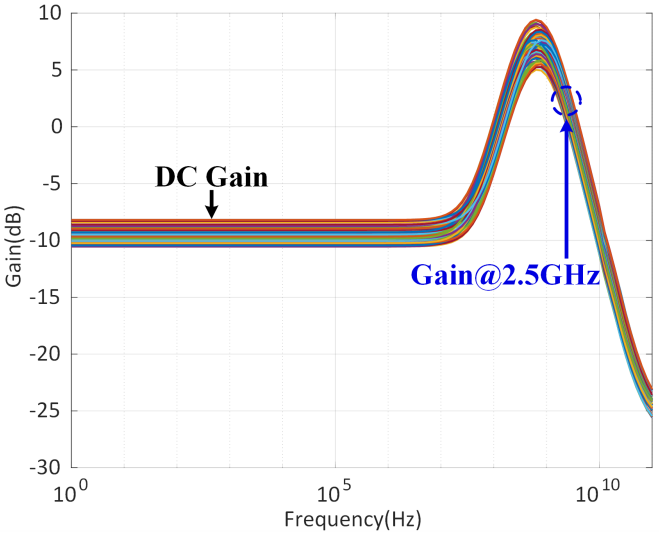
Figure 11. Bandwidth extension implementing RC degeneration.



The increment of bandwidth provided by the capacitive degeneration technique depends on the transconductance of the amplifier transistor (g_m). As the classical model of the transistor exhibits, g_m parameter is directly proportional to the drain current. Therefore, to have large transconductance, high current consumption is required.

The equalizer circuit design applies the capacitive degeneration technique.

Figure 12. Results for frequency response for CD equalizer.



The circuit is implemented pushing the zero caused by C_S at a lower frequency than the pole caused by C_L. It generates a boost in the gain that must be pushed in the frequency range of interest, in this case, the $2.5GHz$ range. Fig.12 shows the results of the frequency response varying the corners of process, voltage, and temperature (PVT) for the maximum possible value of gain at $2.5GHz$. The maximum gain boosting occurs around $1GHz$, and beyond this value, the influence of the pole due to the load capacitance drop the circuit gain. Therefore, even in cases where current increases to push the pole caused by the capacitive degeneration to the highest frequencies, the gain is decreased.

Although the circuit design exhibits a peaking behavior for frequencies above $1GHz$, this peaking gain falls off with the increment of the temperature for all the corner cases, as Fig.13 shows. According to the specifications for the VGA-CTLE block, the minimum gain at $2.5GHz$ must be $2dB$, and this specification must be fulfilled in all the corners cases. Thus, for the capacitive load of $700pF$, the use of the capacitance in the source is not enough to meet the USB 3.0 specifications.

1.2.2. Inductive Peaking One of the simplest ways to compensate the capacitive effect in a node of a circuit is to connect an inductance to the same node of the circuit so that the inductance generates a zero to compensate the output pole produced by the capacitance. This technique is also applicable to broadband amplifiers, and, as Kim et al. (36) describe, when this inductance is applied in a common-source amplifier, inductive peaking can expand the bandwidth by up to 70%. The peaking is done replacing the drain resistor by an inductor (16; 18; 33). However, in an integrated circuit, a passive inductor represents a large silicon area (comparable to hundreds of transistors), and in most standard CMOS technologies it does not have a good quality factor. For this reason in the design of

Figure 13. Results for PVT corners for gain at 2.5GHz in CD equalizer.

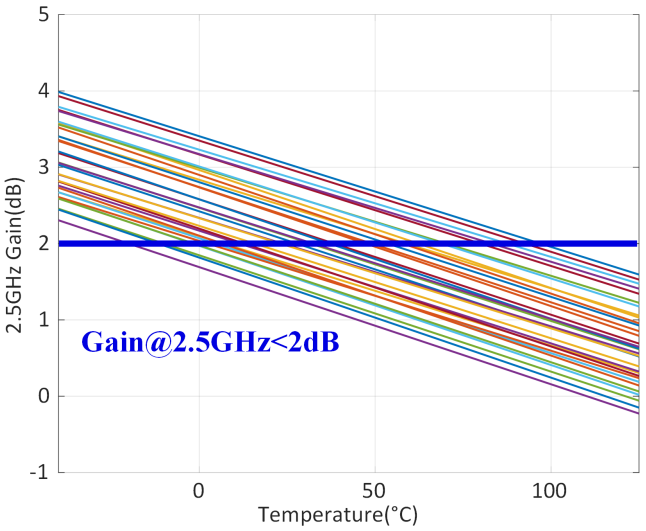
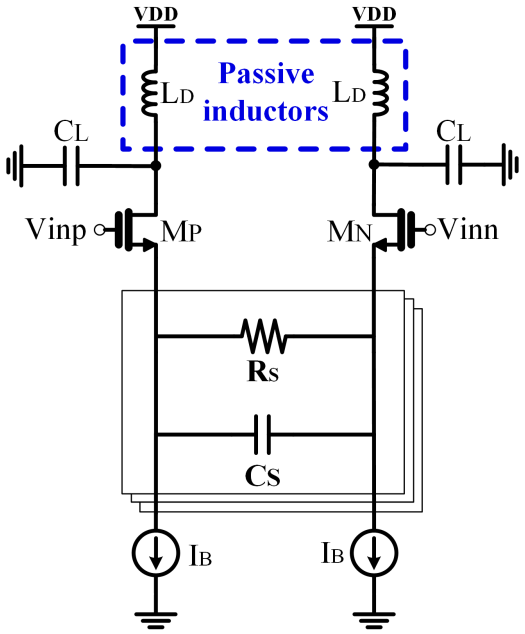


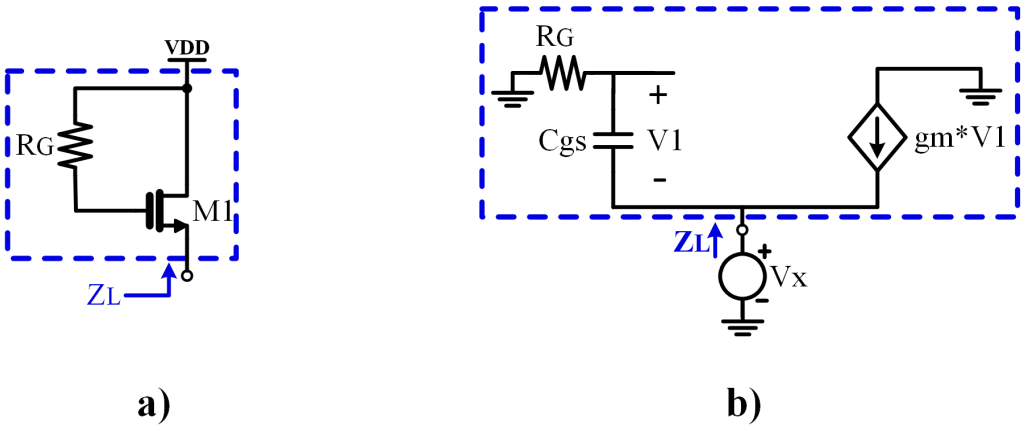
Figure 14. Differential pair with RC degenerated and passive inductor.



integrated broadband circuits is preferred to seek for a circuit that behaves like an inductor, which means its impedance varies directly proportional to the frequency.

The inductors implemented using active devices are known as active induc-

Figure 15. Folded active inductor circuit.



tors. They offer advantages like small chip area, tunable inductance, and compatibility with low-cost digital oriented CMOS processes. Nevertheless, as with the circuits integrated into a silicon substrate, active inductors may suffer difficulties such as limited dynamic range, supply voltage fluctuation, and sensitivity to process variations. Innovative designs, according to its application, allow handling with these limitations obtaining good results in high-speed interfaces(19; 30; 31).

Circuit topologies implementing active inductors have been reported in the literature (37; 38; 39; 40). Due to its simplicity and the current-reuse, the most commonly used in high-speed circuits is proposed by Wu (41). Fig. 15a) shows the schematic of the gate-peaking circuit. Fig. 15b) depicts the small-signal model to obtain an expression of the impedance Z_L. Neglecting Cgd and other parasitic capacitances to simplify the analysis, Z_L can be obtained with:

$$sV_1C_{gs} + gmV_1 = -I_X. \tag{1.3}$$

Since $V_1 C_{gs} s R_G + V_1 = -V_X$,

$$Z_L = \frac{sR_G C_{gs} + 1}{gm + sC_{gs}}. \tag{1.4}$$

Taking into account $|Z_L(s = 0)| = 1/gm$ and $|Z_L(s = \infty)| = R_G$, hence, if $R_G \gg 1/gm$, then $|Z_{out}|$ raises with frequency, achieving an inductive behavior. The corner angular frequency of the zero introduced by the active inductor is $w_Z = -1/C_{gs}R_G$ if this zero cancels the output pole of the amplifier, the bandwidth of the common-source amplifier increases.

Usually, the inductive peaking is implemented in combination with the source capacitive degeneration. Then the gain at high frequencies could be equalized varying the capacitance and/ or the resistance R_G of the active inductor.

A VGA-CTLE design is performed using the IP broadband circuit technique join with the capacitive degeneration. The active inductor was characterized in-

Figure 16. Results for frequency response of IP equalizer.

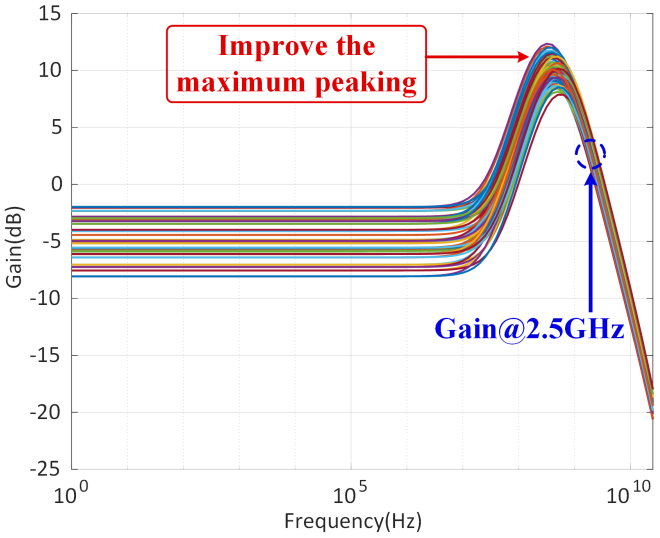
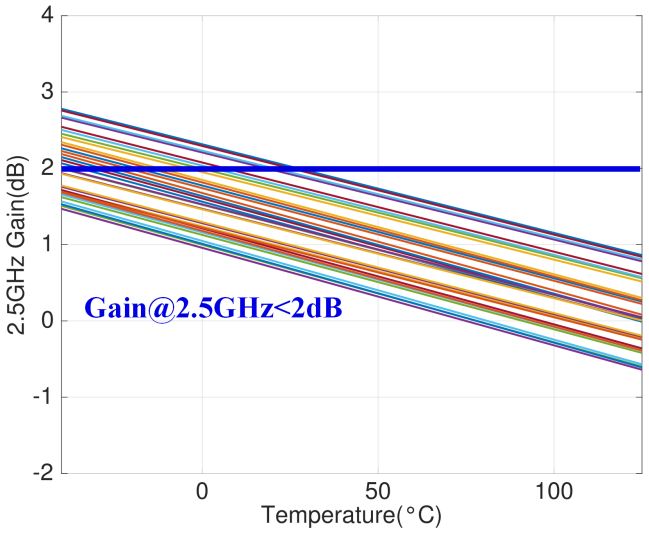


Figure 17. Results for PVT corners for gain at 2.5GHz in IP equalizer.

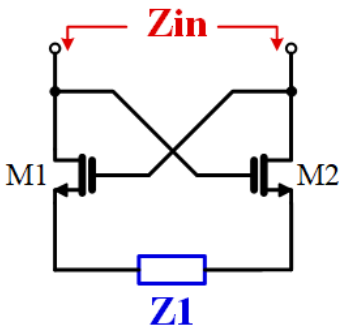


dependently to alleviate the effect of the load capacitance. Fig.17 shows the results for PVT variations using the maximum value of capacitance in the source of the NMOS transistors. The addition of IP circuit rises the gain at low-frequency and produces a higher peak than the CD equalizer. However, this peak is still located in a frequency of $700MHz$ and fall faster than in capacitive circuit design.

Consequently, at $2.5GHz$, the two equalization circuits have the same gain. In fact, as is shown Fig.17, the IP implementation has a worse response when the temperature increases. This loss of gain is due to the proportional temperature dependence of the IP circuit impedance. Thus, the combination of CD and IP equalizer do not accomplish the specification of minimum gain at $2.5GHz$ with the budget current of $6mA$.

1.2.3. Negative Capacitance with Cross-coupled Pair Equalizer The cross-coupled pair (XCP) is a well-known circuit that due to the internal positive feed-

Figure 18. Cross-couple pair as negative impedance converter.



$$Zin = -Z_1 - \frac{2}{gm}. \tag{1.5}$$

back can operate as an impedance negator. Fig.18 depicts the topology of the XCP circuit. The circuit comprises two transistors connected as a latch and in the case of the impedance negator an impedance Z1. If the XCP is in equilibrium (its drain voltages are equal) the equivalent impedance (Zin) can be expressed by equation 1.5 (42).

If Z_1 is a capacitor, the circuit represents a negative capacitance in series with resistance $2/gm$. The negator feature is useful in multiple circuits of high-speed links because it allows relieving the effect of positive capacitances in nodes where the XCP is connected, the balance produced by the negative capacitance of the XCP diminish the effective capacitance in the node, relocating the pole and improving the speed of the circuit.

Fig.19 illustrates the application of XCP negative capacitance in the I/O pads and the ESD circuit attached in on-chip applications. The nodes of the I/O port exhibits a high capacitance due to the physical structure of the pad, the parasitic capacitances of the ESD circuit and the termination resistors. Usually, a T-coil is connected to the termination nodes in order to fix the imaginary part of the coupling impedance circuit. However, sometimes the silicon area is reduced, and on this aspect, the T-coil size is critical. Adding an XCP with a negative capacitance

helps to mitigate the capacitance of the I/O port nodes and, in consequence, the size of the T-coil can be reduced only to the needed for adjusting the impedance.

Another application of the XCP as impedance negator is high-speed equalizers. To achieve an efficient gain balance of the data signal, a CTLE with capacitive degeneration requires to make a gain variation in the Nyquist frequency, which in this case would be in GHz range. In low-cost CMOS technologies (long channel transistors), to generate gain in the high frequencies range is required to drive high currents. Then, due to the constraints of current density in materials, the transistors and layout routing paths tend to be wide, exhibiting large parasitic capacitances. These capacitances and the high C_L, due to the multiple taps and wide input transistors of the subsequent circuit blocks makes difficult to get gain in GHz range. If the XCP is joined to the CTLE output nodes as shown in Fig.20, the effect of the positive capacitance on this node will be lesser. Furthermore, for the implementation of XCP in a CTLE circuit, it is important to consider the trade-off

Figure 19. XCP as a capacitance negator to increase bandwidth of I/O termination.

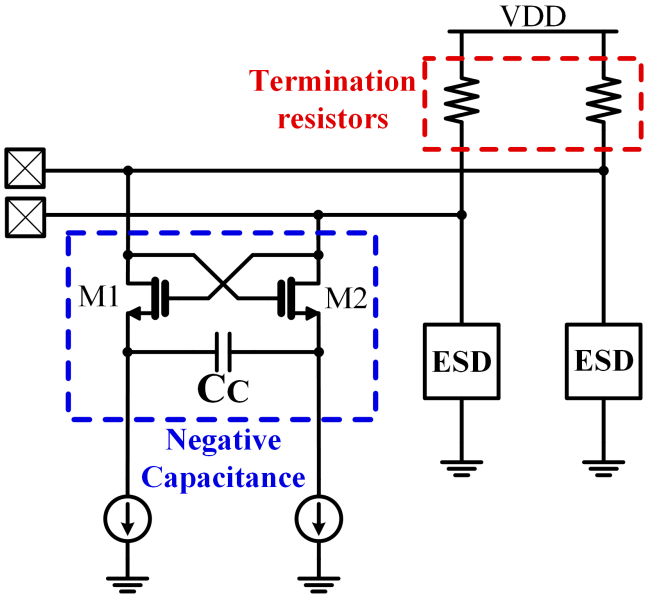
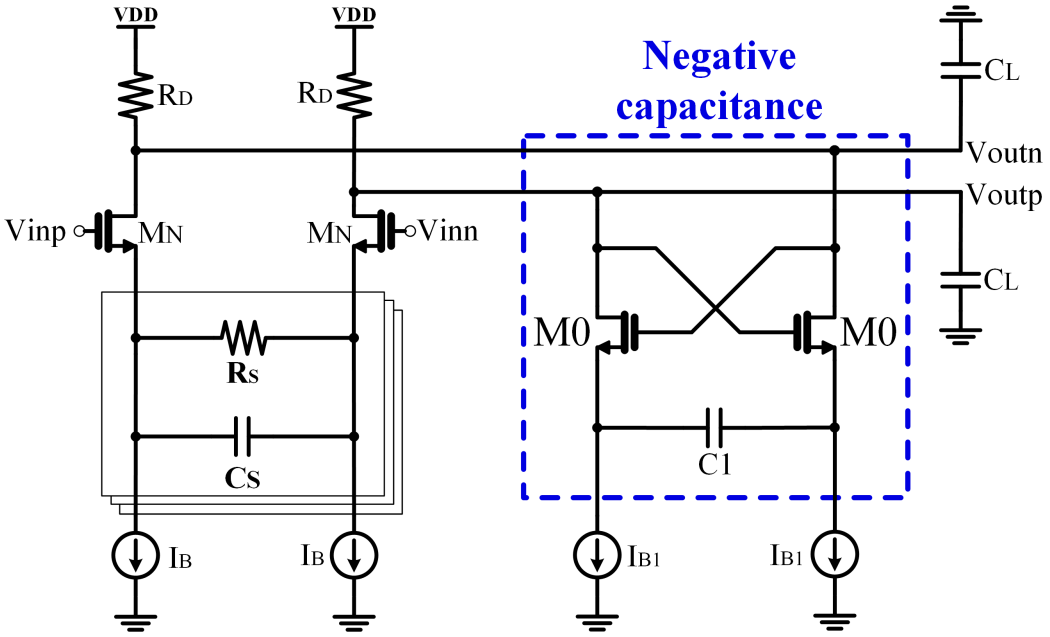


Figure 20. Differential pair with RC degeneration and negative capacitance.

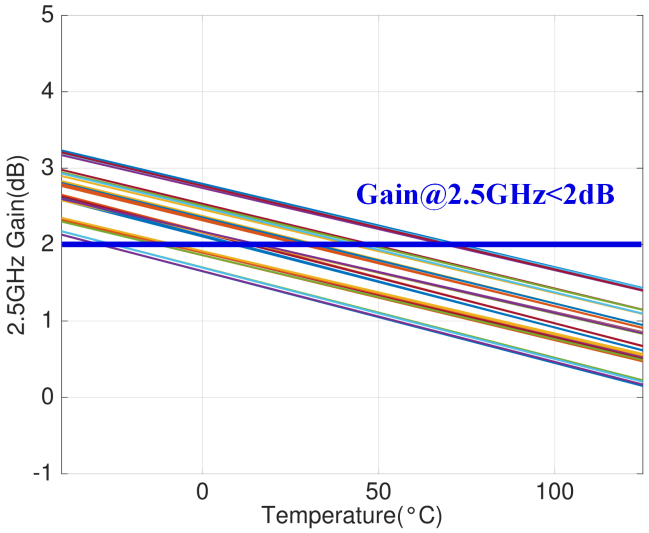


between the addition of the XCP negative capacitance cell and drive more current in the main differential pair. Although usually is possible to enhance the bandwidth of the amplifier increasing the current through the transistors, sometimes transistors are in the edge of speed response, making an insignificant increment (35).

Simulations were performed for the implementation of the XCP employing the same power budget of the previous circuit techniques. Fig.21 shows the results for the gain at $2.5GHz$ ($A_{2.5GHz}$) for PVT variations. Although at $-45 \circ C$ all the corners have a voltage gain above the specification of $2dB$, this gain decreases with the rising of the temperature. Therefore, the VGA-CTLE circuit using the XCP does not complaint the specifications of the USB 3.0 standard.

1.2.4. Cherry-Hooper Amplifier (CH) The Cherry-Hooper amplifier consists of the application of local feedback in the drain of the amplifier transistor to im-

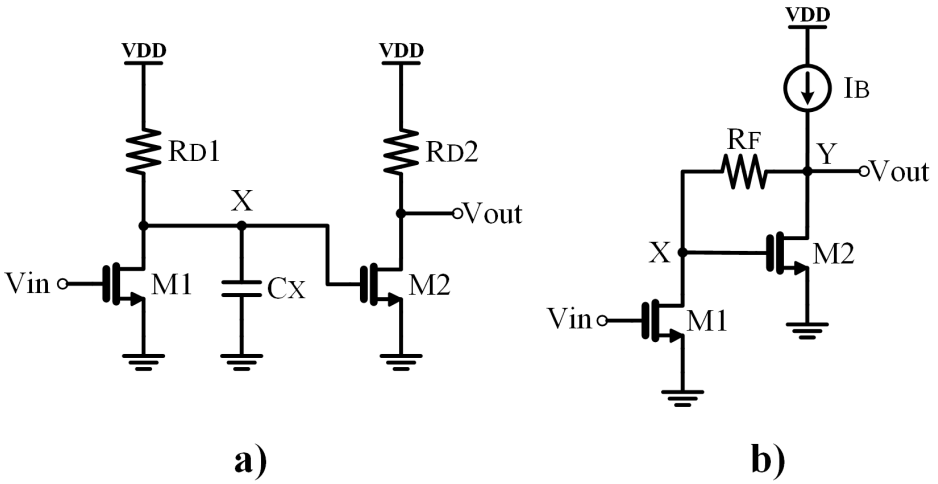
Figure 21. Results for PVT corners for gain at 2.5GHz in NC equalizer.



prove the speed. The Cherry-Hooper concept is based on the the cascade common-source stages shown in Fig.22, where C_X corresponds to the total capacitance seen from node X to ground (3). In this topology, the voltage gain and bandwidth of the first stage are $|A_V| = g_{m1}R_{D1}$ and $w_{p,X} = (R_{D1}C_X)^{-1}$ respectively. Since M2 must be wide enough to get a significative gain in the second stage, its C_{GS2} will be large, reducing the bandwidth. Additionally, the Miller effect of C_{GD2} also affects the speed of the amplifier.

The circuit topology shown in Fig.22b) is proposed to resolve the issues produced by the application of a second stage. This topology joins a feedback resistor R_F around M2 by sensing the output voltage and returning a proportional current to X. Including it modification the circuit has two paths to the output: one caused by the feedback and another through M2. A proper amplifier design limits the signal flowing through R_F because it opposes that generated by M2. The low-low frequency gain of the circuit is calculated assuming I_B is ideal. The small-

Figure 22. Cherry Hooper amplifier basic circuit.



signal current generated by the drain of M1 flows through R_F, creating a voltage drop equal to $g_{m1}V_{in}R_F$. Thus,

$$V_{out} - g_{m1}V_{in}R_F = V_X. \tag{1.6}$$

By its part, the small-signal current produced by M2 $(= g_{m2}V_X)$ must flow through R_F:

$$g_{m2}(V_{out} - g_{m1}V_{in}R_F) = -g_{m1}V_{in}. \tag{1.7}$$

Then the voltage gain is given by:

$$\frac{V_{out}}{V_{in}} = g_{m1}R_F - \frac{g_{m1}}{g_{m2}}, \tag{1.8}$$

from this equation if $R_F >> {g_{m2}}^{-1}$, the voltage gain will be equal to the obtained using the common-source stage with a load resistance R_F.

The main advantage of the R_F modification is the resultant small-signal resistance seen at nodes X and Y. This resistance is ${g_{m2}}^{-1}$ for both nodes, a value typ-

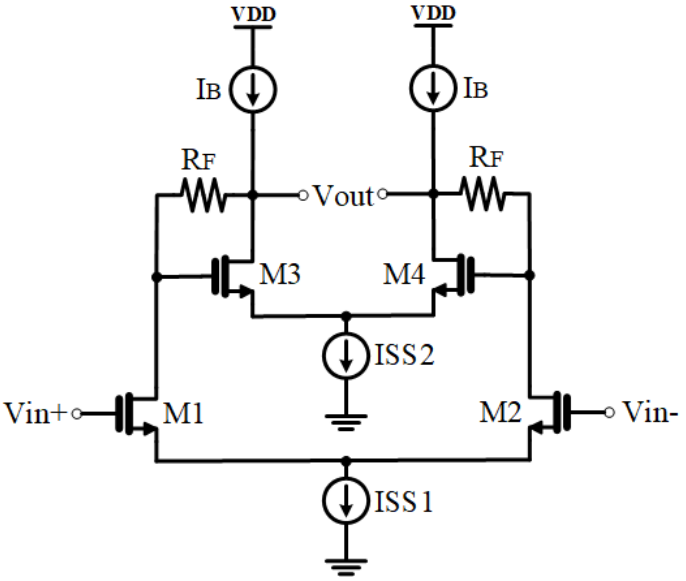
ically much less than R_F. Thus taking into account the capacitances at nodes X and Y, the pole frequencies are in the order of $w_{p,X} \approx g_{m2}/C_X$ and $w_{p,Y} \approx g_{m2}/C_Y$, which are located in frequencies higher than the poles obtained using the cascode common-source stage.

In summary, the Cherry-Hooper amplifier provides approximately the same voltage gain but with low resistance levels at nodes X and Y, moving the poles and extending the bandwidth of the circuit. Fig.23 shows the differential version of the Cherry-Hooper amplifier. The main drawback of this topology is the voltage headroom required to compensate the drop across the devices connected between VDD and GND.

1.3. CIRCUIT DESIGN METHODOLOGY

Fig.24 shows the design methodology proposed and implemented to obtain a favorable design that fulfills the requirements of USB *SuperSpeed* standard. The

Figure 23. Differential Cherry-Hooper amplifier with current-source loads.



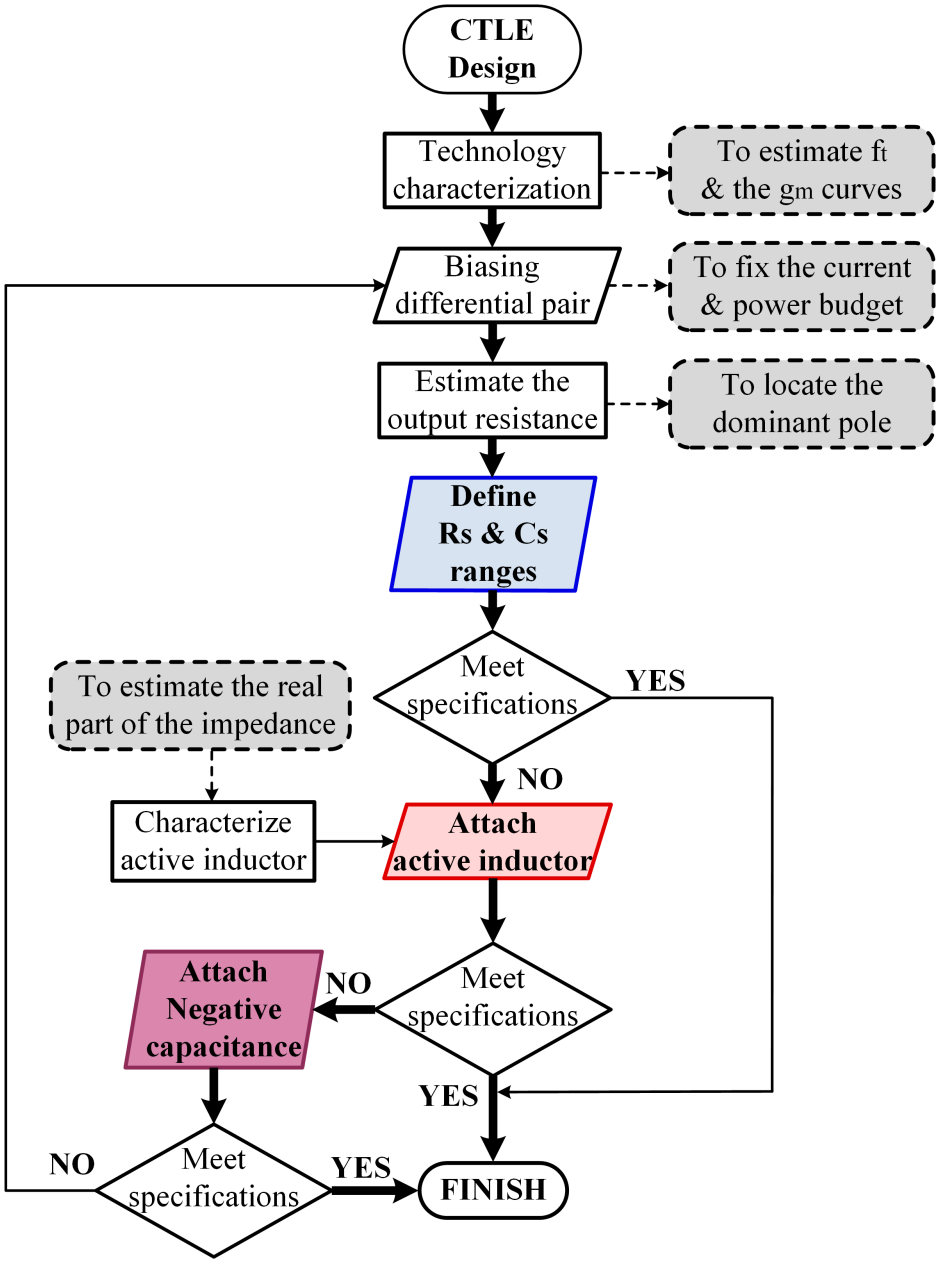
technology characterization is the first step in any CMOS design process. In this instance, design curves are used to obtain behaviors and parameters similar to the real ones. The curve that relates the transistor parameters gm and f_T allows obtaining an optimum biasing point of the transistors M_N that compound the input differential pair.

The RX equalizer architecture is implementation specific. However, the design guidelines suggest a second order continuous time filter transfer function which is correlated with a capacitive degenerated differential pair. This circuit was shown previously in Fig.9. The design of the equalizer starts biasing the input transistors in a suitable operation point. It is obtained through technology characterization. This first implementation allows making simulations to get an estimation of the resistance seen at the drain of the input transistor. The drain resistance and the load capacitor generates the pole ($R_D C_L$) at the output node.

As was mentioned in the description of the capacitive degeneration technique, the capacitor and resistor degenerating the differential pair produce a zero to counterbalance the output pole. Once the values of R_D and C_L are known is possible to determine values for the source capacitor (C_S) and resistor (R_S). These values establish the A_{LF} and peaking specifications and must be chosen in a range that allows obtaining the low-frequency gain range desired, and the position of the zero at which the frequency gain kicks in to amplify the frequency components of interest.

The addition of the capacitive degeneration produces a gain boosting according to the position of the introduced zero. Due to the technology restriction is not easy to realize considerable transconductance without the use of a large amount of current, making difficult to get gain in the Nyquist frequency of $2.5GHz$ especially for slow-corners process. Reaching the reduction of power consumption

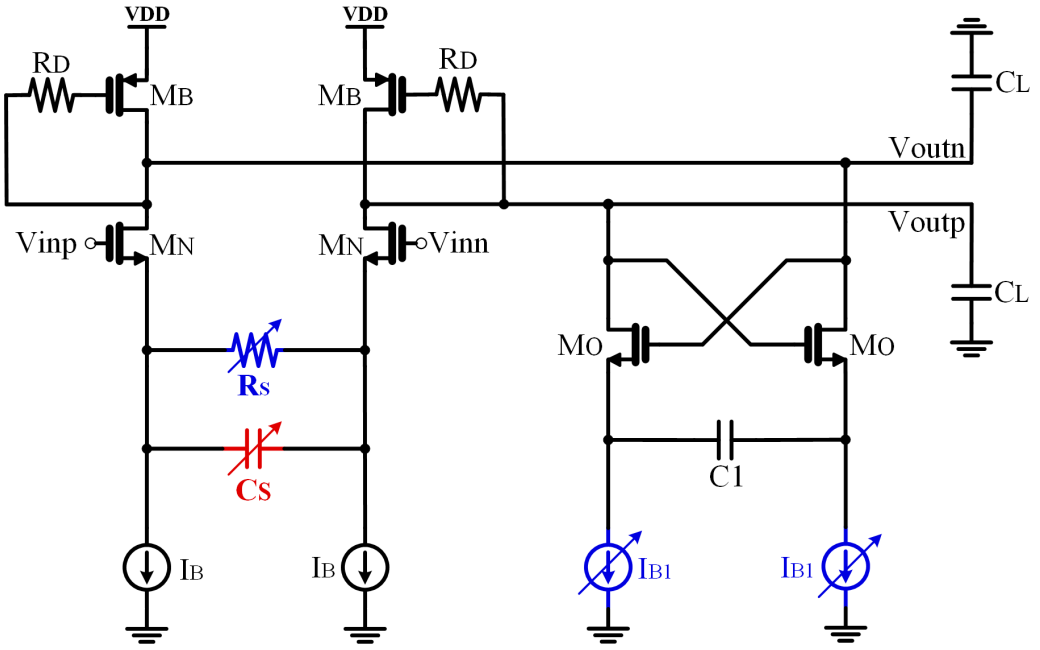
Figure 24. CTLE design methodology.



which is one of the main goals of modern high-speed interfaces, we implement additional broadband techniques to get the final design.

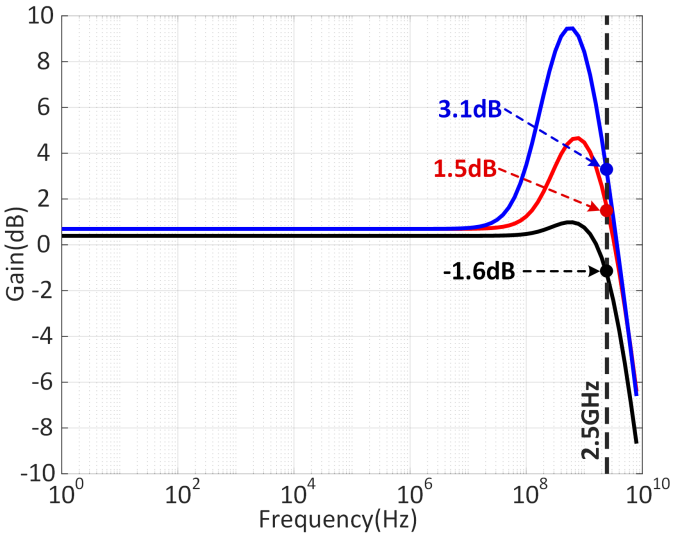
Fig.25 depicts the topology of the CTLE circuit designed in this research project. Three of the circuit techniques mentioned above are applied to achieve

Figure 25. Topology of the CTLE proposed.



compliance with the specifications. The already mentioned capacitive degeneration, the active inductor compound by R_D and transistors M_B, and finally, the negative capacitance cell is the cross-coupled pair of M_O and the capacitor $C1$. The active inductor was characterized separately and attached to the CTLE trying to get another zero in the position of interest. The main advantage of use PMOS based active inductor in this topology is the fact that no additional current is needed. Implementing the active inductor only critical corners does not get $A_{2.5GHz}$ specification. Two possible solutions were considered at this point: the implementation of an additional differential pair to contribute with the main transconductance and the negative capacitance. Running simulations for both options a better result was obtained for the negative capacitance case. Additionally, in the negative capacitance biasing current two bits were added for trimming, those bits are used in corners which do not require the full effect of negative capacitance.

Figure 26. Overview of the equalization function.



The design obtained using the proposed methodology is an adaptable CTLE with A_{LF} tunable using the eight bits to adjust the value of R_S and two bits for I_{B1}. The $A_{2.5GHz}$ value is varied using four bits to select different C_S. The amount of peaking could be adjusted using the combination of tuning possibilities.

1.4. SIMULATION RESULTS

The proposed CTLE circuit is designed using TSMC $0.18\mu m$ CMOS technology with a supply voltage of $1.8V$, and the operation is verified through circuit level simulations. For the testbench configuration, a pseudo-random number generator (PRBS) is used with a differential peak-to-peak voltage of $800mV$ and a frequency of $2.5GHz$ to emulate the output data signal of the transmitter. This signal is the input of the channel model depicted in Fig.7. The CTLE is connected at the output of the channel model block. The blocks for impedance adaptation and ESD protection was neglected.

Fig.26 depicts the equalization function for three different circuit configurations for the nominal process corners. Ideally, the gain boosting of the transfer function must be in the frequency of $2.5GHz$, but due to the speed limitation of the technology, the peak is gotten around $1GHz$. Despite this at the $2.5GHz$ frequency, the circuit still provides gain, making possible to perform the equalization function.

Fig.27 shows the A_{LF} variation for the nominal corner. It low-frequency gain can be modified shifting the bits assigned to select one of the eight possible resistor values of the bank. The values of each resistor branch were selected in order to get a linear and monolithic function of the low-frequency gain. The resistors implemented into the bank allow satisfying the A_{LF} specifications range for all the corners. In addition to the variation that can be done by switching the resistors, this range can also be modified by switching the current sources I_{B1} of the negative capacitance. As Fig.28 shows, three low-frequency gain ranges are obtained changing the current driven through the negative capacitance, it is use-

Figure 27. Low-frequency gain variation changing Rs for typical corner.

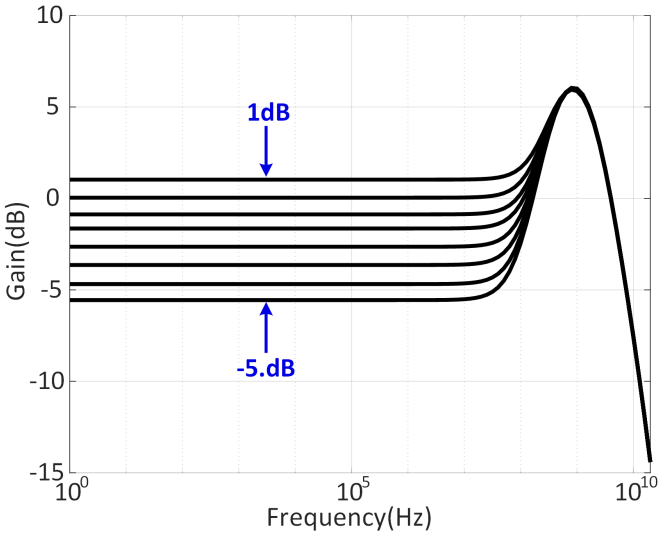
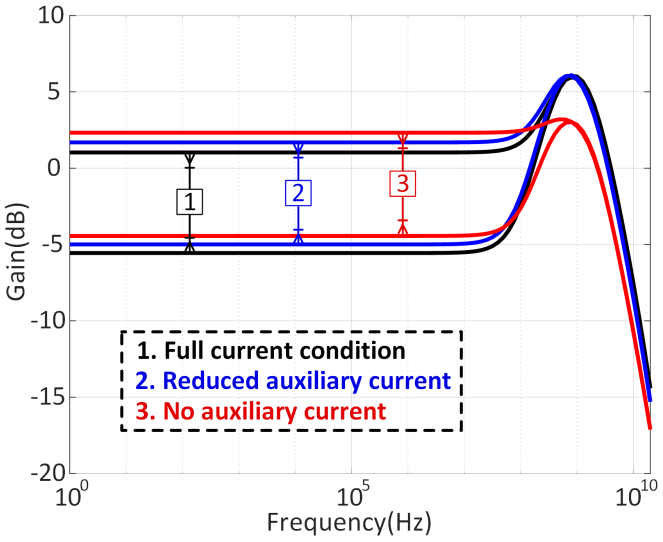


Figure 28. Low-frequency gain intervals for the three current conditions.



ful to cancel out the variation produced by the temperature resistors. Using the switching of the resistor bank and the current sources is obtained a swing range of $9dB$ for low-frequency gain.

The robustness of the circuit design was verified using simulations for process, voltage, and temperature corners variations. The fast and slow models of the semiconductor technology provided by the foundry were used for the process corners. The temperature varies between $-40°C$ to $125°C$ while for the voltage variation, it is assumed 10% of the nominal value. Fig.29 shows the equalizer frequency response for maximum peaking and flat response in best, typical, and worst corners cases. The worst corner case of high frequency boosting shown in Fig. 29a) occurs in the slow-slow process, low voltage, and high-temperature conditions. In this case, the mobility of current carriers is reduced, making difficult the current driving. However, even in the worst corner case, the $A_{2.5GHz}$ specification is accomplished with $2.2dB$ of gain.

Figure 29. Corners variations for the CTLE boosting and flat response.

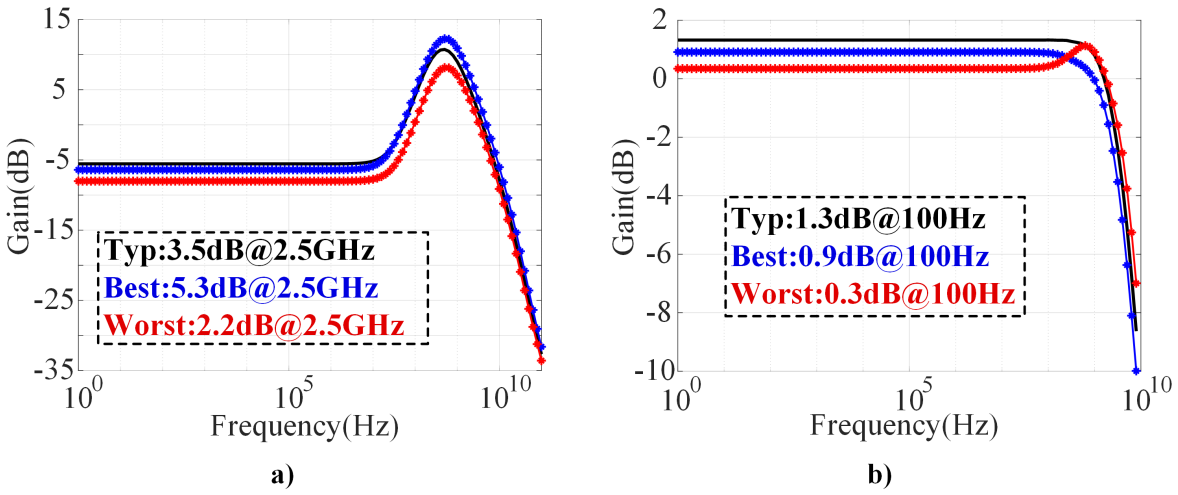
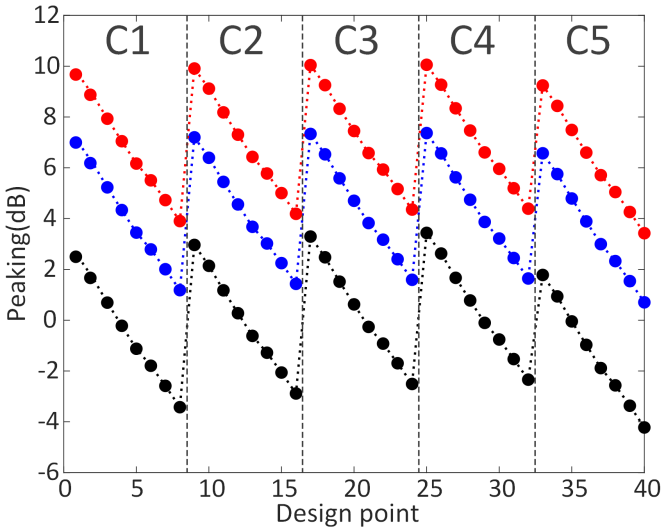


Figure 30. CTLE peaking values for all RC combinations.



The flat response is shown in Fig. 29b). It is achieved when R_S is in the minimum value. As was mentioned above, it is useful when the received signal does not require equalization, for example, if the received data signal oscillates at frequencies of previous versions of the USB standard ($60Mbit/s, 480Mbit/s$),

Table 3. CTLE performance results.

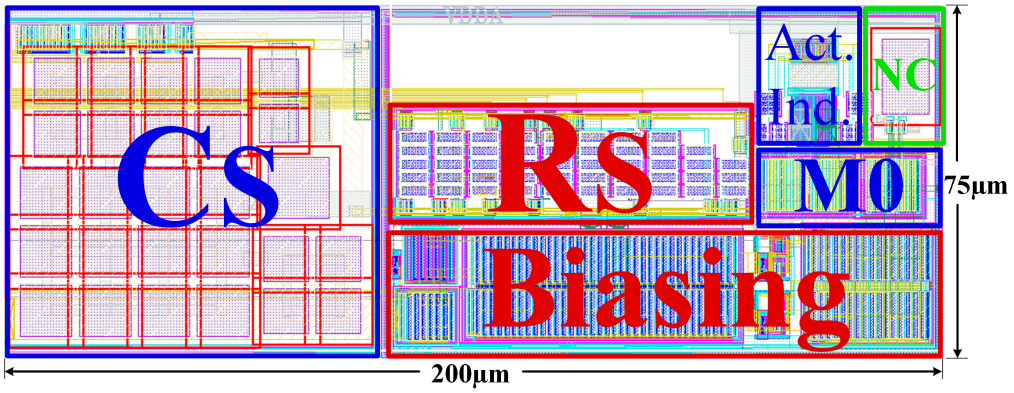
Reference	**This work**		(17)	(24)
Nyquist Frequency	2.5GHz		2.5GHz	2.7GHz
A_{NF}	-2dB to 5.4dB		11dB	-4dB to 18dB
A_{DC}	-5dB to 1dB		N/A	N/A
Peaking	-2dB to 7.2dB		11dB	-4dB to 18dB
Power Consumption	Full 11.7mW	Reduced 8.1mW	18mW	26mW
Area	0,015μm^2		N/A	0,12μm^2
Process	$0,18\mu m$		$0,18\mu m$	$0,13\mu m$

which, being low-frequency are not so much attenuated by the channel. The corners variation for A_{LF} gain is maximum $2dB$ and could be trimmed using the bits that fixes the R_S values.

The peaking is the difference between $A_{2.5GHz}$ and A_{LF} values. Combining the selection of $A_{2.5GHz}$ and A_{LF} different peaking values are obtained, which means the equalization function is realized. Fig.30 shows the peaking for all the bit selections of R_S, C_S, and I_{B1}. Five positions for capacitors, seven for resistors and three for I_{B1} give 120 possibilities of equalization which must be selected according to the conditions of the received signal and the whole interface. According to the design specifications, the peaking should be able to vary in a range of $0db$ to $2dB$. This specification is remarkably met, getting a circuit whit a wide peaking range from $-4dB$ to $10dB$.

The circuit design achieves all the specifications for the CTLE circuit established by the USB-IF. Compared to the area consumption of equalizers designed in similar CMOS technologies, the circuit has a remarkable performance. Additionally, the circuit offers the possibility of current reduction when such a large equalization is not required. Table 3 summarizes the performance results achieved with the designed CTLE.

Figure 31. CTLE layout design.



The design of the CTLE physical implementation is shown in Fig.31. It was performed in a professional circuit design tool. Short lengths for critical signal paths were used in order to maintain a low parasitic capacitance. The current mirrors are designed symmetrically aiming to get a non-variant biasing current. The resistors and capacitors are also matched to avoid variations.

2. A PROGRAMMABLE NAUTA GM-C FILTER FOR CHANNEL EMULATION

One of the leading sources of costs rising in the production of integrated circuits is the testing stage of prototypes. The validation of circuit designs requires skilled labor and expensive laboratory equipment. Moreover, due to statistical experiments, the characterization stage can take a long time, which contributes to increasing prototyping costs. However, previous research in testing of high-speed interfaces underestimates the possibility of on-chip integration of testing circuits to reduce the equipment or the human labor required to validate a prototype (43). This chapter presents a programmable Nauta Gm-C filter integrated into a circuit technique for the characterization of the eye diagram of high-speed circuits. The programmable filter enables the emulation of multiple channel environments, which contributes to reducing the need for various channels and allows to automate the circuit testing. The filter was embedded in a high-speed circuit characterization technique and integrated in a CMOS $0.13\mu m$ CMOS technology.

2.1. INTRODUCTION

The scaling of CMOS technology and implementation of broadband techniques had made possible increase the speed of many communications interfaces to the order of GHz. This technology scaling also has incremented the sensitivity of integrated circuits to PVT variations. Due to this sensitivity, the testing and debugging of high-speed circuits has become critical for the circuit validation (44). This testing of the high-speed circuits is a challenge due to the implications of signal integrity and parasitic loads that can be affected even for minor perturbations added by the test equipment. Therefore, the characterization of high-speed

circuits requires elaborated test benches to warrant the operation of the circuits (45).

The design of structured tests, especially for mass production chips, is limited by some technological and economic factors. The equipment required for the characterization of high-speed interfaces must have a larger bandwidth than the device under test (DUT). Additionally, this equipment needs to be updated to faster and more expensive versions to support ever-increasing interfaces speeds(46). On the other hand, minor perturbations in the test can introduce erroneous results causing issues in the characterization. These results can cause loss of information and data corrupting in high-speed links when the DUT is operating with the whole system.

To prevent the loss of information and recover the signal successfully is possible to integrate into on-chip circuits for the built-in test. In the testing of analog circuits, the built-in test blocks can perform part of the characterization allowing digitize the characterization signals. This partial processing avoids the requirements of output pins and expensive equipment.

Here, it is presented a Gm-C filter embedded in a circuit characterization technique for the eye diagram of high-speed circuits. This technique allows characterizing the analog front-end using the comparator for sampling the data signal. The programmable Gm-C filter allows emulating the frequency response of multiple transmission lines. The programmable filter enables to script probes for different channel losses.

2.2. TEST PLATFORM FOR HIGH-SPEED INTERFACES.

The eye-height and jitter comprise the two main measurements required to build the eye diagram. The jitter is the deviation of a timing event of a signal from its

ideal position in time. Data errors result when this deviation extends past the sampling point at the receiver. The eye-height corresponds to the amplitude voltage margin of the for logic high and logic low while running at speed. The measurements strategies aim to detect the edges of the eye diagram at the output of the DUT. This characterization is performed by the time-margining test techniques that look for the timing specification, and voltage-margining techniques that target eye-height measurement.

We implement a characterization technique that allows constructing eye diagram through a dynamic location of the sampling point of the DUT (47). The comparator under-test provides a unique voltage comparison level and sampling instant, which is not enough to build the eye diagram. Therefore, we propose to shift the sampling point location along the x-axis (time) and y-axis (voltage amplitude) of the eye diagram, as Fig.32 shows. While we shift the sampling point location, the bit-error-rate calculation is employed to determine if the current sampling point is in an open or closed region of the eye diagram.

Fig.33 shows the test platform used to perform the eye diagram characteri-

Figure 32. Concept of eye diagram characterization using voltage and phase shifting.

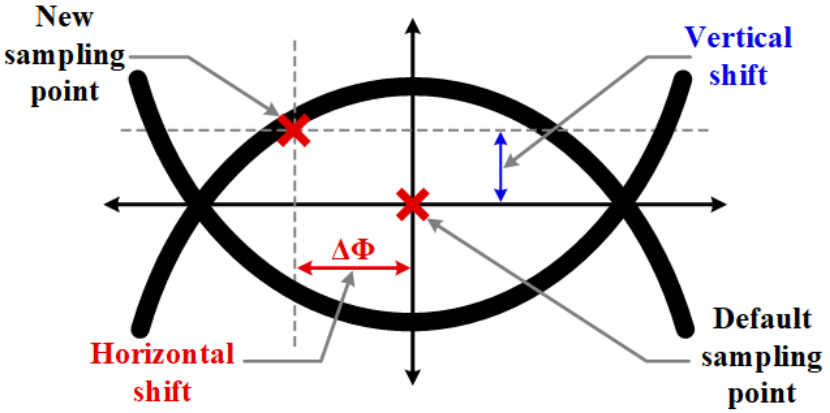
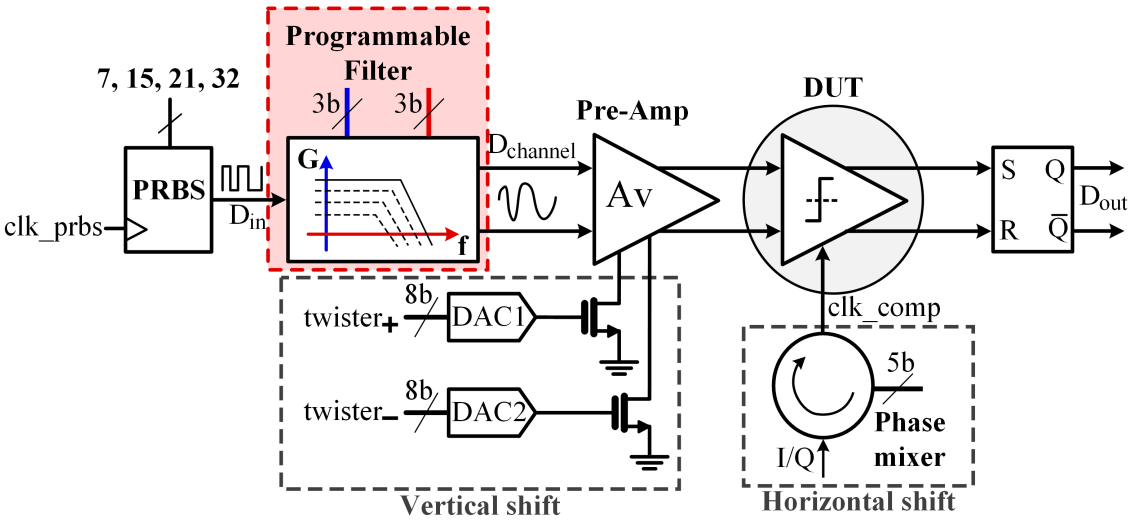


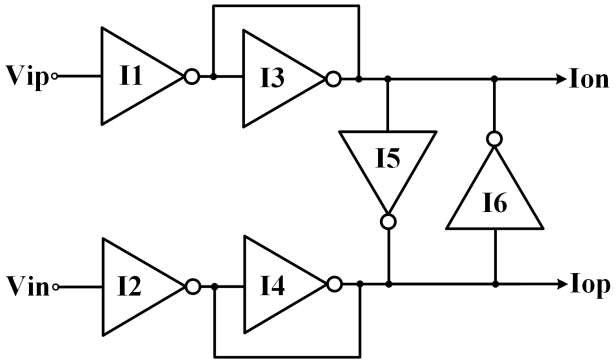
Figure 33. Eye diagram characterization technique.



zation. The horizontal shift location of the sampling point is done using a phase mixer. The clock phase of the comparator is shifted with the PRBS clock, and then it is possible to sample the eye diagram in multiple time points. On the otter hand, we measure the voltage margin manipulating the voltage offset of the pre-amplifier. The digital-to-analog converters (DAC1 and DAC2) vary the branch current of the differential pre-amplifier. This variation induces offset voltage in both vertical directions of the eye diagram. Using a pass rate based BER of 10^{-5}, we determine if the sampling point is in the eye diagram open region.

To complete the test platform, we add two blocks to emulate the transmitter and the channel of the high-speed interface. A programmable PRBS generator provides the digital signal considered like the information. It can be configured to generate 7, 15, 21, and 32 data frames. Programmable filter emulates the transmission channel because it is not easy to get multiple transmission lines that provide channels with different frequency response. The filter can be varied in frequency and gain to provide different values of attenuation and bandwidth. Finally, we do and off-chip calculation of the BER at the output of the test platform.

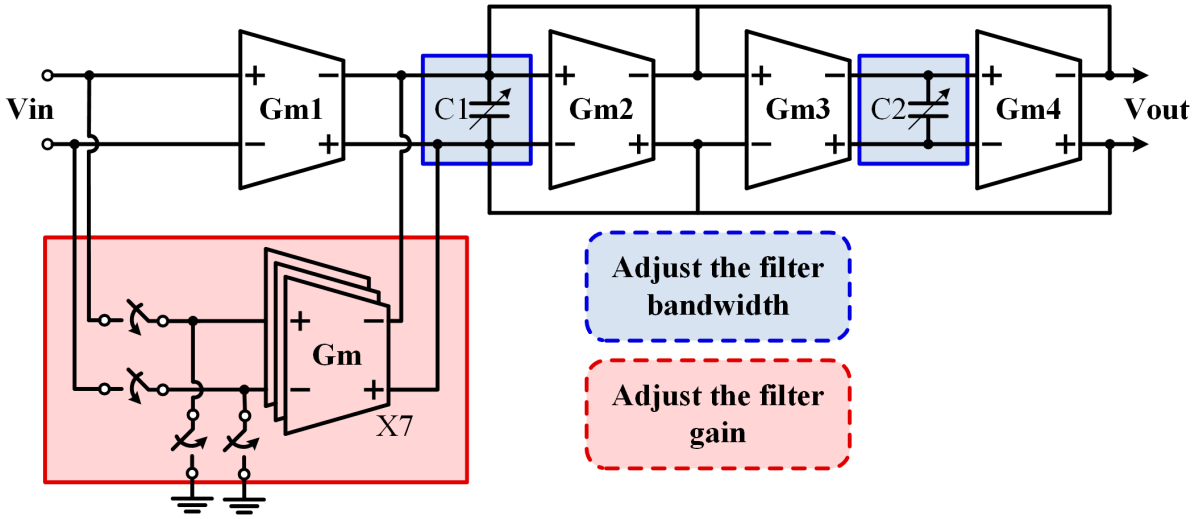
Figure 34. Nauta operational transconductance amplifier (48).



2.3. GM-C FILTER TUNABLE FILTER USING NAUTA OTA.

Gm-C filters are a widespread continuous time circuit composed by a transconductance and a capacitance. The critical component of a Gm-C filter is the operational transconductance (OTA). The voltage-to-current conversion is the primary function of the OTA. This OTA integrated with a capacitance composes the integrator, the basic function of a Gm-C filter. The transconductance and the capacitance can be adjusted to modify the frequency characteristic of the filter. In this work, the Nauta transconductance is applied because of its simple architecture

Figure 35. Programmable Biquad Gm-C filter topology.



and stability against PVT variations.

The Nauta transconductance architecture is shown in Fig.34. This transconductance is comprised of six CMOS inverters. I1 and I2 act as the differential voltage-to-current converters. Using the I-V characteristic of the transistor, the differential gain of the transconductance can be expressed as:

$$\frac{I_{od}}{Vid} = \frac{I_p - I_n}{V_p - V_n} = (VDD - V_{thn} + V_{thp})\sqrt{\beta_n \cdot \beta_p} \tag{2.1}$$

where VDD is the supply voltage, V_{thn} and V_{thp} the threshold voltages of the NMOS and PMOS transistors respectively and β_n, p the relation of the process parameters and sizes of the transistors. To perform a linear operation, the β factors of n-channel and p-channel transistors are perfectly matched. I3, I4, I5, and I6 helps in common-mode stability and boost the differential mode gain (48).

The Biquad Gm-C filter is a circuit with advantages such as simplicity, modularity, and tunability. Fig.35 shows the circuit topology (49). The DC gain (A_o) and the cutoff frequency (w_o) can be expressed as:

$$A_o = \frac{Gm1}{Gm4} \qquad w_o = \sqrt{\frac{Gm3 \cdot Gm4}{C1 \cdot C2}}. \tag{2.2}$$

Due to the dependence of the filter gain to the transconductances $Gm1$ and $Gm4$, it is possible to adjust the filter gain modifying one of these transconductances. The transconductances Gm are added in parallel to $Gm1$ to perform the voltage gain adaptation. These transconductances can be switched to increase or decrease the total transconductance according to the gain required by the application. Meanwhile, the cutoff frequency can also be modified changing the capacitances C1 and C2, according to 2.2 . Hence, the capacitances are integrated using a matrix of capacitors. These capacitors can be switched to adjust

the cutoff frequency of the Gm-C filter.

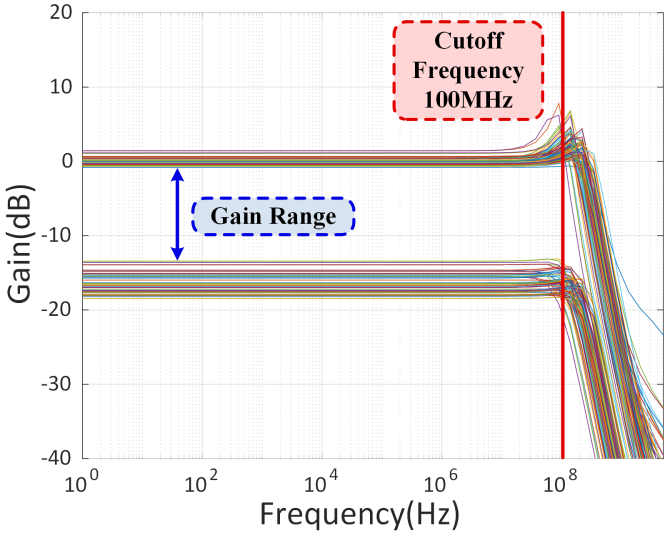
2.4. RESULTS

The test platform was implemented using a TSMC $0.13\mu m$ CMOS technology with a supply voltage of $1.2V$. The Biquad filter is embedded in the test platform. Thus, the filter was simulated as a standalone circuit instance to get the tuning curves for cutoff frequency and voltage gain.

Fig.36 shows the PVT corners results for the maximum and minimum gain when the cutoff frequency is set in the minimum value of $100MHz$. The filter gain has a tuning range of $15dB$ switching the transconductance Gm. The filter has a good behavior against PVT variations with a maximum gain variation of $3dB$.

The results for the maximum cutoff frequency are shown in Fig.37. Using the same transconductance the circuit performs the same range for gain, but the selection of a different capacitance enhances the bandwidth. The maximum filter

Figure 36. PVT corners variation for the maximum bandwidth and gain.



cutoff frequency obtained switching the capacitances C1 and C2 is $1GHz$.

The two degrees of freedom obtained with the circuit design allows emulating a variety of transmission lines. Because the switching of transconductances and capacitances can be programmed, the filter enables the possibility of program different test benches using a variety of emulated channel losses. This programmable filter contributes to facilitating the test-ability of high-speed circuits.

The total power consumption is $120\mu W$ with $1.2V$ supply voltage in the typical corner case. This power consumption includes the transconductances and the digital circuitry integrated for circuit tuning.

Fig.38 shows the microphotograph of the characterization technique and the Gm-C filter. The total area of the circuit is $400x150\mu m$ including two banks of capacitors.

Figure 37. PVT corners variation for the maximum bandwidth and minimum gain.

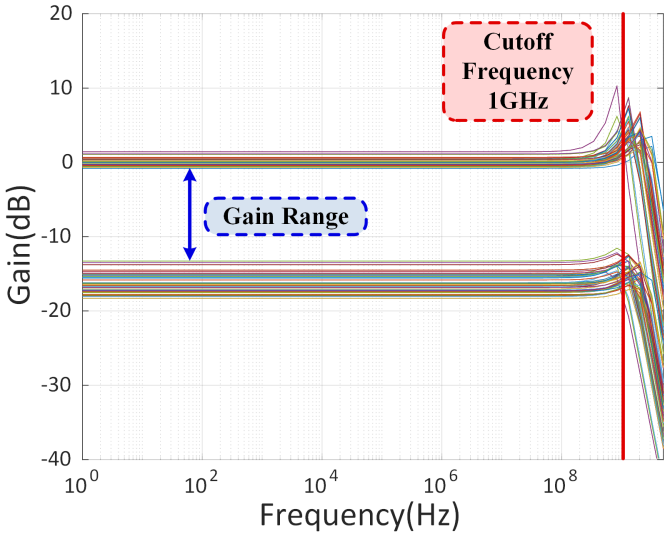
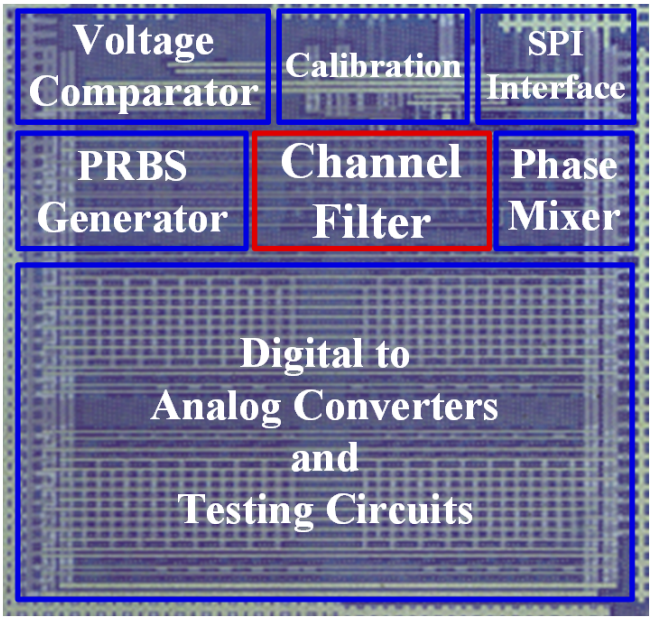


Figure 38. Microphotograph of the low-pass filter integrated in the characterization technique.



3. ON THE DESIGN OF RELIABLE CURRENT REFERENCES FOR HIGH-ACCURACY APPLICATIONS

Reference circuits to provide reference voltages or currents are essential SoC circuits that integrate analog and mixed-signal blocks. Current references are preferred than voltage references in large integrated circuits because they are not affected by the IR drop that occurs when a voltage is transferred across a metal line. A current reference circuit provides bias current for different analog blocks such as operational amplifiers, equalizers, filters, analog buffers, and data converters. The performance of these circuits is proportionally affected by the accuracy and stability of their bias current (50). Thus, stable analog circuit applications require a high-precision current with temperature, power supply, and process independent operation. The works reported in the literature provides many topologies to generate the desired current. However, those works neglect to consider the cost of the implementation of a current reference in a future electronic product. This chapter proposes a straightforward circuit technique to reduce the costs caused by human labor when the number of analog peripherals is augmented requiring additional current references. The technique is based on adjusting the physical implementation to reduce the time of re-design. The technique was applied in two circuit designs integrated into a $0.18\mu m$ CMOS technology and measured results show an error of less than 1%.

3.1. INTRODUCTION

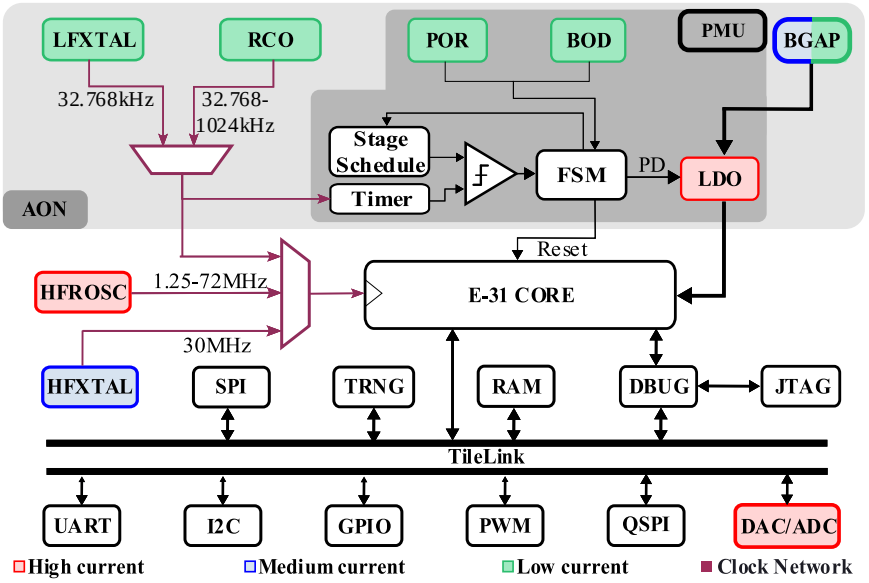
A regular strategy to save power consumption in system-on-chip (SoC) applications resides in reducing the biasing current of the circuit blocks during some

power modes. This approach leads to a trade-off between power and performance in the system, which is commonly addressed by implementing multiple power domains within the SoC. Multi-domain schemes allow suitably biasing low-performance circuits without impacting negatively on blocks with high-yield requirements.

The accuracy of the current-reference implemented in each power domain of an SoC has a decisive role in the whole system yield. Fig. 39 illustrates an SoC implementation with three different power/current domains. The low-current domain comprises watchdog timers and wake-up analog elements that generally are always on (AON) operating in deep-sleep power modes. AON blocks must operate with the minimum current when the system enters into an energy saving mode. On the other hand, when the system is processing or transferring data, blocks such as low-noise amplifiers, data converters, oscillators, and filters might be on, demanding higher currents to satisfy the required error-rate, speed or accuracy.

SoC applications with multiple current domains require discussing the specifications and the most appropriate architecture to implement the biasing sources of each domain. Due to the impact of the reference current on the circuit performance, high-accuracy and reliability all over a wide temperature and supply voltage range(51) become a priority. Additionally, the current-reference circuit must accomplish the biasing current requirements depending on the target power domain or application. In this work, we discuss some practical principles and design concepts to select a suitable current reference topology for each power domain. Focusing on high-accuracy applications, we also explain an effective cascode-configuration strategy to enhance the traditional voltage-to-current converter precision without affecting the circuit stability. The employment of a com-

Figure 39. Overview of an SoC with current domains association.



pensation network guarantees a circuit phase margin of 68°. Post-silicon and simulation measurements reveal an error $< 1\%$ in the current value and a robust PSRR of 80dB at 100MHz all over the industrial range of voltage and temperature variations.

3.2. CURRENT REFERENCE DESIGN CONSIDERATIONS

The diverse application environments for SoCs produce heterogeneous specifications for current-reference sources. Systems with multiple power domains require the implementation of specific current-reference values by domain, as Fig. 39 illustrates. The proper selection of the current-reference circuit for an SoC application is essential due to the impact of the biasing current on the precision of analog circuitry and power consumption of the whole system. The current-reference design must guarantee less power consumption than the biased circuits. For instance, in SoCs with multiple power modes such as active, sleep, and

Figure 40. Conventional approach of a PTAT-CTAT subtraction-based current reference source.

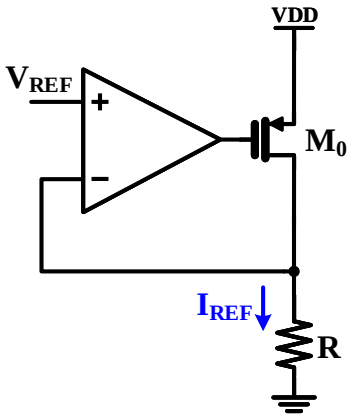
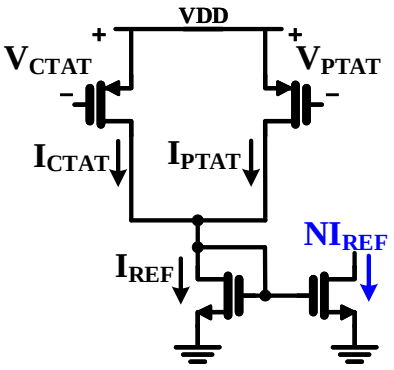


Figure 41. Conventional approach of a voltage-reference-based current reference source.



deep sleep modes, there is a requirement for current-references for each current domain or an adjustment method to achieve the power demands of the operating states. Additionally, these current-references should be insensitive to supply voltage, temperature, and process variations (PVT).

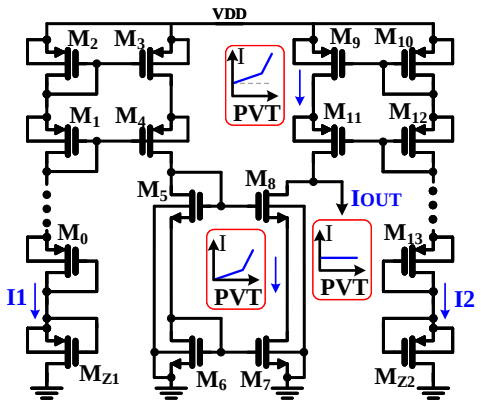
The specifications of the current-reference circuit are established according to the operating requirements of the system. When the application demands high-speed or precision performance, the circuits are power-hungry to achieve a broad bandwidth, low noise, and reduced error. In contrast, restricted energy

applications should maintain a low-power consumption, forcing the analog circuits to operate with biasing currents in the order of nano-amperes. This variety of power consumption environments implies different design considerations for current-reference circuits, which may be addressed in two domains: nano-ampere and micro-ampere.

3.2.1. Nano-Ampere Domain The voltage-reference-based current (VRBC) source of Fig. 40 results impractical in the nano-ampere domain. To produce a nano-ampere current, the resistance required to define the current-reference value must be extremely large, increasing the whole circuit area. Although some implementations use the transistor leakage to construct resistor-less current-references, these circuits require fine adjustment due to the strong temperature dependence on tunneling currents (52; 53). On the other hand, when the reference resistance is outside the chip, the minimum current-reference value is restricted by the electrostatic discharge protection (ESD) circuit. The ESD diodes integrated into the die pad suffer from leakage current. If the leakage currents magnitude is similar to the reference current I_{REF} value, it is difficult to design a precise reference current. Due to this constraint, circuit topologies without resistance may be more appropriate for the nano-ampere domain.

The implementation of nano-ampere current-references using only MOS devices becomes a challenge considering compensation of temperature and supply voltage variations. Since transistors must operate in the sub-threshold region to achieve low current, their exponential behavior amplifies any small temperature variation. Santamaria et al. (54) present some solutions to construct resistor-less nano-ampere current-references by compensating the proportional-to-absolute-temperature (PTAT) and complementary-to-absolute-temperature (CTAT) current

Figure 42. Nano-ampere current reference with PTAT-CTAT subtraction approach (54).

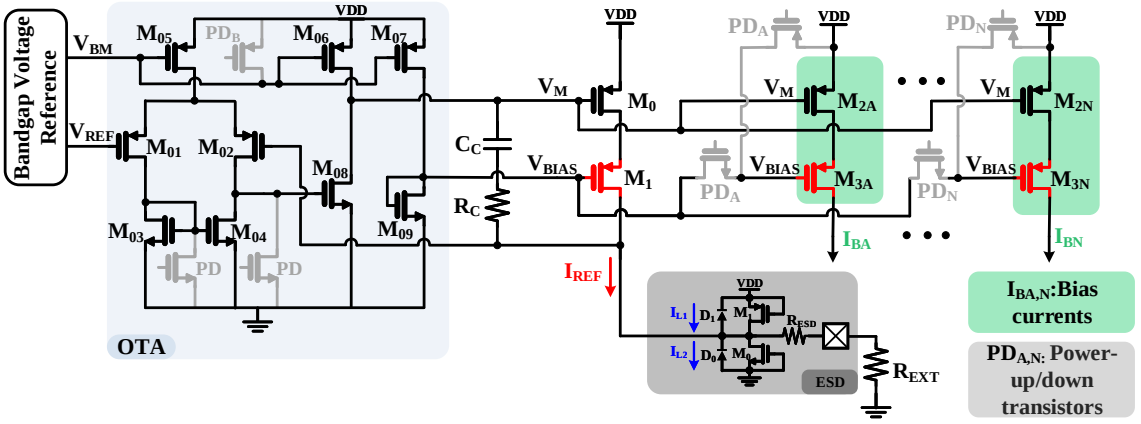


behaviors. The mentioned work introduces three nano-ampere current-reference topologies based on synthesizing a CTAT source-gate voltage required to balance the PTAT behavior of the pMOS drain sub-threshold current.

Fig. 42 presents one of the nano-ampere current-references proposed in (54). The depicted topology voids the current-reference value dependence on PVT variations through a current subtraction scheme. Handling the size and number of diode-connected transistors, it is possible to generate two scaled currents (I_1 and I_2) with similar PVT behavior. The proposed circuit allows subtracting these two currents to generate a current-reference value independent on PVT variations. This qualitative analysis of the current-source advantages is confirmed by the authors, who report a temperature coefficient of 182ppm/°C all over the industrial temperature range for the mean current-reference value of 2.7nA.

3.2.2. Micro-Ampere Domain Current references in the micro-ampere domain are useful for biasing of circuits with high precision, low noise, or speed requirements. Increasing the current-reference value allows implementing circuits with enhanced accuracy under PVT variations. Two common circuit concepts are

Figure 43. Topology of the current reference with the addition of the cascode transistor.



used in the generation of micro-ampere current-references. The first one is the use of a temperature-compensated voltage reference, such as a bandgap, combined with resistances as current defining devices, as shown in Fig. 40 (51; 55). The second principle works with the inverse dependence on temperature of the threshold voltage and carrier mobility. The balance of this relation produces an invariant to absolute temperature (ZTAT) current-reference as Fig. 41 depicts. In the micro-ampere domain, the current-reference based on the voltage-to-current converter results more attractive due to its high accuracy, smooth implementation, and scalable nature.

A relevant consideration in the design of the VRBC source is related to the required resistance and the voltage reference. If we use the bandgap voltage as the voltage reference, a large resistor (tens of kilo-ohms) is necessary to obtain a current-reference of hundreds of micro-amperes. The on-chip implementation of large resistances implies more area occupied, becoming impractical in area-constrained systems. To replace this resistance, some authors proposed the use of transistors operating in the triode region or switched capacitors (51; 55). However, these implementations entail larger current errors caused by PVT variations,

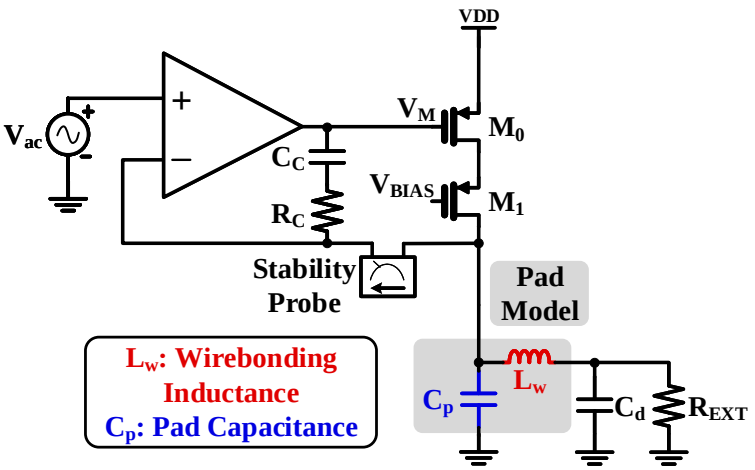
requiring extra circuitry to adjust the current-reference which increases the power consumption.

3.2.3. High-precision Voltage-Reference-to-Current Source The implementation of current-references using the voltage-to-current converter along with external resistance avoids the area constraints of its integrated resistance counterpart. However, the external resistance approach makes the current-reference accuracy dependent on resistance precision. This drawback is more representative in applications that require a few micro-ampere currents because the resistance value should be higher, i.e., more inaccurate. Furthermore, as high-precision resistances are more expensive, their use increases the cost of the system implementation. Nonetheless, as the external resistance does not suffer from variations caused by process and temperature, it is still useful in current-reference implementations.

The accuracy of the external-resistor current-reference can be improved by using a cascode transistor. As Fig. 43 highlights in red, transistor M_1 is placed in cascode configuration with M_0. This architecture modification increases the output impedance of the current-reference, enhancing the precision of the current-reference I_{REF} and the PSRR bandwidth. However, the cascode transistor also makes the feedback loop more prone to instability.

Fig. 44 shows the stability scheme employed to compensate for the effect of the described cascode configuration. The conventional implementation of Miller compensation splits the poles of each circuit node and also produces a right-half-plane zero (RHPZ). If this RHPZ is close to the frequency of unity gain bandwidth, it may cause a phase shift and consequently, loop instability. A resistor is placed in series to the compensation capacitance to counteract the effect of the RHPZ

Figure 44. Circuit scheme for the current source stability analysis.



(56).

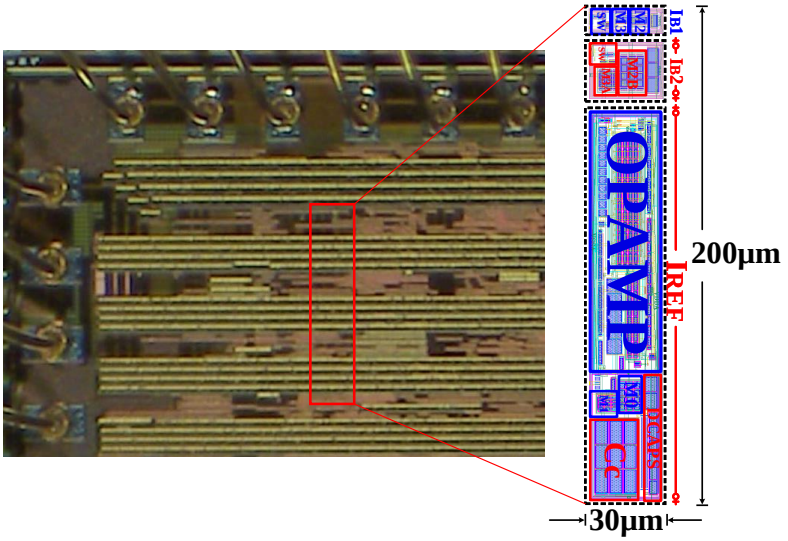
3.3. EXPERIMENTAL RESULTS

Circuit blocks such as buffers for data converters, clock/data recovery circuits, and equalizers schemes for high-speed interfaces, require high-precision and broad-bandwidth response current-references for their correct operation. As these requirements entail a high-current biasing, we designed the VRBC source of Fig. 43, to generate currents in the micro-ampere domain looking for high-accuracy against supply voltage variations. The VRBC source was fabricated in a 0.18μm CMOS standard process with a nominal supply voltage of 3.3V. Fig. 45 presents a partial microphotograph of the SoC along with the detailed layout view of the designed current-reference. The total area occupied by the current-reference, including two current mirrors (I_{B1} and I_{BN}), is 200μm$\times$30μm.

Seeking to endorse the design considerations and concepts discussed in the present work, we carried out Monte Carlo* and PVT corners† simulations on the

*Performed with both process and mismatch variations, using a random sampling method.
†Process, voltage and temperature (PVT) corner simulations, using the following order: Pro-

Figure 45. Microphotograph of the current-reference in use within a SoC.



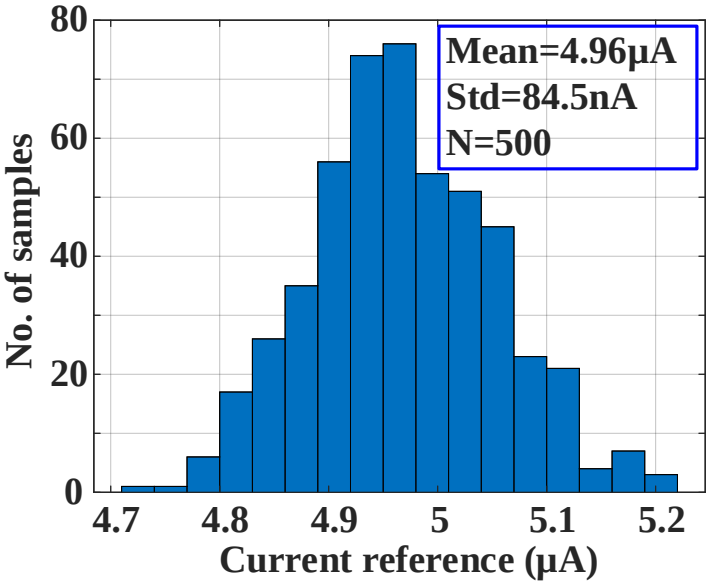
designed current-reference. Regarding the PVT testing setup, the supply voltage varies $\pm 10\%$ from the nominal value and temperature ranges from -40$^{\circ}C$ to 125$^{\circ}C$. We design the circuit assuming an external resistor of 255$k\Omega$ with a maximum tolerance of 1%. This R_{EXT} was selected aiming to obtain a reference current where the variations caused by the leakage current ($I_{L1,2}$) of the ESD diodes becomes negligible. The voltage reference depicted in Fig. 43 is 1.26V and it comes from a bandgap circuit integrated into the same SoC, whose maximum voltage error is 2%.

Fig. 46 summarizes the results of Monte Carlo simulations for process and mismatch. Over 500 samples, the mean current-reference value results in roughly 5μA. The standard deviation on I_{REF} is 84.5nA, which represents a dispersion of $\pm 0.85\%$ from the average current value. These results disclose a robust performance and reliability against random variations.

As stated in previous sections, adding the cascode transistor M_1 highlighted

cess NMOS - Process PMOS - Supply Voltage - Temperature; i.e., TTNN indicates Typical - Typical - Nominal - Nominal.

Figure 46. Monte Carlo results for the current-reference of $5\mu A$.



in Fig. 43 enhances the current-reference accuracy, but impacts on the circuit stability. Thus, we tested the compensation network (combination of R_C and C_C) effect through stability simulations on the current source feedback loop. Fig. 47 depicts the gain and phase frequency response of the feedback loop including the pad capacitance and the wire bond impedance. This figure also demonstrates robust circuit stability through a phase margin of $68°$ at a unity gain frequency of 398kHz. The power-supply rejection ratio (PSRR), defined in the present application as the rejection factor of the output current variation against supply voltage variation, reaches 140dB at 10kHz and 80dB at 110MHz, as shown in Fig. 48. The cascode transistor M_1 inclusion makes the circuit suitable for applications with high PSRR requirements. Clock data recovery circuits are an application example, since the variations of the reference current produce jitter issues.

Post-silicon measurements endorse the concepts and design considerations presented in this work. We tested the fabricated current source by ranging tem-

Figure 47. Frequency response analysis of the implemented current-reference: loop feedback stability analysis.

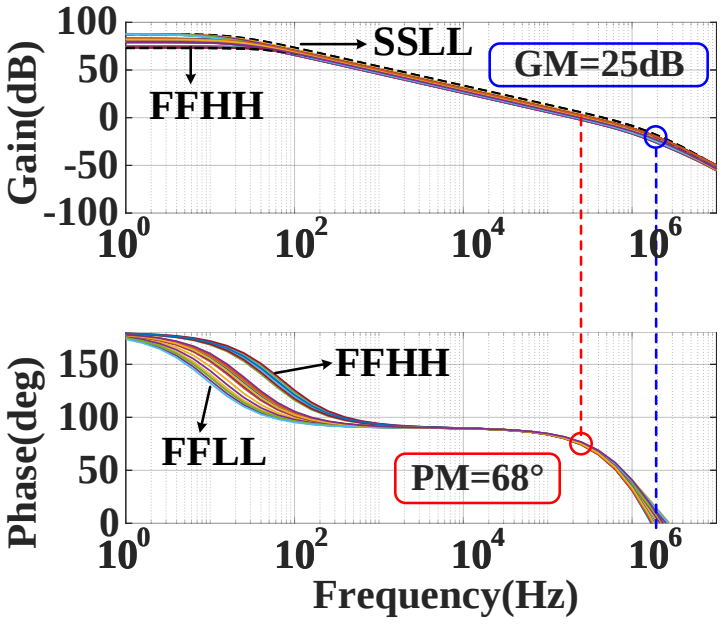


Figure 48. Frequency response analysis of the implemented current-reference: power supply rejection ratio.

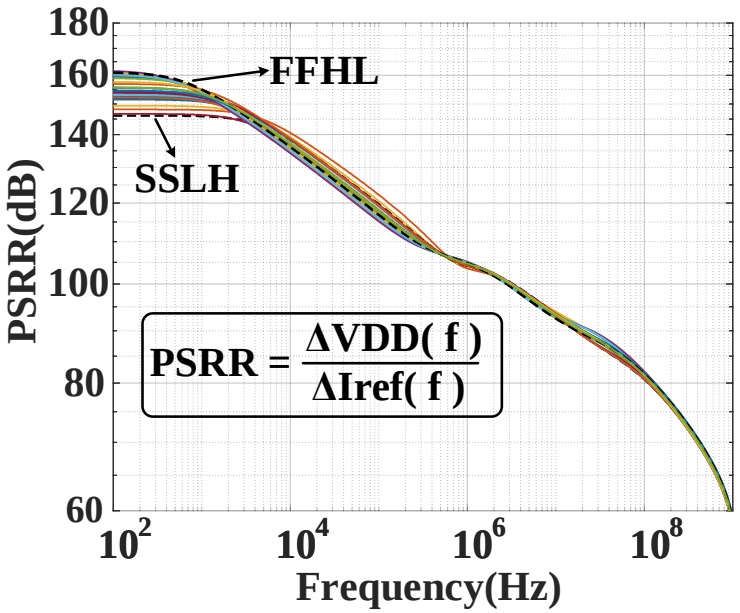


Figure 49. Measured $5\mu A$ current-reference sensitivity: temperature sensitivity.

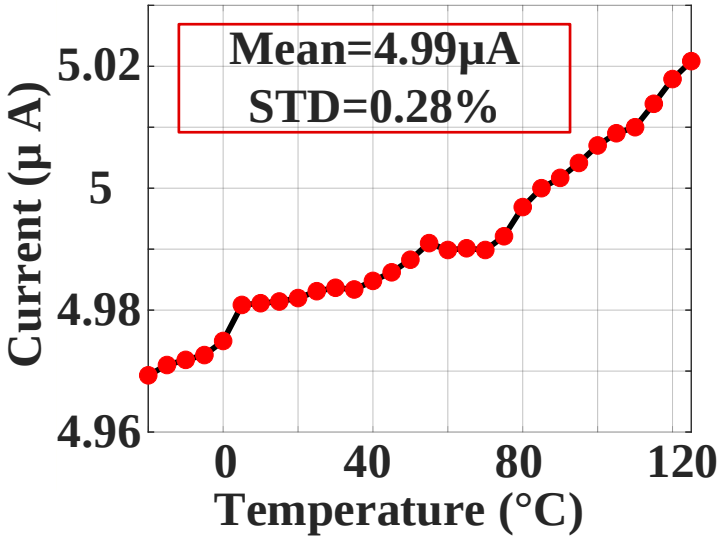
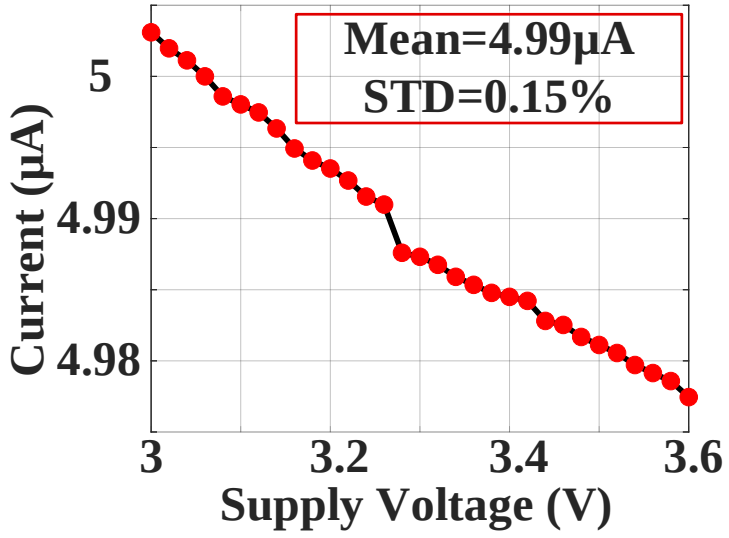


Figure 50. Measured $5\mu A$ current-reference sensitivity: supply voltage sensitivity.



perature and supply voltage over -20$^{\circ}C$ to 125$^{\circ}C$ and 3V to 3.6V, respectively. The I_{REF} current values are extracted from the voltage drop across the external resistance. Fig. 49 shows the experimental results and leads to a temperature coefficient calculation of 1178$ppm/^{\circ}C$. The circuit also exposes a robust performance against supply voltage fluctuations, achieving an error lower than 1% for a maximum supply variation of $\pm 10\%$ from the nominal value, as reported in Fig. 50.

3.4. CCONCLUSION

In this work, a review of practical current-references selection criteria and design considerations depending on the target power domain is presented. As traditional current references ensure high accuracy and reliability, they are still implemented in SoC applications. Therefore, we discuss relevant design considerations to optimize the performance of conventional bandgap-based current reference in high-accuracy and large PSRR applications. Post-silicon, PVT and Monte Carlo results validate our design by disclosing a $< 1\%$ error in the current value, a PSRR of 80dB at 100MHz and a phase margin of 68°.

4. SUMMARY OF CONTRIBUTIONS AND CONCLUSIONS

This chapter describes the summary of the contributions made by this research work and how the research work opens the doors to new ideas of research and development. The summary presents the main conclusions of each of the circuits developed into this research project. The contributions section presents a review of scientific divulgation articles, presentations, and undergraduate projects related to this research work. Finally, the future work presents some ideas to continue with the development of the low-cost circuit blocks for a high-speed interface.

4.1. SUMMARY

We present three circuit employed in different blocks of high-speed interfaces. These circuits are integrated in a $0,18\mu m$ CMOS technology. A summary of the circuits developed along this research project is listed below:

- We present the design of a CTLE for USB3.0 standard in a $0,18\mu m$ CMOS technology. The circuit consumes a total current of $6.5mA$ and occupies and area of $0,15mm^2$. Power and area results show a good performance even with CTLEs designed in more advanced technology nodes. Additionally, we present a comparative study of the state of the art circuit techniques employed in high-speed linear equalizers.

- We present a configurable Gm-C filter to emulate the channel response of transmission lines. It circuit allows to program the bandwidth and attenuation of its frequency response. This configuration allow to emulate different cases of channel losses that could be presented in a high-speed link. The

filter is integrated in a test platform that can perform the eye diagram construction for the characterization of high-speed interfaces samplers.

- We present a modular bandgap-based bias current source for circuits that require currents in the order of μAs. The currents provided by the source have a precision of 1% in a temperature range from $-40°C$ to $125°C$. A remarkable characteristic of the source that we propose is its modular integration which allow to integrate the number of required bias currents only placing a new module in the layout. It avoids a lot of rountig work on the integration flow.

4.2. CONTRIBUTIONS

Publishing is an important measure in academia and an imperative way to contribute to the public knowledge. In this chapter, published works related to this microcontroller are shown. Published articles will be listed in section 4.2.1 and presentations deeply related with the circuits designed in this research work in section 4.2.2.

4.2.1. Related articles

- **A System-on-Chip Platform for the Internet of Things featuring a 32-bit RISC-V based Microcontroller** (LASCAS 2017) (57)

  Ckristian Duran, Luis E. Rueda G., Andres Amaya, **Rolando Torres**, Javier Ardila, Luis Rueda D., Giovanny Castillo, Anderson Agudelo, Camilo Rojas, Luis Chaparro, Harry Hurtado, Juan Romero, Wilmer Ramirez, Hector Gomez, Hugo Hernandez and Elkim Roa

A tested and measured 32-bit microcontroller used as an open-source platform for Internet of Things was presented in this paper. This paper was published as the first silicon-proven 32-bit microcontroller sporting a RISC-V core. A brief description about the implemented system was shown, along with reports of the implemented SoC such as area, real measurements of power consumption and maximum frequency. It is shown that the use of AXI-4 lite bus for communication considers the possible implementation of accelerators for specialized applications. This paper was presented and published by 2017 IEEE 8th Latin American Symposium on Circuits & Systems (LASCAS).

- **On the Design of Reliable Current References for High-Accuracy Applications** (Submitted: ICECS2019)

  Rolando Torres, Nestor Cuevas and Elkim Roa

  This paper presents a summary of the design and implementation considerations that must be taken into account in the implementation of current sources for different current domains. Finally, the paper shows a circuit for the generation of a high precision current reference (error $< 1\%$) for circuits that require high speed or precision. This work was recently submitted to the "26th IEEE International Conference on Electronics Circuits and Systems".

4.2.2. Related presentations

- **Boosting RISC-V ISA with Open Source Peripherals: An SoC for Low Power Sensors** (7th RISC-V Workshop - 2017) (58)

Megan Wachs, Luis E. Rueda G., Albert Huntington, Javier Ardila, Jack Kang, Andres Amaya, Ckristian Duran, Hector Gomez, Juan Moya, Laude Fernandez, Laura Navarro, **Rolando Torres**, Juan Romero, Daniel Ramirez, Julian Arenas, Juan Gomez, Hanssel Morales, Elkim Roa and Krste Asanovic.

In this presentation is shown a library of low-power analog peripherals commonly employed in microprocessors that includes an AON domain. The library includes circuits such as crystal oscillator, current bias source, voltage regulator, bandgap voltage source, data converters and circuits for supply voltage monitors. These peripherals are integrated in a RISC-V microprocessor developed by SiFive, one of the companies leaders in the development of on-chip free hardware systems. Presentation was leaded by Prof. Elkim Roa at 2017 7th RISC-V Workshop.

- **YoPuzzle: A mRISC-V Development Platform for Next Generations** (5th RISC-V Workshop) (59)

  Ckristian Duran, Luis E. Rueda G., Andres Amaya, **Rolando Torres**, Javier Ardila, Luis Rueda D., Giovanny Castillo, Anderson Agudelo, Camilo Rojas, Luis Chaparro, Harry Hurtado, Juan Romero, Wilmer Ramirez, Hector Gomez, Hugo Hernandez and Elkim Roa

  In this presentation an idea for full PCB implementation and platforming of the mRISC-V (or Open-V) microcontroller (named YoPuzzle) was proposed. YoPuzzle is a way to do dynamic and fun ways to do programming aimed to young people. The purpose of the Puzzle is encouraging young people to use Open platforming to do projects, allowing to understand all functionality

from the minimum detail. Also, the fabricated silicon and test PCB was presented, along with a live demo featuring different kind of tests with LEDs. Presentation was leaded by Prof. Elkim Roa and Ckristian Duran (demo only) at 2016 5th RISC-V Workshop.

- **RISC-V Community Needs Peripheral Cores** (5th RISC-V Workshop) (60)

  Ckristian Duran, Luis E. Rueda G., Andres Amaya, **Rolando Torres**, Javier Ardila, Luis Rueda D., Giovanny Castillo, Anderson Agudelo, Camilo Rojas, Luis Chaparro, Harry Hurtado, Juan Romero, Wilmer Ramirez, Hector Gomez, Hugo Hernandez and Elkim Roa

  This presentation shows ideas of solution about the disadvantages about Intellectual Property (IP) peripheral silicon implementation inside RISC-V platforms. It was exposed that Open-Hardware is the main way to avoid different non-standardized problems. These problems are such as quality Open Linux driver coding, solving bottlenecks about information throughput, and standardize analog devices such as GPIO. As examples of developing work-in-process circuitry were presented the Open-V microcontroller, Analog-to-Digital converter, Clock Data Recovery (CDR), Phase-Locked Loop oscillator (PLL), USB 3.1 Gen 2 and its different analog modules, Pseudo-Random Bit Shift (PRBS) generation and checking, lpDDR3 interface controller using VIP and UVM to strong verification, Trusted Platform Module (TPM) as key handshaker, True-Random Noise Generator (TRNG), and Non-Volatile RAM (NVRAM). Presentation was leaded by Prof. Elkim Roa at 2016 5rd RISC-V Workshop.

4.3. FUTURE WORK

4.3.1. CTLE implementation and measurement. The CTLE presented in this research work should be tape out and implemented in a USB3.0 interface. The results of measurement allows a characterization and generates feedback for possible circuit improvements and optimization. Making a full characterization gives information such as changes in ranges and steps of tuning. This results helps to take decisions about the automatic gain control required by the CTLE.

4.3.2. Training CTLE algorithm design and implementation. Several algorithms and routines for automatic equalization has been reported in the literature. The CTLE designed is tunable but for a real application it must be automatic adjusted to obtain the performance required for each specific case.

4.3.3. Low-power precision current source. The current reference sources are an essential circuit in integrated circuits. In modern systems where power consumption is highly restricted and design time is very short, it is important that current references circuits are low power consumption and easy to integrate. Besides, it does not require pads an it should maintain low area and accuracy.

This work explored two circuit implementation alternatives to generate an accurate reference current. However, it is recommendable to research in the field of only MOSFET based current sources that avoids use of resistors and allow to get reference currents in nanoamperes range.

REFERENCES

[1] D. C. Daly and et al., “Through the Looking Glass - The 2018 Edition: Trends in Solid-State Circuits from the 65th ISSCC,” *IEEE Solid-State Circuits Magazine*, 2018.

[2] J. F. Bulzacchelli and et al., “A 10-gb/s 5-tap dfe/4-tap ffe transceiver in 90-nm cmos technology,” *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, pp. 2885–2900, Dec 2006.

[3] Y. Wang and et al., “A 2.5mW Inductorless Wideband VGA with dual Feedback DC-offset Correction in 90nm CMOS Technology,” in *2008 IEEE Radio Frequency Integrated Circuits Symposium*, 2008.

[4] W. Rhines, “What Will Stimulate the Next Wave of Semiconductor Industry Growth?” *The ConFab*, 2016.

[5] Y. Lin and et al., “A 5–20Gb/s Power Scalable Adaptive Linear Equalizer Using Edge Counting,” in *2014 IEEE Asian Solid-State Circuits Conference (A-SSCC)*, 2014.

[6] V. Balan and et al., “26.1 a 130mw 20gb/s half-duplex serial link in 28nm cmos,” in *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, 2014.

[7] U. S. B. Organization, “USB3.0 SuperSpeed Equalizer Design Guidelines,” 2008.

[8] ——, “USB3.1 Channel Loss Budgets,” 2015.

[9] ——, “Universal Serial Bus 3.0 Specification,” 2008.

[10] H. Kimura and et al., “2.1 28Gb/s 560mW Multi-standard SerDes with Single-stage Analog Front-end and 14-tap Decision-feedback equalizer in 28nm CMOS,” in *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, 2014.

[11] Y. Choi and Y. Kim, “A 10-Gb/s Receiver with a Continuous-time Linear Equalizer and 1-tap Decision-feedback Equalizer,” in *2015 IEEE 58th International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2015.

[12] C.-F. Liao and S.-I. Liu, “A 10Gb/s CMOS AGC Amplifier with 35dB Dynamic Range for 10Gb Ethernet,” in *2006 IEEE International Solid State Circuits Conference - Digest of Technical Papers*, 2006.

[13] Y. Kim and et al., “A 21Gbit/s 1.63pJ/bit Adaptive CTLE and One-Tap DFE With Single Loop Spectrum Balancing Method,” *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 2016.

[14] J. W. Jung and B. Razavi, “A 25Gb/s 5.8mW CMOS Equalizer,” *IEEE Journal of Solid-State Circuits*, 2015.

[15] Q. Pan and et al., “A 30Gb/s 1.37pJ/b CMOS Receiver for Optical Interconnects,” *Journal of Lightwave Technology*, 2015.

[16] R. Navid and et al., “A 40Gb/s Serial Link Transceiver in 28nm CMOS Technology,” *IEEE Journal of Solid-State Circuits*, 2015.

[17] S. Agarwal and V. S. R. Pasupureddi, “A 5Gb/s Adaptive CTLE with Eye-monitoring for Multi-drop Bus Applications,” in *2014 IEEE 57th International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2014.

[18] T. Shibasaki and et al., “A 56Gb/s Receiver Front-end with a CTLE and 1-tap DFE in 20nm CMOS,” in *2014 Symposium on VLSI Circuits Digest of Technical Papers*, 2014.

[19] H. D. Lee and et al., “A Wideband CMOS Variable Gain Amplifier With an Exponential Gain Control,” *IEEE Transactions on Microwave Theory and Techniques*, 2007.

[20] D. Duvvuri and V. S. R. Pasupureddi, “An Integrated Common Gate CTLE Receiver Front End with Charge Mode Adaptation,” in *2016 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, 2016.

[21] Y. Wang and et al., “Design of a Low Power, Inductorless Wideband Variable-Gain Amplifier for High-Speed Receiver Systems,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2012.

[22] M. Erett and et al., “A 126mW 56Gb/s NRZ Wireline Transceiver for Synchronous Short-reach Applications in 16nm FinFET,” in *2018 IEEE International Solid - State Circuits Conference - (ISSCC)*, 2018.

[23] S. Parikh and et al., “A 32Gb/s Wireline Receiver with a Low-frequency Equalizer, CTLE and 2-tap DFE in 28nm CMOS,” in *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers*, 2013.

[24] W. Kim and et al., “A 5.4Gbit/s Adaptive Continuous-Time Linear Equalizer Using Asynchronous Undersampling Histograms,” *IEEE Transactions on Circuits and Systems II: Express Briefs*, 2012.

[25] L. Wu and et al., “Co-design of 40Gb/s Equalizers for Wireline Transceiver in

65nm CMOS Technology," in *2014 IEEE International Conference on Electron Devices and Solid-State Circuits*, 2014.

[26] T. Toifl and et al., "A 2.6mW/Gbps 12.5Gbps RX With 8-Tap Switched-Capacitor DFE in 32nm CMOS," *IEEE Journal of Solid-State Circuits*, 2012.

[27] J. Lee, "A 20Gb/s Adaptive Equalizer in 0.13um CMOS Technology," *IEEE Journal of Solid-State Circuits*, 2006.

[28] N. Kocaman and et al., "A 3.8mW/Gbps Quad-Channel 8.5–13Gbps Serial Link With a 5 Tap DFE and a 4 Tap Transmit FFE in 28nm CMOS," *IEEE Journal of Solid-State Circuits*, 2016.

[29] W. Cao and et al., "A 15Gb/s Wireline Repeater in 65nm CMOS Technology," in *2015 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC)*, 2015.

[30] Y. Kim and et al., "A 21-Gbit/s 1.63-pJ/bit Adaptive CTLE and One-Tap DFE With Single Loop Spectrum Balancing Method," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 2016.

[31] T. Musah and et al., "A 4–32Gb/s Bidirectional Link With 3-Tap FFE/6-Tap DFE and Collaborative CDR in 22nm CMOS," *IEEE Journal of Solid-State Circuits*, 2014.

[32] M. Kim and et al., "A 24-mW 28-Gb/s Wireline Receiver with Low-frequency Equalizing CTLE and 2-tap Speculative DFE," in *2015 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2015.

[33] H. Won and et al., "A 28-Gb/s Receiver With Self-contained Adaptive Equalization and Sampling Point Control Using Stochastic Sigma-Tracking Eye-

Opening Monitor," *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2017.

[34] W. Rahman and et al., "6.6 A 22.5-to-32Gb/s 3.2pJ/b Referenceless Baud-rate Digital CDR with DFE and CTLE in 28nm CMOS," in *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, 2017.

[35] C. Aprile and et al., "An Eight-Lane 7-Gb/s/pin Source Synchronous Single-Ended RX With Equalization and Far-End Crosstalk Cancellation for Backplane Channels," *IEEE Journal of Solid-State Circuits*, 2018.

[36] S. S. Mohan and et al., "Bandwidth Extension in CMOS with Optimized On-chip Inductors," *IEEE Journal of Solid-State Circuits*, 2000.

[37] Y. Wu and et al., "CMOS VHF/RF CCO Based on Active Inductors," *Electronics Letters*, 2001.

[38] M. Grozing and et al., "A 2.5V CMOS Differential Active Inductor with Tunable L and Q for Frequencies up to 5GHz," in *2001 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium (IEEE Cat. No.01CH37173)*, 2001.

[39] Z. Gao and et al., "Wide Tuning Range of a CMOS RF Bandpass Filter For Wireless Applications," in *2005 IEEE Conference on Electron Devices and Solid-State Circuits*, 2005.

[40] F. Yuan, *CMOS Active Inductors and Transformers: Principle, Implementation, and Applications*, 1st ed. Springer Publishing Company, Incorporated, 2010.

[41] C.-H. Wu and et al., "A 1V 4.2mW Fully Integrated 2.5Gb/s CMOS Limiting

Amplifier Using Folded Active Inductors," in *2004 IEEE International Symposium on Circuits and Systems (IEEE Cat. No.04CH37512)*, 2004.

[42] B. Razavi, "The Cross-Coupled Pair - Part III [A Circuit for All Seasons]," *IEEE Solid-State Circuits Magazine*, 2015.

[43] D. C. Keezer, "Challenges and solutions for multi-gigahertz testing," in *Proceedings. International Test Conference*, Oct 2002, pp. 1230–.

[44] J. Park and et al., "At-speed Test of High-Speed DUT Using Built-Off Test Interface," in *19th IEEE Asian Test Symposium*, 2010.

[45] J. H. Chun and et al., "Test of phase interpolators in high speed i/os using a sliding window search," April 2012, pp. 134–139.

[46] S. Abdennadher and S. A. Shaikh, "Practices in high-speed io testing," in *2016 21th IEEE European Test Symposium (ETS)*, May 2016, pp. 1–8.

[47] A. Amaya, J. Ardila, and E. Roa, "A digital offset reduction method for dynamic comparators based on phase measurement," in *2017 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, July 2017, pp. 661–664.

[48] B. Nauta, "A CMOS Transconductance-C Filter Technique for Very High Frequencies," *IEEE Journal of Solid-State Circuits*, 1992.

[49] P. Crombez, J. Craninckx, and M. Steyaert, "A 100khz – 20mhz reconfigurable nauta gm-c biquad low-pass filter in 0.13μm cmos," in *2007 IEEE Asian Solid-State Circuits Conference*, Nov 2007, pp. 444–447.

[50] L. Najafizadeh, "Reference Circuits for Emerging Applications-from Extreme Environment Electronics to Internet of Things," in *2017 IEEE 60th International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2017.

[51] M. Kim, H. Lee, and C. Kim, “PVT Variation Tolerant Current Source With On-Chip Digital Self-Calibration,” *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, April 2012.

[52] H. Wang and P. P. Mercier, “A 14.5 pW, 31 ppm/°C Resistor-Less 5 pA Current Reference Employing a Self-Regulated Push-Pull Voltage Reference Generator,” in *IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2016.

[53] ——, “A 3.4-pw 0.4-v 469.3 ppm/°c five-transistor current reference generator,” *IEEE Solid-State Circuits Letters*, vol. 1, no. 5, pp. 122–125, May 2018.

[54] J. Santamaria, N. Cuevas, G. L. E. Rueda, J. Ardila, and E. Roa, “A Family of Compact Trim-Free CMOS Nano-Ampere Current References,” in *IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2019.

[55] M. Ghovanloo and K. Najafi, “A Compact Large Voltage-Compliance High Output-impedance Programmable Current Source for Implantable Microstimulators,” *IEEE Transactions on Biomedical Engineering*, Jan 2005.

[56] R. J. Baker, *CMOS Circuit Design, Layout, and Simulation*, 3rd ed. Wiley-IEEE Press, 2010.

[57] C. Duran, R. Torres, and et al., “A System-on-chip Platform for the Internet of Things Featuring a 32-bit RISC-V Based Microcontroller,” in *2017 IEEE 8th Latin American Symposium on Circuits Systems (LASCAS)*, 2017.

[58] E. Roa, “Boosting RISC-V ISA with Open Source Peripherals: An SoC for Low Power Sensors,” in *7th RISC-V Workshop*, 2017.

[59] ——, “YoPuzzle: A mRISC-V Development Platform for Next Generations,” in *5th RISC-V Workshop*, 2016.

[60] ——, “RISC-V Comunity Needs Peripheral Cores,” in *5th RISC-V Workshop*, 2016.

BIBLIOGRAPHY

F. Yuan, CMOS Active Inductors and Transformers: Principle, Implementation, and Applications, 1st ed. Springer Publishing Company, Incorporated, 2010.

Gray, Paul R., Analysis and Design of Analog Integrated Circuits, Wiley Publishing, 2009.

R. J. Baker, CMOS Circuit Design, Layout, and Simulation, 3rd ed. Wiley-IEEE Press, 2010.

U. S. B. Organization, “USB3.0 SuperSpeed Equalizer Design Guidelines,” 2008.

U. S. B. Organization, “USB3.1 Channel Loss Budgets,” 2015.

U. S. B. Organization, “Universal Serial Bus 3.0 Specification,” 2008.