DESIGN OF A MODULAR BIASING CONTROL FOR MICRO-AMPERE CURRENT SOURCES IN 28 NM

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Degree work presented as a requirement to qualify for the title of Electronic Engineering

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With appreciation,
Juan Carlos Rondón Delgado

Dedicated to my family and friends.

And to our team, with whom we started and finished this amazing journey.

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TÍTULO: DISEÑO DE UN CONTROL DE POLARIZACIÓN MODULAR PARA FUENTES DE CORRIENTE DE MICROAMPERIOS EN 28 NM [*]

AUTOR: JUAN CARLOS RONDÓN DELGADO [**]

PALABRAS CLAVE: TECNOLOGÍA CMOS, SYSTEM-ON-CHIP (SOC), CORRIENTE DE POLARIZACIÓN.

DESCRIPCIÓN:

En el panorama actual de las tecnologías de circuitos integrados, la demanda por reducciones de tamaño, aumento de velocidad, disminución de consumo y mayor integración en los diseños de Sistemas en un Chip (SoC) es cada vez más imperativa. Motivados por estos desafíos y oportunidades, los estudiantes de pregrado del grupo de investigación Onchip se plantearon como objetivo concebir y desarrollar un circuito integrado que incorpore todos los bloques esenciales de un SoC, haciendo uso de la avanzada tecnología CMOS de 28 nm. En este contexto, el proyecto encargado del control de polarización modular de la fuente de corriente desempeña un papel crucial, pues es el encargado de garantizar el punto de operación óptimo para los diversos bloques funcionales dentro del circuito integrado, proponiéndose así como meta suministrar corrientes estables al nivel de los micro amperios con alta precisión e invariabilidad.

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[*] Trabajo de Grado

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Director: ING. SERGIO ANDRÉS RUEDA GÓMEZ

ABSTRACT

TITLE: DESIGN OF A MODULAR BIASING CONTROL FOR MICRO-AMPERE CURRENT SOURCES IN 28 NM [*]

AUTHOR: JUAN CARLOS RONDÓN DELGADO [**]

KEYWORDS: CMOS TECHNOLOGY, SYSTEM-ON-CHIP (SOC), BIASING CURRENT.

DESCRIPTION:

In the current landscape of integrated circuit technologies, the demand for reductions in size, increased speed, decreased power consumption, and greater integration in System-on-Chip (SoC) designs is becoming drastically increased. Motivated by these challenges and opportunities, undergraduate students from the Onchip research group have set out to conceive and develop an integrated circuit that incorporates all the essential blocks of an SoC, leveraging advanced 28 nm CMOS technology. In this context, the project tasked with the modular biasing control of the current source plays a crucial role, as it is responsible for ensuring the optimal operating point for the various functional blocks within the integrated circuit, aiming to provide stable currents at the microampere level with high precision and consistency.

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[*] BSc Thesis

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INTRODUCTION

Recent technological progress has been largely driven by improvements in integrated circuits and computational systems. These advancements have had a significant impact by providing increasingly powerful and sophisticated functionalities in electronic devices of all sizes. The design and implementation of integrated circuits have become complex. As time progresses, there is a constant demand of achieving higher performance, occupying less space, and ensuring greater stability in electronic devices, presenting significant challenges for designers. In this regard, the objective of this thesis is to design a circuit capable of generating biasing sources for the modules of a System on a Chip (SoC), with the particularity of being designed using 28nm technology. This entails adjusting and additional modifications to the existing circuits to adapt them to the specific requirements and constraints of this advanced technology.

Nevertheless, this project is not solely focused on achieving technological development but also carries an educational focus. It aims to strengthen the professional skills of the researcher by addressing problems and challenges from a more professional perspective, promoting the development of a critical vision, and the utilization of cutting-edge tools and applications for state-of-the-art design.

In summary, the approach and development of this project aim to pursue both technological advancement and the development of professional skills, utilizing tools and applications currently available for SoC circuit design.

1. PROJECT OVERVIEW

1.1. MOTIVATION AND OBJETIVES

The motivations and objectives of this project are divided into three distinct stages. First, considering the notable advancement of microcontrollers today and the deep exploration and development in the field of microelectronics, undergraduate students of the OnChip research group aim to create a System-on-Chip (SoC) for general-purpose on a 28nm technology, equipped with essential modules. Aspiring not only to complete the design but also to carry out its manufacturing and physical testing in the near future.

Secondly, concerning this particular project, the aim is to develop a high-precision and stable current bias generator module in the microampere range, to serve as a current reference for other chip modules. This module is part of the fundamental supplies upon which subsequent stages depend entirely. Hence, ensuring maximum precision is imperative to prevent error propagation. Additionally, a complete design flow is proposed, ranging from stat of the art exploration and circuit definition to exhaustive analysis of specifications and obtaining satisfactory results in simulation. This process will lead to layout creation and simulations to validate the design specifications in a more realistic environment.

Finally, on a personal level, this project has represented a significant challenge, as it requires the investment and application of a large amount of time, concentration, and knowledge to overcome.

1.2. BASIC OPERATING PRINCIPLE

The main function of the current generator is to provide the polarization currents required by other modules. It is directly connected to the power supply voltage and depends solely on the bandgap, which is responsible for generating its input reference voltage[1]. Using a reference voltage of 1.2V, the current generator is expected to produce two currents at the microampere level with high precision and consistency.

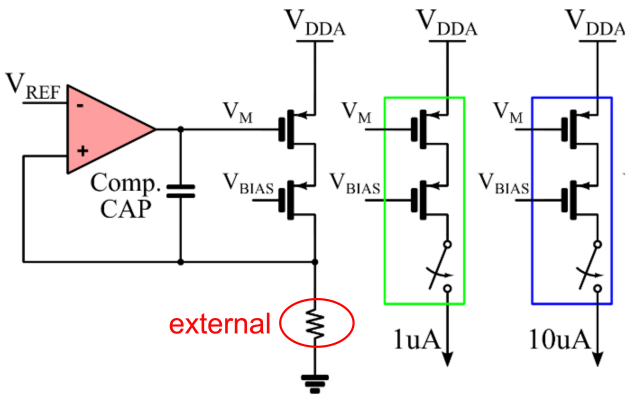

Figure 1. Postulated Proyect

The operation of the module in Figure1 depends solely on two external stimules: the supply voltage that provides power to the circuit and the reference voltage. This reference voltage is utilized by a negative feedback amplifier block that adjusts the value of the reference voltage at the output node of the main current mirror. This, along with the external resistance, determines the flow of current through the branch. Once the value of the base current is determined, cascode mirrors are employed to take this current and reflect it with different values through changes in aspect ratio, thereby enabling the delivery of various current values at the output with high precision.

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[1] J. SANTAMARIA et al. “A Family of Compact Trim-Free CMOS Nano-Ampere Current References”. In: (2019).

1.3. DESIGN SPECIFICATIONS

Given that this circuit serves as a reference to other blocks, the OnChip research group has established certain specifications to ensure an optimal performance. These specifications are detailed in Table 1. Within these values, the notation ”to be defined” (TBD) is included, indicating that the student, in collaboration with their thesis advisor, will be responsible for determining the most appropriate value for this parameter, as will be detailed a couple of sections later.

Table 1. Initial Specifications

PARAMETER	**SPECIFICATIONS**		
Range	Min	Typ	Max
VDD [V]	1,62	1,80	1,98
Iqscnt [µA]			TBD
Phase Margin [°]	55,00	65,00	
Gain Margin [dB]	10,00		
I1 [µA]	0,97	0,995	1,02
I10 [µA]	9,78	9,995	10,13
PSR DC[dB]		TBD	
Noise [nA]		TBD	

As can be seen in the table, the circuit must operate within a supply voltage range between 1.62 and 1.98 V, ensuring a maximum consumption current that will be defined later. Additionally, since the system features negative feedback, minimum margins in phase and gain are established to determine system stability. Furthermore, as high precision currents resistant to supply variations are required, a limit is set for the maximum noise and power supply rejection (PSR) for each of the obtained currents.

2. CIRCUIT DEFINITION

2.1. SINGLE STAGE AMPLIFIER

One of the most important modules is the amplifier, which can be considered the heart of the circuit and the main design element. Currently, many amplifier circuits can operate within the required parameters, so it is necessary not only to conduct extensive research but also an analysis of the specific conditions of this particular design. From this point, two specific conditions that must be satisfied by the amplifier module are recognized. Firstly, the stability of the design will depend on the distribution of poles and zeros that may appear at a general level due to the parasitic capacitances of the transistors. Understanding this will help to recognize the level that the amplifier module can reach, as the output module independently imposes a pole on the system. Taking this into account, and aiming to facilitate future compensation, all candidate amplifiers of level 2 or higher are discarded, so the choice should be a single-stage amplifier.

As a second requirement for the amplifier module, the required gain emerges, on which an approximation can be calculated based on the given specifications. Under the condition of unit gain on the output module, it is possible to calculate the approximate gain that the amplifier module must provide to meet the maximum current variations, as shown below.

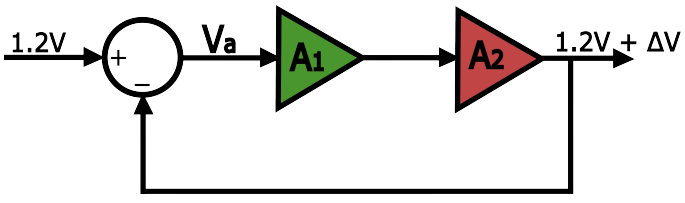

Figure 2. Gain Loop

$$A_1 = \frac{1.2 - \Delta_V}{\Delta_V} \tag{1}$$

$$\Delta_I = 26nA \quad \rightarrow \quad \Delta_V = 3.12mV \tag{2}$$

$$A_1 \cong \frac{1.2V}{3.12mV} \cong 52dB \tag{3}$$

If an output resistance close to 120kΩ is used, a gain of approximately 52 decibels is required, as well as an amplifier capable of generating this gain without difficulty. Taking into account the two conditions mentioned, it is determined that the module should be a single-stage amplifier with high gain[2]. Therefore, the preferred choice was the folded cascode operational transconductance amplifier, which fully meets both requirements and allows flexibility in the design process.

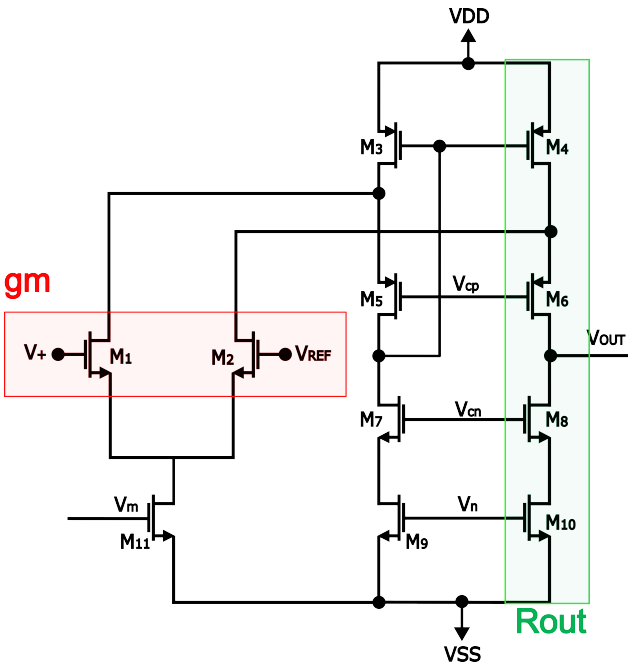

Figure 3. Folded Cascode OTA Gain

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[2] R. S. ASSAAD and J. SILVA-MARTINEZ. "The Recycling Folded Cascode: A General Enhancement of the Folded Cascode Amplifier". In: *IEEE Journal of Solid-State Circuits* 44.9 (2009), pp. 2535–2542.

$$A_0 = gm_{1,2} * R_{out} \tag{4}$$

$$A_0 = gm_{1,2} * (gm_8 ro_8 ro_{10} || gm_6 ro_6 (ro_2 || ro_4)) \tag{5}$$

2.2. SUPPLY INDEPENDENT BIASING

Given the above, while it is true that the folded cascode OTA meets the amplifier module requirements without issue, this circuit has multiple voltage levels that need to be biased. Therefore, an additional module is required to generate these voltage levels. This is why supply-independent biasing is added to the design.

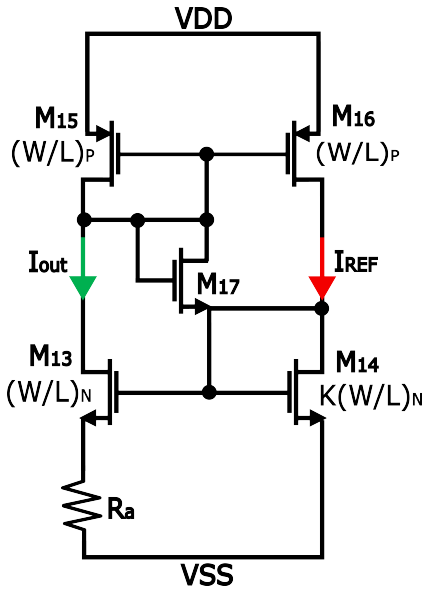

Figure 4. Supply Independent Biasing

This circuit can generate pseudo-independently constant currents regardless of the supply, allowing the implementation of multiple current mirrors to generate voltage

points that satisfy the biasing conditions of the amplifier module[3][4]. However, this circuit has a particular issue, which is its bistability. It can reach its stable state at two different points, either at zero magnitude output current or at output current Iout, depending on its initial conditions.

Therefore, an additional sub-module known as ”start-up” must be added, which, composed of M17, will be responsible for forcing the second state of functionality, behaving like a short circuit that forces the flow of current through the transistors as the supply voltage grows, and then transforming into an open circuit once its job is done, thus reducing additional current consumption and maintaining this behavior as long as the conditions to be shown below are met.[5][6]

$$V_{TH14} + V_{TH17} + |V_{TH15}| < VDD \tag{6}$$

$$V_{GS14} + V_{TH17} + |V_{GS15}| > VDD \tag{7}$$

2.3. OUTPUT SATGE

Now that the amplification stage has been clarified, it’s possible to analyze the circuit’s output stage, which is divided into two parts: The one responsible for generating the reference current and the other responsible for the compensation loop.

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[3] S. YAMAMOTO and ET AL. “Self-biasing MOS Reference Current Sources Insensitive to Supply Voltage and Temperature”. In: (2021), pp. 29–35.

[4] C. WU and ET AL. “A low TC, supply independent and process compensated current reference”. In: (2015), pp. 1–4.

[5] B. ZHANG and ET AL. “An Enhanced Start-up Circuit Eliminating All Trojan States in Self-biased Reference Generators”. In: (2022), pp. 848–851.

[6] B. RAZAVI. “Design of Analog CMOS Integrated Circuits (2nd ed.)” In: (2016).

On one hand, the circuit generating the reference current consists of a transistor and its cascode. These components convert the amplifier's output voltage into current, along with an external resistor that determines the output current value at the 1.2V node in the feedback loop. On the other hand, the compensation branch aims to enhance the circuit's stability. By employing the Miller effect and pole-splitting effect, the compensation RC branch extends stability margins through the addition of Cc [7].

Due to the configuration of the compensation capacitor, it's necessary to add a resistor Rc. This resistor alters the position of the zero generated in the right-half plane in the poles and zeros diagram due to the connection of an additional feedback loop, shifting that zero to the left-half plane and eliminating instability at high gains.

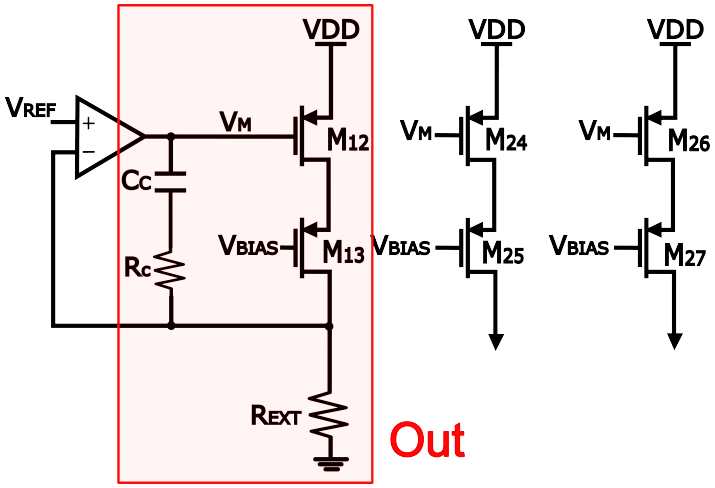

Figure 5. Output Stage

[7] M. MOHAMMADPOUR and M. ROSTAMPOUR. "Indirect Miller effect based compensation in Low power two-stage operational Amplifiers". In: (2012), pp. 1113–1116.

2.4. OUTPUT CURRENT MIRRORS

Given the specifications, it is necessary to generate two different levels of output current, both 1 and 10 microamperes. For this purpose, cascode current mirrors are implemented [8], which take the output module as a reference and reflect the amplified parameters to achieve their specific value. Assuming that their result depends only on the aspect ratio between the transistors, the value of the output currents will be determined as shown below:

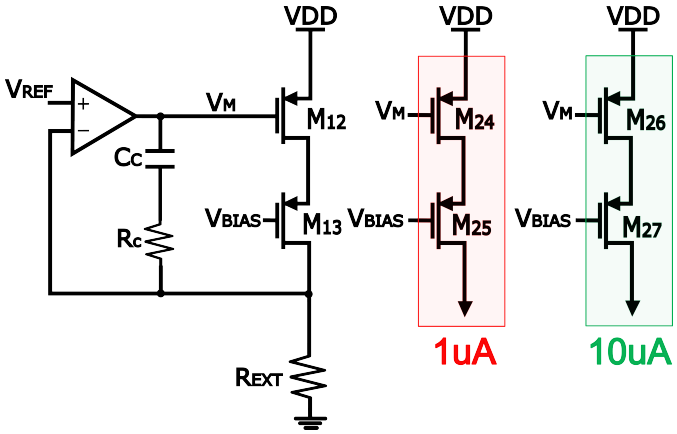

Figure 6. Output Current Mirrors

$$I_m = \frac{1.2V}{R_{ext}} \tag{8}$$

$$\frac{I_m}{I_1} = \frac{(W/L)_m}{(W/L)_1} \tag{9}$$

$$\frac{I_m}{I_{10}} = \frac{(W/L)_m}{(W/L)_{10}} \tag{10}$$

[8] MONIKA. “Different Current Mirror Topologies at Multiple Technology Nodes: Performance Comparison and Parameters Extraction”. In: (2021).

2.5. INDIRECT FEEDBACK COMPENSATION

Considering the previous stages, it is evident that the system belongs to the second order, as it will have two dominant poles that must be controlled to achieve the stability margins specified in the requirements. Typically, the easiest way to compensate a second-order system is through Miller compensation[9], which involves adding a capacitor in series with a resistor between the nodes responsible for the dominant poles. However, in this particular case, an alternative approach was chosen: indirect feedback compensation[10], which will offer greater benefits later on. This compensation method changes the connection points of the feedback loop, from the dominant pole to one of the amplifier nodes. In this way, an inversion on zero is generated from the addition of the loop, making its position no longer a possible factor of instability. Thanks to this, it is possible to eliminate the resistance Rc from the compensation loop.

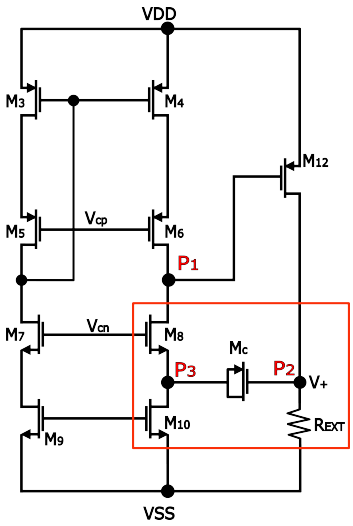

Figure 7. Indirect Feedback Compensation

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9 K. R. LAKER and W. M. C. SANSEN. "Design of analog integrated circuits and systems". In: (1994).

10 A. D. GRASSO, G. PALUMBO, and S. PENNISI. "Comparison of the frequency compensation techniques for CMOS two-stage miller OTAs". In: *IEEE transactions on circuits and systems. II, Express briefs* 55.11 (2008), pp. 1099–1103.

Once all the modules have been described, the selected schematics are compiled to visualize the complete circuit that needs to be designed, as follows:

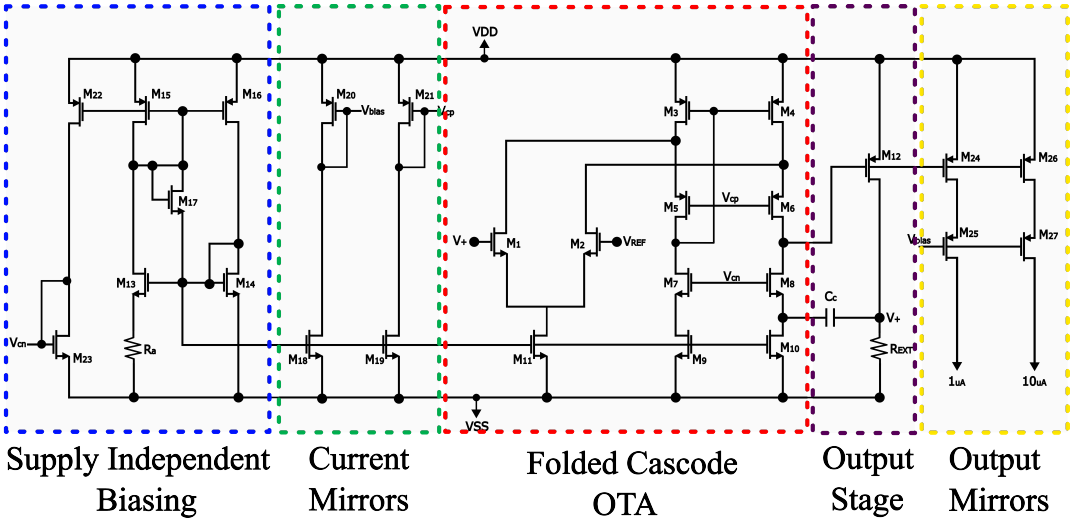

Figure 8. Complete Schematic

3. SPECIFICATIONS ANALYSIS

Once the schematic structure composing the bias current generator circuit is completed, an exhaustive analysis is conducted to determine the main variables that directly influence the value of the specifications provided in Table 1. This analysis provides a deep understanding of the variables and their functioning within the circuit.
Based on the results of this analysis, a detailed work plan is developed to maximize the utilization of the circuit's inherent characteristics. This plan focuses on optimizing the circuit's performance and meeting the specific project requirements, ensuring its effectiveness and functionality.

3.1. PSR

The Power Supply Rejection (PSR) is a fundamental metric for understanding how the power supply voltage and its variations affect a circuit's response. In this context, it's essential to identify and mitigate this influence to ensure that the output bias currents remain stable, regardless of fluctuations in the power supply. Achieving this requires a small-signal analysis to identify the key variables affecting this metric.

In this particular case, as illustrated in Figure 9, there are two main paths between the power supply node and the output. This means that there are two routes connecting the power supply node and its fluctuations with the circuit's final response.

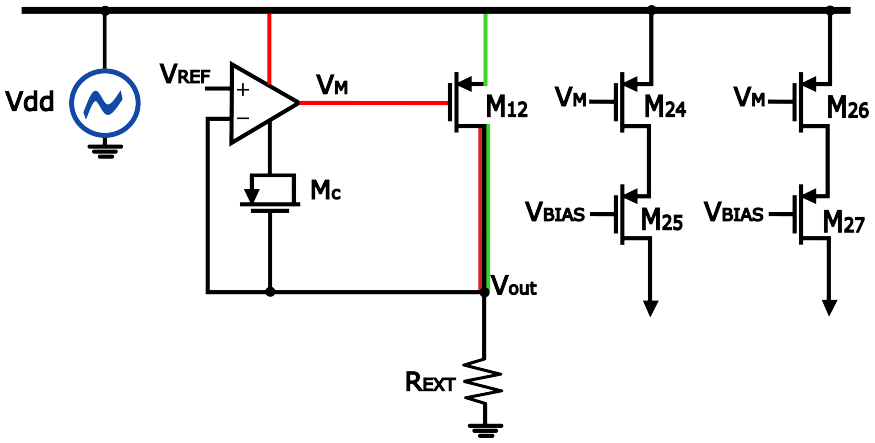

Figure 9. PSR

3.1.1. PSR in folded cascode OTA An analysis is carried out on the path that crosses the perational amplifier, so it is necessary to carry out the transformation of the folded OTA helmet to its small signal counterpart and determine the resulting transfer function using the supply node as a stimulus, as shown below:

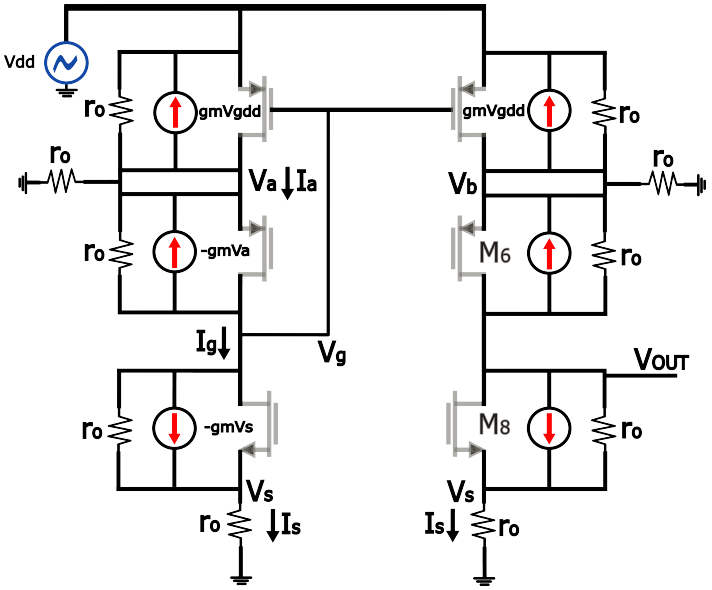

Figure 10. PSR in Folded OTA

Once the system is developed, it is possible to determine a transfer function for the circuit in terms of the transconductance g_m and output resistance r_o of each transistor, resulting in the following expression:

$$\frac{V_o}{V_{dd}} = \frac{gm + \frac{1}{r_o}}{\frac{1}{r_o(2+gmr_o)} + gm + \frac{2}{gm+\frac{1}{r_o}-\frac{1}{r_o(2+gmr_o)}}} \cong 1 \tag{11}$$

3.1.2. PSR in output stage In the design approximation made on equation 11, the value of the transfer function can be considered unitary. This implies that voltage fluctuations from the power supply are directly reflected onto the gate of M_{12}, as shown in Figure 9. A similar analysis is carried out on the second signal path. Consequently, the circuit is transformed into its small-signal equivalent, as detailed below:

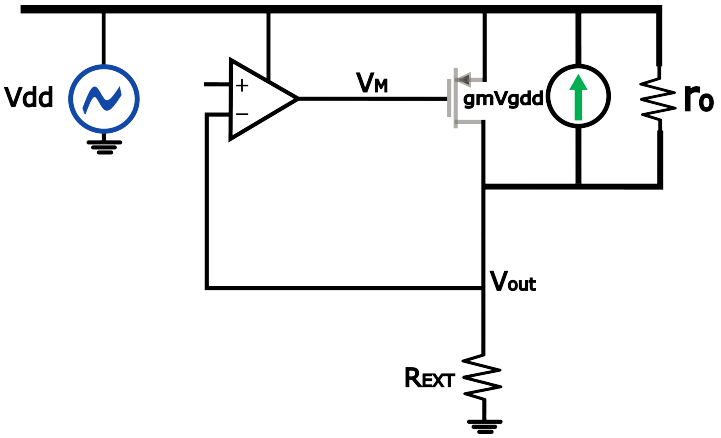

Figure 11. PSR in Output Stage

When considering the operational amplifier as an ideal element with a gain A_o, it is determined that the voltage at node V_m for this analysis corresponds to the sum of the supply voltage and the amplified output voltage, due to the feedback loop. By incorporating this expression along with the small-signal model of transistor M12, a new expression for the total transfer function is derived, and simultaneously an expression for the Power supply rejection PSR of the circuit is obtained.

$$\frac{V_o}{V_{dd}} = \frac{r_o}{gmA_o + \frac{1}{r_o}} \tag{12}$$

$$PSR = 20Log\left(\frac{1}{gmA_o r_o}\right) \tag{13}$$

As can be noted, an expression for the PSR in terms of the transconductance and resistance of the transistors was obtained, considering the equation 4 as an equivalence for A_o. Moreover, it is straightforward to determine the principal variable significantly affecting this specification, which is the gain of the operational amplifier.

3.2. NOISE

Circuit noise refers to all unwanted disturbances that may appear on electrical signals. This phenomenon is intrinsic to electrical components and can be caused by various sources that must be taken into consideration during design. For this project, two different sources of noise were taken into consideration.

Thermal noise, also known as Johnson-Nyquist noise, originates from the thermal agitation of charge carriers in conductors and is linked to both temperature and the random motion of electrons within them[11]. Mathematically, this noise can be modeled as an independent current source applied in parallel to the element under evaluation, as shown below, resulting in an approximate expression for its value.

[11] Roland Thewes RALF BREDERLOW1 Georg Wenig2. “Investigation of the Thermal Noise of CMOS Transistors under Analog and RF Operating Conditions”. In: (), pp. 1–4.

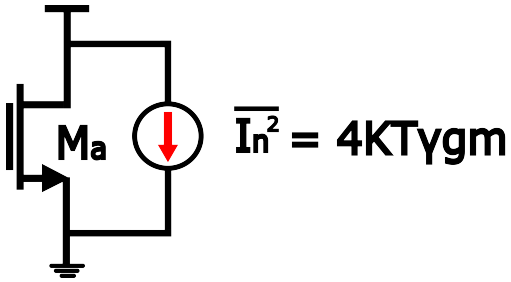

Figure 12. Thermal Noise Model

As a second source of noise considered, there is the 1/f noise or Flicker noise, which is associated with slow fluctuations in device conditions, such as variations in charge carrier mobility, and is characterized by reducing its power spectral density as frequency increases[12]. Similar to thermal noise, this phenomenon can be modeled as an independent voltage source, applied to the gates of the transistors responsible for it.

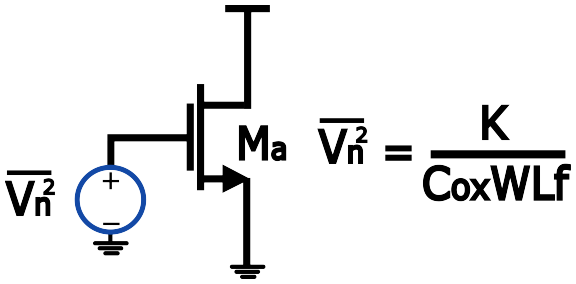

Figure 13. Flicker Noise Model

Once the above conditions are stated, the mathematical calculation of noise throughout the circuit is performed to understand the main elements and variables that must be controlled during the design process. For this purpose, a step-by-step analysis is conducted, obtaining an expression for the approximate value of noise at the circuit input, which can subsequently be referenced at the output as an equivalent noise in current.

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[12] Abbas El Gamal HUI TIAN. “Analysis of 1/f noise in CMOS APS”. in: (), pp. 1–9.

3.2.1. Noise in folded cascode OTA To calculate the total noise in the Folded Cascode OTA referenced to the input, it is necessary to convert each of the independent noise sources generated by each transistor. This process involves determining the individual contribution to the noise from each component of the circuit. Subsequently, the effects of these noise sources are brought to the gate of the differential pair. This allows for the evaluation of the cumulative impact of noise on the overall circuit operation.

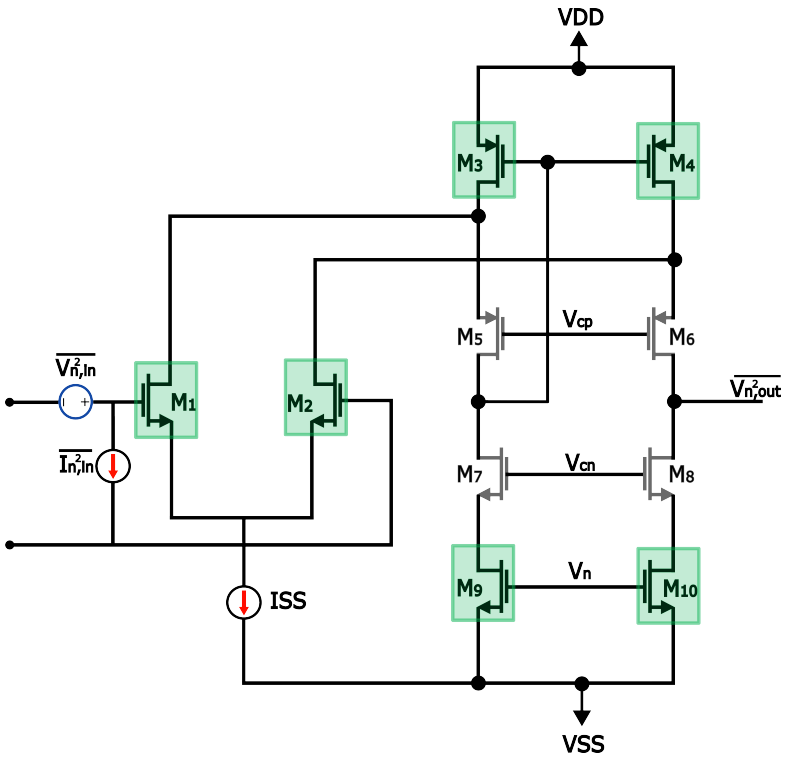

Figure 14. OTA Noise

As expected, this process must be carried out for each of the transistors in the OTA. However, there are specific transistors that do not contribute to the system noise, known as cascodes. When performing noise analysis on these transistors, it is observed that the equivalent current noise generated remains encapsulated in a loop through the transistor, resulting in a negligible contribution to the output noise.
Taking this into account, it is possible to exclude transistors from M5 to M8 in Figure 14

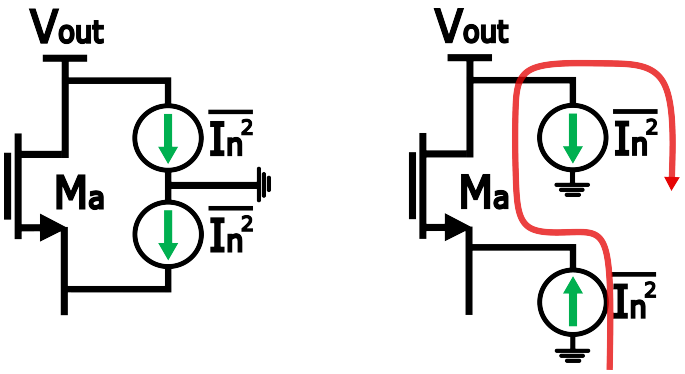

Figure 15. Noise in Cascodes

and focus on the remaining ones. To begin with, the thermal noise of each transistor is calculated using the current source approximation mentioned earlier. By summing these currents, an equivalent current in the differential pair is obtained, which can be referenced to the input as an independent voltage source by dividing it by the square of the transconductance of the differential pair.

$$\overline{Vn^2_{in_T}} = \frac{8KT\gamma}{gm^2_{1,2}} * (gm_{3,4} + gm_{9,10} + gm_{1,2}) \tag{14}$$

Similarly, it is possible to calculate the equivalent flicker noise at the input of the differential pair by approximating the noise on each transistor with the independent voltage source mentioned earlier. This voltage source can be transformed into its current counterpart by multiplying it by the square of the transconductance of each transistor. Once the corresponding currents for each transistor are obtained, it is possible to sum them up, and then reference the equivalent current to the input of the differential pair by the square of the transconductance, as in the case of thermal noise.

$$\overline{Vn^2_{in_f}} = \frac{2K}{C_{ox}f} * \left(\frac{1}{WL_{1,2}} + \frac{gm^2_{3,4}}{WL_{3,4}gm^2_{1,2}} + \frac{gm^2_{9,10}}{WL_{9,10}gm^2_{1,2}} \right) \tag{15}$$

3.2.2. Noise in output stage Similarly to the previous case, noise calculations are performed using model approximations as independent sources, both for the output transistor M_{12} and for the external resistance, for which its contribution to thermal noise was taken into account. Just like with the OTA noise, each independent noise source is referenced to the circuit input.

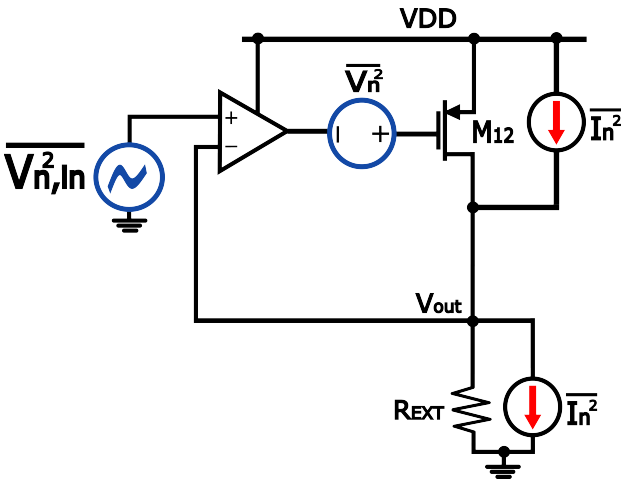

Figure 16. Noise in Output Stage

In this specific case, the current noise generated by M12 and the resistance R_{ext} are transferred to the transistor's gate through its transconductance. Then, together with the flicker noise, they are referenced to the circuit input using the square of the amplifier gain, thus obtaining the total noise of the second stage referenced to the input.

$$\overline{Vn_{in,2d}^2} = \frac{1}{(gm_{1,2}R_{out,OTA})^2} * \left(\frac{K}{C_{ox}WL_{1,2}f} + \frac{4KT\gamma}{gm_{1,2}} + \frac{4KT}{R_{ext}gm_{1,2}^2} \right) \tag{16}$$

Finally, the values obtained in the last sections are summed to obtain the total noise of the circuit referenced to the input. However, since it is desired to know the total noise at the output, the noise is converted and transferred to the final node using the amplifier gain and the transconductance of M_{12}.

Thus, the final value of the noise in current is obtained as follows:

$$\overline{In_{out}^2} = (gm_{12}gm_{1,2}R_{out,OTA})^2 * \left(\overline{Vn_{in,2d}^2} + \overline{Vn_{in_T}^2} + \overline{Vn_{in_f}^2}\right) \tag{17}$$

Additionally, it is necessary to mention one more variable, from which fruitful insights can be gained in the design process. Since the expression for the noise Inout depends on frequency, it is integrated over the bandwidth of the circuit. This is a variable to consider, as configuring it correctly can lead to design benefits.

$$I_{noise} = \int_0^B \overline{In_{out}^2}\, df \tag{18}$$

3.3. PHASE MARGIN

The phase margin is a crucial measure in the analysis of circuit stability, especially in feedback systems. This concept refers to the amount of margin between the phase of the system gain and the phase at the instability point. In other words, the phase margin specifies the range of phase available before the circuit stops functioning properly.
The calculation of the phase margin is closely related to the system gain and the poles present in it. The following expression provides an approximation that can offer a useful perspective when designing a system.

$$PM = 90 - tan^{-1}\left(\frac{A_o P_1}{P_2}\right) \tag{19}$$

Taking into account the equation presented, it is crucial to find the expressions for each of its variables, which will allow simplifying the equation in terms of design values that can be controlled. As shown previously, the expression for the system gain is:

$$A_o \cong (gm_{1,2}r_o/2)^2 \tag{20}$$

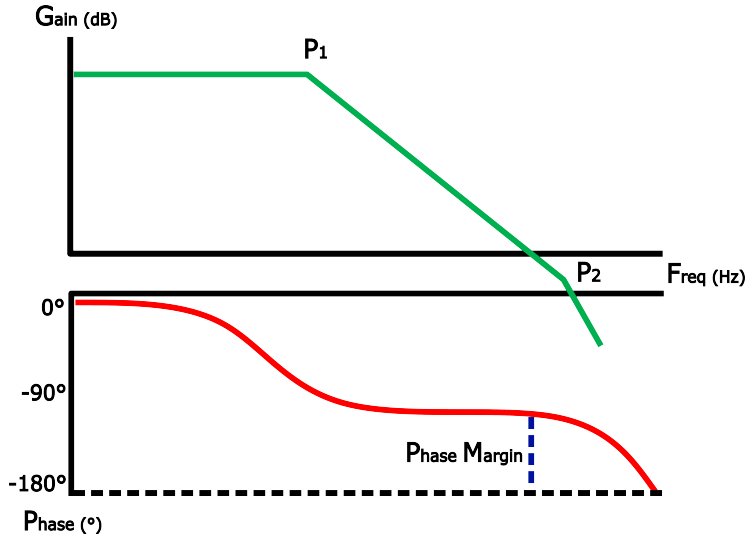

Figure 17. Phase Margin Bode Graphic

Therefore, the missing variables are the poles present in the system, for which the approximation of the inverse of the product of resistance and capacitance will be used.

3.3.1. Poles in OTA To determine the poles existing within the folded cascode OTA, the nodes where an independent energy-storing element may appear are identified, namely any node with an independent capacitance. This methodology reveals six different poles, as depicted in Figure 18.

$$P_1 = \frac{-4}{gm_{6,8} r_o^2 \sum Cp_2} \tag{21}$$

$$P_{2,5} = \frac{-gm_{7,8}}{\sum Cp_{2,5}} \tag{22}$$

$$P_{3,4} = \frac{-gm_{5,6}}{\sum Cp_{3,4}} \tag{23}$$

$$P_6 = \frac{-gm_3}{\sum Cp_6} \tag{24}$$

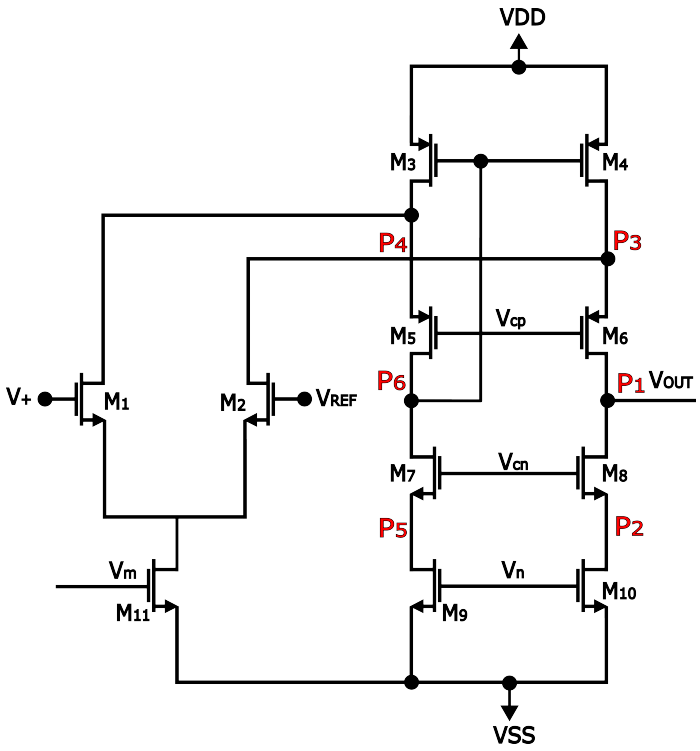

Figure 18. Poles in OTA

As can be observed, only pole P1 appears at low frequencies due to the transconductance of transistors M6 and M8 and the resistance r_o. Conversely, the remaining poles occur at very high frequencies, making their contribution practically negligible in the stability calculations performed.

3.3.2. Poles in output stage Using the same methodology applied previously to determine the number of poles, a single pole is identified in the circuit shown in Figure 19.

$$P_2 = \frac{-1}{(ro_{12}//R_{ext}) * (Cds_{12} + Cgd_{12})} \tag{25}$$

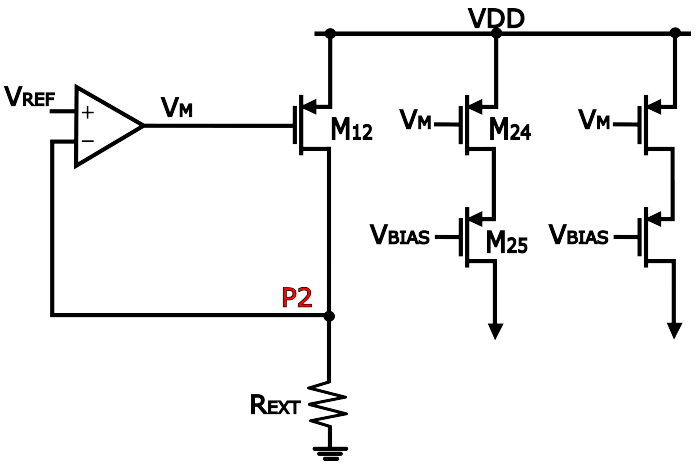

Figure 19. Pole in Output Stage

3.3.3. Compensation As mentioned earlier, the separation between the dominant poles of the system determines the level of stability. To address this aspect, compensation methodologies are commonly employed to facilitate the process. One of the most common techniques is Miller compensation, which involves applying an RC feedback loop between the poles responsible for system dominance, thereby generating a pole-splitting effect.

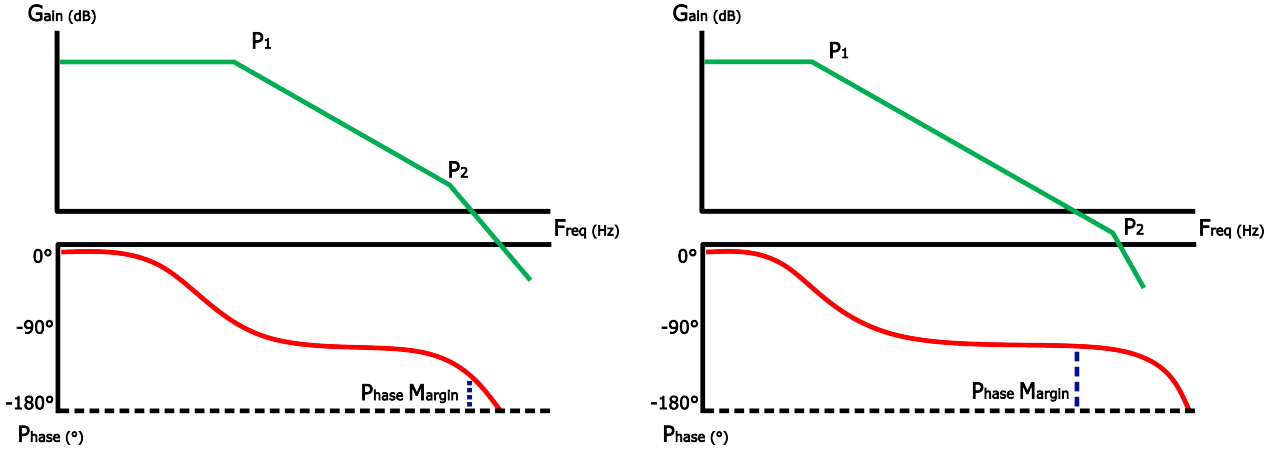

Figure 20. Miller Compensation

For this project, as explained in Section 2, a different compensation methodology was

used to optimize the system parameters[13]. This methodology involved connecting a feedback loop with a transistor operating in capacitor mode indirectly. This allowed increasing the voltage differential across the loop nodes, applying the pole splitting effect on pole P2 without affecting the relative position of the dominant pole P1, as shown in Figure 21.

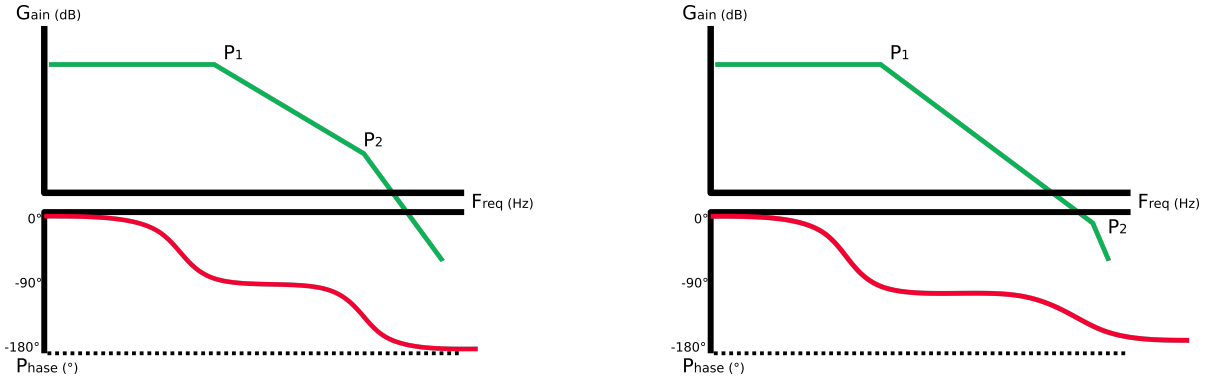

Figure 21. Indirect Feedback Compensation

When applying the compensation loop, the resulting equation that explicitly expresses the value of the post-compensation phase margin is:

$$PM = 90 - Tan^{-1}\left(\frac{A_o * \frac{-4}{gm_{6,8}ro^2\sum Cp_1}}{\frac{-G_2(C_c+\sum Cp_3)-gm_{12}C_c}{\sum Cp_2(\sum Cp_3+C_c)+\sum Cp_3C_c}}\right) \tag{26}$$

3.4. GAIN MARGIN

The gain margin, like its phase counterpart, is crucial in determining circuit stability. From the perspective of the Bode diagram, it can be understood as the distance in decibels that separates the system's magnitude response from the unity gain point when the phase response undergoes a 180° phase reversal, as shown in Figure 22.

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[13] V. SAXENA and R. J. BAKER. "Indirect feedback compensation of CMOS op-amps". In: (2006), pp. 2–4.

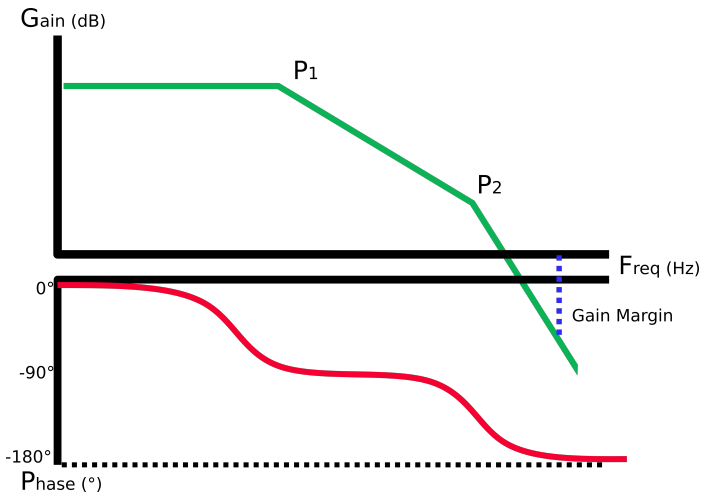

Figure 22. Gain Margin

$$GM = -20Log(A_{0L_{0dB}}) \tag{27}$$

From the viewpoint of the pole-zero diagram, the understanding is more straightforward. Open-loop poles tend to move towards the location of closed-loop zeros as loop gain increases, potentially causing instability in the system. While zeros located in the right half-plane of the pole-zero diagram do not inherently cause instability, increasing the gain can affect the poles by attracting them towards the positive side of the plane, leading to instability. Therefore, the gain margin is defined as the range of decibels available that can be added to the system from the amplifier before the poles reach the right half-plane of the pole-zero diagram.

Although this specification may seem to contradict the others, which generally improve with increasing gain, the required margin is relatively low, so it does not interfere significantly. Therefore, it is established that the gain supplied by the amplifier will be the value that minimizes the gain margin, with an additional margin for safety. This allows maximizing the contributions of the amplifier's gain to other specifications without negatively affecting system stability.

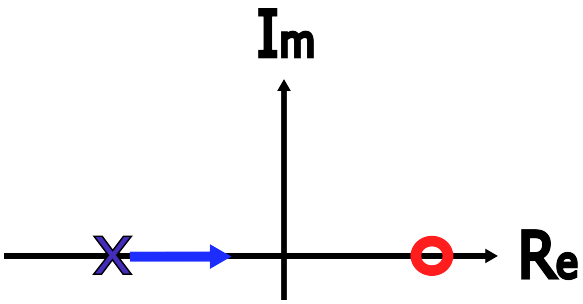

Figure 23. Poles and Zeros Graph

3.5. QUIESCENT CURRENT

The quiescent current, also known as idle current, refers to all the current necessary for the circuit's operation that is not directly reflected in its output. In this particular case, it encompasses all the currents that flow constantly through the module, except for the specified output currents, which are one and ten microamperes respectively. Once this concept is defined, a detailed analysis of the components influencing this specification is carried out, and a strategy is devised to optimize the project parameters.

Firstly, it is important to note that there are two main segments of current consumption in the circuit as shown in Figure 24. The first one is the current I_1, used as a supply for the operational amplifier and its corresponding current mirrors needed for biasing. Additionally, there is the current I_2, employed to bias the output stage and serves as a reference current for the output mirrors.

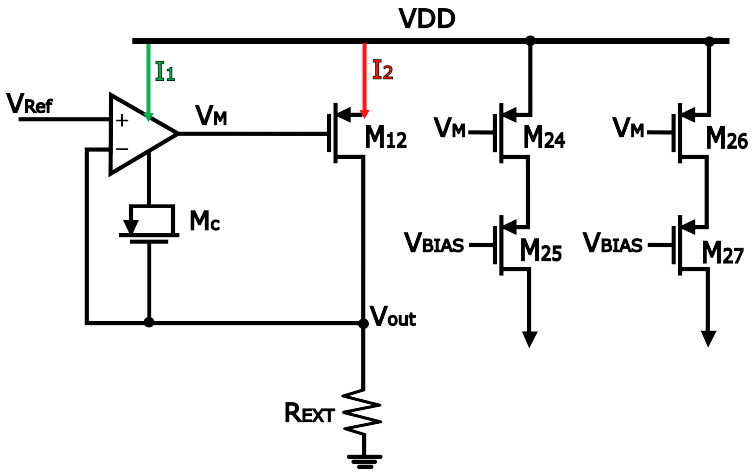

Figure 24. Main Current Consuption

To begin with, the current I_1 flowing through the folded cascode OTA in Figure 25 can also be separated and characterized based on the path it takes, dividing it into I_a, which is directed to the differential pair, and I_b, which is intended to flow through the cascodes of the amplifier [14]. With this clarified, a detailed analysis is conducted to determine a possible distribution of the current I_1.

On one hand, it is stipulated that I_a should be, as much as possible, a significantly large magnitude, since for a fixed gate-source voltage, a higher flow of current through the transistors of the differential pair results in a larger aspect ratio W/L and, consequently, a higher transconductance in the differential pair, leading to a proportional increase in the amplifier gain as I_a is also increased. On the other hand, a similar analysis is conducted for the current I_b, which operates in the opposite manner to its counterpart, as for a fixed supply voltage V_{DD}, as I_b decreases, the output resistance of the amplifier (R_{out}) increases, leading to a contrary effect to I_a; that is, as I_b decreases, the amplifier gain is proportionally increased.

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[14] J. ROH. "High-Gain Class-AB OTA with Low Quiescent Current". In: *Analog Integr. Circuits Signal Process.* 47.2 (Feb. 2006), pp. 225–228.

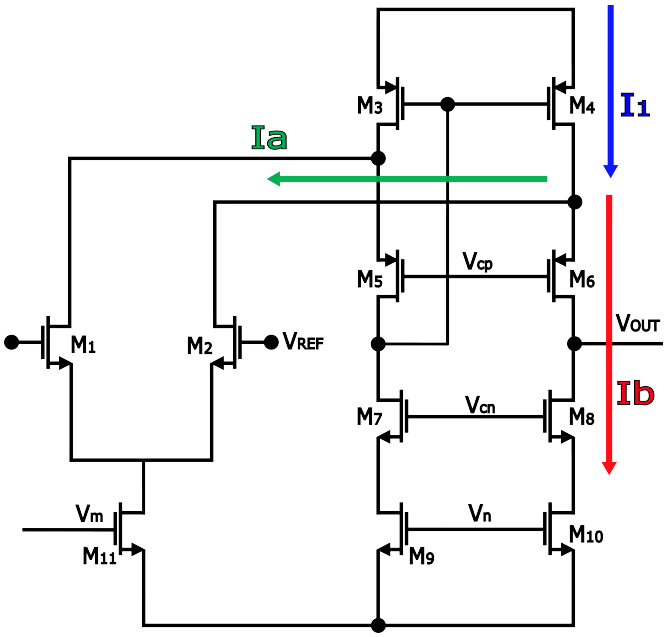

Figure 25. I1 Current Distribution

Now, there exists a second current I_2 as shown below in Figure 26 flowing through the circuit's output stage and serving as a reference for the final current mirrors.When analyzing current I_2, there are two aspects to address and appropriate decisions are made based on them.

Firstly, there is a fixed voltage of 1.2 V across the external resistor due to the reference value and amplification stage. In other words, the value of current I_2 is simply the quotient of the reference voltage and the applied external resistance. However, there is no restriction on the value that R_{ext} can take, so the value of I_2 is not conditioned by the magnitude of R_{ext}.

The second aspect to consider is the sizing of transistor M12, as it determines the optimal value for the current. Since I_2 is a current that will be mirrored, achieving the greatest possible matching between the current mirrors is crucial. To accomplish this, the maximum Vov voltage possible must be applied to M12, or equivalently, the maximum

gate-source voltage must be applied. However, this voltage is limited by the reference voltage of 1.2 V. Therefore, the actual value of I_2 will be the minimum current obtained when applying the maximum gate-source voltage for which the circuit remains operational, minimizing power consumption and maximizing matching between the current mirrors of the circuit.

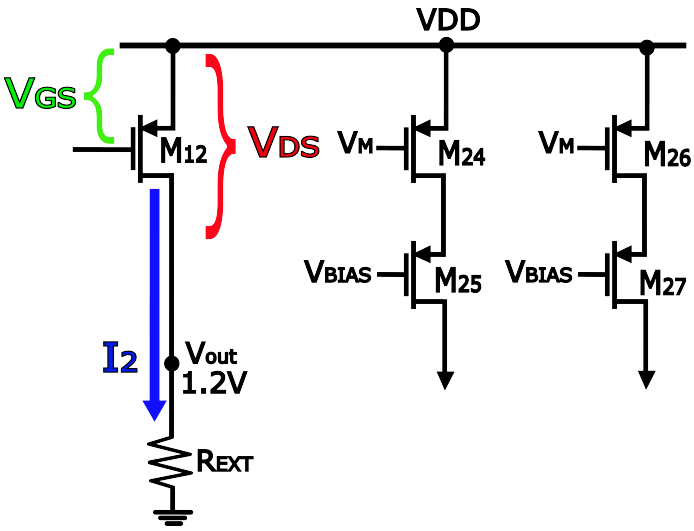

Figure 26. I2 Current Distribution

4. DESIGN DECISIONS

Once the different specifications have been analyzed, along with their functioning and considering the interdependencies among them, specific design decisions are made for the project. These decisions aim not only to meet the specified ranges in the requirements but also to optimize each of them to efficiently achieve the project's objectives. In this section, the design decision-making process will be explained, along with the criteria considered for these decisions and how they contribute to the overall success of the project.

4.1. DIFERENTIAL PAIR IN STRONG INVERSION

Usually, when designing operational amplifiers, the goal is to achieve the highest possible gain, and as described in section 2.1, this translates to an increase in the transconductance of the differential pair or the output resistance of the amplifier, with the first being the most common option. To achieve this, differential pairs in weak inversion are commonly used, taking advantage of the higher transconductance gm typically found in this operating region. However, this implementation comes with a high surface area consumption, with the differential pair being one of the modules with the highest area consumption. Given this challenge, a different approach is adopted for this project, opting to keep the transistors of the differential pair in strong inversion, which results in a reduction in the transconductance of the differential pair and, consequently, a decrease in the gain of the amplifier. This approach is chosen for its ability to significantly reduce the area used; however, it is essential to implement other methods through which the lost gain range is restored, a method that will be described later on.

4.2. LOW CURRENT THROUGH OTA'S CASCODE

As mentioned in Section 4.1, enhancing the gain of the amplifier module is crucial and is equivalent to increasing the transconductance gm of the differential pair or the output resistance R_{out}. Since the first option was ruled out at the beginning of this section, the only way to boost the gain is by increasing the output resistance of the folded cascode OTA to compensate for and surpass the lost gain in Section 4.1. This can be achieved by reducing the current passing through the cascodes of the operational amplifier. This decision has the effect of making the output resistance the primary variable for gain, rather than relying mainly on the transconductance of the differential pair.

In addition to contributing to the gain enhancement, this decision offers other significant advantages. By reducing the value of the current flowing through the cascodes, the quiescent current I_{qscnt} is also reduced. This reduction not only improves the gain and the power supply rejection ratio $PSRR$ simultaneously, as discussed in Section 3, but also has a positive effect on reducing the bandwidth. This is because the main pole of the circuit is inversely influenced by the output resistance of the operational amplifier. Therefore, an increase in the output resistance also increases the dominance of the main pole, which in turn improves stability and reduces the noise level by limiting the bandwidth over which the spectral noise density is integrated.

4.3. HIGH CURRENT THROUGH DIFFERENTIAL PAIR

As demonstrated in the explanation of the quiescent current I_{qscnt} in section 3.5, increasing the current through the differential pair results in a proportional increase in both the transconductance and the gain of the amplifier. This action complements the design decision made in section 4.2, allowing for further elevation of the implemented

gain levels and leading to a simultaneous improvement in $PSRR$ due to the increased gain. Additionally, there is an additional improvement in reducing noise at the output of the circuit for the increased transconductance of the differential pair.

With that said, the result of implementing the first three design decisions yields a level of gain comparable to conventional methods but provides clear improvements in other aspects such as current consumption, occupied area, noise, and stability.

4.4. DOMINANT POLE P1 AT LOW FREQUENCY

As demonstrated in the stability analysis in section 3.3, achieving a significant separation between the poles is crucial to ensure optimal phase and gain margins. In this particular case, leveraging the increase in output resistance to make the main pole highly dominant seems like an excellent design decision. However, this choice presents a problem that must be addressed before implementation.

Pushing the dominant pole P_1 to the bandwidth limit poses a challenge when applying compensation loops. These methods affect each of the involved poles differently when performing pole splitting among them. While the correction of pole P_2 by the compensation loop provides stability benefits by increasing its appearance frequency, this is not the case for pole P_1. Although pole splitting usually benefits the stability of the system, it can also critically affect the bandwidth magnitude.

Therefore, it is crucial to find a solution that maintains stability benefits without compromising the bandwidth. A solution to address this challenge is proposed below.

4.5. USE A MOSCAP WITH INDIRECT FEEDBACK COMPENSATION

This is one of the most important design decisions, so it will be described step by step for better understanding. To begin with, as mentioned earlier, frequency compensation is a tool that must be used to achieve the desired stability margins [10]. Typically, a capacitor is connected between the nodes responsible for the dominant poles of the circuit. This, by taking advantage of the Miller effect, generates a separation between the poles, thus increasing stability. Since this generates a zero in the right half-plane of the poles and zeros diagram, a resistor is added in series with the capacitor to eliminate adverse effects.

However, implementing a capacitor and a resistor entails a high area consumption, so they are not ideal elements. Based on this, it was decided to use a transistor in capacitive mode, which eliminates the area problem associated with the capacitor but adds as a requirement a minimum voltage level between the terminals due to the way this type of transistor operates. However, this requirement cannot be met by the current circuit, at least not with a conventional connection. That's why indirect compensation was chosen, changing the connection node of the operational amplifier's output pole to one of its cascodes. This has several advantages: first, the voltage requirement can be easily met as the nodes are at very different levels. Furthermore, since an inversion is generated over the zero of the right half-plane of the poles and zeros diagram, the implementation of the resistor that mitigated these effects is no longer necessary and can be eliminated, along with the area it consumed.

On the other hand, the problem raised in section 4.4 is also solved because the dominant pole is not connected to the compensation branch, so it is not affected by it and its position will not be modified. This allows increasing the separation between the poles through compensation, which changes the position of the second pole freely and without counter effects. This design decision brings about significant benefits, as the

reduced area is truly considerable. Additionally, it allows for the adjustment of phase margin as desired by varying the capacitance and controlling bandwidth by adjusting the current flow through the operational amplifier.

4.6. USE MAXIMUM VGS IN M12

With basis on the analysis of the current consumption I_{qscnt} in the final stage of the circuit, depicted in Figure 26, the decision has been made to utilize the minimum current obtained when applying the maximum gate-source voltage to the output transistor M_{12}, thus keeping the transistor operational. This choice entails a series of significant benefits. Firstly, employing the minimum required current with maximum V_{ov} efficiently optimizes the available resources and enhances matching between mirrors. Furthermore, since the current through the output branch depends mainly on the voltage across the transistor terminals rather than its physical dimensions, it is possible to minimize the transconductance of the output transistor M_{12} to reduce noise referred to the circuit's output.

This decision also has a direct effect on reducing occupied area. By maximizing V_{ov} between the mirrors, the scaling required for the transistors to achieve a level of invariability in output currents of 1μA and 10μA is minimized. This comprehensive approach not only improves circuit efficiency but also contributes to noise reduction and area savings, both fundamental elements for successful circuit design.

4.7. MINIMIZE NOISE SOURCES

As a final design decision, the noise analysis conducted in Section 3.2 was taken into consideration, leading to the adoption of measures to minimize the individual effects of transistors on noise generation. To achieve this, specific strategies addressing different aspects of the circuit design were implemented.

Firstly, the transconductance of transistors M9 and M10 was reduced by minimizing the current passing through them. Decreasing the current contributes to reducing the amplitude of current fluctuations, thereby helping to mitigate noise generation associated with these transistors.

On the other hand, this method is not applicable to reduce the transconductance of transistors M3 and M4, as these transistors are responsible for carrying all the current of the operational amplifier and although its magnitude can be minimized, it is significantly higher than the previous case. However, another strategy can be implemented to minimize their impact on noise. Instead of directly controlling the current magnitude, it is possible to control the voltage between the terminals of the transistors to make this voltage the primary factor determining the current magnitude, rather than their physical dimensions. This allowed adjusting the aspect ratio W/L of the transistors and, consequently, the equivalent transconductance, which helped to reduce noise generation.

These combined measures of current and voltage control significantly contributed to minimizing individual noise sources in the circuit, thereby improving its overall performance and its ability to deliver clean and precise signals.

5. RESULTS

5.1. SPECIFICATIONS SUPPLEMENT

To establish the missing specifications for the bias current generator project, a search for suitable values was carried out in collaboration with the research project director. Since there were no specified values for some of the given specifications, a solid starting point was sought. In this regard, the specifications of a similar circuit developed within the same research group were taken as an approximate target. This similar circuit, previously implemented in chip form, is part of the Tucán module. The choice of this circuit as a reference was based on its characteristics and similarities with our project, making it a useful guide for setting initial objectives.

Taking advantage of the possibility of accessing the libraries of the Tucan module, detailed simulations were carried out to obtain the values of the target specifications within the bias current generator module of this SoC. These simulations were conducted using the libraries of the mentioned circuit, allowing for an accurate representation of its behavior under different conditions. The simulation process included varying key parameters and evaluating the circuit's performance in various scenarios. As a result, the desired values for the remaining specifications were obtained, which are presented in the table below. The table displays the simulated values of the key specifications and their compliance with the project requirements, providing a clear insight into the expected performance for the current circuit.

Table 2. Complete Specifications

PARAMETER		SPECIFICATIONS		
Range		Min	Typ	Max
VDD [V]		1,62	1,80	1,98
Temp [ºC]		-40,00	37.33	125,00
Rext [kΩ]				
Iqscnt [µA]				64,16
Phase Margin [º]		55,00	65,00	
Gain Margin [dB]		10,00		
I1 [µA]		0,97	0,995	1,02
I10 [µA]		9,78	9,995	10,13
I1	PSR [dB]		-166,00	
	Noise [nA]			1,55
I10	PSR [dB]		-145,00	
	Noise [nA]			10,93
Area [µm²]				11427

5.2. SIMULATION VALUES

Once the schematization and design of the circuit are completed, its resilience to certain variations is verified, ensuring that the specifications are met even under such conditions. The whole possible variations have been taken into account, such as fluctuations in power supply due to a 10 % error in the source, process variations that may alter component behavior, and temperature variations ranging from -40ºC to 125ºC, as is commonly required.

In addition to these considerations, two additional variations have been taken into account. The first concerns the value of the external resistance, which may change due to its tolerance and temperature coefficient, potentially causing deviations of up to 200Ω when applying a tolerance of 0.1% and a temperature coefficient of 10 $ppm/$ºC, as indicated in the datasheet of the RG2012P-125-B-T5. The second variation re-

lates to the reference voltage, which has been addressed by connecting the reference node to a real output provided by the bandgap, created within the same research group.

By ensuring the correct operation of the circuit under these adversities, both individually and in combination, it is certified that even under the worst valid working conditions, the circuit will fulfill its function, as shown below in Table 3.

Table 3. Pre-Layout Corners Results

PARAMETER		**SPECIFICATIONS**			**PRE-LAYOUT**		
Range		Min	Typ	Max	Min	Typ	Max
VDD [V]		1,62	1,80	1,98	1,62	1,80	1,98
Temp [℃]		-40,00	37.33	125,00	-40,00	37.33	125,00
Rext [kΩ]					120,90	121,00	121,10
Iqscnt [µA]				64,16	13,20	16,81	21,89
Phase Margin [°]		55,00	65,00		63,66	70,85	75,41
Gain Margin [dB]		10,00			13,68	16,41	18,20
I1 [µA]		0,97	0,995	1,02	0,97	1,00	1,01
I10 [µA]		9,78	9,995	10,13	9,80	9,95	10,08
I1	PSR [dB]		-166,00		-185,00	-156,00	-138,00
	Noise [nA]			1,55	0,72	0,86	1,02
I10	PSR [dB]		-145,00		-155,00	-136,00	-122,00
	Noise [nA]			10,93	6,70	8,18	10,27
Area [µm²]				11427	1620		

In addition to the previous tests, a Monte Carlo simulation in table 4 is conducted with a thousand sampling points, which ensures that the results regarding the specifications are statistically valid and accurate.

Table 4. Pre-Layout Montecarlo Results

PARAMETER		SPECIFICATIONS		SIMULATION	
Range		Mean	Sigma	Mean	Sigma
Iqscnt [uA]				15,17	0,21
Phase Margin º				66,84	0,55
Gain Margin [dB]				15,90	0,22
I1 [uA]		0,995	0,013	1,00	0,007
I10 [uA]		9,95	0,081	9,96	0,066
I1	PSR [dB]			-157,00	0,68
	Noise [nA]			0,86	0,003
I10	PSR [dB]			-137,00	0,69
	Noise [nA]			8,18	0,03

5.3. FINAL DIMENSIONS

5.3.1. Supply independent biasing The dimensions of the supply independent biasing transistors and resistence Ra in Figure 4 are shown below:

Table 5. Supply Independent Biasing Dimensions

Transistor	W [nm]	L [μm]	Multiplier	Serie
M13	270	2	2	1
M14	270	2	1	4
M15	750n	2	1	4
M16	750n	2	1	4
M17	270	2	1	1
M18	270	2	1	4
M19	270	2	1	4
M20	270	2	1	4
M21	270	2	1	5
M22	270	2	1	4
M23	270	2	1	8

5.3.2. Folded cascode OTA Similarly, the dimensions of the transistors used to make the amplifier module in Figure 3 are denoted in Table 6 below.

Table 6. Folded Cascode OTA Dimensions

Transistor	W [nm]	L [μm]	Multiplier	Serie
M1	270	2	2	1
M2	270	2	2	1
M3	270	2	2	1
M4	270	2	2	1
M5	270	2	4	1
M6	270	2	4	1
M7	270	2	1	1
M8	270	2	1	1
M9	270	2	1	4
M10	270	2	1	4
M11	270	2	1	1

5.3.3. Output stage and current mirrors Finally, the dimensions of the final stage of the circuit, along with the sizes of the transistors comprising the output current mirrors, are presented in Figure 5. Additionally, the specification of the output resistance used is provided.

Table 7. Output Stage and Current Mirros Dimensions

Transistor	W [nm]	L [μm]	Multiplier	Serie
M24	270	2	4	4
M25	1000	0.2	8	1
M26	270	2	40	4
M27	1000	0.2	80	1
Mc	1000	2	2	1

5.4. LAYOUT

As the next step in the design flow, the layout creation emerges as a fundamental component that brings calculations and measurements closer to the physical element that will be generated from the circuit. This stage intricately displays the positioning of each involved element, allowing for a more concrete understanding of how theoretical concepts will materialize in the final electronic device. This section delves deeply into the layout design process, from translating the circuit schematic to the physical arrangement of components under simulator parameters, highlighting the importance of considering aspects such as component distribution and transistor matching care[15].

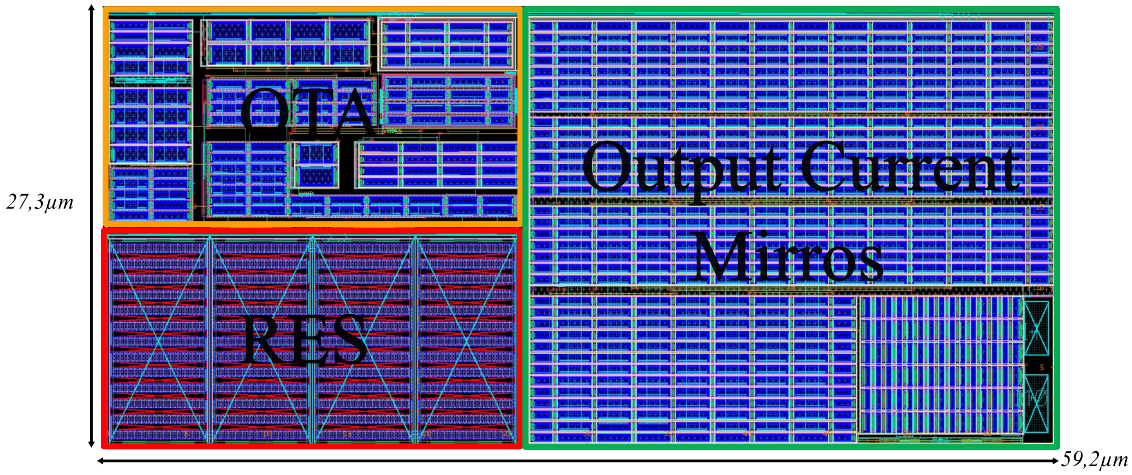

Figure 27. Layout

5.4.1. Key points

- Standardization of transistor size: It was decided to use a uniform size for all transistors present in the circuit, simplifying the design and assembly process, and improving the uniformity and consistency of the performance of each component.

[15] A. BERIAIN et al. “Challenge oriented methodology for analog integrated circuit layout design training”. In: (2014), pp. 1–5.

- Standardization of metals: A standard configuration was established for the different types of metals used in the interconnection of elements, depending on the direction in which the connections were arranged. In this particular case, only three different types of metals were used, maintaining an order over the interconnections that allowed for proper adjustment of the components without accessing upper layers, to avoid future interference problems with other connections when compiling elements into higher-level modules.

- Implementation of interdigitated and common centroid techniques [16]: Assembly techniques such as interdigitated and common centroid were used in the arrangement of components. This facilitated the creation of homogeneous transistor blocks that distribute gradients that may appear during manufacturing equitably, and allows for changes in positioning in the design if necessary in the future.

- Implementation of guard rings and transistors as dummies [17]: Guard rings and dummies were strategically placed around sensitive blocks of specific transistors, such as current mirrors and the differential pair, to protect them from possible external interferences and improve the homogeneity of the design, ensuring a more stable and reliable operation of the circuit.

- Implementation of common centroid triple on the output current mirrors[18]: This methodology was designed to mitigate the adverse effects of doping gradients and other factors that may arise during the manufacturing process of the circuit, which could critically affect the operation of the design. Through this method,

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16 R. J. BAKER. “Cmos: Circuit Design, Layout, and Simulation”. In: (2011).

17 T. C. CARUSONE. “Analog integrated circuit design (2nd ed.)” In: (2011).

18 P. K. CHAWDA. “A simplified methodology for complex analog module layout generation”. In: (2018), pp. 82–87.

homogeneity is ensured over the output currents and the area used is reduced by compiling the elements into a single block with high resilience to external factors.

5.5. POST-LAYOUT

As the final step in the design flow, the extraction of parasitic capacitances and resistances from the created layout is carried out. This stage is crucial to verify the final operation of the module, as it provides an accurate assessment of the physical circuit's behavior on the chip. The extraction of parasitic capacitances and resistances enables the identification of potential interferences and design issues that could impact the circuit's performance. Additionally, the importance of measurements and adjustments in the post-design stage is emphasized.

5.5.1. Corners's graphics To facilitate the understanding of the obtained results, as well as to clarify the strengths and weaknesses of each specification, the measurement results are graphically represented in relation to the limits of the obtained data. In this order, min, typ and Max corners results are plotted in red, blue and green respectively.

5.5.1.1. PSR As can be observed in Figures 28 and 29, the PSR value for currents of 1 and 10 microamperes exhibits a significant range between its maximum and minimum values. However, even the highest value meets the expected values satisfactorily. Additionally, although the specification is determined for direct current (DC), the system's resilience can be noted as the operating frequency increases.

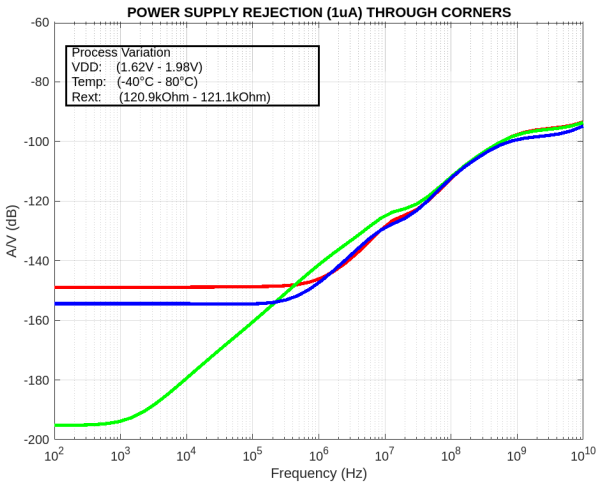

Figure 28. PSR 1uA

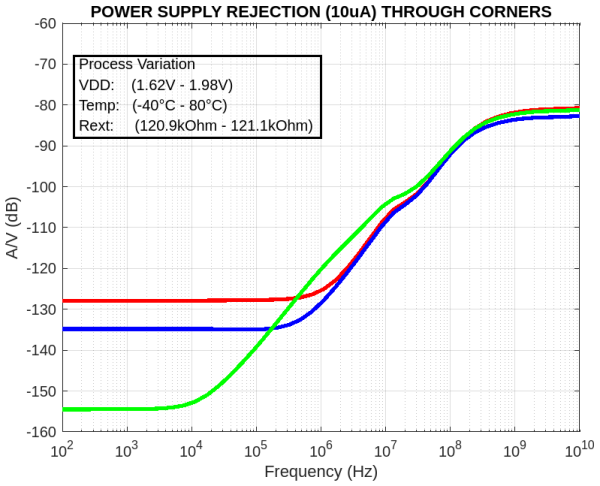

Figure 29. PSR 10uA

5.5.1.2. Noise Although the graphs of the noise spectral densities do not provide clear information for qualitative analysis, it is possible to visually observe the separation between the extreme corners obtained. Additionally, one can appreciate how the characteristics of the noise vary at different frequencies, which contributes to a better understanding of the system's behavior under various operating conditions.

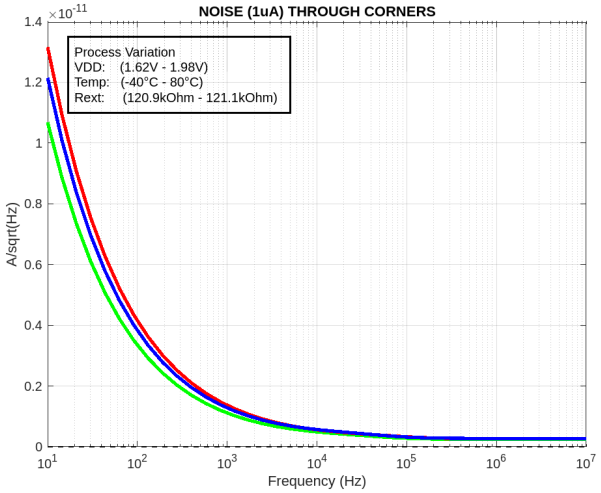

Figure 30. Noise 1uA

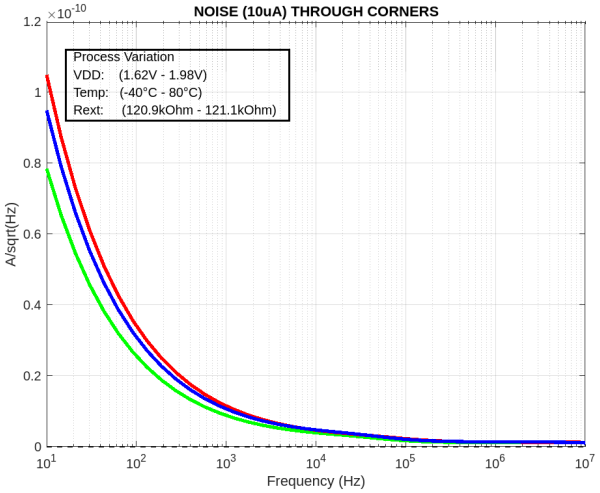

Figure 31. Noise 10uA

5.5.1.3. Stability In terms of stability, significant variations in gain are observed within the magnitude Bode plot, reaching even the calculated minimum extreme in section 2.1. Additionally, this loss of gain induces a shift in the poles that determine the circuit's frequency response. However, even under these circumstances, the stability margins are not significantly affected, as can be seen in Figure 32.

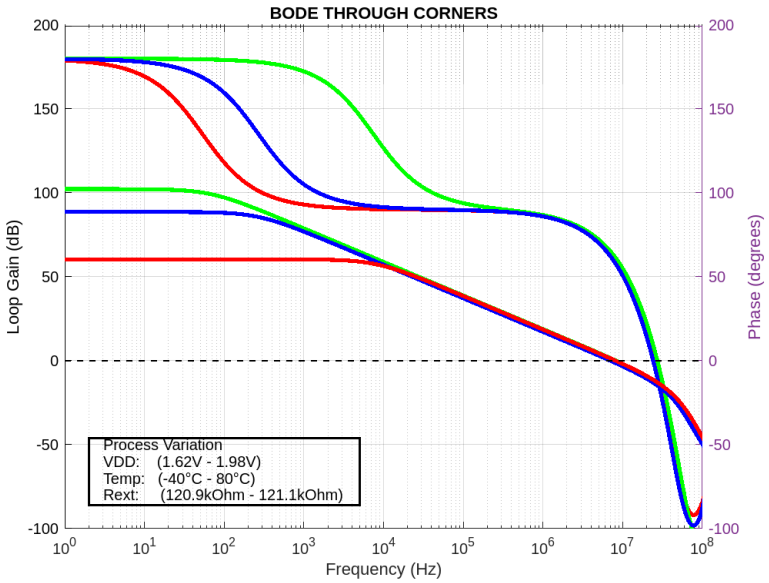

Figure 32. Bode Plot

5.5.1.4. Iout Finally, since the most significant result is the high-precision currents, graphs have been generated to illustrate the effects of the various considered variations on each of these normalized currents.

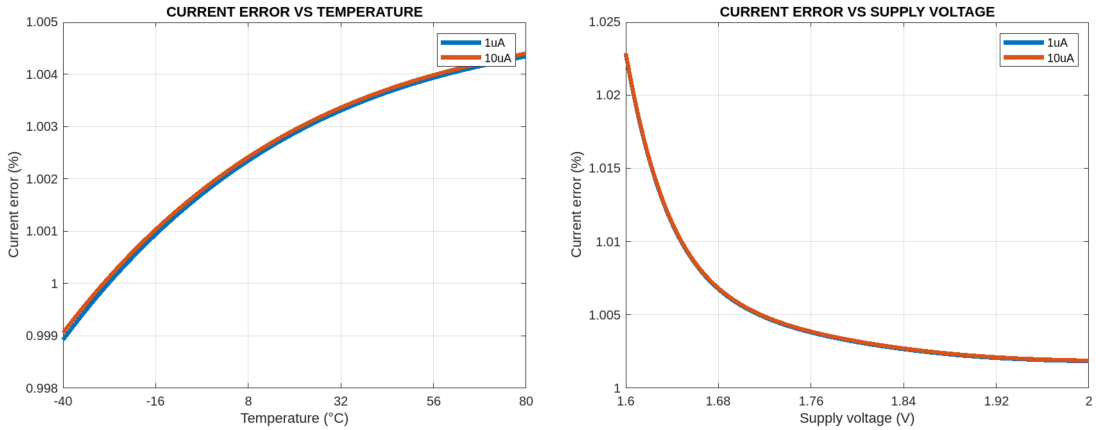

Figure 33. Iout Variations

5.5.2. Final corners results During this phase, detailed measurements of key parameters are conducted, and values are adjusted as necessary to ensure that the circuit meets the provided specifications.

Table 8. Post Layout Corners Result

PARAMETER		SPECIFICATIONS			POST-LAYOUT		
Range		Min	Typ	Max	Min	Typ	Max
VDD [V]		1,62	1,80	1,98	1,62	1,80	1,98
Temp [°C]		-40,00	37.33	125,00	-40,00	37.33	80,00
Rext [kΩ]					120,90	121,00	121,10
Iqscnt [µA]				64,16	13,05	15,30	19,55
Phase Margin [°]		55,00	65,00		53,34	61,77	67,34
Gain Margin [dB]		10,00			11,31	13,34	14,95
I1 [µA]		0,97	0,995	1,02	0,99	1,01	1,02
I10 [µA]		9,78	9,995	10,13	9,83	10,05	10,13
I1	PSR [dB]		-166,00		-195,00	-156,00	-148,00
	Noise [nA]			1,55	0,74	0,81	0,92
I10	PSR [dB]		-145,00		-154,00	-136,70	-128,00
	Noise [nA]			10,93	5,56	6,31	7,70
Area [µm²]				11427	1620		

As can be observed, most specifications experience reductions in their values during the post-layout phase. This reduction was expected, as more real-world values than ideal ones are considered in this process. However, despite these reductions, the obtained results still satisfactorily meet the specifications, providing greater certainty about the chip's operation once manufactured. This consistency in meeting the specifications underscores the robustness of the design and its ability to effectively adapt to real-world conditions, thus ensuring reliable circuit operation once implemented.

5.6. COMPARISON WITH OTHER PROJECTS

The Table 9 allows for a comparison between previously developed projects and the current one, highlighting the characteristics and main outcomes of each project. This facilitates an assessment of the design's strengths and weaknesses. Multiple projects developed within the OnChip research group are included, with the TUCAN project being among the most significant[19].

Table 9. Results Comparison

	Research Paper**[20]	Research Paper**[21]	Research Paper**[22]	Research Paper*[23]	Research Paper**[24]	TUCAN*		This work **	
Technology (nm)	180	180	180	350	80	180		28	
VDD (V)	3,3	3,3	-	1.3	1	3,3		1,8	
Temp Range (ºC)	-40 - 125	-40 -125	0 -110	-20 - 80	-	-40 - 125		-40 - 80	
Vref (V)	1,26	-	1,24	-	0.15	1,2		1,213	
Output Current (A)	5u	2,7n	6,6n	9,95n	100u	1u	10u	1u	10u
Current Error Rate (Max.)	1%	8 %	12%		2%	3,90%	2,67%	2,10%	1,98%
Current Consuption (uA)	12	0,013	-	0,0681	94	61,03		16,2	
Area (um)2	6000	9268	55000	128100	18000	11427		1620	

[19] * Pre Layout Simulation **Post Layout Simulation

6. CONCLUSIONS AND FUTURE WORK

6.1. CONCLUSIONS

- A modular polarization circuit was designed with capabilities to generate currents in the microampere range using 28 nm CMOS technology, meeting the specifications set by the Onchip research group, along with a complete design flow execution that included analysis, schematization, simulation, layout structuring and post-layout simulation with satisfactory results.

- An exhaustive analysis of current distribution throughout the design was carried out, enabling precise manipulation of transistor transconductance and resistance to directly control operational ranges. This fine-tuning capability was fundamental as it allowed for optimizing system performance, thus ensuring compliance with established design criteria solely through precise current management.

- An alternative method of indirect compensation was implemented to replace the classic Miller compensation. This involved replacing the RC network with a transistor in capacitor mode within a feedback loop connected to the lower cascode of the amplifier module. This approach allowed for manipulation of stability margins and system bandwidth at will by varying the aspect ratio, thereby reducing area consumption to the equivalent of a transistor in capacitor mode (Moscap).

- An optimal reduction in consumed area was achieved through the identification, reduction, and/or elimination of large components. Among the adjustments made to achieve this goal is the maximization of Vov voltage in the current mirrors, as well as the replacement of the compensation RC network. Additionally, during layout creation, a common triple centroid design was implemented in the current mirrors, which not only optimized the area consumed by them but also enhanced

transistor matching.

- Once the final simulation was completed in conjunction with the extraction of parasitic capacitances and resistances, a degradation in the obtained values compared to the specifications was noted, as expected since it represents a more realistic approximation of the values that will be obtained by the physical circuit. However, even with this reduction, the results fully meet the given specifications, confirming the level of resilience of the design and the quality of the structured layout.

6.2. FUTURE WORK

- Considering that the design flow for this project was fully implemented and satisfactory values were achieved in the post-layout simulation, it is safe to say that adjustments to the current design will not be necessary. However, if desired, it is possible to explore modifying the circuit architecture by replacing the external resistance with an internal one. This would involve designing a trimming circuit and its corresponding layout. Although not strictly necessary, this could be an interesting design activity to consider.

- On the other hand, as mentioned at the outset of this document, this work is part of a larger project undertaken by the Onchip research group. Our current objective is to develop a System on Chip (SoC) from scratch, with undergraduate students responsible for the basic functional modules. Once each of the proposed modules is individually developed, all circuits will be compiled into a single SoC, which will then be sent for manufacturing.

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