AN 8-BIT GENERAL PURPOSE IO FOR A 32-BIT MICROCONTROLLER

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Giovanny Castillo Castillo

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RESUMEN

TÍTULO 8-BIT DE ENTRADA/SALIDA DE PROPÓSITO GENERAL PARA UN MICROCONTROLADOR DE 32-BIT.[*]

Autores Anderson Joan Agudelo Molina, Giovanny Castillo Castillo.[**]

Palabras clave Microelectrónica, GPIO, APB, AXI-4 Lite, periférico, protocolo, arquitectura, microcontrolador.

DESCRIPCIÓN

En este trabajo se proponen dos sistemas de control digital para un periférico *General Purpose Input Output* (GPIO). Un GPIO es un circuito que se puede programar como entrada o salidas digitales y es de propósito general, es decir se puede usar en gran variedad de aplicaciones. Estos circuitos al ser implementados en un microcontrolador pueden ser programados por el usuario en tiempo real. Se discuten las estructuras típicas de un GPIO cuando funciona como entrada o salida y se realiza un análisis de sus características y funcionamiento.

El GPIO será implementado en el primer microcontrolador de 32-bit en arquitectura RISC-V diseñado por el grupo de investigación *OnChip*. Dichos controladores están basados en los protocolos *Advanced Peripheral Bus* (APB) y *Advanced Extensible Interface 4 Lite* (AXI4-*Lite*). La metodología de diseño se centra en la optimización del área, la velocidad y el consumo de energía. Los resultados experimentales indican una densidad de potencia total de 6.5µW/MHz para el controlador digital AXI4-*Lite* y 2.8µW/MHz para el controlador digital APB. El área ocupada por el controlador digital AXI4-*Lite* es de $3024\mu m^2$ y $2846\mu m^2$ para el controlador digital APB. El GPIO se implementó como parte de *System-on-a-chip* (SoC) en tecnología CMOS de 130nm y servirá para futuros proyectos en el área de la microelectrónica.

[*] Trabajo de grado.

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Director: Elkim Felipe Roa Fuentes. Co-Director: Ckristian Ricardo Esteban Duran Blanco.

ABSTRACT

TÍTLE AN 8-BIT GENERAL PURPOSE IO FOR A 32-BIT MICROCONTROLLER.[*]

Authors Anderson Joan Agudelo Molina, Giovanny Castillo Castillo.[**]

Keywords Microelectronics, GPIO, APB, AXI-4 Lite, peripheral, protocol, architecture, microcontroller.

DESCRIPTION

In this work two digital control systems for a General Purpose Input Output (GPIO) are proposed. A GPIO is a circuit that can be programmed as digital inputs or digital outputs and it is of general purpose, it can be used in a wide variety of applications. When these circuits are implemented in a microcontroller can be programmed by the user in real time. The typical structures of a GPIO when it functions as input or output are discussed and an analysis of its characteristics and functioning is performed.

The GPIO was implemented in the first 32-bit RISC-V architecture based microcontroller designed by the research group OnChip. These controllers are based on the Advanced Peripheral Bus (APB) and Advanced Extensible Interface 4 Lite (AXI4-Lite) protocols. The design methodology focuses on optimizing the area, speed and energy consumption. The experimental results indicate a total power density of 6.5µW/MHz for the AXI4-Lite digital controller and 2.8 µW/MHz for the digital APB controller. The area occupied by the AXI4-Lite digital controller is $3024\mu m^2$ and $2846\mu m^2$ for the digital APB controller. The GPIO was implemented as part of System-on-a-chip (SoC) in 130nm CMOS technology and will serve to future projects in the microelectronic area.

[*] Bachelor degree.

[**] Faculty of Physico-Mechanical Engineering. School of Electronics and Electrical engineering and telecommunications. Advisor: Elkim Felipe Roa Fuentes. Co-Advisor: Ckristian Ricardo Esteban Duran Blanco.

INTRODUCTION

IO circuits are used as an interface that allows a safe communication between the chip internal circuits and the external data. Considering that voltage levels of external data can be different from the chip's, IO circuits are interposed to communicate signaling and convert it into data that the core can recognize. The most common IO circuits are the GPIOs which can operate as input, output or bidirectional circuits. The GPIO are distinguished by the applications in which they are applied and these are manifested in the nature of signals they interact, either analog or digital signals.

GPIO ports are incorporated in most SoCs, usually as programmable bidirectional digital ports. Within a SoC, the digital core requires communication with peripherals around it. For instance, a 32-bit microcontroller commonly uses a communication bridge between the peripherals and the RISC-V processor [1]. Establishing defined structures of communication is necessary to get an effective and synchronized transaction between the instances driven the GPIO and the GPIO. AXI4-Lite [2] and APB protocols [3] are used in this work for proposing low area and low power digital controllers. Lean controllers are possible by taking into consideration the design details of the IO circuitry.

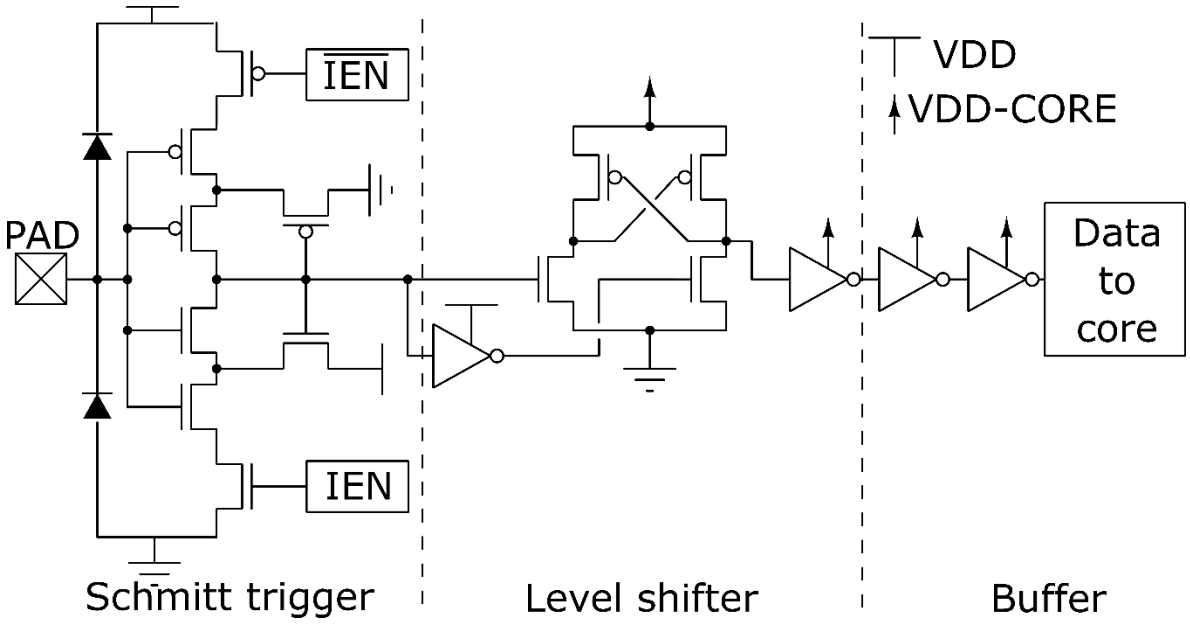
1. ANALYSIS OF GPIO STRUCTURE

Reported literature discusses individual blocks of the IO interface, such as the ESD devices, drivers and level shifters, but there is not a well-documented work on the GPIO circuitry and the digital interface. This paper presents the two proposed digital controllers and discusses details of the common implementation of a GPIO input and output circuit.

1.1 INPUT BUFFER TOPOLOGIES

In the case that a GPIO is programmed as an input, the circuit must be configured to receive and translate data from the PAD so that the processor can process them. Due to the above, the GPIO input circuit must include protection circuits against ESD, level shifter, and buffer stages.

Figure 1. A conventional architecture for a GPIO input circuit.



A common implementation of a GPIO input circuit is indicated in Fig. 1, this design incorporates a Schmitt trigger, an ESD protection, a level shifter, and a buffer stage.

The CMOS ICs are susceptible to electrostatic discharge (ESD) due to their small size cannot dissipate large amounts of energy. The chip ESD occurrences are common due to manual or mechanical handling and present a high risk to the chip, because the manifestation of high currents may damage the internal circuitry. The ESD protection circuits based on the use of NMOS transistors and diodes are shown in Fig. 2 and Fig. 3, they have an NMOS clamp, the clamp is used to conduct the current generated in an ESD to the ground and thus protect the ICs.

Figure 2*. ESD circuits topology with NMOS transistors.*

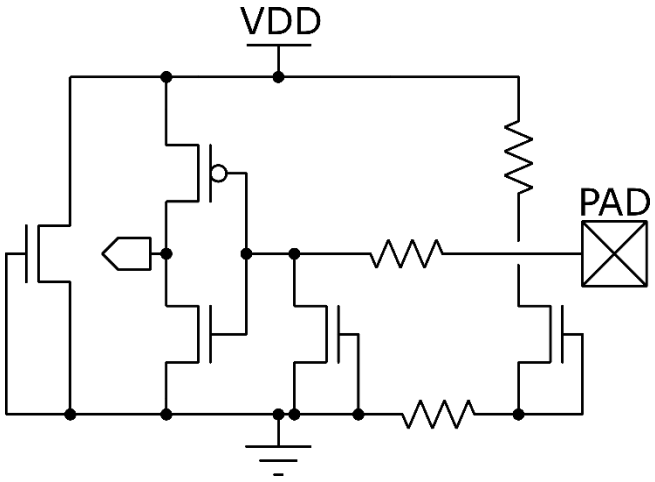


Figure 3. ESD circuits topology with diodes.

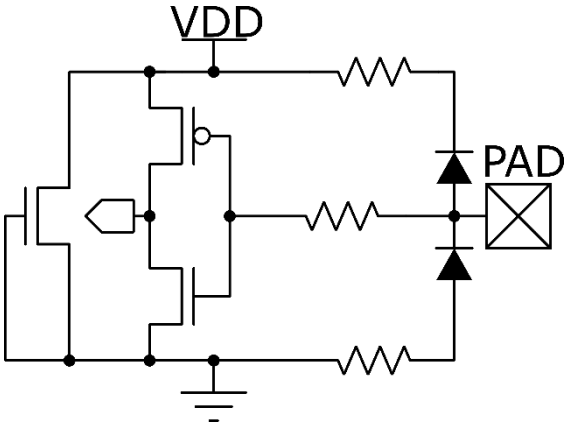
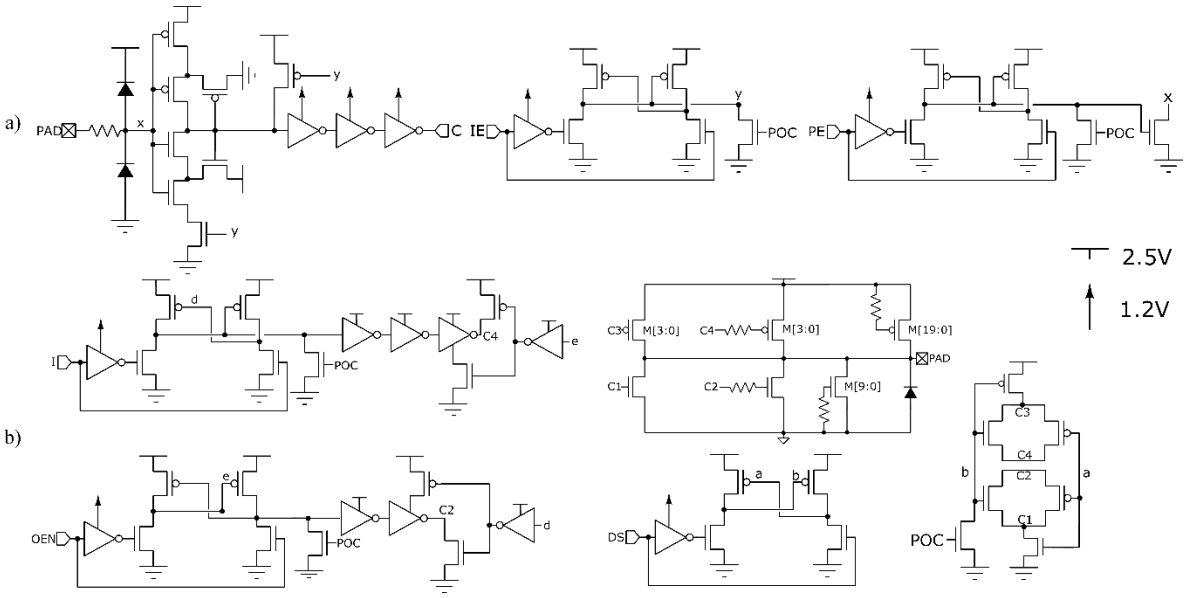
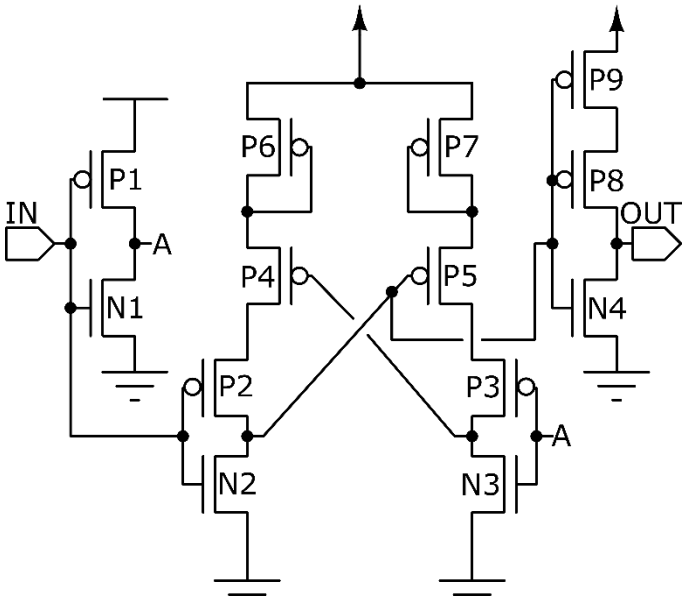


Figure 4. Selected cell schematic: a) input schematic circuit, b) output schematic circuit.



The internal circuits generally do not have the same voltage than the chip peripherals. Consequently, a level shifter is required to convert one voltage into another. Fig. 1 and Fig. 5 show a traditional level shifter architecture, the first figure has a PMOS stack (P8 and P9) limit the leakage current, P6 and P7 diode-connected transistor help to reduce the emitter voltage and the threshold voltage, therefore P4 and P5 can be switched on more quickly .

Figure 5. A conventional topology for a low-power level shifter.

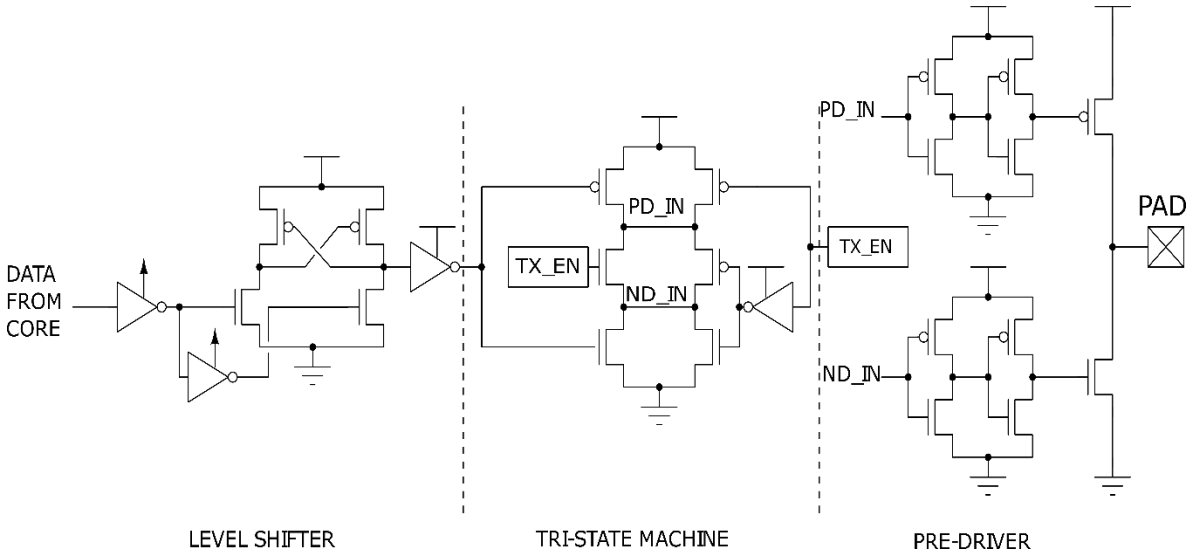


The general diagram of the selected cell is presented in Fig. 4, it has a Schmitt trigger, level shifter, a tri-state machine, ESD protection, pull-down enable, and driver stages.

1.2 OUTPUT BUFFER TOPOLOGIES

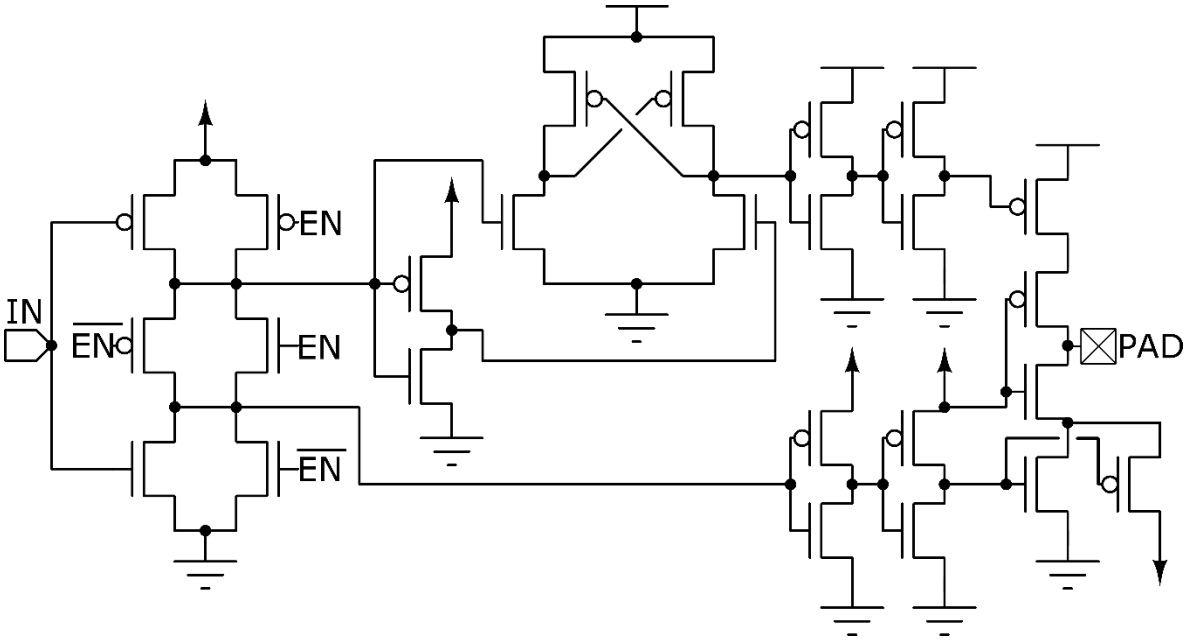
In the case that the GPIO is working as an output, the signals go from the core to the PAD. The design normally has a level shifter, a tri-state machine, and driver stages; Fig. 6 shows this structure. Additionally, other frameworks can be implemented when the circuit needs to work with high-level outputs, therefore it is necessary to implement other topologies with specific functions.

Figure 6. ***A conventional architecture for a GPIO output circuit.***



Depending on the required parameters, alternative designs of output-buffer circuits can be implemented. Fig. 7 shows a proposed design to drive high-voltage signals for peripheral component interconnect extended (PCI-X) applications. The PCI-X is a 3.3V interface, IO structures in this voltage level, will suffer the high-voltage gate-oxide stress problem. The proposed topology can solve this problem .

Figure 7. Another conventional topology for a GPIO output buffer [7].



1.3 IMPLEMENTED INPUT CELL.

The PAD input process to C is shown in Fig. 3(a), this process is composed of an ESD protection, a Schmitt-trigger input control, a level shifter, a pull-down enable, and buffers. Sometimes, the reading process can be affected by electronic noises. A suitable circuit to avoid the above is the Schmitt trigger, which is a special type of comparator that can be implemented using hysteresis to prevent false-state changes due to noise. Pull-down defines a logic level when the external devices are disconnected or the port is in high impedance state.

1.4 IMPLEMENTED OUTPUT CELL.

The output process I to PAD is shown in Fig. 4(b), it is composed of a level shifter, buffers, a tri-state machine, and driver stages. The tri-state machine is the circuit

that generates separated controls for P-drivers and N-drivers. This is achieved by ensuring that the power-on circuit is turned off before the other is turned on. Drivers are responsible for the regulation of power flow and ensure the supply voltage and current independently of any change produced in the system. Furthermore, these prevent voltage fluctuations which can cause system drivers by excessive voltages. Power On Control (POC) system is necessary to prevent IO unknown states. An unknown state may cause high IO crowbar current or bus contention when the IO voltage is powered up before the core voltage.

2 IMPLEMENTATION OF THE DIGITAL CONTROLLERS

This section presents the digital control system designed for the selected GPIO cell. The controllers are focused on the implementation of the APB bridge and AXI4-Lite protocols. Using Verilog and the selected cell circuit it is viable to design two digital blocks that enable effective communication between the GPIO peripheral and the RISC-V processor. The datapath is designed to control the IO cell and, at the same time, is controlled by a state machine whose operation is based on the AXI4-Lite protocol or APB bridge.

Figure 8*. Proposed AXI4-Lite state machine*

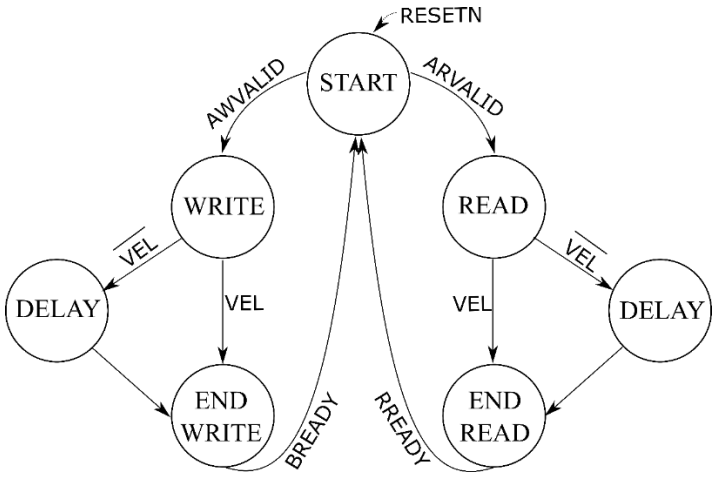
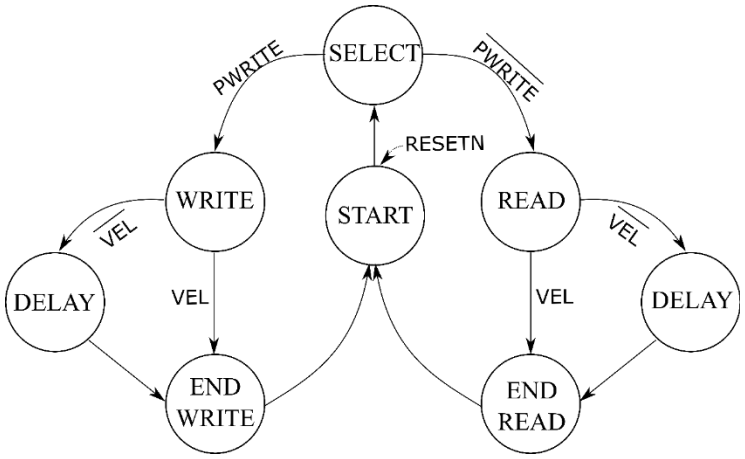


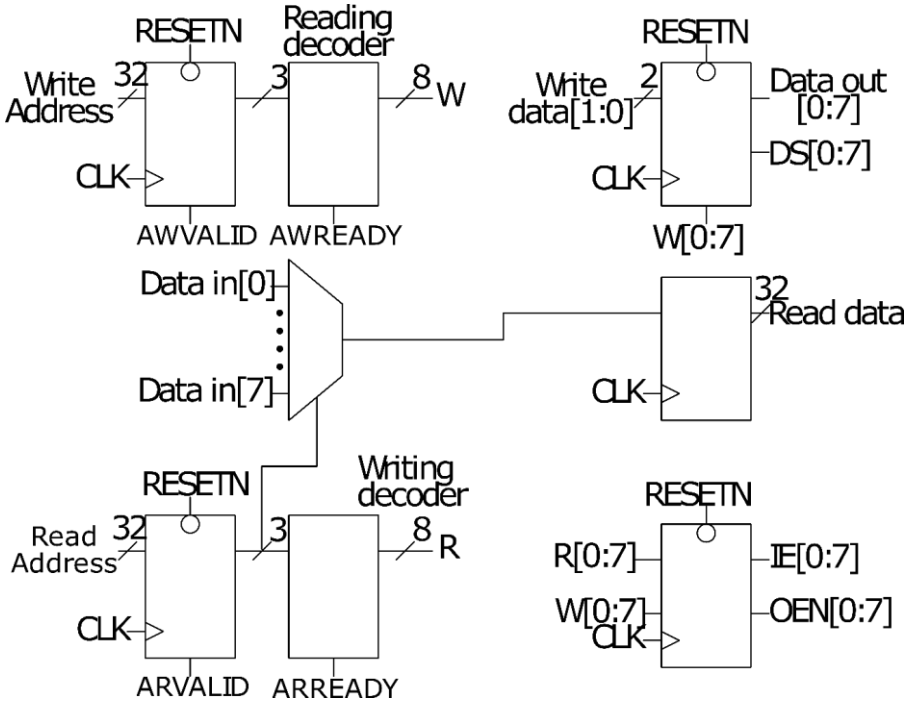
Figure 9. Proposed APB state machine



2.1 AXI4-LITE DIGITAL CONTROLLER

The design of the AXI4-Lite digital controller incorporates a state machine as shown in Fig. 8, and a datapath as in Fig. 10. The state machine has two main control loops, which integrated the control signals of the AXI4-Lite protocol. One loop belongs to the reading transaction, the other control loop belongs to the writing transaction. The datapath is designed to synchronize with the state machine and its structure is based on two digital circuits, one of them works for the writing transaction and the other with the reading transaction, configuring the cell as output or input respectively and connecting with the 32-bit bus.

Figure 10*. Proposed AXI4-Lite GPIO datapath.*



The logic operation of the AXI4-Lite digital controller is based on the following steps:

***Acquisition of the address*:** The master sends the *AWVALID* or *ARVALID* signals. When the datapath receives them, the address is stored in a register.

Enabling GPIOs: The state machine sends *ARREADY* or *AWREADY* signals to enable writing or reading decoder respectively. The value of the address [2:0] generates R and W signals. When these pass through the flip-flop, the input enable (*IE signal*) or output enable (*OEN signal*) turn on the reading or the writing circuit of the selected GPIO cell.

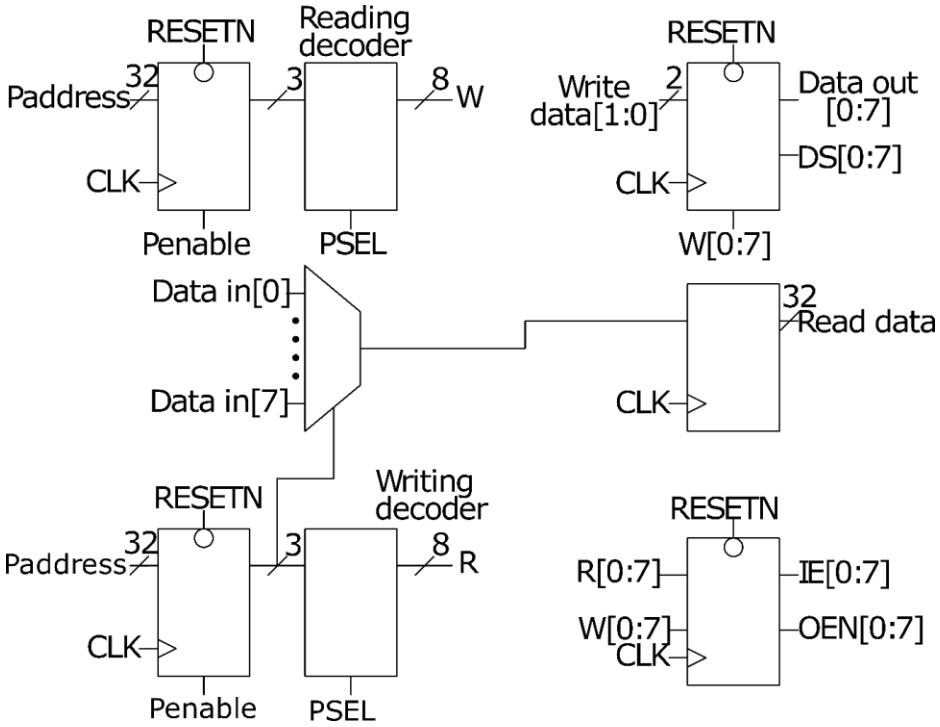
Transaction data: At this stage, the data is acquired. For the reading phase, the *RVALID* signal indicates that the data is available. For the writing process, the

signal *WVALID* has similar function like *RVALID* signal. The process is terminated when *BREADY* or *RREADY* are turned on.

2.2 APB BRIDGE DIGITAL CONTROLLER

Similar to the case of the AXI4-Lite protocol, the APB digital controller incorporates a state machine as shown in Fig. 9, and a datapath as in Fig. 11. The APB protocol in contrast to AXI4-Lite protocol requires fewer signals to communicate with peripherals and its power consumption is lower.

Figure 11*. Proposed APB GPIO datapath.*



The logic operation of the APB digital controller is based on the following steps:

Receiving address: The *Paddr* signal is sent through the APB bridge to the GPIO peripherals, which the main function is to select the enable GPIO PAD.

Enabling input or output: The signal *PWRITE* indicates the writing if is "one" or reading process if is "zero".

Transaction data: At this stage, the data is read or written. The state machine sends *PREADY* signal that indicates a correct process.

3. RESULTS

The AXI4-Lite and APB digital controllers are fully synthesized in 130nm CMOS technology to be include in a full 32-bit RISC-V based microcontroller. Synthesis results of the GPIO digital controller are shown in Table 1 using a clock frequency of 100MHz. The final AXI4-Lite digital controller layout is presented in Fig. 12, its area is 3024μm^2 and its power consumption is 6.52 µW/MHz. Fig. 13 shows the microphotograph microcontroller with an 8-bit GPIO using the proposed digital controller.

Measurements show that the power performance adjusts to the results obtained during design. Further testing has shown that the GPIO is capable to work when the AXI4-Lite bus is clocked at 200MHz.

The highlight ports in Fig. 11 are connected directly to the pads of the chip without additional external buffering.

Table 1. Power, timing and area breakout of the GPIO digital controllers.

Core	Power [μW/MHz]	Time Slack [ns @ 100MHz]	Area [μm^2]
AXI4-Lite-GPIO	6.52	7.9	3024
APB-GPIO	2.80	8.6	2846

Figure 12. AXI4-Lite digital controller on RISC-V based processor.

Figure 13. Microphotograph of the RISC-V based microcontroller.

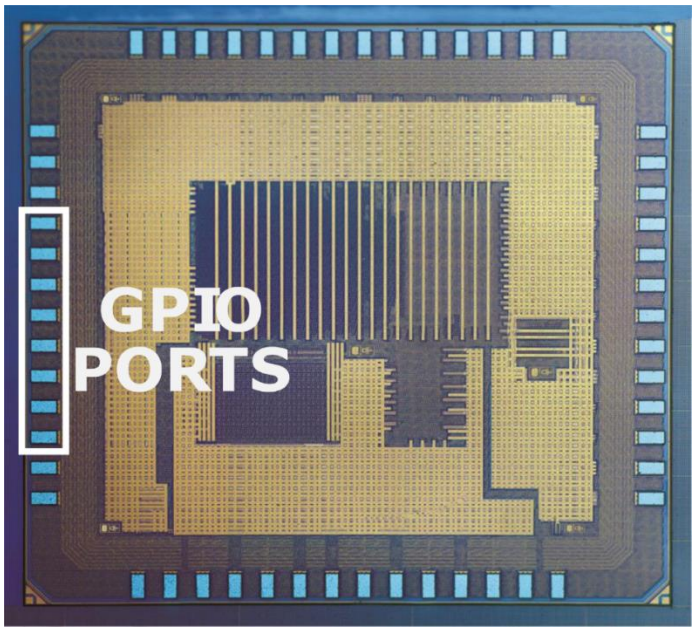
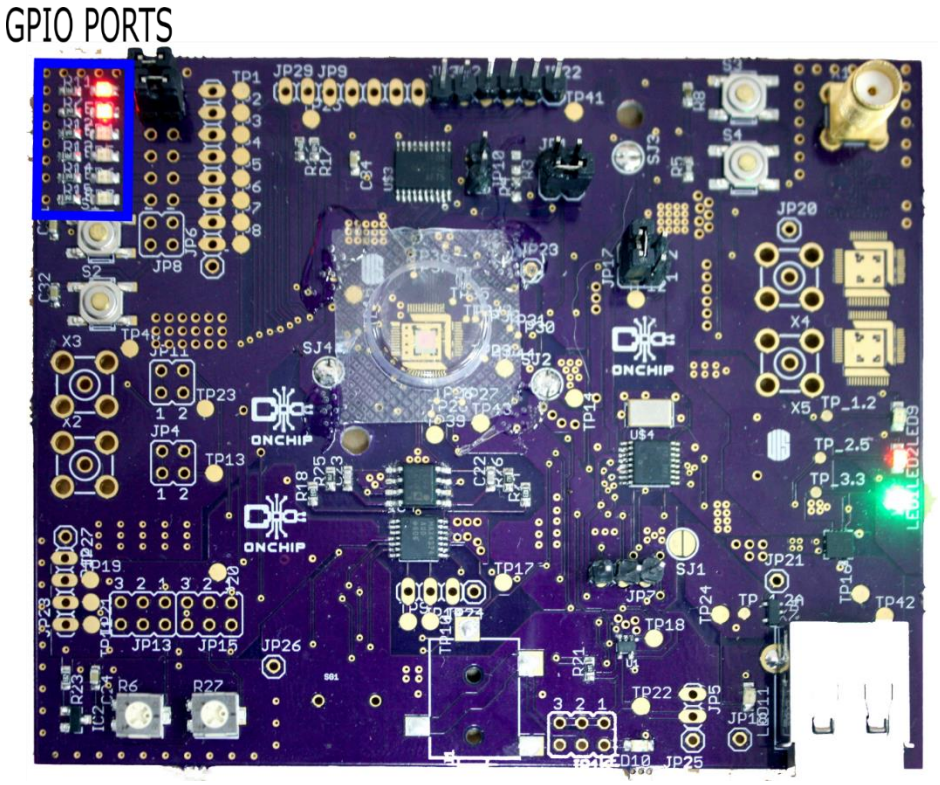


Figure 14. Test setup board for the 32-bit microcontroller.



4. CONCLUSION

An interconnected GPIO architecture is proposed with the RISC-V based processor through a circuit designed based on the AXI4-Lite protocol and APB bridge. The design of the GPIO digital controllers for the first RISC-V based microcontroller is emphasized optimization of the area, speed and power consumption. The contribution of work conducted RISC-V microcontroller development as the first of its kind free hardware. The considerations made regarding the design, selection and implementation of GPIO structure can be applied to future jobs.

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