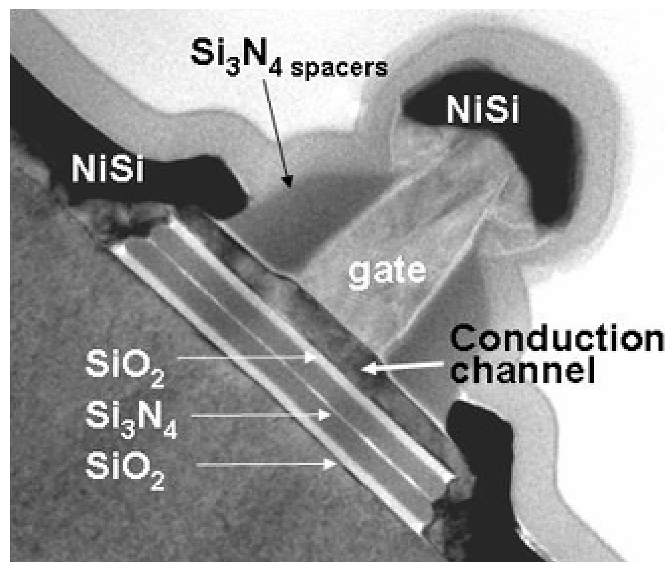
ESTUDIO DE LAS PROPIEDADES ELÉCTRICAS DE TRANSISTORES NANOMÉTRICOS DE CAPA DELGADA BASADOS EN LA TECNOLOGÍA "SON"

ANDRES LEONIDAS QUIROGA PINEDA



UNIVERSIDAD INDUSTRIAL DE SANTANDER
FACULTAD DE INGENIERIAS FISICO MECÁNICAS
ESCUELA DE INGENIERIAS ELÉCTRICA, ELECTRÓNICA Y DE TELECOMUNICACIONES
BUCARAMANGA
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ANDRES LEONIDAS QUIROGA PINEDA

Este proyecto es presentado como requisito para optar al título de Ingeniero Electrónico

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RESUMEN

TITULO: ESTUDIO DE LAS PROPIEDADES ELÉCTRICAS DE TRANSISTORES NANOMÉTRICOS DE CAPAS DELGADAS BASADOS EN LA TECNOLOGÍA "SON".[*]

AUTOR: QUIROGA PINEDA, ANDRES LEONIDAS[**]

PALABRAS CLAVES: Transistor MOSFET, efecto cuerpo, pendiente de umbral, SON, LSOI, tensión de umbral, espesor de capa, longitud de canal, BOX, oxido de compuerta, modelo de interfase, tensión del substrato.

DESCRIPCIÓN:

El procedimiento LSOI (Localised Silicon On Insulator) es un innovador enfoque de bajo costo, dedicado a los dispositivos de baja potencia; este procedimiento esta basado en la tecnología SON (Silicon On Nothing), donde la capa de aislante típica (SiO_2) de los transistores SOI puede ser remplazada por diferentes tipos de aislante.

En el presente informe se muestra el estudio hecho de las propiedades eléctricas de los transistores LSOI, la variación de estas propiedades en relación a la longitud de compuerta (Gate), de los diferentes espesores, de las capas bajo la compuerta (óxido de compuerta, canal, aislante, sustrato) y la densidad de estados de interfase entre cada material. Con el fin de facilitar el cálculo de los parámetros analizados se desarrollaron aplicaciones informáticas específicas en VBA (Visual Basic for Applications). El modelo establecido (Lime&Fosum) se estudio y se comprobó experimentalmente, se pudo concluir que los dispositivos LSOI tienen un fuerte valor de coeficiente de acoplamiento, lo que permite controlar de manera eficiente la corriente de fuga (Ioff).

A través de las medidas experimentales y los resultados obtenidos hemos comprobado que es más grande la variación en el valor del coeficiente de acoplamiento cuando se trabaja con espesores más pequeños.

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[*] Modalidad: Trabajo de grado.

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SUMMARY

TITLE: STUDY OF THE ELECTRICAL PROPERTIES OF THIN-FILM NANOMETRIC TRANSISTORS BASED ON SILICON ON NOTHING TECHNOLOGY. *

AUTHOR: QUIROGA PINEDA, ANDRES LEONIDAS**

KEY WORDS: MOSFET transistor, body factor, subthreshold swing, SON, LSOI, threshold voltage, thickness film, gate length channel, BOX, oxide substrate, interface model, substrate voltage.

DESCRIPTION:
This report refers to work completed during my internship with STMicroelectronics at CEA (French Atomic Energy Agency), France from Mars 19th,2007 until September 14th, 2007. At CEA I worked at the Leti-MINATEC laboratory one of Europe's principal centre in Micro and Nano-technologies. The work was located at the Nanotechnologies Department at the Nanoelectronic Devices Laboratory.

My work consisted to study the electric properties of the Localized SOI transistors and their variations according to the length of gate, the different films- thicknesses under the gate (oxide-gate, channel, box, substrate) and the interface state density. Therefore, I analyzed the coupling phenomenon between the silicon conduction channel and the substrate by taking analytical models established and the experimental results obtained during the electrical measurements on several chips into different silicon wafers. In order to facilitate the parameters calculation with the established analytical models, and the experimental data processing I worked with VBA (Visual BASIC for Applications) Excel.

Some of the results of this study were used for elaborate an article on LSOI transistors presented at the International Electron Devices Meeting (IEDM): “Localized SOI technology: an innovative Low Cost self-aligned process for Ultra Thin Si-film on thin BOX integration for Low Power applications “ [Monfray 07].

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* Degree Project

** Physics Mechanical Engineering Faculty. Electric, Electronic and Telecommunications School. Director: Dr. Stéphane Monfray (STMicroelectronics-CEA Leti, France). Co-Director: Dr. Azzedine Gaci (CPE Lyon, France).

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GLOSSARY

BOX	Buried Oxide
CMOS	Complementary Metal-Oxide Semiconductor
DIBL	Drain Induced Barrier Lowering
DIT	Interface Trap Density
FD	Fully Depleted
HF	Hydrofluoric Acid
HfO2	Hafnium Oxide
LSOI	Localised Silicon on Insulator
MOS	Metal-Oxide-Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field-Effect
PECVD	Plasma Enhanced Chemical Vapor Deposition
S	Subthreshold Swing
S\D	Source Drain
SiGe	Silicon Germanium
SoC	System-on-Chip
SOI	Silicon on Insulator
STI	Shallow-Trench Isolation
SON	Silicon on nothing
Tdep	Depletion Thickness
TSi3N4	Silicon nitride Thickness

Vb, Vg2, Vsub	Substrate Voltage
VBA	Visual Basic for Applications
Vd	Drain Voltage
VDT	Voltage Doping Transformation
Vg	Gate Voltage
Vth	Subthreshold Voltage
γ	Body Factor

INTRODUCTION

The work described in this report belongs to those new technologies which improve MOSFET transistor characteristics while maintaining low cost. This internship is part of the advanced CMOS development team located at STMicroelectronics, Crolles2 in France.

At Leti, I worked with the Nanotechnologies Department in the Nanoelectronic Devices Laboratory. Here, 40 researchers work in several topics but all of them in relation with the nanoelectronics and the last advances in this technology, it is possible to find study subjects like: Double Gate transistors, FinFet transistors, Silicon Nanowire transistors, floating-gate memories, among others. It is in this rewarding atmosphere of research that my internship has been developed.

The aggressive reduction of MOS transistor dimensions has brought with it physical economical and technological problems, but has promoted new technologies at the same time. Among these new technologies we find one very promising by its characteristics and results: Silicon on Nothing (SON).

Conventional CMOS processes have supported many generations of shrinking, with each new generation bringing predictable advantages in terms of cost, speed and power consumption. However they are rapidly approaching a brick wall where the cost of further progress will outweigh the benefits. Today’s 45nm production technology is close to the cusp of this historic trend and it is highly probable that entirely new transistor architectures will be required below 32nm.

Semiconductor manufacturers have been investigating alternative transistor architectures such as double-gated MOSFETs and SOI (Silicon-on-Insulator) technology but a major problem is the manufacturability of these processes.

The transistor architecture conceived by the STMicroelectronics, called Silicon-on-Nothing (SON), offers a highly promising solution to this problem. SON allows extremely thin buried dielectrics and silicon films, no more than a few nanometers thick, to be fabricated with high accuracy within the methodologies of conventional epitaxial technology. This characteristic positions it as a leading candidate for future system-on-chip (SoC) technology where ever-increasing levels of system integration must be achieved with processes that are compatible with spiraling high-volume/low-cost manufacturing constraints.

In consequence, the objective of my work was to study more deeply the electric properties of this SON-based device (called Localised SOI), in particular the coupling phenomenon between the conduction channel and the substrate.

1. COMPANY PROFILE AND INTERNSHIP LOCATION

1.1 STMICROELECTRONICS

STMicroelectronics was created in 1987 by the merger of SGS Microelettronica of Italy and Thomson Semiconducteurs of France with the aim of becoming a world leader in the sub-micron era. The new company pursued an aggressive growth strategy, investing heavily in R&D, forging strategic alliances with blue-chip customers and academia, building up an integrated presence in major economic regions, and honing one of the world's most efficient manufacturing operations.

Since its formation, ST has grown faster than the semiconductor industry as a whole and it has been one of the world's Top Ten semiconductor suppliers since 1999. Today, an unrivalled combination of silicon and system expertise, manufacturing strength, Intellectual Property (IP) portfolio, industrial and academic partnerships, and one of the industry's broadest product ranges makes ST a world leader in developing and delivering semiconductor solutions across the spectrum of microelectronics applications.

Market Position

ST is one of the world's largest semiconductor companies, with net revenues of US$9.85 billion in 2006 and market leadership that is spread across many fields. For example, according to the latest industry data, ST is the world's fifth largest semiconductor company and has leading positions in sales of Analog Products, Analog Application Specific Integrated Circuits and Analog Application Specific Standard Products. ST is also number one in camera modules for mobile phones,

number two in discretes and analog, and number three in NOR Flash, as well as in the application segments of Automotive, Industrial, and Wireless. ST is also the leading supplier of semiconductors for set-top boxes and power management devices. Furthermore, ST was the 3rd biggest semiconductor supplier in China in 2005.

Product Portfolio

ST offers one of the world's broadest product ranges, with over 3,000 main types of products. The carefully balanced portfolio includes both application-specific products containing a large proprietary IP content and multi-segment products that range from discrete devices to high-performance microcontrollers. The Company's sales are well balanced between the industry's five major high-growth sectors: Communications (38%), Consumer (16%), Computer (17%), Automotive (15%) and Industrial (14%). ST pioneered and continues to refine the use of platform-based design methodologies for complex ICs in demanding applications such as set-top boxes, secure smart cards and mobile multimedia, which minimizes development time and cost. The balanced portfolio approach allows ST to address the needs of all microelectronics users, from global strategic customers for whom ST is the partner of choice for major System-on-Chip (SoC) projects to local enterprises that need fully-supported general-purpose devices.

Research and Development

Since its creation, ST has exhibited an unwavering commitment to R&D. In 2006, ST spent US$1.667 billion in R&D, which was some 16.9% of its 2006 revenues. That effort produced 607 patent applications in 2006, maintaining ST's track record as one of the industry's most innovative and prolific inventors. ST is also active in numerous collaborative research projects worldwide as well as playing a key role in Europe's advanced technology research programs such as MEDEA+ and the framework programs of the European Union. It is also a leader in important

forward-looking industry initiatives such as ENIAC (European Nanoelectronics Initiative Advisory Council) at the European level or the “Poles de Compétitivité” (e.g. Minalogic near Grenoble and SCS in the Provence area) at the regional level.

The Knowledge Network

ST has developed a worldwide network of strategic alliances, including product development with key customers, technology development with customers and other semiconductor manufacturers, and equipment- and CAD-development alliances with major suppliers. These industrial partnerships are complemented by a wide range of research programs conducted with leading universities and research institutes around the world. By augmenting its rich portfolio of proprietary technologies and core competencies with complementary expertise from a variety of carefully chosen strategic partners, ST has developed an unsurpassed capability to offer leading-edge solutions to customers in all segments of the electronics industry.

Many of ST’s research and development programs are managed by its AST (Advanced System Technology) organization, whose mission is to develop the strategic system knowledge that will be required within 3-5 years by ST’s product divisions. Among AST’s significant recent achievements are innovative technologies for digital consumer, networking, mobile security, and on-chip interconnect.

1.2 CEA-LETI

The CEA is the French Atomic Energy Agency (Commissariat à l'énergie atomique). It is a public body established in October 1945 by General de Gaulle. A leader in research, development and innovation, the CEA mission statement has two main objectives: To become the leading technological research organization in Europe and to ensure that the nuclear deterrent remains effective in the future. CEA is active in three main fields: Energy, information and health technologies, and defense and national security. In each of these fields, the CEA maintains a cross-disciplinary culture of engineers and researchers, building on the synergies between fundamental and technological research.

In 2006, the total CEA workforce consisted of 14 910 employees (52 % of whom were in management grades). Across the whole of the CEA (including both civilian and military research), there were 1,017 PhD students and 278 post-docs.
In 2004, the civilian programs of the CEA received 55 % of their funding from the French government, and 35 % from external sources (partner companies and the European Union). The remaining 10 % was provided from a fund dedicated to the decommissioning and clean-up of civilian nuclear plants. The military programs are mainly funded directly by the French Ministry of Defense.

LETI

Leti is a CEA laboratory located in Grenoble which is one of the main European applied research centres in electronics. More than 85% of its activity is devoted to research that is conducted with outside partners.
Leti is a partner to the industrial world, with 200 collaborators and 350 contracts a year. Leti has led to the creation of almost 30 start-ups in high-technology, including Soitec, the world leader in Silicon-On-Insulator (SOI). In the files it is

possible to find some 180 patents a year and manage a portfolio of 1,000 inventions protected by patents.

Areas of activity

- Micro- and nano-technologies for microelectronics,
- Technologies, design and integration of microsystems,
- Imaging technologies,
- Micro- and nano-technologies for biology and health,
- Communication technologies and nomad objects.

Leti is endowed with an annual budget of 174 M€ and employs 1,000 people with, in addition, more than 500 external collaborators (postgraduates, research partners and industrialists). We have 11,000m² of clean rooms, an equipment portfolio worth 200 M€ and we invest more than 40 M€ a year on new equipment.
Leti is one of the main forces behind **Minatec®**, Europe's premier Centre of Excellence in Micro- and Nano-technologies. In the future **Minatec®** is destined to bring together more than 4,000 researchers, industrialists and teaching staff in Grenoble.

2. THE MOS TRANSISTOR

The most basic element in the design of a large scale integrated circuit is the transistor, and the MOS transistor is the most important device for very-large-scale integrated circuits (VLSI) such as microprocessors and semiconductor memories. It has many acronyms including IGFET (Insulate-Gate Field-Effect Transistor) and MOSFET (Metal-insulator-semiconductor Field-Effect Transistor). The principle of the surface field-effect transistor was first proposed in the early 1930s by Lilienfeld [Lilienfeld 30] and Heil [Heil 35]. It was subsequently studied by Shockley and Pearson [Shockley 48]. In 1960, Kahng and Atalla [Kahng 64] proposed and fabricated the first MOS Transistor using a thermally oxidized silicon structure. The basic device characteristics have been subsequently studied by Ihantola [Ihantola 61] and Moll [Ihantola 64], Sah [Sah 64], and Hofsteing and Heiman [Hofstein 63]. The technology, application, and device physics have been reviewed by Wallmark and Johnson [Wallmark 66], and Richman [Richman 73].

2.1 STRUCTURE AND OPERATION

The MOS transistor is a member of the field-effect transistors family. The current is transported predominantly by carriers and a vertical electric field is modulating the density of carriers into the channel. This field, called gate field, will modulate a potential barrier forming a conduction channel between two zones of the type opposed to the channel, source and drain zones. If the channel is P-type and the source and drain areas are N-type, we have a NMOS transistor, if the channel is N-Type and the source and drain areas are P-type we have a PMOS transistor.

When there is no gate field, there is no carries into channel; thus current between source and drain (Figure 1). In the presence of a gate field, carriers can flow through the channel, and the transistor releases a current flow between source and drain (Figure 2) [Skotnicky 03].

Figure 1: **MOSFET-OFF.** There is no carriers through the channel, then the MOSFET is blocked.

Figure 2: MOSFET-ON. Because of gate the carries are generated and the current flows.

The characteristics dimensions in a transistor are the length gate L, the width W, the gate oxide thickness. The actives zones are isolated by Shallow Trench Isolation (STI), the gate is isolate from the others electrodes by the spacers, which allow also to adjust source and drain doping and of the extensions (figure 3) .

Figure 3: General structure of a conventional bulk MOS transistor.

Source and drain are doped heavily until its degeneration, the silicon get a behaviour quasi metallic. Xj is the extension depth and determines the extensions spreading ΔL under the gate; it is possible to remark that the electric gate length is lower than L.

2.2 THRESHOLD VOLTAGE

As we mentioned, the conduction in a MOS transistor is controlled by the gate field, created in the semiconductor–oxide interface. In the case of a NMOS device (channel type P and source-drain type N) for example, there are three different situations for the evolution of the conduction and valence bands according to a longitudinal axis in reference to channel (x axis) and transverse (y axis taken in the channel centre), in function to VG voltage applied on the gate, [Skotnicky 03].

2.3 ACCUMULATION REGION

A negative value of the gate voltage VG attracts the holes on the channel surface. Then the transistor is in accumulation mode. The channel potential energy is higher than source potential energy and makes a high barrier of

$$\phi_d = \frac{kT}{a}\ln\left(\frac{N_{ext}N_B}{n_i^2}\right)$$

In this region, the valence band on the surface is closer to the Fermi level than in volume. The channel thus has a negative potential.

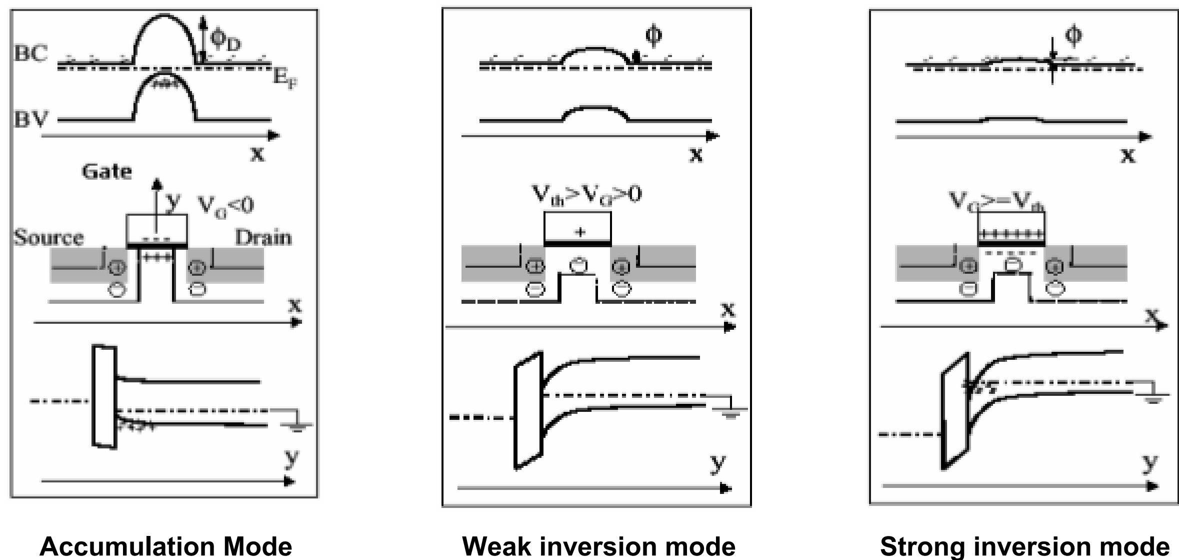

Figure 4: Band gap evolutions in function of gate voltage in a NMOS transistor. First section is a longitudinal cut of channel energy. Second section is a schema of MOS transistor with the type of carriers into channel. The last section show the energy according to one transversal cut into channel of MOSFET.

2.4 WEAK INVERSION REGION

In this mode, the gate polarization is such that the holes are pushed back of surface, leaving only fixed charges of opposite type in the channel. The conduction band on the surface is then curved towards the Fermi level. The channel potential remains then lower than source potential and the current doesn't pass through even if Φ barrier has been reduced.

2.5 STRONG INVERSION REGION

When the conduction band is curved more strongly towards Fermi level: source-channel potential barrier Φ vanishes. The strong inversion condition is reached when the surface potential in the channel is twice the difference between Fermi level and silicon intrinsic level (middle of forbidden band-gap, Figure 5)

$$\phi_d = 2\phi_F = \frac{kT}{a} \ln\left(\frac{N_B}{n_i}\right)^2$$

In this mode, gate polarization allows electrons flow in the channel.

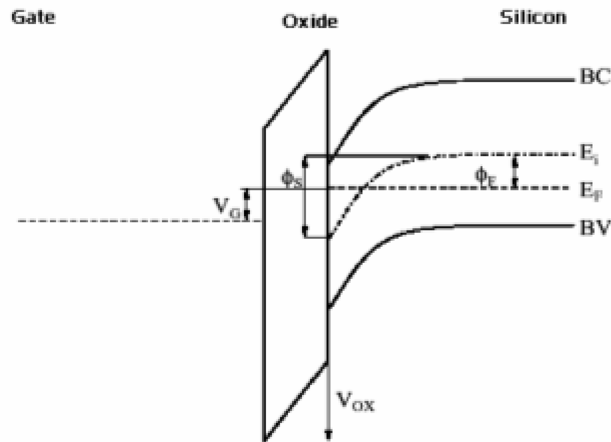

Figure 5: Bands curves in strong inversion region. Definition of Fermi surface potentials.

In order to generate the conduction in a MOS transistor, it is necessary to induce the strong inversion regime into the channel. This condition guarantees that the channel contains carriers of the same type than source and drain. The transistor act like three resistances in series of the same type: n+/n/n+ for NMOS [Skotnicky 03].

3. SON AND LSOI TECHNOLOGY

3.1 FULLY DEPLETED TRANSISTORS

The fully depleted transistor (FD-SOI) is distinguished from the conventional MOS or bulk because of its conduction channel which is isolated from the substrate by a layer of Buried Oxide (BOX). In weak inversion, the totality of the conduction channel is depleted because of the use of a thin channel (typically less than 20 nm).There is no more neutral zone into the substrate, which leads to a better coupling between the front interface and the inversion charge. As the depth depletion is limited by the thickness of silicon film, this architecture minimizes short channel effects and improves the performances compared to a conventional bulk transistor.

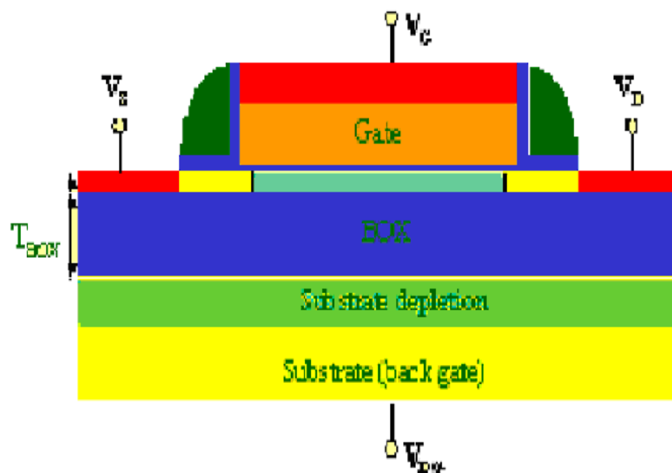

Figure 6: Fully Depleted SOI Transistor. It is possible to see the different thicknesses under de gate (oxide, channel, BOX, substrate), as well as the substrate depletion.

3.2 THE THIN FILMS

The short channels effects arise in MOS transistor depend of gate field interaction with the electrostatic coupling between source and drain through the channel. These parasitic effects are minimized when the gate voltage controls the entire conduction channel. In short transistors, lateral coupling, become stronger and the gate loses control of part of the channel. In order to surpass this problem and block

the lateral coupling, an excellent solution is to limit the channel thickness. A thick channel layer allows the coupling between source and drain (Figure 7c), this lateral coupling become weak with a thin film (Figure 7a). The silicon channel thickness has, in consequence a direct impact on the short channel effects (Figure 7b).

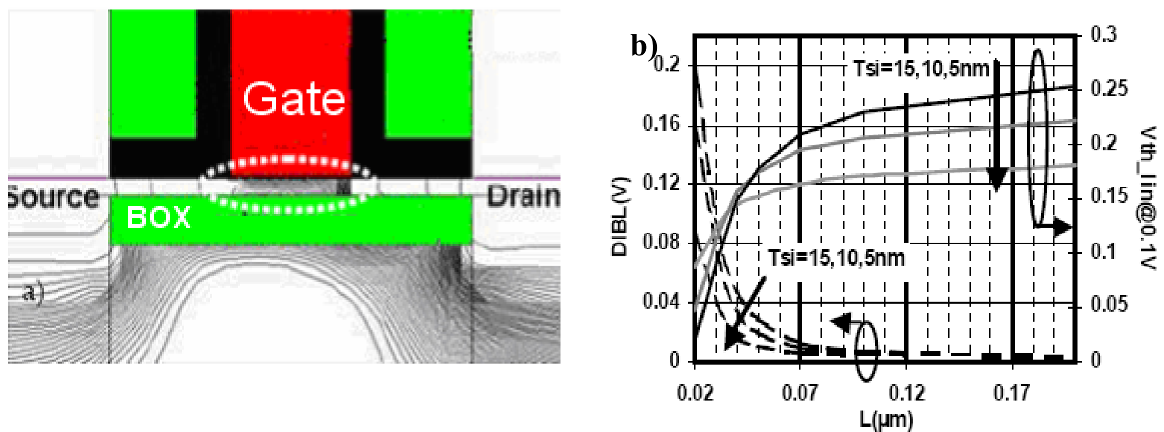

Figure 7: Coupling between source and drain. a) A thin Silicon film avoids the lateral coupling, minimizes thus the short channel effects b) Impact of the Silicon film thickness with length gate c) Coupling between source and drain.

3.3 SILICON ON NOTHING TECHNOLOGY

Silicon on nothing architecture allows extremely thin (in the order of a few nanometers) buried dielectrics and silicon films to be fabricated with high resolution and uniformity by epitaxial process. The SON process allows the buried dielectric (which may be an oxide but also an air gap) to be fabricated locally in dedicated parts of the chip, which may present advantages in terms of cost and facility of system-on-chip integration.

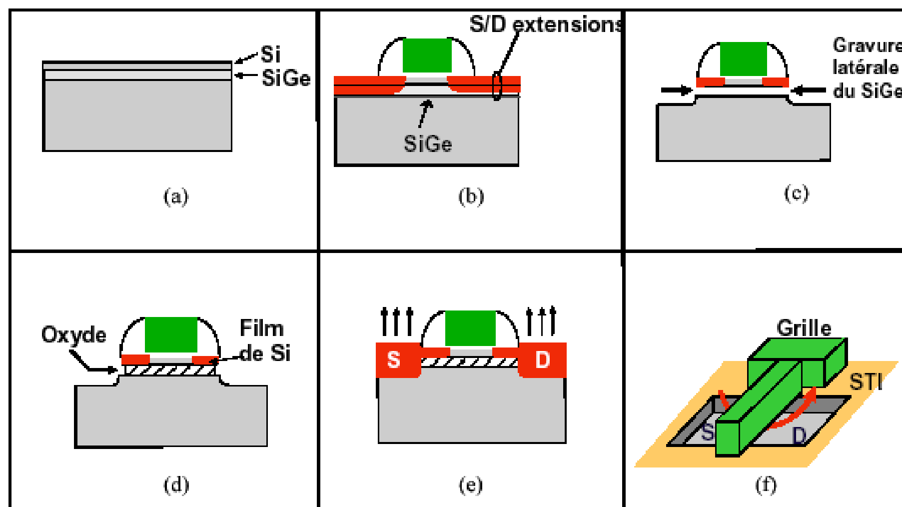

Figure 8: SON process steps

The Figure 8 shows the steps in the manufacture of a SON transistor, which, unlike other SOI technologies, allows silicon films and buried insulators, both of nanometric scale, to be defined by epitaxy on a bulk substrate. The fabrication process starts with a conventional bulk silicon wafer, upon which a layer of silicon-germanium (SiGe) is formed, followed by a silicon cap layer that will subsequently be used to form the transistor channel (Figure 8a). Next, conventional CMOS process steps are carried out until the formation of the spacers (Figure 8b). After this, anisotropic plasma etching is used to form trenches in the source and drain regions, opening up access to the SiGe, which is then selectively etched to form an air tunnel, which isolates the gate from the substrate (Figure 8c).
Figure 8c shows why the process is called Silicon on Nothing; the SiGe underneath the gate is removed, leaving a space that can be either left void or filled with a suitable dielectric. Despite the air tunnel, the gate does not collapse because it bridges the active area and is supported at both ends as shown in (Figure 8f).

After the lateral etching of the SiGe, the tunnel can be optionally filled with a dielectric, as shown in Figure 8d.

In the first test structures, thermal oxidation was used to fill the tunnel with oxide; subsequently, devices were successfully built where the tunnel also contains a thin layer of silicon nitride.

Figure 8e shows selective epitaxy in the source drain (S/D) areas (process equivalent to the so-called elevated or raised S/D) that accomplishes the SON specific steps and further flow merges with the conventional bulk CMOS process. [Monfray 01]

3.4 LOCALISED SOI ARCHITECTURE

3.4.1 Principle and General Description

Localized SOI (LSOI) is an innovative low cost approach, dedicated to Low Power devices, based on the SON technology [Jurczak 00], where the buried SiGe can be removed directly from the edges of the active areas.

This process has been developed to obtain a "FDSOI-like" transistor, made on a typical low cost silicon substrate. The morphology of a LSOI device is very similar to the FDSOI transistor, integrated with a thin BOX (Buried Oxide) and with a ground plane area below the local isolation, the LSOI structure gives too the possibility to introduce different dielectric materials inside the tunnel. As starting from a standard Si-wafer, the most important advantage of this approach is the possibility to co-integrate it with conventional bulk transistors or functionalities. This can be of great interest for SoC applications and dedicate products.

The process is self aligned, and forms an entire device structure isolated from the substrate. This approach allows the control of the Si-film and of the buried dielectric thicknesses with the precision of the epitaxy process, offers the possibility

to change the nature of the buried isolating layer, and to implement easily Ground-Plane implantations to improve the DIBL so as the body factor [Monfray 07].

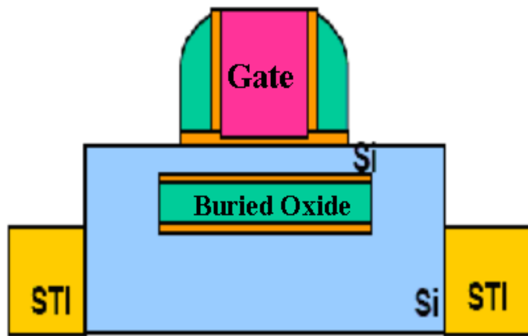

Figure 9: SON structure

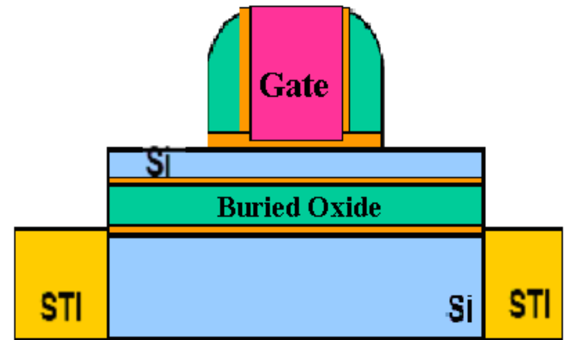

Figure 10: LSOI structure

As we have mentioned previously in SON procedure the SiGe layer is etched at the same time with the channel section that is no below of the spacers which protect the gate oxide, i.e., the channel is cut. This is the principal difference in the elaboration process with the Localised SOI, due to that in LSOI process the channel is preserved completely (Figures 9 and 10).

3.4.2 Technological stages

The architecture presented here could be called SON without channel cutting because the silicon channel is preserved completely during the selective etching; the access to the SiGe layer is opened by an STI recess in hydrofluoric acid. As the SiGe removal has to be performed under the entire active area, the circuits better adapted for LSOI are those with a small width (W) [Chanemougame 05].

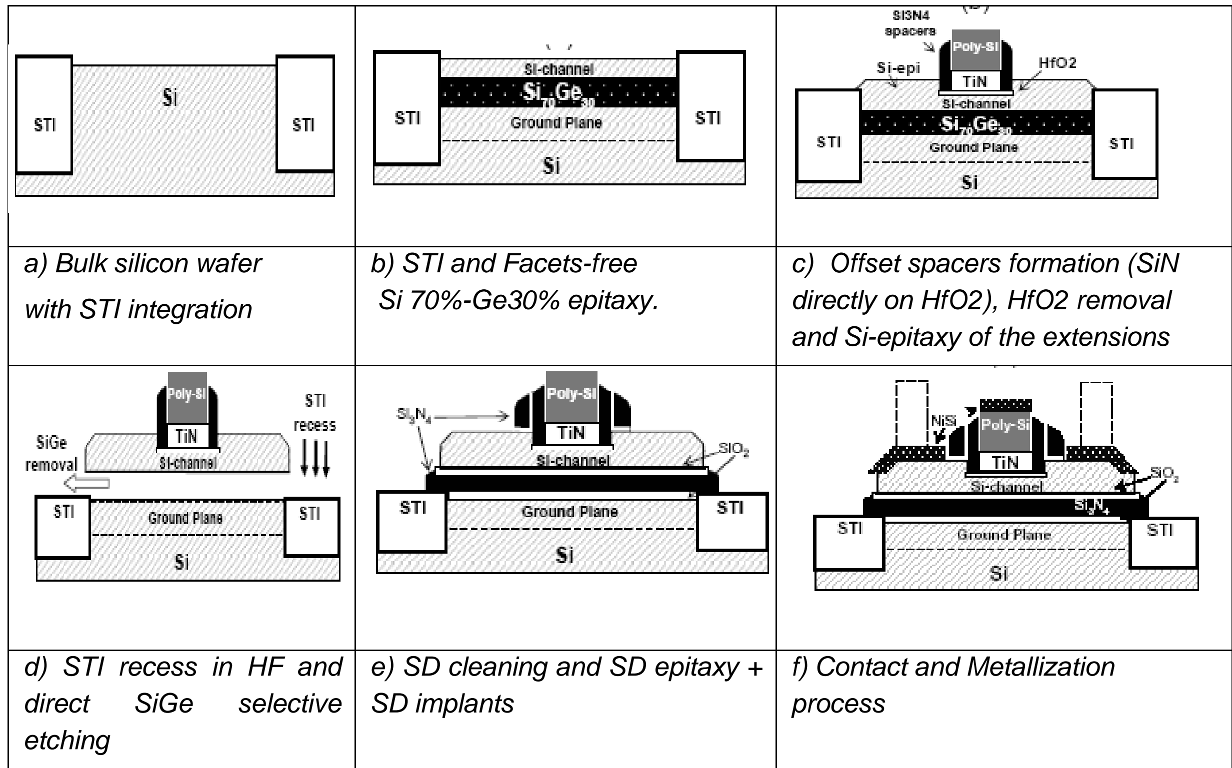

Figure 11: Localised SOI Specific steps ([Monfray 07] to be published at IEDM 07-confidential-)

4. COUPLING EFFECTS IN LSOI TRANSISTORS

Fully depleted transistors are influenced by BOX Thickness, constitution of the back-interface (Si film/BOX), and back-gate bias. By varying the back-gate voltage it is possible to study the coupling effect between the channel region and the bulk silicon substrate. Numerical simulation have revealed that in short-channel SON MOSFETs, the extension of the source an drain junctions underneath the BOX, and their interaction when they are closed enough cause an increase of the depletion layer in the substrate. In order to represent this effect a solution has been proposed by the concept of Voltage Doping Transformation (VDT) [Skotnicki 88].

This model, however, needs to be adapted to LSOI devices, and is described in the following sections.

4.1 FRONT CONDUCTION MODULATED BY THE BACK GATE

The coupling between the front and back gates is a well known phenomenon in fully depleted SOI MOSFETs [Lim 83], and by its morphology, it is present in LSOI transistor too; it allows to study the properties of the back interfaces. The coupling effect is visible in LSOI transistors where the critical parameters are the different thicknesses between the electrodes Vg1 and Vg2. The substrate voltage has an important influence on the conduction channel too.

For low drain voltage, the dependency of threshold voltage on substrate bias is as described in [Kuo 92]. Figure (5.1) shows the experimentally measured shift of threshold voltage as a function of substrate bias for the case of Vd=O.1V. From Vg2 of OV to roughly -15V, the threshold voltage increases with increasing magnitude of Vg2 in a linear fashion because of the capacitive coupling between the substrate and front channel.

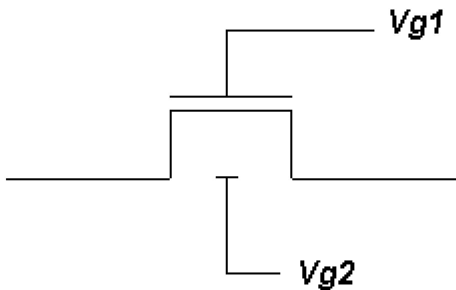

Figure 12: Gate voltage (Vg1) and Substrate voltage (Vg2) in MOSFETs.

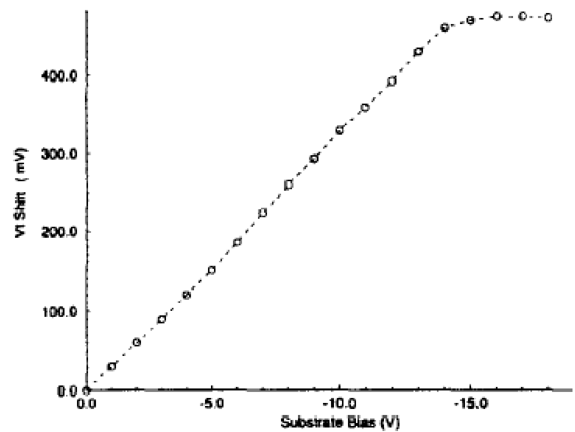

Figure 13: Shift of threshold voltage as a function of substrate bias.

4.2 BODY FACTOR

In MOSFET transistors Vth is increased by a reverse body bias to suppress Ioff in the standby mode, and Vth is reduced to increase Ion in the active mode. The body factor (γ) determines the change in Vth, and therefore, it is the key parameter defined as

$$\gamma = \frac{\Delta V_{\text{th}}}{\Delta V_{\text{sub}}},$$

where ΔVth and ΔVsub are the changes in Vth and body bias (Vsub), then if we can control the body factor value we can modulate the threshold voltage, therefore, an extremely thin BOX is required to obtain a sufficient γ.

4.3 ULTRA-THIN BODY EFFECTS

The thinning of the Si film is the most efficient strategy for scaling down SOI MOSFETs [Cristoloveanu 02, Cristoloveanu 03]: short-channel effects (charge sharing, DIBL, fringing fields) are well controlled if the film thickness is about 25 %

of the channel length. The threshold voltage can be adjusted by the use of gate materials with appropriate work function; in this case, the film can be left undoped in order to preserve a high carrier mobility.

In thin fully-depleted films, the interface coupling effects are strongly amplified. According to Lim and Fossum [Lim 83], the threshold voltage of the front channel (or back channel, respectively) decreases with increasing back-gate voltage (or front-gate voltage, respectively). When drawing both characteristics Vth(Vg2) on the same graph, the two curves are in general different.

5. ANALYTICAL MODELS FOR BODY FACTOR AND VBA TOOLS FOR LSOI TRANSISTORS ANALYSIS

The interface state density plays a crucial role in determining the device performances and affects the reliability and lifetime of the device. The measurement and characterization of the interfaces states are needed to understand the origin and physical properties of the interface states in a MOS system. Interface states can capture and emit charge carriers and their amount determines the device characteristics [Duyet 99].

By its morphology, very similar to SOI devices, the LSOI transistor are analysed with reliable analytical models for thin-films and ultra-thin-films SOI MOSFET for two interfaces. Next we considered others more exactly three interfaces models for ultra-thin-films, and finally we chose the most accurate model for LSOI devices in relation to the obtained results. To make the models comparison, we took advantage of the Visual Basic for Applications Excel (VBA Excel) tools which help us to gain time and accuracy.

5.1 THE TWO-INTERFACES MODEL

The first model study was the Lim Fossum model [Lim 83], this approach considers the front and back gates of thin-film SOI MOSFET to calculate the threshold voltage and the drain current in strong inversion. It takes into account the first interface (gate oxide-channel) and the second interface (channel-box). The expressions clearly show the dependence of the linear-region channel conductance on the back-gates bias and on the device parameters, including those of the back silicon-insulator interface.
This model no simulate weak inversion regime and do not take into account the Si substrate. The equation for body factor is:

$$\gamma_{Lim\&F} = \frac{C_{ox2}C_{Si}}{C_{ox1}(C_{Si} + C_{ox2} + C_{it2})}$$

5.2 THE THREE-INTERFACES MODEL

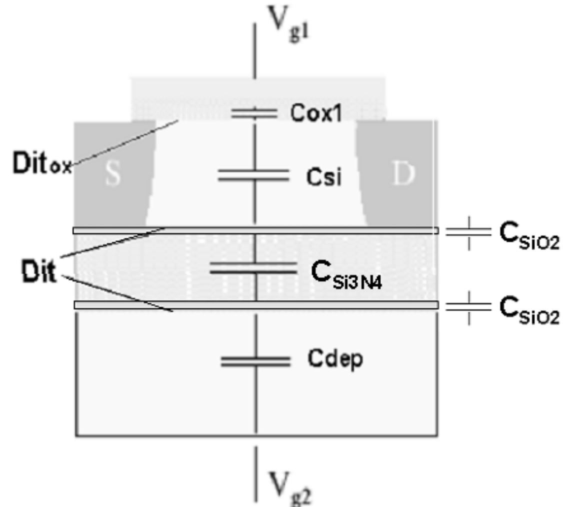

Figure 14: LSOI MOSFET with its different capacitances and the three Interfaces Trap Density. It is possible to see that the Cbox capacitance is composed of the capacitances of oxide and the capacitance of the Silicon nitride.

In order to describe the SOI MOSFETs behaviour, reliable analytical models for thin-film and ultra-thin-film were developed by Balestra [Balestra 90]. These models give the main electrical MOSFET parameters in ohmic operation (subthreshold swing and threshold voltage) for structures with two or three interfaces with silicon as a substrate.

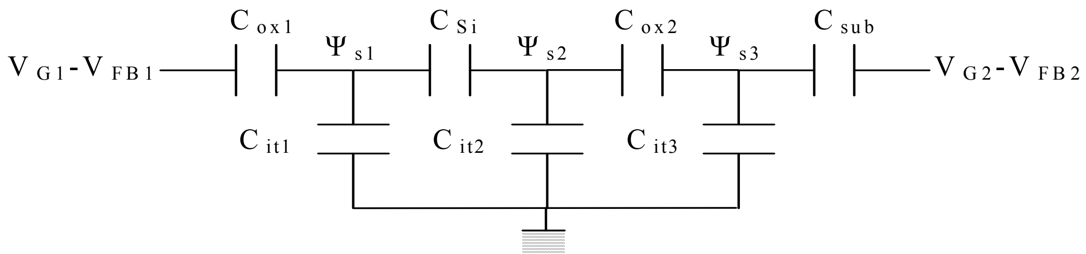

Figure 15: Equivalent circuit for the three interfaces SON model.

Because of the strong third interface influence, and substrate depletion in SON transistors a three-interface model with the junction induced 2D-effects has been proposed [Pretet 04], this model combine the SON MOSFET three interface equivalent circuit (Figure 15) with VDT approximation [Skotnicki 88]. According to the Ohm's law for each knot, the relation for the three surface potentials is:

$$\Psi_{s1}(C_{ox1}+C_{it1}+C_{si})=C_{ox1}\left(V_{G1}-V_{FB1}+\frac{2Q_{c1}+Q_{si}}{2C_{ox1}}\right)+C_{si}\Psi_{s2}$$

$$\Psi_{s2}(C_{ox2}+C_{it2}+C_{si})=C_{ox2}\left(\Psi_{s3}+\frac{2Q_{c2}+Q_{si}}{2C_{ox2}}\right)+C_{si}\Psi_{s1}$$

$$\Psi_{s3}(C_{ox2}+C_{it3}+C_{sub})=C_{ox2}+\Psi_{s2}+C_{sub}(V_{G2}-V_{FB2})$$

with subscript 1 for gate-oxide/Si-film, 2 for Si-film/box and 3 for BOX/Bulk-Si interfaces. The interface trap capacitance is given by Cit=qDit and the depletion charge by Qsi=-qNa. The depletion capacitance Csub is calculated with the effective channel doping provided by VDT model.

Through the previous equations and for $\Psi_{s1}=2\varphi_F$ the threshold voltage for SON Transistors is:

$$V_{T1}=V_{FB1}+2\varphi_F\left(1+\frac{C_{it1}+C_{si}}{C_{ox1}}-\frac{C_{si^2}}{AC_{ox1}}(C_{ox2}+C_{it3}+C_{sub})\right)$$

$$-\frac{2Q_{c1}+Q_{si}}{2C_{ox1}}-\frac{2Q_{c2}+Q_{si}}{2}(C_{ox2}+C_{it3}+C_{sub})\frac{C_{si}}{AC_{ox1}}-\frac{C_{si}C_{ox2}C_{sub}}{AC_{ox1}}(V_{G2}-V_{FB2})$$

with $A=(C_{it2}+C_{si})(C_{ox2}+C_{it3}+C_{sub})+C_{ox2}(C_{it3}+C_{sub})$

Body factor in this expression is done by:

$$\gamma_{Pretet} = \frac{C_{ox2} C_{Si} C_{dep}}{C_{ox1}\left[(C_{it2}+C_{Si})(C_{ox2}+C_{it3}+C_{dep})+C_{ox2}(C_{it3}+C_{dep})\right]}$$

C_{dep} is the depletion capacitance : $\frac{1}{C_{dep}} = \frac{1}{C_{Si}} + \frac{1}{C_{ox2}}$,

C_{ox2} is the BOX capacitance : $\frac{1}{C_{ox2}} = \frac{1}{C_{Si_3N_4}} + \frac{2}{C_{SiO_2}}$,

C_{Si} is the silicon film capacitance $C_{Si} = \frac{\varepsilon_{Si}}{T_{Si}}$

$C_{Si_3N_4}$ is the silicon-nitride capacitance $C_{Si_3N_4} = \frac{\varepsilon_{Si_3N_4}}{T_{Si_3N_4}}$

C_{SiO_2} is the oxide capacitance into the BOX $C_{SiO_2} = \frac{\varepsilon_{ox}}{T_{ox2}}$

C_{ox1} is the oxide capacitance under the gate $C_{ox1} = \frac{\varepsilon_{ox}}{T_{ox1}}$

C_{it1} , C_{it2} and C_{it3} are the capacitances of the first (gate-oxide/Si-film), second (Si-film/BOX) and third interfaces (BOX/Bulk-Si).

$C_{it2} = qD_{it2}$ $C_{it3} = qD_{it3}$

5.3 VBA TOOLS

To study the differences between Lim&Fossum and Pretet models, we developed with VBA (Visual Basic for Applications) Excel informatics tools which help to

process great amount of information and make a comparison among the different parameters that influence the behavior of the LSOI transistor.

Trough this VBA Macro we can calculate the body factor and subthreshold swing with the possibility of changing the values of several parameters: gate oxide thickness (Tox), the two box components: Si3N4 thickness (TSi3N4), SiO2 thickness (TSiO2); Substrate Depletion (Tdep), and the first Interface state density (Ditox) (Table 1).

Input Data		Output Data Two and Three interfaces model		Output Data Three Interfaces model	
Tox	2.30E-09	Cdep	1.32E-03	A	4.67E-04
TSi	1.50E-08	CSiO2	6.91E-03		
TSiO2	5.00E-09	CSi3N4	3.32E-03		
TSi3N4	2.00E-08	Cboxeq	7.41E-04	Cit	1.60E-02
Tdep	8.00E-08	Cox1	1.50E-02	Citox	3.68E-03
Tboxeq	0.00E+00	CSi	7.02E-03		
Dit	1.00E+17	S	9.39E-02	S	9.41E-02
Ditox	2.30E+16	γ	1.46E-02	γ	2.23E-03
		α	7.04E-01	α Pretet	7.14E-01
		Cbox	1.69E-03		

Table 1: Several parameters variation into the excel-macro for LSOI MOSFETs three interfaces model. In the first column it is possible to change the different thicknesses and the Dit. In the second column we can observe the variation of the different capacitances, the subthreshold swing and the body factor according to two interfaces model. In the third column we find the interfaces capacitances, the subthreshold swing and body factor values according to the three interfaces model.

Next to chose different parameters values the macro will calculate and draw automatically body factor (γ) and subthreshold swing (S) in function of the silicon channel thickness (TSi) from 7 to 15 nanometres and the Dit (second and third interface state density) from 1E10 to 1E14 states/cm² (Figure 16c).

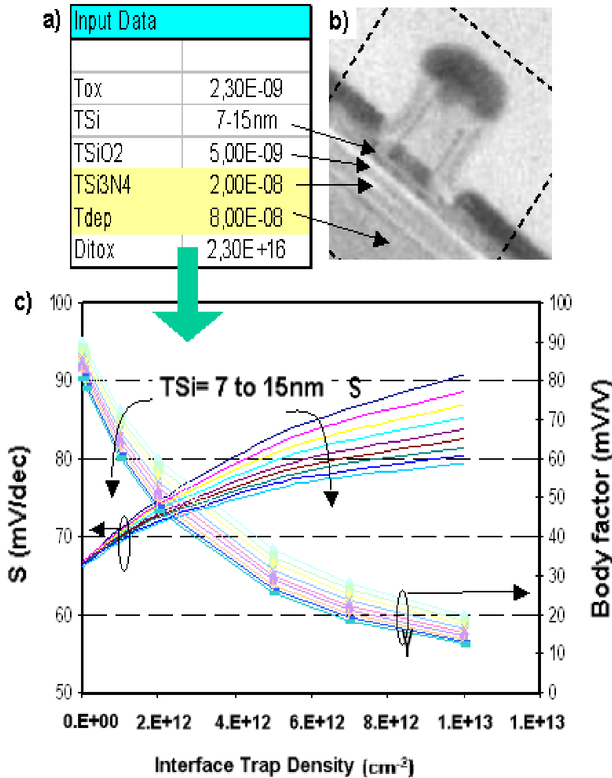

Figure 16: Excel-macro in short. a) Parameters calibration b) Cross section of the LSOI Transistor, the arrows indicates the layer thicknesses and its respective value c) Graphic obtained for Subthreshold Swing and Body factor according to the entered values.

For our study we changed principally TSi3N4, and Tdep because they are the parameters that are not precisely known, next we obtained body factor and subthreshold swing values.

5.4 LSOI TRANSISTOR MODEL

The SOI devices are composed of three interfaces: the first interface is located between the gate oxide and the silicon channel, the second between the silicon channel and the box, finally the third interface is between the box and the substrate.

For LSOI devices, the interface states density and the substrate depletion are very important in the transistor parameters determination, for that reason we have compared and analysed the two and three interfaces model and its behavior in relation to body factor and subthreshold swing. Thereby we draw for the same transistor parameters values, the body factor and the subthreshold swing. It is possible to see that for the subthreshold swing there is not a considerable variation (Figure 18), but for the body factor there is an important difference (Figure 17). As it is shown in the graph when Dit increases, the body factor decreases stronger in 3-interfaces than 2-interfaces model. Body factor also has a more accentuated variation in relation to the silicon channel thickness in the 2-interfaces model.

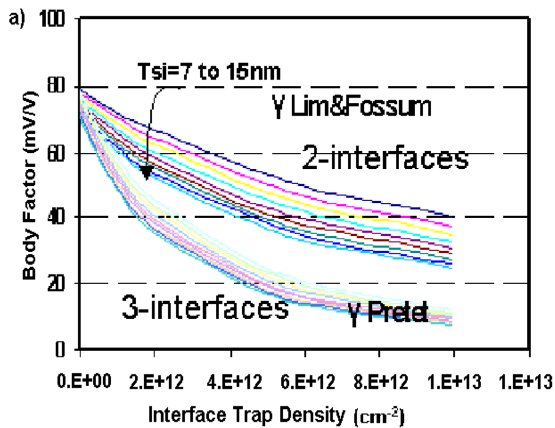

Figure 17: Body factor comparison between 2 and 3 interfaces analytical models.

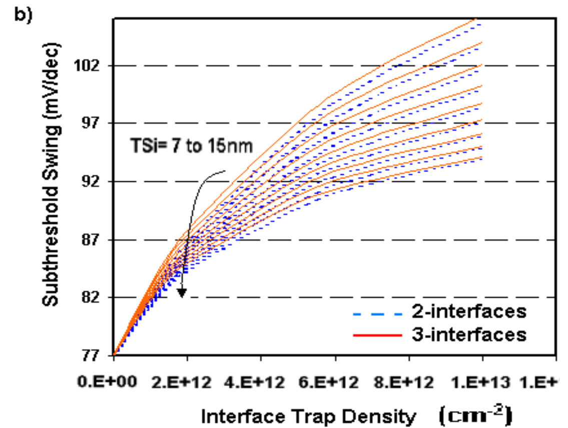

Figure 18 : Subthreshold Swing 2-interfaces model vs 3-interfaces model.

According to the results, the Localised SOI MOSFETs morphology and the importance of the third interface state on these transistors, we can affirm that the two-interfaces model overestimates the body factor value in LSOI transistors, for this reason from now, we will work with the 3-interfaces model.

6. EXPERIMENTAL RESULTS

The electrical measures were done at the characterization laboratory of MINATEC into CEA. To make the measures, I worked with the Cascade Microtech machine and Nucleos software to handle the different wafers, with a HP Basic environment to select the gate length, and with the semiconductor parameter analyzer to take the measures on each chip and to draw the graphs. I worked with DUNE mask on 200mm diameter wafers.

6.1 BODY FACTOR EXTRACTION METHODOLOGY

6.1.1 Measurements validation

When Id (Vg) measures are taken on the CMOS transistor we must verify that no memory effect affect the device. In thin film, fully depleted (FD) SOI MOSFETs, the electrical characteristics are affected by front and back-gate bias changes through the interface coupling. Although FD SOI MOSFETs are considered to be immune to standard FBE (floating body effect), the body potential is still floating and may lead to effects which depends on the front-gate voltage VG1 scan (Figure 19), and can be observed only when the front interface moves from depletion to inversion [Bawedin 05].

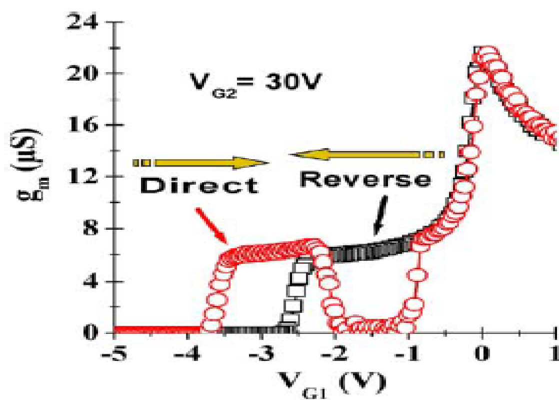

Figure 19: Measured transconductance g_m versus decreasing (reverse scan) and increasing (direct scan) front-gate bias V_{G1}. Memory effect is observed for direct scan. The applied source, drain and back-gate voltages are 0 V, 0.1 V and 30 V, respectively. The holding and integration time are 0 s and 20 ms (medium). The front-gate voltage step is 40 mV.

In fully depleted LSOI MOSFET measurement we verified that there was no memory effect by drawing a first curve Id(Vg) for Vb (substrate voltage) from 0 to –6 (V), next we drew a second curve for Vb from –6 to 0 (V), finally we superposed both curves and we got the same result (Figure 20).

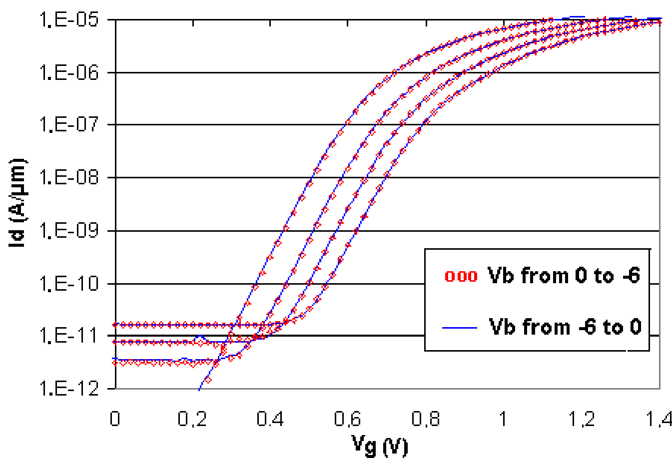

Figure 20: Test to verify that no memory effect affect the Localised SOI MOSFETs. The curves are superposed regardless of the direction change of the substrate voltage during the measurement.

6.1.2 Vth extraction

An important parameter in MOS Transitor is the threshold voltage. It affects directly the Ioff and the Isaturation. Its evolution in function of the substrate voltage (Vb) allows us to know the body factor value.

For Vth extraction, Id (Vg) for Vb from 0 to 1.5V (-1.5 to 0 for PMOS) with an interval of 0.25V were drawn (Figure 21a). Then the Vth value was extracted by the

constant current method (Figure 21b), and finally we plotted Vth in function of Vb. The slope of the curve is the body factor (Figure 21c).

The constant current method consists in establishing an Ith value in function of the transistor dimensions, typically Ith= 70nA x W/L, and the gate voltage corresponding to this current is Vth.

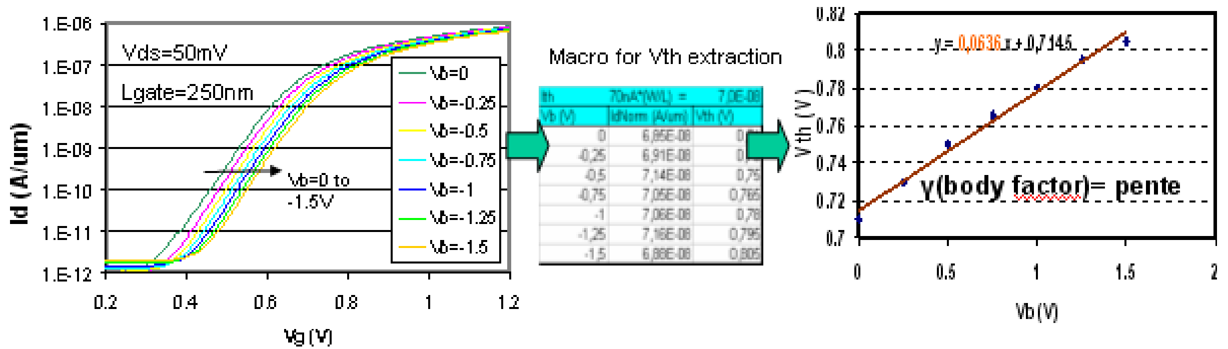

Figure 21 : Body factor variation. a) Curves of Id versus Vg for Vb = 0 to 1.5V for NMOS (-1.5 to 0 for PMOS) b) Vth extraction by the constant current method. Here we took advantage of VBA Excel. We have made a macro which find the most closed value to Ith for each Vb in a table of 1700 rows and give the corresponding Vth. c) Obtaining of the body factor value next to graph Vth vs Vb. The Slope of the curve is the body factor.

6.1.3 Body factor value

Finally, for the body factor it is necessary to represent Vth in function of Vb, and to draw the curve in order to obtain the slope. This value correspond to body factor, i.e. that when the variation of Vth for Vb=0 and Vth for Vb=1.5 increases then the body is high. It is possible to see this effect on Id(Vg) graphic. More separation between the curves for different Vb leads to higher body factor.

6.2 BODY FACTOR NMOS

For the NMOS, we found for example, on a silicon channel thickness (TSi) of 7nm and a gate length of 50nm, a body factor average of 49,37 (mV/V). For a transistor

with the same gate length but a TSi of 11nm we found an average value of 38,76 i.e. that the body factor increases for the thinnest Si-film. We can observe that the dispersion in γ value is also more pronounced for the thinnest film.

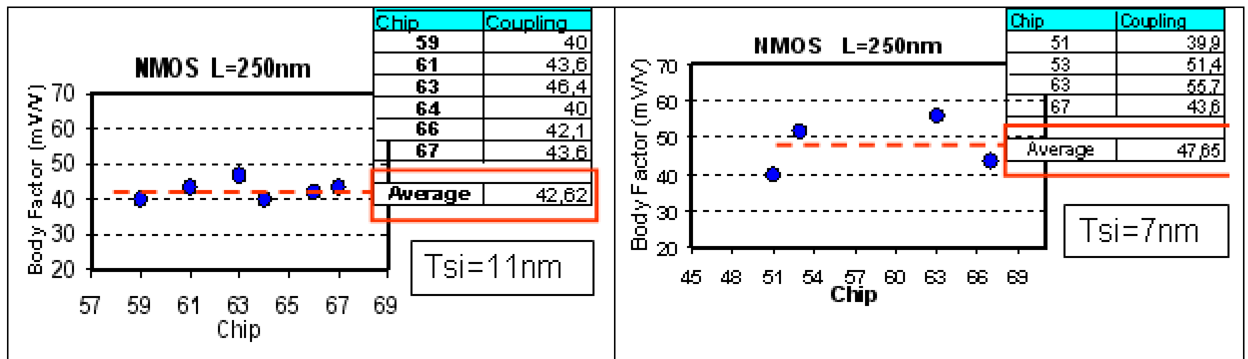

Figure 22: Experimental results for the body factor in NMOS. It is seen that the body factor value is stronger in the thinner thicknesses. For the same Lg it is obtain a bigger γ for TSi=7nm. In other way a stronger dispersion is seen for the thinner thicknesses.

6.3 BODY FACTOR PMOS

In PMOS transistors, we found for a TSi of 7nm and a length gate of 75nm a body factor value of 62,98 mV/V , For the same length gate and a silicon channel thickness of 11nm we found a γ value of 48,2. As for NMOS devices, the body factor is stronger into transistors with thinner films. According to the measures, we found that the dispersion in PMOS increases for the thinnest films.

We also found for PMOS and NMOS devices that for Tsi from 7nm to 11nm thickness, body factors have an average variation of 5mV/V.

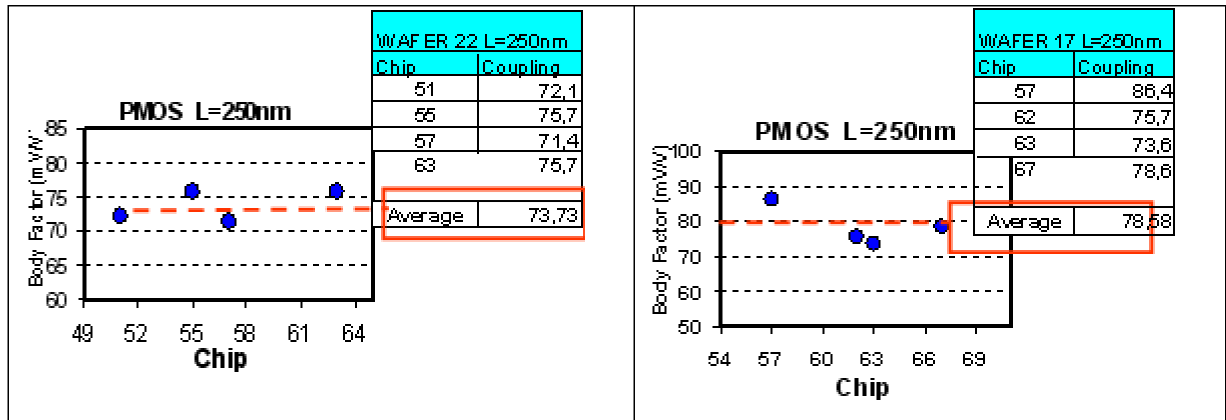

Figure 23: Experimental results for the body factor in PMOS. It is seen a strong dispersion for the thinner thicknesses (same as in the NMOS case). The body factor value is stronger for the thinner thicknesses as in the NMOS transistor.

7. ANALYSIS

7.1 VARIATION OF BODY FACTOR WITH DIFFERENT PARAMETERS

For this analysis we worked with the three interfaces model because, as it was seen in 5.4, it is the most accurate for LSOI transistors. In the next paragraphs we will present influence of different thicknesses and of the interface states density on the LSOI MOSFETs with the three-interface model implementation in an excel macro.

The fluctuations of the coupling between the channel region and the bulk silicon substrate result principally from the substrate depletion, gate channel length, interface trap density, silicon-nitride thickness, and silicon channel thickness.

7.1.1 Substrate depletion influence

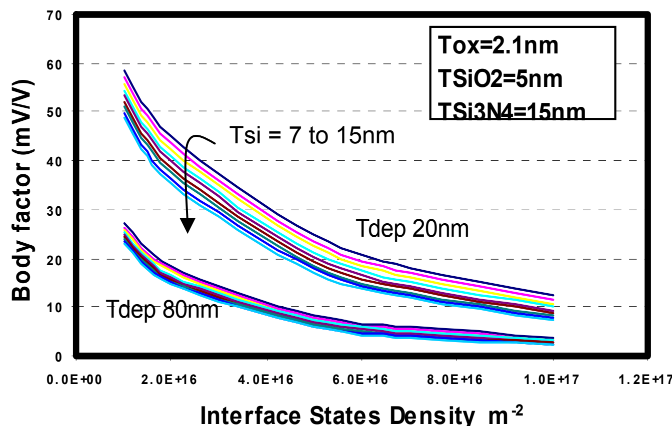

Figure 24: Influence of the depletion depth on body factor. When the depletion depth is weak e.g. 20nm the film thickness influence in LSOI MOSFETs is increased.

A very important parameter for the body factor value is Tdep, and one of our objectives was to determine its influence in the LSOI transistor coupling. By means of 3-interfaces model simulations we got its variation in relation to the different parameters (Figure 24 and 25), thus when the depletion thickness is reduced the body factor increases and when depletion thickness is enough stronger e.g. 80nm the film thickness and silicon-nitride thickness have not a notorious impact in the LSOI transistor behaviour.

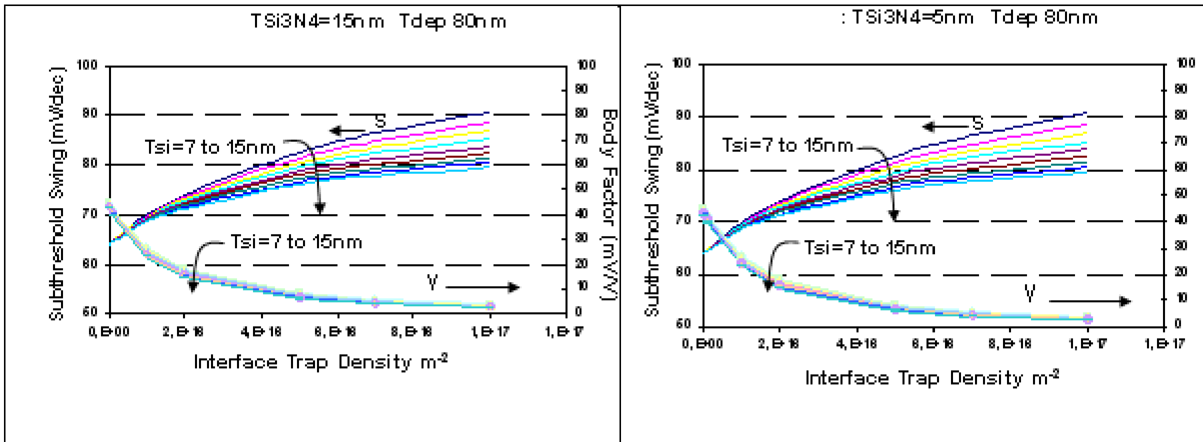

Figure 25: Impact of the depletion depth in subthreshold swing and body factor. When Tdep is largest other parameters in LSOI transistor have not effect. Here the silicon-nitride and the silicon-film thicknesses have no influence on S and γ variation for a depth depletion of 80nm.

In LSOI MOSFETs we have the possibility of doping the substrate during the fabrication process (Ground Plane Effect) before to the SiO2 oxidation and the Si3N4 PECVD. With the substrate doping the depth depletion (Tdep) is reduced, and the equivalent buried oxide become thinner, leading to better short channels effects control.

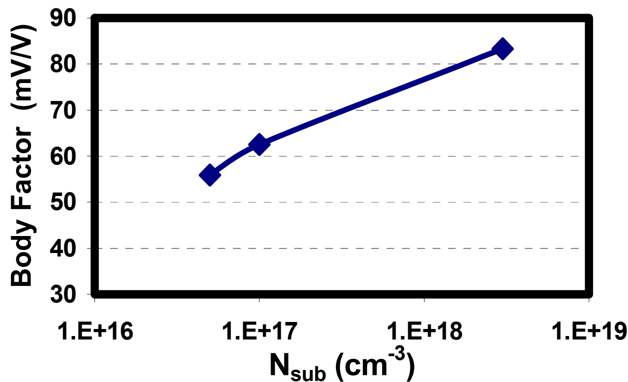

Figure 26: TCAD simulation. Body factor variation in relation to the substrate doping. In order to diminish the depth depletion and for increase the body factor value a heavy doping implantation is required.

TCAD simulations have show the strong impact of the doping in the body factor value and consequently in the electric characteristics of LSOI Transistors.

The substrate doping in LSOI devices is the principal lever for the depth depletion control. We have shown the important role of this parameter and how its reduction allows playing with others parameters especially with TSi and TSi3N4 (Figure 26).

7.1.2 Interface trap density

The interface trap density (Dit) is an important factor in the reliability study of MOS transistor processes, because MOS transistors are strongly dependent on this density due to the surface conduction channel during operation [Deferm 88].

The Dit is a factor who shows the quality of the oxide-silicon interface in MOS transistor. For LSOI MOSFETs, there are, three interfaces trap density: we know the first Dit1 (oxide-gate) but we don't know the exactly value for Dit2 (channel-box) and Dit3 (box-substrate) . In this study we took the same value for Dit2 and Dit3 in the three-interface equation because the difference is negligible (both interfaces are processed at the same time with the same process).

7.1.3 Si3N4 thickness

If long channel transistors are considered, we can to observe that the use of a thick BOX leads an improvement of the subthreshold swing. This is due to the BOX capacity reduction which allows a decrease of coupling between the channel region and the bulk silicon substrate.

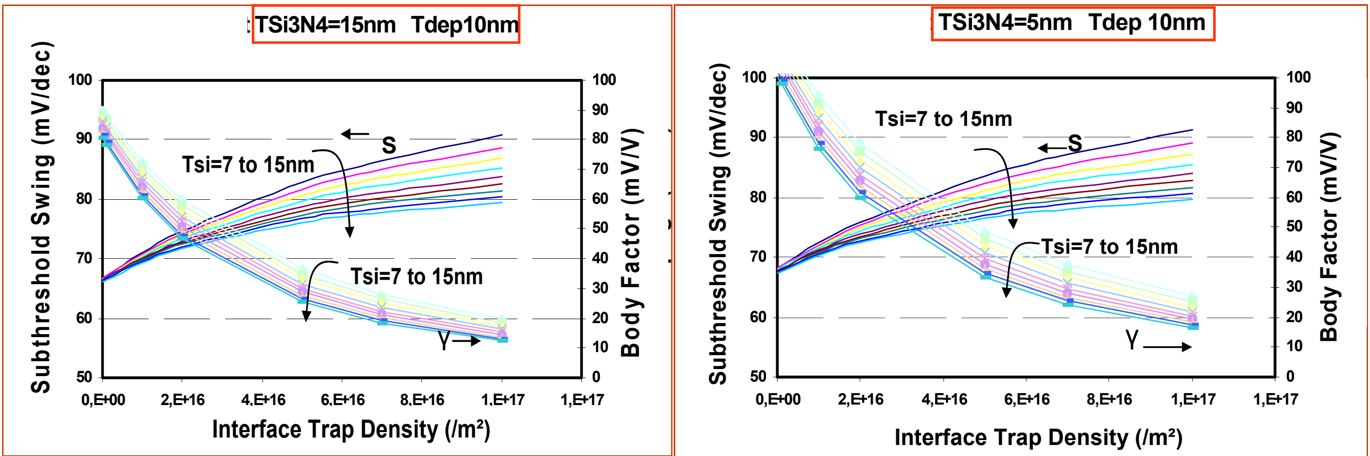

Figure 27: Simulation of the thickness silicon-nitride with 3-interfaces model. There is no change for subthreshold swing but the body factor is stronger for thinner silicon-nitride.

In SON devices when the BOX thickness decreases, the associated capacity Cbox increases and the device's threshold voltage increases. This hypothesis can be verified with digital simulations where the general increase in threshold voltage is observed when the thickness of the buried dielectric decreases [Monfray 03]. Nevertheless, in order to diminish the short channels effects, it is necessary to work with thinner thicknesses for channel and BOX.

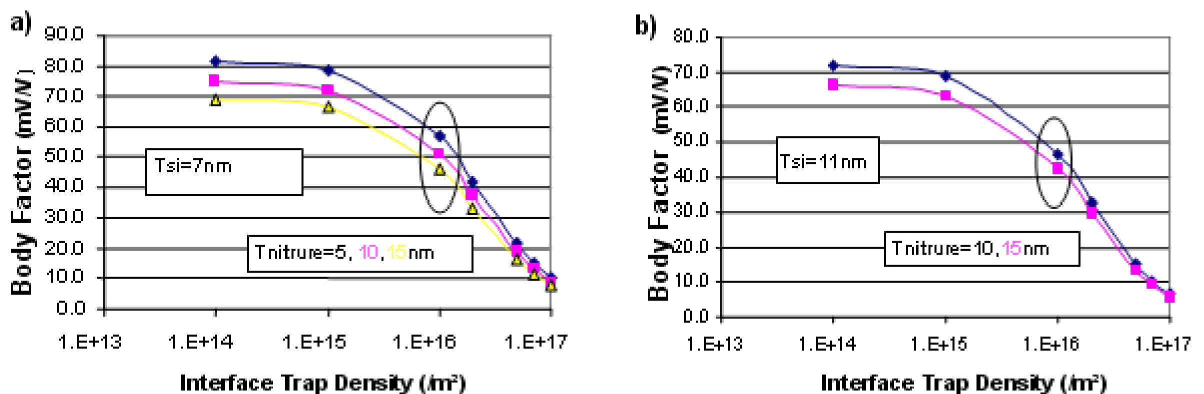

Figure 28: Simulated variation of body factor in NMOS as a function of Dit. a) TSi=7nm b)TSi=11nm

Silcon on Nothing technology allows thanks to silicon channel and silicon-nitride epytaxy to achieve a structure with ultra-thin Silicon-channel and BOX film. With this technology it is possible to get layer thickness of a few tens of nanometers, so that the gate field influence, extends beyond the dielectric buried layer.

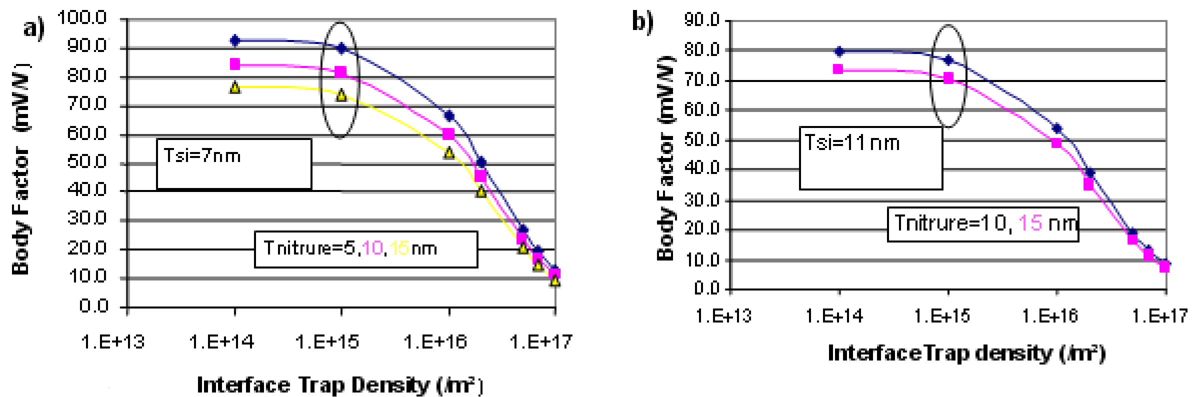

Figure 29: Simulated variation of body factor in PMOS as a function of Dit. a) TSi=7nm b)TSi=11nm

The BOX into LSOI transistor is formed by two components: SiO2 (silicon dioxide) under the silicon film and above the substrate and Si3N4 (silicon nitride) between the two SiO2 layers. The SiO2 is fixed but the SiO2 thickness but the Si3N4 thickness can be subject to variations. For this reason this is an important parameter in our research.

This factor gets a significant influence for small Tdep values. For example when the substrate depletion is 10nm, we find that when TSi3N4 increases the body factor decreases (Figure 29). It is possible also to observe that for smaller TSi3N4 values, the thickness channel variation has higher impact on the body factor value.

7.1.4. Silicon Channel Thickness

In SOI devices one problem is the final dispersion of the films thickness, which can vary according to the position on the wafer of a few nanometers in the best of the

cases. It is well understood that this thickness variation impacts strongly the devices electrical characteristics, in particular, the threshold voltage if the channel thickness is thin. This problem is reduced in SON devices because the Si-film and the BOX thickness are controlled by the precision of the epitaxy process.

Moreover, we could show in an experimental way the influence of conduction channel thickness on the threshold voltage of the devices. In particular, when the film thickness is reduced, the channel depletion load decreases involving a total reduction in the threshold voltage of the transistors, i.e., it is possible to adjusted vth; with this reduction also the short channel effects are reduced due to the gate vertical-field capacitance which dominate the electrostatic coupling between the extensions.

When the substrate depletion is deep (e.g. 80nm), TSi variation value is negligible for the body factor variation but for smallest substrate depletion values (e.g. 10nm) TSi become important.

7.1.5 Gate channel length

Its reduction is one of the principal issues in the present for the semiconductor industry. This is due to the apparition of non ideal phenomena; these include the short channel effects, which leading to weaken the gate control over the channel charge. The drain source bias induces an additional lowering of the potential barrier near the source, giving rise to further shifts in the threshold voltage.

We worked specifically with LSOI short channel transistors (Lg between 30 and 260nm). In this section, we looked at the impact of the gate length reduction on the body factor.

Through the experimental measurement we found that the body factor behavior in LSOI MOSFETs is different for NMOS and PMOS devices (Figure 8.7). Thus it was found that for PMOS the body factor is stronger than in NMOS for different gate lengths, but in NMOS the body factor is more stable than in PMOS.

Hence PMOS have a value of 79 (mV/V) for Lg=250nm and TSi=7nm that is much more stronger than γ in NMOS, where the value is 50 (mV/V) for the same Lg and TSi. For Lg=30nm the γ value is 48 (mV/V) in PMOS while that for NMOS it is of 50 (mV/V) again.

Nevertheless the PMOS keeps a better body-factor value in relation to NMOS in the most of the cases. Thus the LSOI architecture has a better behaviour in PMOS than NMOS in term of body coupling. This phenomenon is due principally to the depth depletion and to the interface trap density that are smaller in the PMOS case.

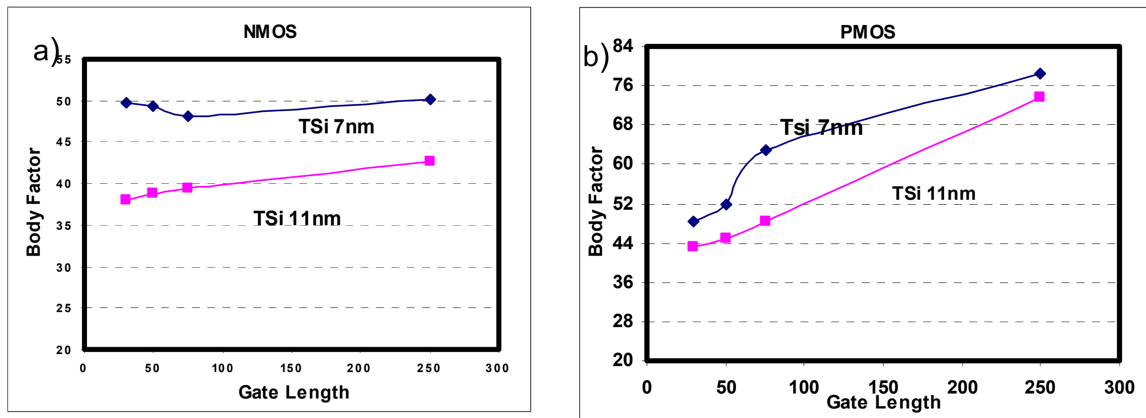

Figure 30: Measurement results for NMOS and PMOS LSOI devices. With the channel length reduction there is a loss of control on Vth. This effect is much more evident in PMOS than NMOS. In PMOS we have obtained body factor values up to 87 (mV/V) for TSi=7nm and Lg=250nm but there is a strong decrease when the Lg is diminished, thus for the same TSi and for Lg = 30nm we have got body factor values of 48 (mV/V).

In relation to the film thickness it is shown its influence is very significant in PMOS for gate lengths above of 75nm for TSi=11nm (Figure 31b). For TSi=7nm γ has a great importance for gate lengths above of 50nm in PMOS (Figure 8.7a). Thereby if the silicon-film thickness is thinner we will obtain a better body factor and more control on the threshold voltage. This impact is more noticeable on NMOS than PMOS transistors (Figure 30) where γ is almost a 25% larger for TSi=7nm than TSi=11nm.

It is possible to observe in (Figure 30a) that the gate length have not an important effect in NMOS devices. The body factor values are not very different for Lg=250nm and Lg=30nm especially for the films thinner, here TSi=7nm.

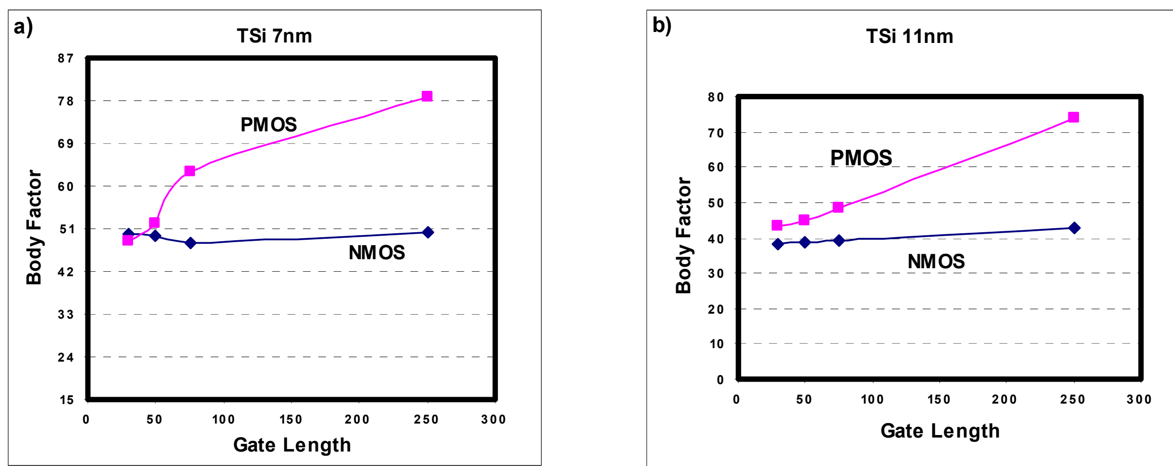

Figure 31: Body factor evolution with reference to the gate length reduction for NMOS and PMOS LSOI MOSFETs. a) For TSi =7nm b)For TSi= 11nm

7.2 COMPARISON OF MODEL AND EXPERIMENTAL RESULTS

After the choice of the three interface states model for LSOI devices, it is necessary to check its consistency with the experimental results. We plotted the body factor with the three interfaces states model for a silicon channel thickness of 7 and 11nm (same thickness of the measured transistors) and we got a delta of

5mV/V between both; the same value was obtained from the experimental measurements.

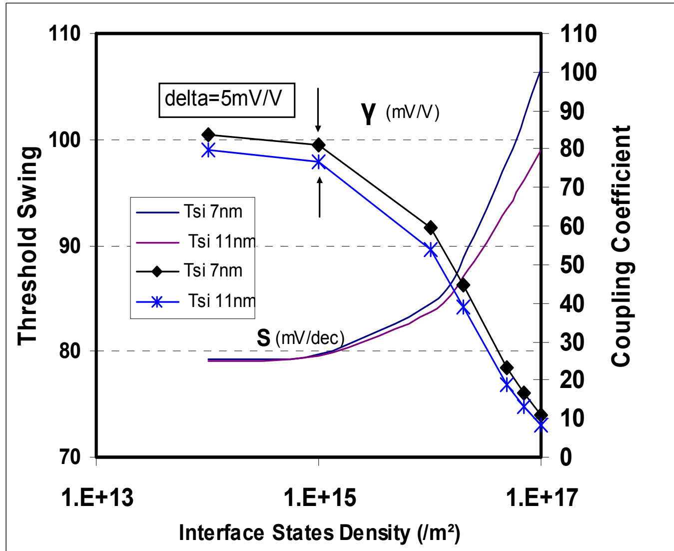

Figure 32: Representation of a PMOS LSOI MOSFET with the 3-interfaces model. Here we take Tdep=30nm and TSi3N4=10nm. A delta of 5m V/V is obtained, same result than experimental measurement.

Now it is possible to say that the coupling values in NMOS are smaller compared to PMOS. In addition, the Dit into BOX stronger than Dit in PMOS, we also can observe that the substrate depletion is stronger for NMOS than for PMOS. This difference is related to the conditions of the implantations realized below the buried dielectric.

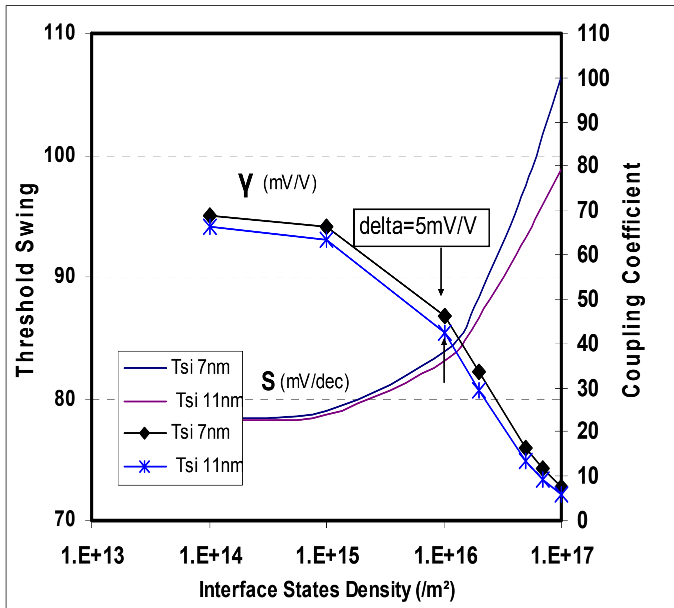

Figure 33: Representation of a NMOS LSOI MOSFET with the 3-interfaces model. Here we take Tdep~40nm and TSi3N4=15nm. A delta of 5m V/V is obtained, same result than experimental measurement.

According to the measures and model the TSi3N4 variations are weaker for Tsi of 11nm, then if the channel thickness is increased, body factor dependency of TSi3N4 is smaller for NMOS and PMOS.

8. CONCLUSIONS

The coupling effect between silicon channel and substrate occurring on LSOI transistor was investigated, and, for this purpose, different transistor parameters were varied. The established model has been studied and experimentally verified, showing that the Localised SOI devices have a strong body factor value, allowing the possibility to control the Ioff through an additional technique named “power management”, where threshold voltage is increased by a bias applied to the transistor body.

The Localised SOI transistor takes the advantages of the threshold voltage control, Vth can be modulate by the different parameters: the reduction of the channel thickness contributes strongly to the diminution of the film depletion load, which induces a drop in threshold voltage. Inversely, the BOX reduction thickness or the doping substrate increases the coupling phenomenon with the substrate, which induces an increase in Vth. In addition Si-film and BOX thickness controlled by the precision of epitaxy process allow achieve ultra-thin films with a very reduced dispersion. This concept is particularly interesting to achieving CMOS at the nano-scale, to control the power and the threshold-voltage of the devices.

The influence of the thin thickness on LSOI transistors and coupling effects has been emphasized. We have shown that classical front and back interface coupling effects and the third interface importance in LSOI thin devices. Coupling measures have shown body factor value PMOS stronger than NMOS because of substrate depletion, but it is a factor that we can improve by Ground–Plane implantations. Through the experimental measures we have been able to state that the body factor dispersion is stronger on thin thicknesses.

The future is promising for LSOI transistor because the CMOS scaling needs new highly performances structures, and the evolution of the MOS transistor will be continued by shrinking the dimensions of the body, gate oxide and BOX, and by reconsidering the nature of the various layers, in order to infuse new functionality and performances.

These trends open up the space for new mechanisms. The miniaturized LSOI Transistor stands as the perfect device for the transition from microelectronics to nanoelectronics.

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