Design of a low drop-out volatge regulator for system-on-chip applications in a 130 nm cmos technology

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Resumen

Título Diseño de un regulador de voltaje de baja caída de tensión en tecnlogía 130 nm[*]

Autor Laude Andrés Fernández Martínez[**]

Palabras claves Regulador de voltaje, simulaciones de esquinas, compensación,baja caída de tensión

Descripción

Este trabajo presenta un regulador de tres etapas con baja caída de tensión, completamente integrable para applicaciones de sistemas en chips. El circuito es compensado con la técnica indirecta anidada usando seguidores de corriente (RNMCCB). Además, se usó un circuito de polarización dinámica para acelerar la respuesta transitoria y así minimizar el tiempo de establecimiento. El regulador ha sido implementado en tecnología CMOS TSMC 130nm y ocupa una area de 0.007mm^2.

Resultados de simulaciones post-layout — para un rango de temperatura de -20°C hasta 120°C— muestran que el regulador puede entregar una corriente de carga hasta de 50mA con una caída de tensión en el regulador de 200mV; también, su corriente de polarización es 60uA y su tiempo de establecimiento de 0.23us. El regulador sin capacitor externo funciona para un rango de voltaje de entrada de 1.4V hasta 2.2V, tiene un sobre pico y sub pico máximo — para simulaciones de esquinas— de 180mV y 297mV respectivamente. La capacitancia de compensación total es de 5pF alcanzando la estabilidad in todos los casos de corriente de carga, incluso con una capacitancia de carga tan alta de 100pF. Adicionalmente, se propone un análisis de polos y ceros para amplificadores de multietapas, como un complemento a el análisis hecho por el autor en (Garimella, A., Rashid, M. W., & Furth, P. M. 2010).; con el fin de evitar polos en el semiplano derecho que pueden ser generados por los lasos de realimentación de los seguidores de corriente del esquema de compensación en frecuencia (RNMCCB).

[*] Trabajo de grado

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Abstract

Title Design of a low drop-out voltage regulator for system-on-chip applications in a 130 nm cmos technology[*]

Author Laude Andrés Fernández Martínez[**]

Key words Voltage regulator, corner simulations, compensation, low drop-out

DESCRIPTION

This work presents a fully integrated three-stage low drop-out regulator (LDO) for system-on-chip applications. The circuits is compensated with the reverse nested miller technique using current buffers (RNMCCB). Moreover, a dynamic biasing circuit is used to speed up the transient response and thus to minimize the settling time. The regulator has been implemented in a TSMC 130nm CMOS technology and occupies an active chip area of 0.007 mm^2. Post-layout simulation results —for a temperature range from -20°C to 120°C— show that the regulator can deliver up to 50mA of load current at a dropout voltage of 200mV; also, its quiescent current is 60 uA and its settling time is 0.23 us. The capacitor-less regulator works for an input voltage range from 1.4V to 2.2V, it has a maximum overshoot and undershoot —for corner simulations— of 180mV and 297mV respectively. The total compensation capacitance is 5pF achieving stability in all current cases, even with a high output capacitance up to 100pF. Additionally, a pole zero analysis of multi-stage amplifiers is proposed as a complement to the analysis done by the author in (Garimella, A., Rashid, M. W., & Furth, P. M. 2010)., in order to avoid right-half plane poles that can be generated by the feedback loops of the current buffers of the frequency compensation scheme (RNMCCB).

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Introduction

O

ver the past few years, the study of power management techniques has increased drastically, due to the accelerated development of mobile electronic devices. Mobile battery-operated designs such as cellular phones, video cameras and laptops require power management units to extend the battery life and consequently the device operation time (Zhichao, L., Yuntao, L., Zhangqu, K., & Jie, C., 2014). Power management integrated circuits (PMIC) are in charge of controlling the quantity, quality and distribution of power to other circuits.

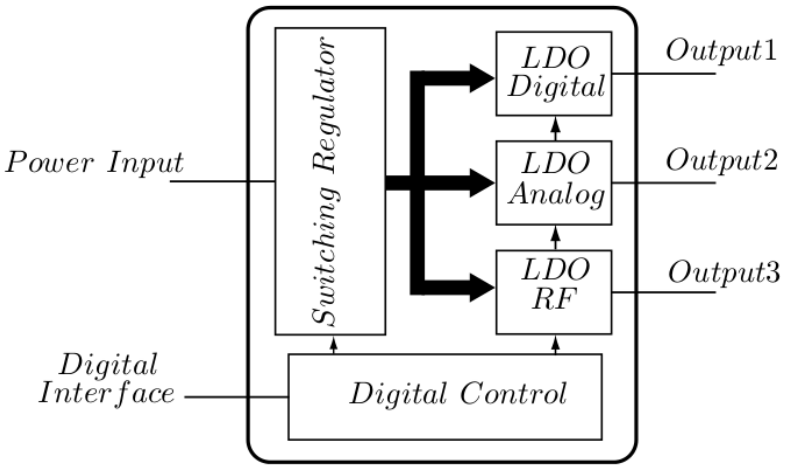

Figure 1. Cell phone power management application.

A typical cell phone power-management system is shown in Fig. 1, which has several subsystems including LDO regulators, switching regulators and control logic. The control logic reconfigures eachsubsystem, turning the outputs on and off as well as modifying the output voltage levels to increase the system power efficiency. Switching regulators establish output voltages to

any desired level with high power efficiency, while LDO regulators are in charge of providing a ripple-free output voltage. Consequently, it is common to use a switching circuit followed by a linear one as shown in Figure 2. Low Drop-out regulators are basically systems that provide stable voltage supply rails under all loading conditions. This conditions include fast current transients and rapid changes in the load impedance, for instance when the powered circuit is completely digital (Milliken, R. J., Silva-Martínez, J., & Sánchez-Sinencio, E. 2007).

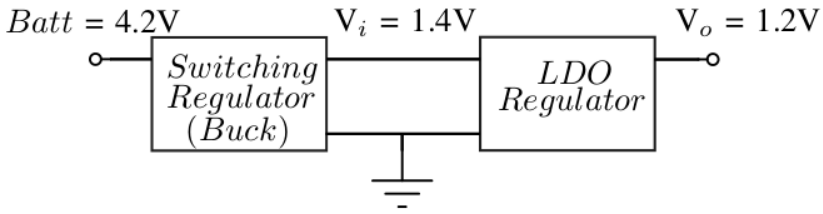

Figure 2. High efficiency regulation.

Due to the negative feedback loop present in a LDO, stability and frequency compensation are important issues to consider in regulator design. The LDO can be internally or externally compensated: external compensation is used for higher power applications (larger load dumps) while internal compensation is used in small-area and low cost applications (Rincon-Mora, G. 2014). This work presents a 1.2V Three-Stage, low drop-out voltage regulator for System-on-Chip applications, which is simulated in a TSMC 130nm CMOS technology. The circuit uses only a internal 5pF capacitor for frequency compensation and stability, allowing a maximum load of 100pF. Section II explains the architecture used and its respective frequency compensation scheme. Section III describes the LDO design. Finally, post-layout simulation results and conclusions are presented in sections IV and V respectively.

1. Architecture

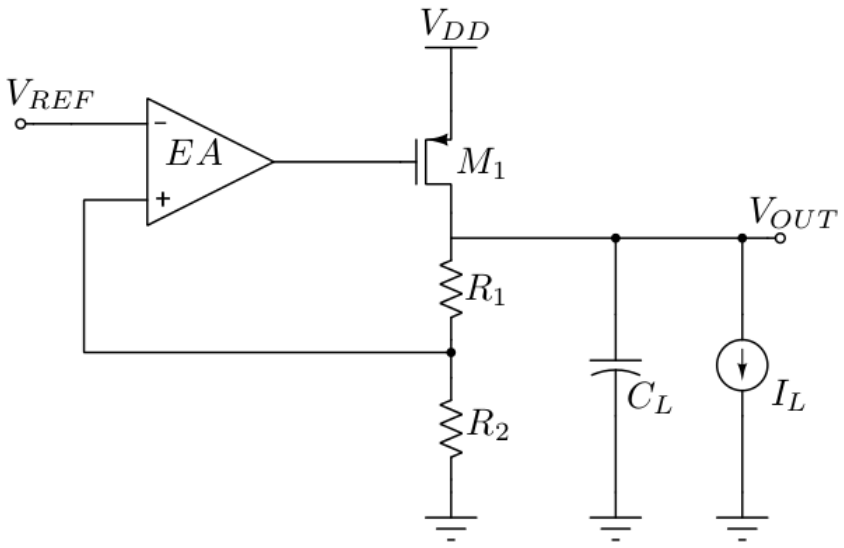

Figure 3. LDO regulator.

The classical structure of a low drop-out regulator is shown in Fig3. It consists of a PMOS transistor which delivers all the current demanded by the load, an error amplifier whose function is to bias the transistor gate, and a resistive feedback network that establishes the output voltage at the required value (Palacios, O.I. 2013). IL and CL represent the load current and capacitance respectively; CL can be determined by the parasitic capacitance of the metal paths that compose power distribution network, such as in (Milliken, R. J., Silva-Martínez, J., & Sánchez-Sinencio, E. 2007)., or by this same capacitance plus some internal or external capacitance added in order to improve the transient response. CL is defined as a parasitic capacitance of 100pF in (Ming, X., Li, N., Zhang, X. M., Lu, Y., Zhou, Z. K., & Wang, Z. 2015) and (Milliken, R. J., Silva-Martínez, J., & Sánchez-Sinencio, E. 2007)., whereas in (Ming, X., Li, Q., Zhou, Z. K., & Zhang, B, 2012).,

(Ming, X., Zhou, Z. K., & Zhang, B. 2011) and (Ho, E. N., & Mok, P. K. 2010), CL represents an off-chip capacitor. In this work, the output capacitance selected is 100pF, it models the parasitic capacitance from the metal path and an internal capacitance added for improving the transient response of the LDO.

1.1 Frequency compensation scheme

The frequency compensation scheme is selected according to the compensation type (external or internal) and the number of stages of the system. It was chosen an internal compensation structure for avoiding the use of an external capacitor. The pass-device is biased in the triode region for obtaining small area, however, this biasing will make necessary three gain stages for getting a high loop gain.

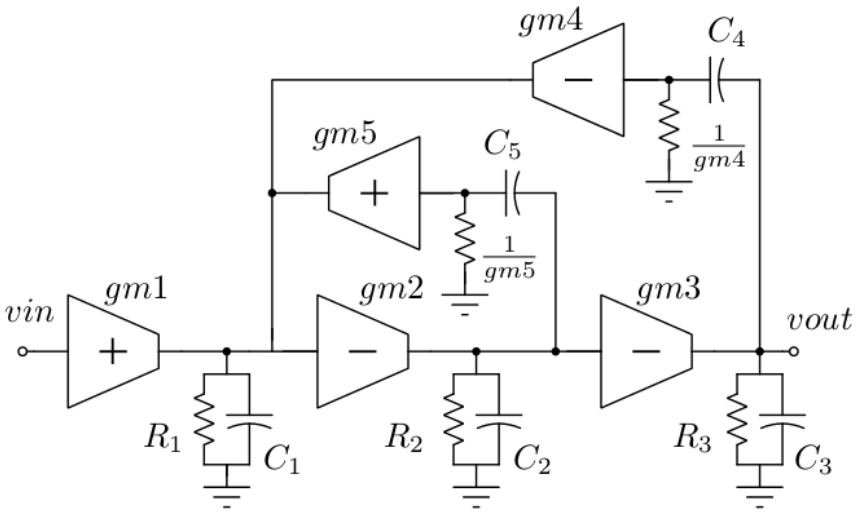

Figure 4. Compensation Scheme RNMCCB.

Fig4. shows the frequency compensation topology used in this paper, which was proposed by (Garimella, A., Rashid, M. W., & Furth, P. M. 2010) as a solution to compensate three-stage LDO, represented by gm 1 , gm 2 and gm 3 . This compensation strategy consists of two feedback loops —implemented with current buffers (gm 4 and gm 5)— to create two left-half-plane (LHP) zeros and cancel one of the nondominat poles, thus improving the system stability. The author in (Garimella, A., Rashid, M. W., & Furth, P. M. 2010) gives the following transfer function:

$$A(s) \simeq A_{DC} \frac{(1 + s\frac{C_5}{gm_5})(1 + s\frac{C_4}{gm_4})}{(1 + \frac{s}{w_{P1}})(\frac{s^2}{w_{P2}w_{P3}} + s(\frac{1}{w_{P2}} + \frac{1}{w_{P3}}) + 1)}$$

$$w_{P1} \simeq -1/R_1C_4gm_2R_2gm_3R_3.$$

$$w_{P2} \simeq -C_4gm_3/C_5C_3 \qquad w_{P3} \simeq -gm_4/C_4.$$

It is assumed that all poles are real and their expressions are given by:

Where it is observed that a LHP zero effectively cancels wP3, which results in a second-order system with a LHP zero, where wP1 is the dominant pole and wP2 the non-dominant one. However, when current buffers are employed for compensation, the feedback loops can generate complex-conjugate poles; those poles could cross to the right-half plane which become the LDO unstable. This work presents a Pole-Zero analysis of multi-stage amplifiers that was carried out for obtaining the expressions of the complex-conjugate poles produced by the feedback loops (Surkanti, P. R., Garimella, A., & Furth, P. M. 2011). Applying the assumption of widely-separated poles with complex pole pair and real poles, the transfer function results in the following:

$$A(s) \simeq A_{DC} \frac{(1 + s\frac{C_5}{gm_5})(1 + s\frac{C_4}{gm_4})}{(1 + \frac{s}{w_{P1}})(s^2/w_n^2 + 2\zeta s/w_n + 1)}$$

$$w_n^2 \simeq \frac{gm_3 gm_5 gm_4}{C_5(gm_5 C_3 + \delta)} \qquad \delta = C_{gd3}(gm_5 - gm_4)$$

If δ = 0 then Wn^2 is equal to the product of wP2 and wP3 of the transfer-function given in 1 and the poles are the same given in 2 and 3. In order to avoid RHP poles, the condition gm5 >> gm4 must be met.

1.2 Dynamic Biasing

In capacitor-less regulators there must always be a fast transient response to sudden changes in the current of the load, the input capacitance of the pass-device requires an amplifier with a good slew rate in order to discharge/charge said capacitance quickly. The dynamic biasing circuit, shown in Fig 6, is used to improve the transient response, either pushing or pulling current during transient variations at a critical point inside LDO loop.

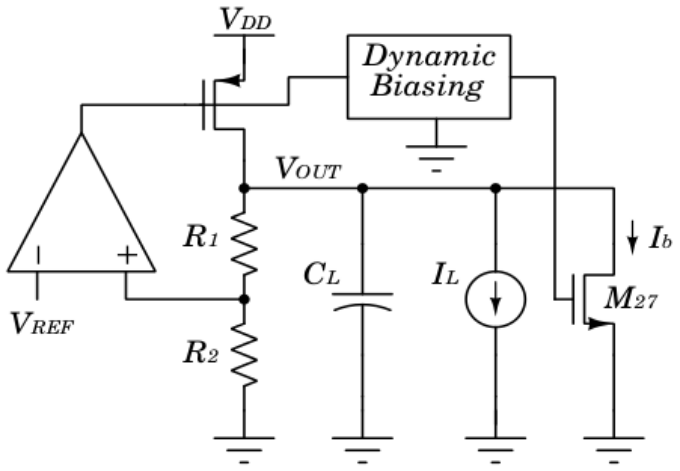

Figure 5. LDO and dynamic biasing.

This circuit was taken from (Amaya, A. F., Gómez, H. I., & Espinosa, G. 2015). Basically, it works sensing voltage changes at the input node Vin, thus generating a current response IB through M27. The cascaded logic inverters regenerate the signal coming from Vin in a shorter time than the given by the bandwidth of the regulator. Then, this regenerated signal is applied to a high-pass filter in order to obtain a small-duration pulse. Finally, transistor M27 converts this pulse to a pulling current where it is necessary.

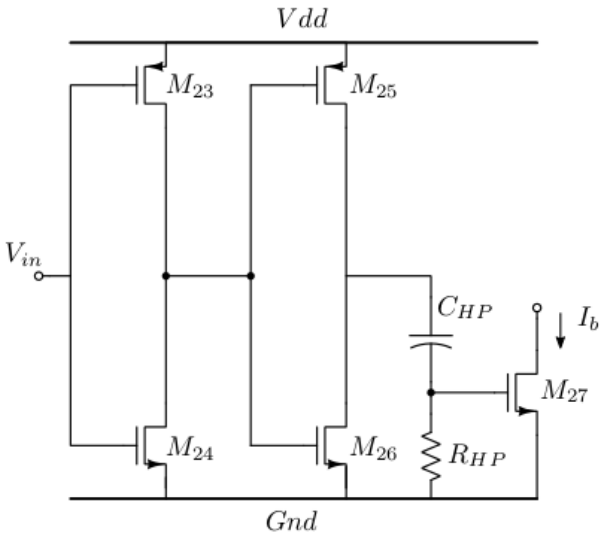

Figure 6. Dynamic Biasing Circuit.

Figure 7 shows the transient behavior of the circuit presented in figure 6, where it is observed that the signal current IB is only generated when the voltage input rises from a low value to a high value, for the other cases I b remains at a zero value. Hence, this is a circuit that only works for transient events consuming some amount of power, whereas for steady-state conditions the power consumption is null.

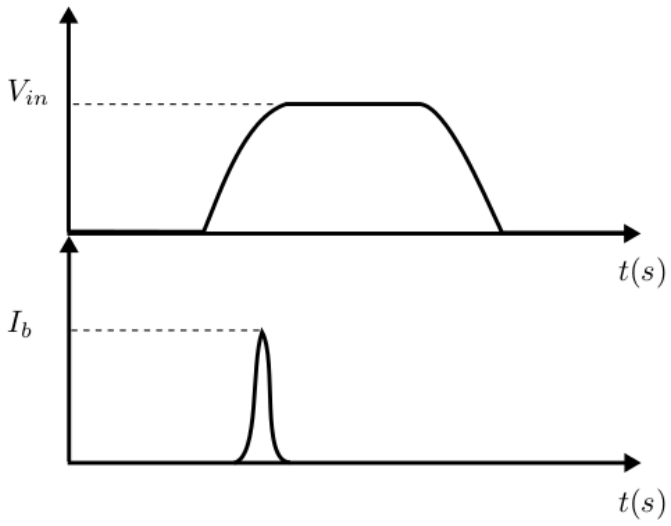

Figure 7. Dynamic Biasing.

The magnitude of the current IB depends on the W/L ratio of M27 and the cutoff frequency of the high-pass filter. When the load current drops suddenly, the gate voltage at the power transistor and the output voltage rise, therefore the dynamic biasing circuit detects such a change and draws a substantial current through M27 in order to quickly discharge the output capacitor and setting it to its targeted regulated voltage.

2. Circuit Design

The design of LDO regulators is given mainly by equation 6. This equation describes the steady-state behavior of the regulator; it relates the output voltage with both feedback resistors and the reference voltage. The latter generally is a parameter given to the designer, it comes from a bandgap voltage reference which is a temperature independent voltage reference circuit; whereas the former is a design parameter that depends on the required output voltage, the bandgap reference and the quiescent current flowing through the PowerMOS in no-load condition. The LDO design presented in this work divides the system in five blocks: feedback network, powermos, operational amplifier, compensation scheme and dynamic biasing design.

$$Vout = (1 + \frac{R_1}{R_2})V_{REF}$$

2.1 Feedback Network

The feedback network was designed according to the bandgap reference value, output voltage desired and current flowing through it, using the equation given in 6. The smaller said current the better the power consumption but the larger the size of the resistors, occupying a major area in the layout. Such a current also plays an important role in the stability of the system, since, some current is necessary for maintaining the nondominant pole far beyond the unity-gain frequency of the LDO loop for no-load conditions.

2.2 Power MOS

The PowerMOS is a PMOS transistor in charge of delivering all the current demanded by the load. On that account, the maximum load current plays an important role for determining the transistor size. When the power transistor is designed to operate in saturation region, its drain current is given by the following equation:

$$I_D = \frac{1}{2} K_p \frac{W}{L} (V_{GS} - V_{TH})^2$$

The dropout voltage of the regulator is the VDS voltage of the powerMOS, and its minimun value corresponds to the overdrive voltage. Bearing this in mind, the lower the dropout voltage and the larger the load current, the larger the dimensions of the power transistor.

$$I_D = K_p \frac{W}{L} ((V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2)$$

In the triode region, there is another design parameter corresponding to VGS voltage. With a high VGS voltage it is possible that the power transistor with a smaller size can provide the same

load current and dropout voltage than in saturation region. Therefore, the area of the power transistor can be minimized with a high VGS voltage. However a high VGS voltage can take transistors of the output stage of the error amplifier to triode region and hence decrease the loop gain system. Another critical drawback of the powerMOS biased in triode region is its poor gain. Which leads to the use of a high-gain error amplifier.

2.3 Error amplifier and compensation scheme

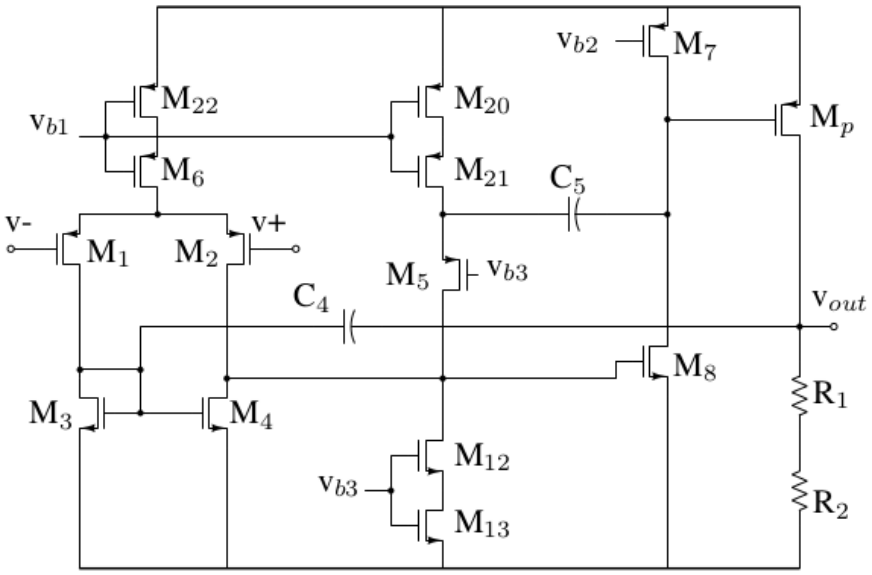

Figure 8. Circuit diagram of the error amplifier and compensation.

Both the error amplifier and Current Buffers (CBs) for compensation of the Fig 4 were designed in parallel in order to set the system poles in the frequency required to achieve stability in all load current conditions. The worst-case stability, in internal-compensated regulators is for low load currents, in such conditions the output pole is closer to the dominant pole, degrading the phase margin. Hence, the system was compensated using the pole expressions given in 2, 3 for light-load conditions and keeping in mind the consideration gm5 >> gm4 in order to avoid complex-conjugated poles in the right-half plane. Besides, the open loop gain specification of the system for the worst case (heavy-load condition) was at least 50 dB. Therefore, the open-loop gain of the amplifier plus the PowerMOS gain including the load added by the current buffers must fulfill such a value.

Fig 8, shows the transistor level implementation of the error amplifier and the compensation scheme. M4 and M5 represent the current buffers for compensation gm4 and gm5 respectively. Said CBs were implemented such as was proposed in (Garimella, A., Rashid, M. W., & Furth, P. M. 2010). This is shown in the figure 9.

Self-cascode composite transistors were used as current mirrors, taking advantage of its high output impedance in order to mitigate the loading effects added at the output node of the first stage by the common-gate amplifier M5 and its biasing circuit. The equivalent output resistance of a self-cascode transistor coincides with the output resistance of two-transistor in cascode configuration and it requires a lower biasing voltage (Sanz, M. T., Celma, S., Calvo, B., & Flandre, D. 2006)..

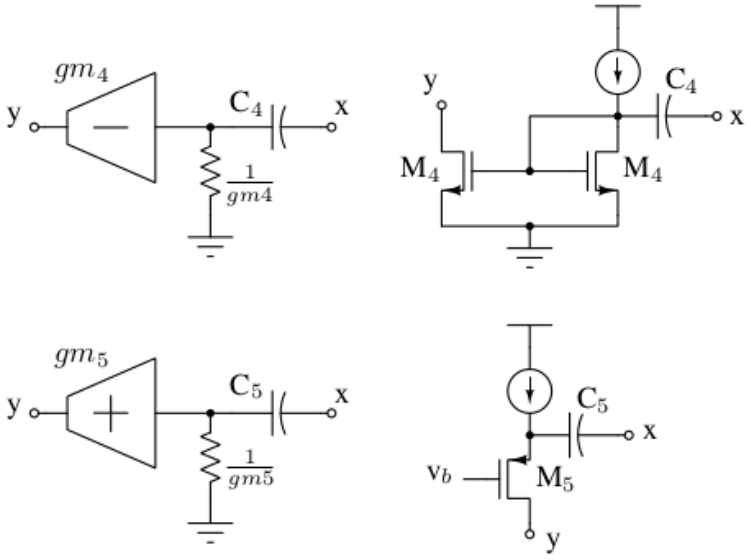

Figure 9. Currents buffer for compensation.

2.4 Dynamic biasing design considerations

As already mentioned, the architecture shown in Fig 6 was used as dynamic biasing circuit in order to improve the transient response. The transient response of the LDO strongly depends on the output stage of the error amplifier, specifically on the error-amplifier ability to charge and discharge the input capacitance of the PowerMOS. As a result, the regulated output has an asymmetrical response in terms of its settling time. This is, the settling time is different for both a negative load dump and a positive load dump (Rincon-Mora, G. 2014). In theory, the amplifier employed in this work has a better performance pulling than pushing current, this means that the powerMOS is better at sourcing current than sinking current to the load which in turn means that the regulator has a higher settling time when load current falls quickly. Taking this into account, the input of the dynamic biasing circuit was connected to the gate of the power transistor and the drain of the transistor M27 connected at the output of the LDO (Figure 5) thus reducing the settling time when the load current drops suddenly.

Inverters were designed taking into account that NMOS transistors have higher mobility than PMOS transistors thereby the W/L ratio of the PMOS transistor is higher than the NMOS

transistor. On the other hand the frequency $f_{HP} = 1/2\pi RC$ was selected such that transistor M27 can be triggered effectively depending on the rise time and the fall time of the current load. The figure 10 presents the schematic of the LDO regulator with all blocks already mentioned previously and implemented at the transistor level. The figure 11 shows the layout of the previous schematic, occupying an area of $0.007\ mm^2$.

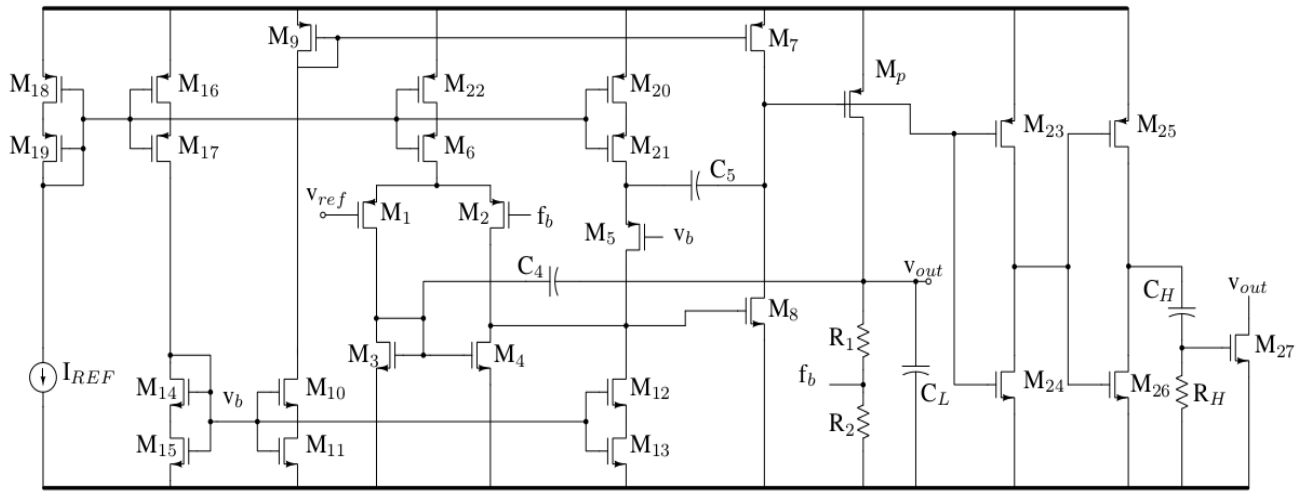

Figure 10. Schematic of the Low Drop-out.

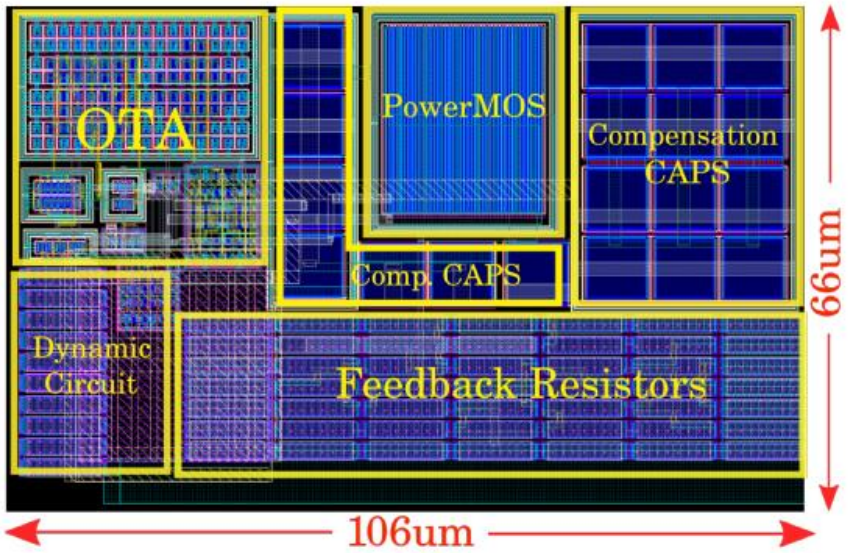

Figure 11. Layout of the LDO.

3. Simulation results and comparative study

The LDO regulator was simulated in a TSMC 130nm CMOS technology. Post-layout simulations were performed varying bias current, temperature and voltage supply. Corner models for transistors were added as well. The simulations are divided by the type of parameter, this is Open-loop AC response, Steady-state response and Dynamic state response.

3.1 Open-Loop Ac Response

The LDO's Open-loop AC response was simulated for light-load, medium-load and heavy-load conditions. This is, when the load current is approximately 100μA, 1mA and 50mA respectively. Parameters such as Loop gain , phase margin and Gain-bandwidth were calculated and summarized for each of the current conditions. These results are shown in the following figures.

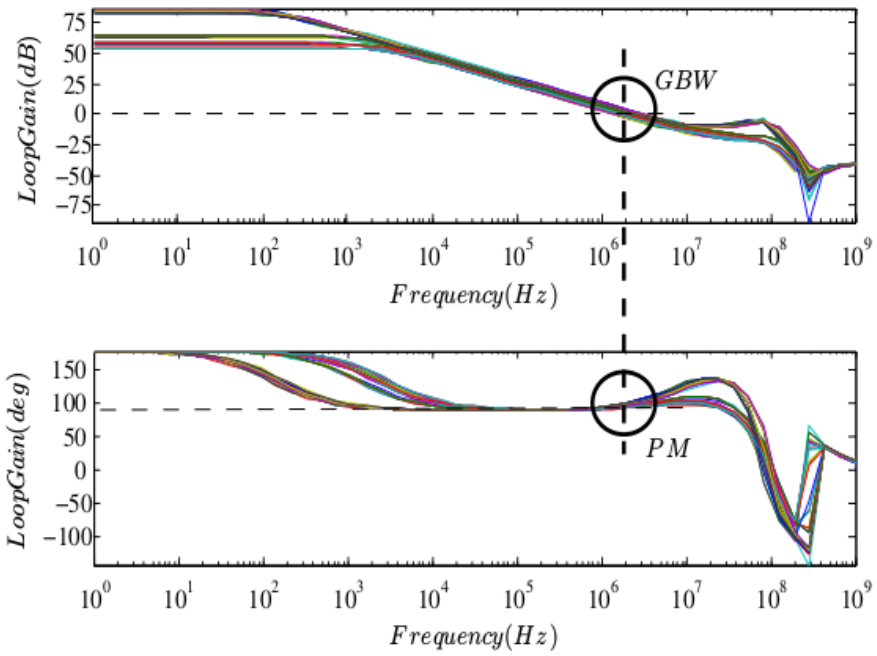

Figure 12. AC response heavy-load condition.

Table 1:
Summary for high load currents.

Parameter	Min	Typ	Max
A_v	53.05	61.05	87.7
PM	91.87	95.85	106.1
GBW	1.34 MHz	2MHz	3.62 MHz

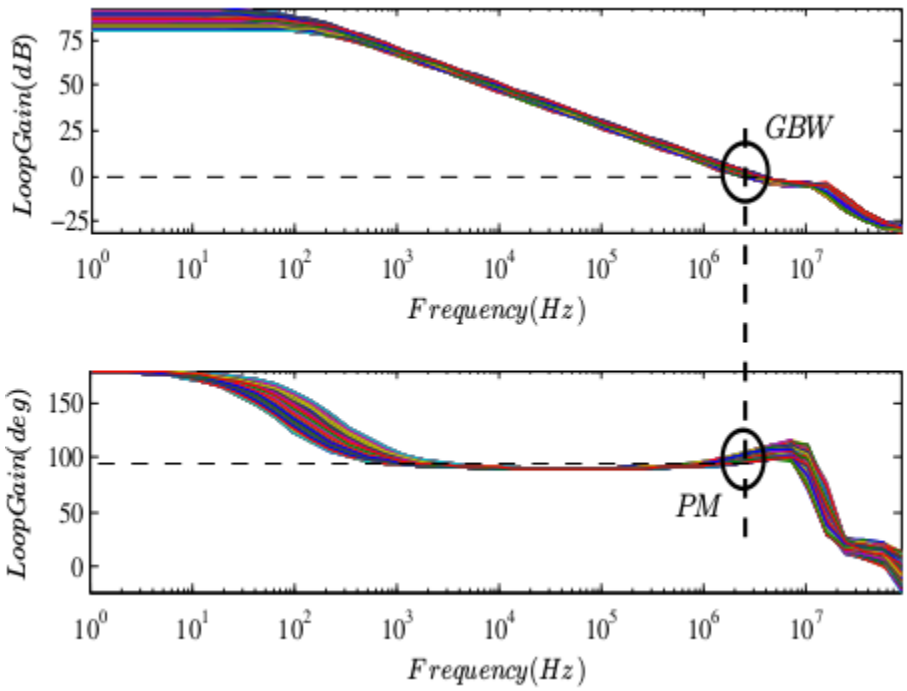

Figure 13. AC response medium-load condition.

Table 2.
Summary for medium loads currents.

Parameter	Min	Typ	Max
A_v	79.73	85.82	92.41
PM	88.2	101	107.7
GBW	2.24 MHz	2.85MHz	3.82 MHz

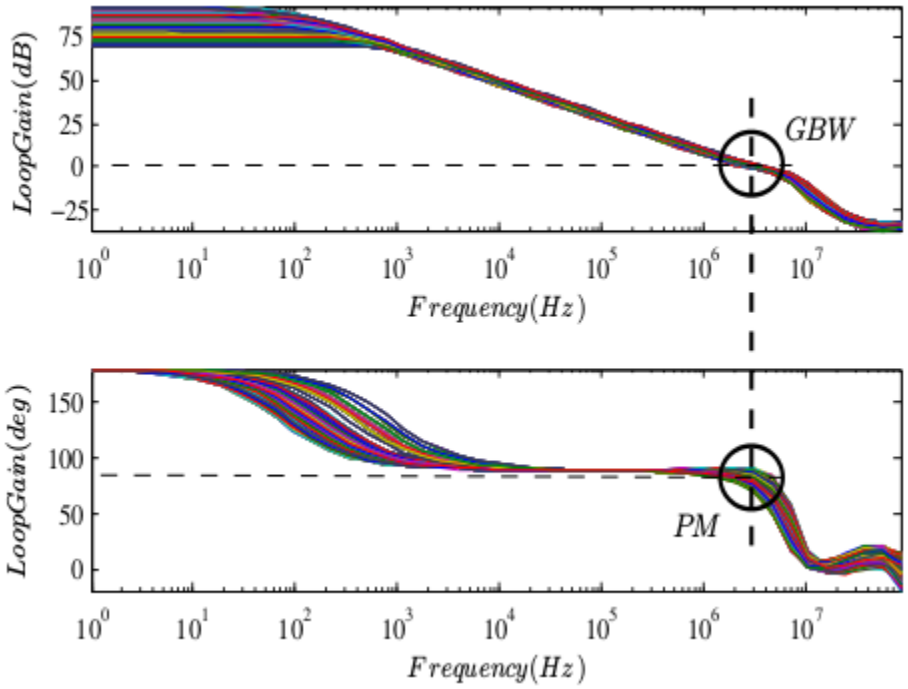

Figure 14. AC response light-load response.

Table 3.
Summary for low load currents.

Parameter	Min	Typ	Max
A_v	69.59	86.02	92.04
PM	66.54	83.29	92.05
GBW	2.52 MHz	3.13MHz	4.14 MHz

According to table 1, 2 and 3 it is observed that high load currents is the worst-case gain but the better-case phase margin, while low load currents is the worst-case phase margin but the better-case gain, as expected.

3.2 Steady-State Response

In steady-state, there are several LDO parameters to consider, for instance, load regulation and line regulation specifications, they are measures to quantize the ability of the LDO to regulate the steady-state output voltage for given voltage supply and load steady-state values. Load regulation is the variation in the regulated voltage due to variations in the load current for static-state conditions. it is quantized thus:

$$LDR = \frac{\Delta V_{out}}{\Delta I_{load}}$$

Line regulation is the variation in the output voltage due to variations in the voltage supply when the regulator has reached static-state. its equation is given thus:

$$LNR = \frac{\Delta V_{out}}{\Delta V_{DD}}$$

The following figures show the simulation results and the table 4 and 5 presents the parameters summarized.

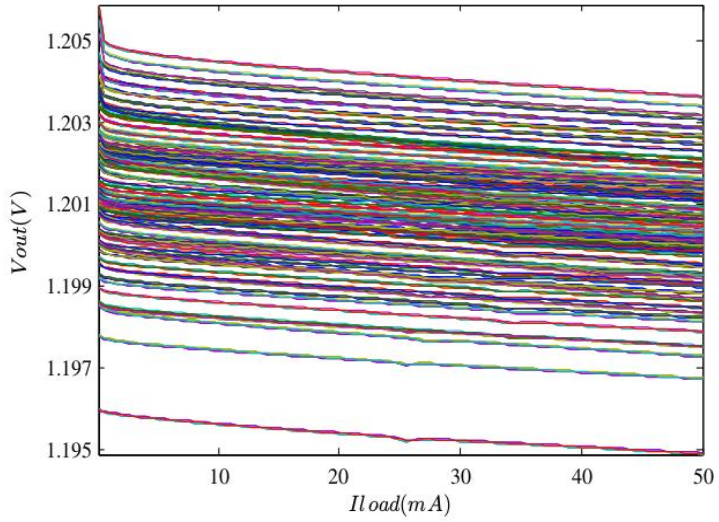

Figure 15. Load regulation.

Table 4.
Summary of the load regulation.

Parameter	Min	Typ	Max	units
LDR	18.77m	22.1m	45.47m	mV/mA

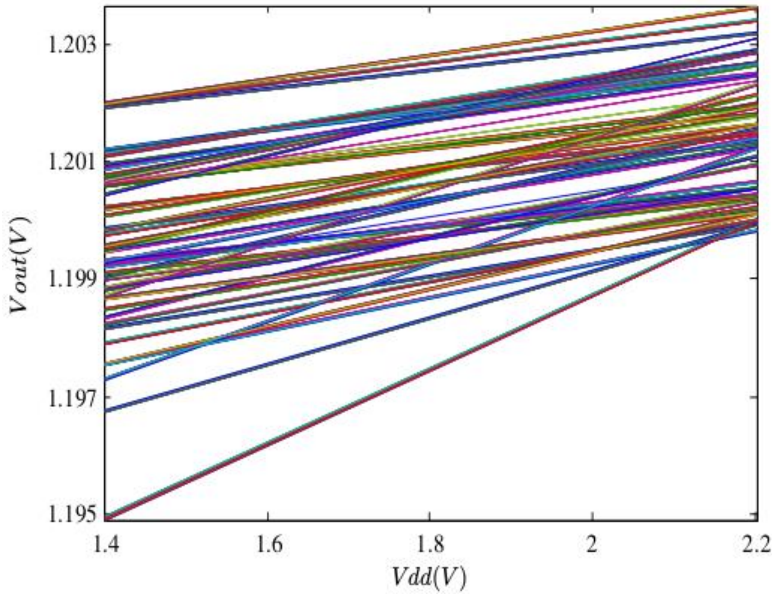

Figure 16. Line regulation.

Table 5.
Summary of the line regulation.

Parameter	Min	Typ	Max	units
LNR	1.4	2.18	6.36	mV/V

3.3 Dynamic State Response

In dynamic state conditions, the LDO's ability to regulate the output voltage due to current load dumps is analyzed. In such a state the LDO must respond quickly in order to reduce variations in the output voltage. The settling time was measured when the LDO experiments a positive load dump, since, as already mentioned, in such a case the LDO response is slow. Parameters like overshoot and undershoot were measured as well.

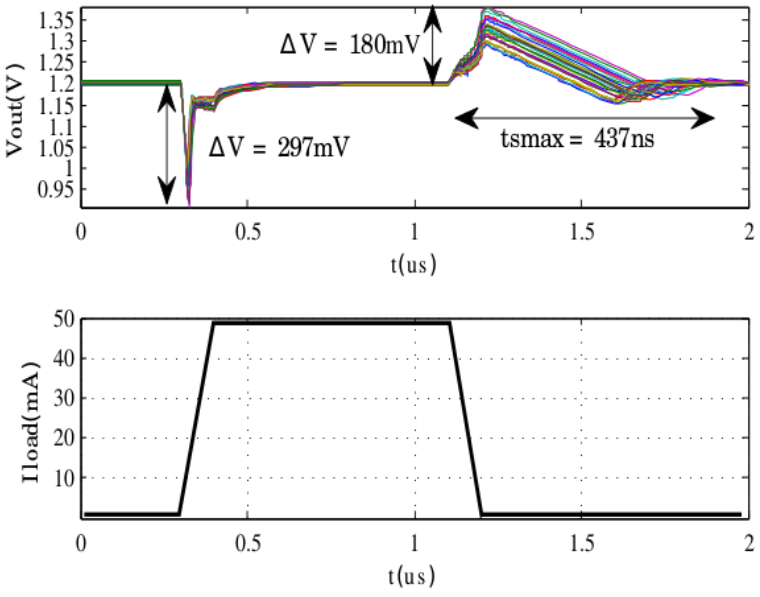

Figure 17. Load transient.

Table 6.
Summary of the load transient.

Parameter	Min	Typ	Max	units
ts	134	237	437	ns
Overshoot	72.04	101	180	mV
Undershoot	161.1	208	297	mV

3.4 Mismatch

The LDO performance, taking into account mismatch on transistors, was characterized as well. Mismatch mainly affects circuits such as Current mirrors and input pairs in error amplifiers, introducing error at the mirrored current or adding offset at the output voltage respectively. For this case, the regulated voltage for low load currents and high load currents was verified in montecarlo. The following table shows the results.

Table 7.
Summary of the regulated voltage in montecarlo.

Parameter	Mean	Sigma
Vo@100uA	1.206 V	12m V
Vo@50mA	1.194V	13.19m V

A performance comparison with some previously reported capacitor-less LDO regulators is given in Table 8.

Table 8.
Comparison of the result.

Parameter	Ref [6]	Ref [13]	Ref [9]	This work
Technology [nm]	350	350	180	130
Input voltage range [V]	1.7-3.3	2-3.3	1.8-3.3	1.4-2.2
Dropout [V]	0.2	0.2	0.2	0.2
LNR [mV/V]	-	13.1	54.7	2.18
LDR [mV/mA]	-	1.05	0.109	22.1m
Compensation Capacitance [pF]	6.8	-	7	5
Output current [mA]	100	60	100	50
Current consumption [uA]	15	54	20	60
Active chip area $[mm^2]$	0.047	0.07	0.145	0.007

4. Conclusions

A 1.2V 130nm CMOS capacitor-less three-stage LDO voltage regulator with maximum load current of 50mA and dropout voltage of 200mV was designed. The RNMCCB architecture allowed to compensate internally a three-stage system with a total compensation capacitance down to 5pF achieving stability in all current cases, even with a high output capacitor of 100pF. The powerMOS was designed to be biased in triode region in order to minimize the area occupied by the regulator. With these advantages, the LDO designed in this work is suitable for System-on-Chip applications.

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