DIGITAL-TO-TIME CIRCUITS FOR CLOCK AND DATA RECOVERY

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Y DE TELECOMINICACIONES
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RESUMEN

TÍTULO: DIGITAL-TO-TIME CIRCUITS FOR CLOCK AND DATA RECOVERY[*]

AUTORES: NESTOR DARIO CUEVAS SANDOVAL[**]

PALABRAS CLAVE: CMOS, CML, mezcla de fases, recuperación de datos y reloj.

DESCRIPCIÓN:

Este documento resume la selección de topologías, el proceso de diseño, la implementación del layout y los resultados de simulaciones post-layout de dos circuitos fundamentales en las arquitecturas del estado del arte de circuitos Clock and Data Recovery. Estos circuitos son el phase interpolator (PI) y el CML to CMOS Converter (CML-to-CMOS), que juntos conforman el sistema de generación del reloj del Clock and Data Recovery. Las topologías para estos circuitos fueron seleccionadas a partir de una revisión del estado del arte, en base a las ventajas y desventajas de desempeño de cada una de ellas. Se propone y describe una metodología de diseño para las arquitecturas seleccionadas, el cual fue estructurado a partir de la experiencia de diseño. El diseño fue validado mediante análisis de variaciones PVT y Monte Carlo, mostrando un desempeño apropiado para aplicaciones de Clock and Data Recovery Los layouts de estos circuitos fueron desarrollados utilizando técnicas como centroide común e interdigitación. Estos circuitos fueron diseñados en una tecnología de 180nm y ocupan un área de 1012μm^2 (CML-to-CMOS) y 10710μm^2 (PI). Finalmente, se reporta la escritura de un artículo científico acerca de una arquitectura novedosa para implementar Level Shifters, desarrollada en paralelo con la presente tesis. El desempeño del Level Shifter también fue evaluado a través de análisis de variaciones PVT y Monte Carlo y su layout ocupa un área de 156$\mathrm{\mu m}^2$.

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ABSTRACT

TITLE: DIGITAL-TO-TIME CIRCUITS FOR CLOCK AND DATA RECOVERY[*]

AUTHOR: Nestor Cuevas[**]

KEYWORDS:.CMOS, CML, phase mixing, clock and data recovery

DESCRIPTION:

This document summarizes the topologies selection process, design procedure, layout implementation and post-layout simulations results of two fundamental circuits within state-of-the-art Clock and Data Recovery architectures. These circuits are the phase interpolator (PI) and the CML to CMOS converter (CML-to-CMOS), which together compose the clock generator system of the Clock and Data Recovery. The topologies for these circuits were selected from a state-of-the-art review, based on the performance advantages and disadvantages of each one of them. We proposed and described a design method for the selected architectures, which was structured from the design experience. The design was validated through PVT and Monte Carlo variations analysis, showing a suitable performance for Clock and Data Recovery applications. The layouts for these circuits were developed by using standard techniques such as common centroid and interdigitation. These circuits were designed in a 180nm technology node and occupy an area of $1012\mu m^2$ (CML-to-CMOS) and $10710\mu m^2$ (PI). Finally, it is described an additional work about a novel level shifter architecture, developed in parallel with the thesis, from which a scientific article was written. The performance of the proposed level shifter was evaluated through PVT and Monte Carlo variations analysis as well and the circuit layout occupied an area of $156\mu m^2$.
Index Terms—High-speed, full-swing, small-swing, phase mixing, current-mode-logic, CMOS-logic.

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INTRODUCTION

The increase in information density, which involves the rise of cloud computing and mobile networks, has driven a great need to expand data communication bandwidth. The constant demand in data transmission is present in several levels of abstractions: internet connections through modems, devices communications using coaxial wire or optical fiber, and the exchanging of data between chips inside the same board or even circuits inside the same chip. Regarding this, communication interfaces play a very important role, pushing the limits of the data rates in an energy-efficient manner.

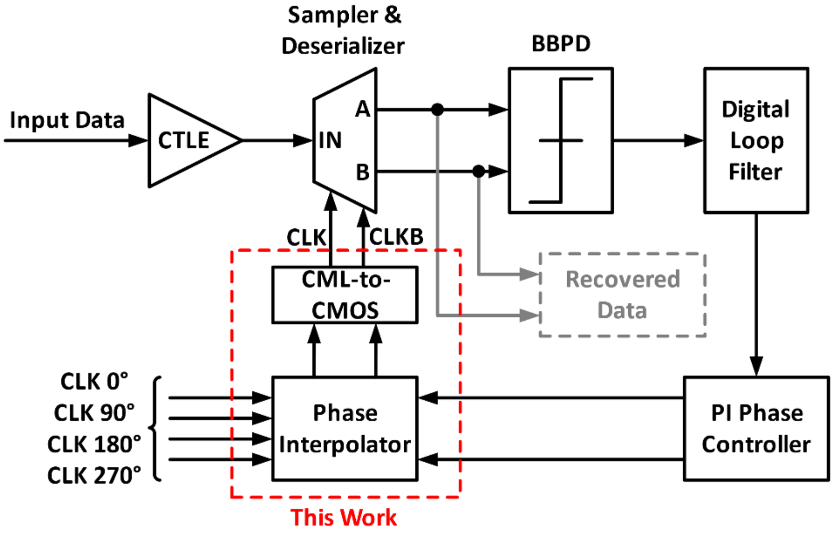
A typical communication system comprises a transmitter (TX), a channel, and a receiver (RX). The transmitter provides the necessary power level to send data through the channel. In the channel, data experiments several undesired effects: crosstalk, channel losses, noise interference, skew and inter-symbol-interference (ISI). All these effects degrade and threat the transmission reliability. The RX recovers and synchronizes the incoming data, ensuring very low bit-error rate (BER).

In high-speed interfaces, the preferred clocking scheme is the plesiochronous approach [1], in which the transmitter delivers only the data to the receiver without any kind of clock signal. The timing synchronization is performed in the RX using a clock and data recovery (CDR) system. In this context, CDR circuits are essential systems in many modern transceiver architectures because they must recover the data and timing information combining high performance, low cost, low power, and small area.

This work is part of a Ph.D. research project associated with the design of a complete digital phase-locked loop CDR (DPLL-CDR) for USB 3.0 protocol [2]–[4]. Fig. 1

shows the CDR architecture used in the aforementioned Ph.D. research project. This system comprises a continuous-time linear equalizer (CTLE), which is in charge of making equalization to the attenuated input signal. This equalized data goes through the sampler-&-deserializer that delivers a well-defined data, resulting from the synchronization and sampling with the recovered clock. This clock signal comes from a phase interpolator (PI) via a current-mode-logic to CMOS-logic converter (CML-to-CMOS). The bang-bang phase detector (BBPD) detects the phase difference between the input data and the clock signal and passes it by a digital loop filter + PI phase controller system. The latter sends a control signal for the PI + CML-to-CMOS system to generate the appropriate clock phase through a phase mixing technique, seeking data and clock synchronization. These two circuits are imperative for the correct operation of the whole system, as the data recovery directly depends on an accurate clock phase adjustment all along the synchronization process. This work is limited and focused in the circuits inside the highlighted red box.

Figure 1. CDR blocks diagram. [5], [6]



The Ph.D. project from which this thesis arises is part of a SoC project of the Integrated Systems Research Group - OnChip, at the Universidad Industrial de Santander. SoC applications typically use multiple voltage domains to reduce power consumption and operate in different modes (e.g. sleep mode). These domains need an interface among them, which ensures proper voltage levels to receive and send control signals along the chip. Level shifter circuits are commonly used to meet this necessity. For this reason, and as an additional work developed in parallel to this thesis, it is proposed a novel all-thin-devices topology for level shifter circuits. This work is condensed in the annexed document to this thesis.

The work presented in this paper is organized as follows: Section II compares several topologies of each circuit in order to select the best option for this application. Section III describes the details of the process performed to achieve a correct design of the selected architectures. Section IV reports the results obtained from post-layout simulations and some analyses to evaluate the performance of the designed circuits. Finally, Section V collects some of the most significant parts of the present work.

1. TOPOLOGIES SELECTION

Based on a state-of-the-art review, this section presents three possible architectures, two for the PI and one for the CML-to-CMOS circuits. To select the more suitable topology for each circuit, different performance parameters such as power consumption, area and performance, were taken into consideration. The following subsections explain some of the advantages and disadvantages for each architecture and give a justification for the selected one.

A. Phase interpolator

Within the CDR operation, the PI must generate a clock with a certain phase depending on a digital word, which controls the output phase. This phase value is obtained from four input clocks, coming from a phase-locked-loop (PLL) circuit. The phases of these clocks are: 0° and 180° (CLKI and CLKIB), as well as their quadratures, 90° and 270° (CLKQ and CLKQB). The latter allows having a clock phase in any of the 4 quadrants. In each quadrant, CDR requires a linear behavior to perform a good synchronization process between the data and the clock.

Fig. 2 shows one of the most used PI topologies in current CDR circuits. This architecture allows a phase interpolation based on a weighted summation of the input clocks. This summation can be expressed as:

$$V_{OUT+} = \alpha_1 * CLKI + \alpha_2 * CLKQ \qquad (1)$$

Where α1 and α2 are factors that depend on the number of active current sources in every branch. These sources, and thus the output phase, are controlled by external signals through switches. Furthermore, this circuit has control signals for the quadrant of the phase shifting (i.e. 0° to 90°, 90° to 180°, etc.). Four switches (S0-3) make this control and allow a phase range of 360°. In terms of disadvantages, the main issue of this circuit is nonlinearity. The constant change of the polarization current will modify the operating point of the input differential pair and the circuit behavior as well. This does not guarantee a linear phase change when a new current source cell is activated or deactivated.

Figure 2. PI topology, proposed in [7], [8].

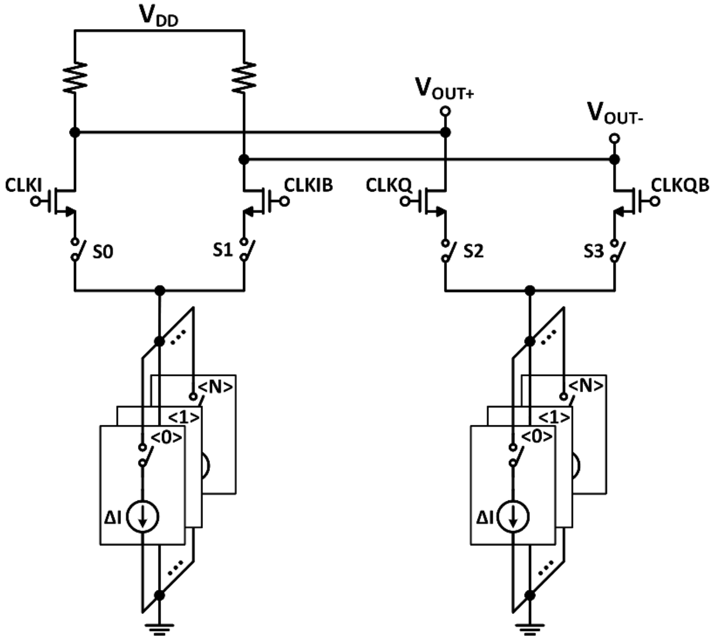


Fig. 3 depicts an all-digital PI topology, based on the use of inverter cells. Its principal advantage is a very reduced area, as only digital circuits comprise it. Inside the unit cell, two inverters with their output terminals connected are in charge of the phase mixing, delivering the average phase of the two input phases. The three unit-cell outputs and the set of 3-to-2 multiplexers allow selecting the desired output phase using a digital number. However, this circuit could present some issues which make it not suitable for the application presented in this work. One of these issues appears when the application needs a large number of phases per quadrant, i.e., a considerable amount of series stages (more than three, based on performed simulations). If the processed signal amplitude, by effect of the muxes or the paths, suffers any type of attenuation, it will not be fixed by the inverter cells and will increase as the signal goes through the circuit. The exposed attenuation problem would appear in the output node and could cause complications with the driving of the circuit load (CML-to-CMOS input), i.e., would make the output signal swing such small that the CML-to-CMOS would not recognize it. Another issue with this topology refers to its single-ended nature, as it creates the necessity of generating the inverse output signal. It could be solved by using an inverter cell at the output node, however, this would also cause a desynchronization between these two clocks, which would mean a new problem to solve. In conclusion, to clear up the issues exposed above, it is necessary to reformulate the topology and this is out of the present work objectives.

Figure 3. PI topology (one quadrant), proposed in [9].

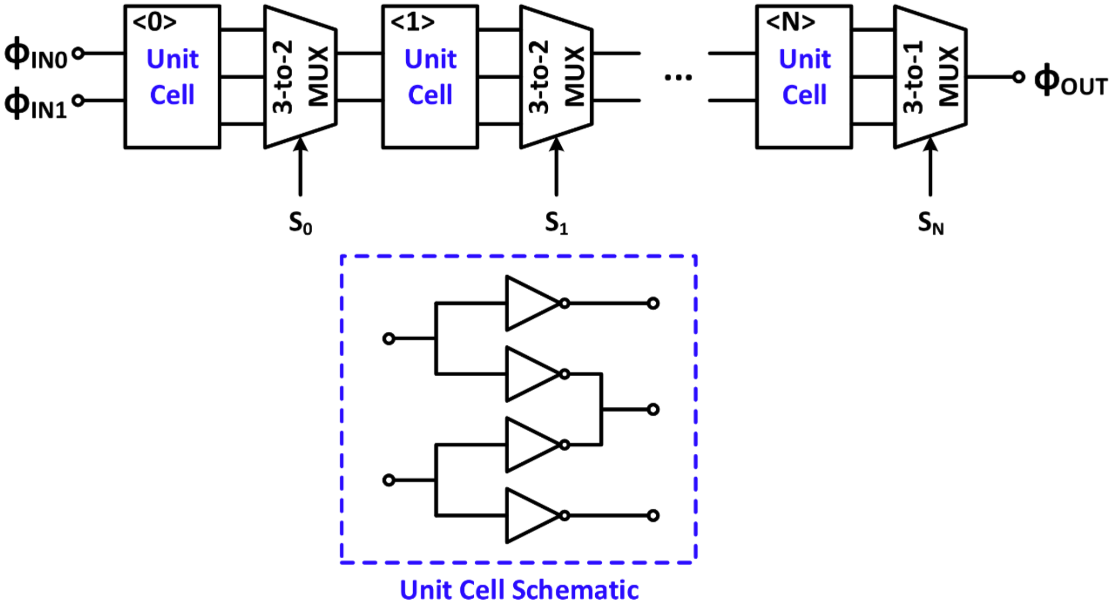
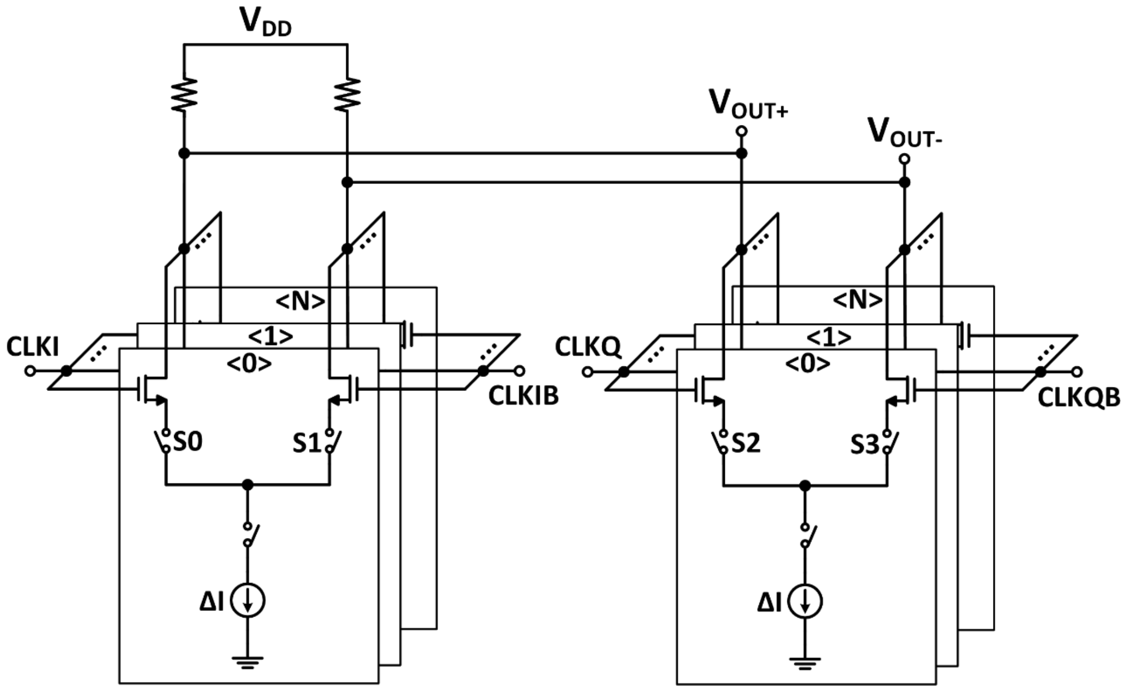


Fig. 4 illustrates the architecture selected for the PI implementation. Its operation is similar to that described by the weighted summation in (1). However, the basic cell of this circuit is composed of the whole differential pair along with its polarization current source, thus, the nonlinearity issue in the first topology described in this section decreases. Furthermore, this circuit has been used in some functional CDR designs [6], [10], [11], achieving good performance results.

Although this architecture is not the most area-efficient, its linear theoretical behavior overcomes the area advantages shown by the other topologies. Taking into account the relevance that this circuit has in the whole CDR operation, described in previous sections, this area expense is necessary to obtain the best possible performance.

Figure 4. Selected topology for PI (one quadrant). [6], [10], [11]



B. CML-to-CMOS converter

The task of this circuit consists in transforming a small-swing signal (CML-type signal coming from the PI) into a full-swing signal (square wave varying between V_{DD} and GND) and provide it to the sampler block (Fig. 1), removing all the noise negative effects.

Fig. 5 depicts a novel CML-to-CMOS circuit, with an active load differential pair as the input amplifier and two modified inverters as output stages. These latter cells allow the final full-swing from GND to V_{DD}. Despite the circuit functionality is quite simple, the components array used for generating the biasing for the differential pair active loads is not optimal. The use of five resistances in this strategy decreases the circuit performance against PVT variations because of their high variation with temperature and increases the needed area as well. This issue could be avoided by using diode-connected transistors as the circuit load. However, other problems will be still present in this topology, such as the performance dependence on the input common-mode level. This voltage will define the input devices polarization point and is defined by the PI output common-mode level, which can be between V_{DD} and GND, depending on that circuit design. Another drawback with this architecture refers to the input amplifier, which must have a very high gain if the input signal has a quite small-swing. This could cause a bigger issue, since it does not follow the recommendations for high-speed design, described [12].

Figure 5. CML-to-CMOS topology, proposed in [13].

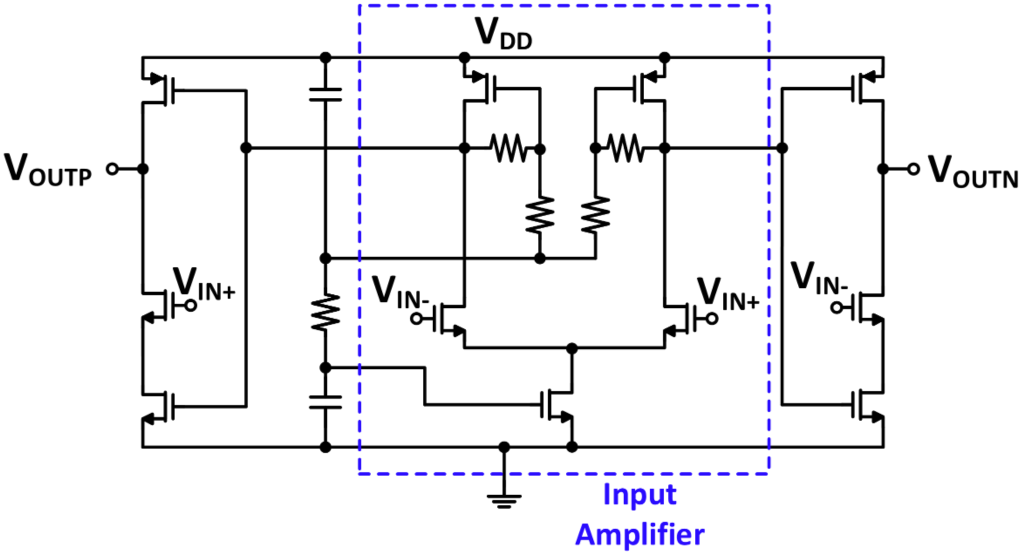
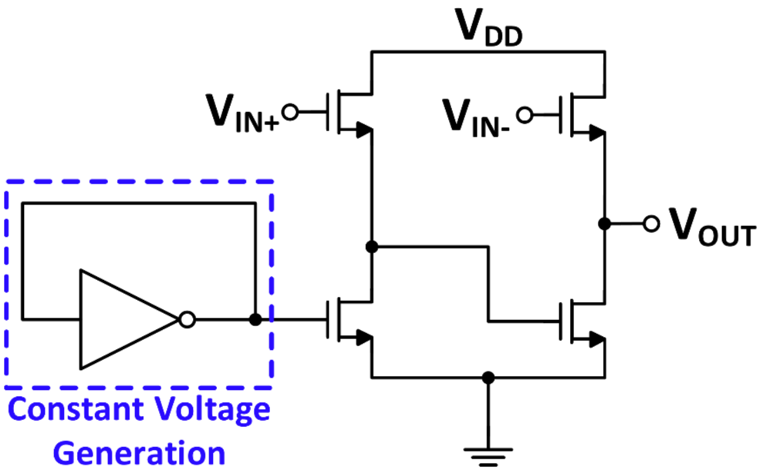


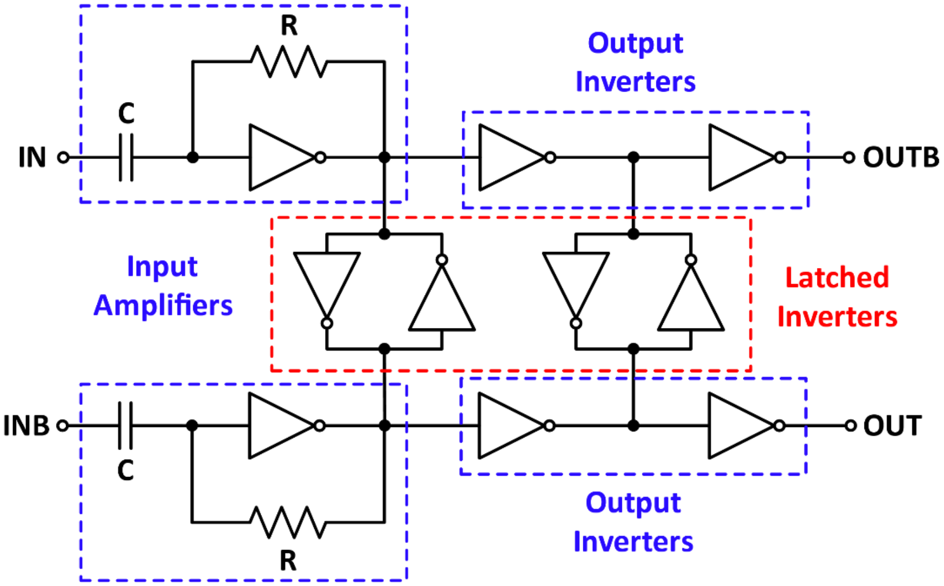
Fig. 6 illustrates an extremely-low area CML-to-CMOS circuit. Although this topology is composed of a small number of components, there are some reasons why it is not the best option for this application. This topology presents the same previously described issue with the input common-mode voltage level. Furthermore, the structure of the constant voltage generation block, generates an ideal short-circuit between V_{DD} and GND every time V_{IN+} is in a high level. Because of the constant voltage generation block composition, there is always another ideal short-circuit inside the inverter cell, caused by the unit gain feedback as it activates the PMOS and NMOS transistors at the same time. In summary, this architecture resigns current consumption to reach a smaller area. Finally, as the circuit is single-ended, it would be necessary to use another inverter for generating the output clock inverse. This latter would cause a desynchronization between the output clock and its inverse, which would need more circuitry to be corrected.

Figure 6. CML-to-CMOS topology, proposed in [14].



In Fig. 7, it is shown the topology selected for the CML-to-CMOS implementation. The architecture of its input amplifiers allows them to fulfill the filtering function as well. Thus, the input capacitors isolate the input common-mode voltage level, avoiding a performance dependence on this variable. The resistive feedback inverter is an analog amplifier, whose gain is directly proportional to the resistance value. The latched inverters allow keeping synchronized the amplified clock with its inverse. Finally, the output inverters give the full-swing and square shape to the clock.

Figure 7. Selected topology for CML-to-CMOS. [15]–[17]



Although this topology (Fig. 7) seems to occupy a large area, its performance evaluation gives a better result than the other architectures. The input DC level isolation, the latches synchronization technique (which does not exist in the previous circuits) and the good features exposed above, make this option the best for the present application.

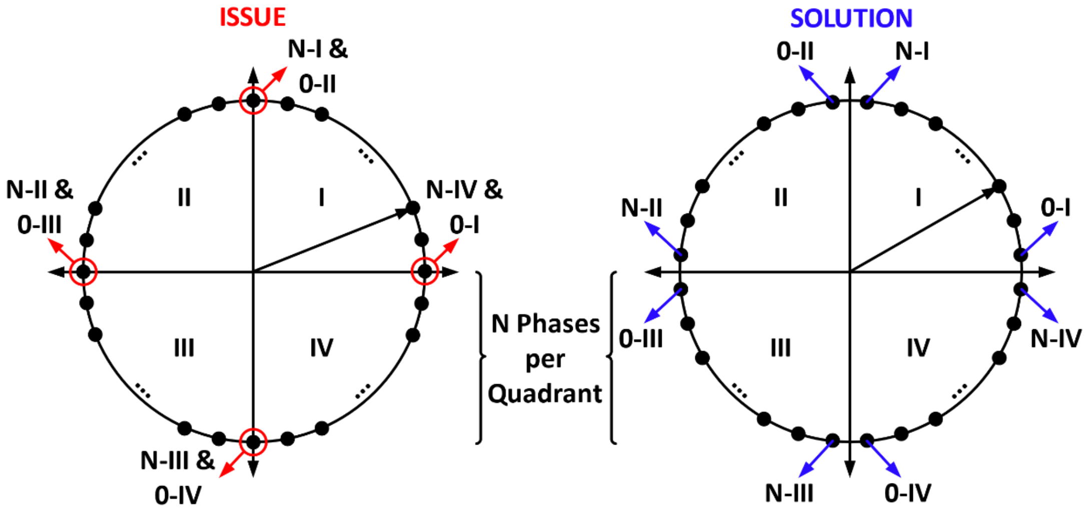
2. DESIGN METHODOLOGIES

A. Phase interpolator

In this design, for accomplishing CDR requirements, we started from the following specifications: an operating frequency of 1.25GHz and a resolution of 32 phases per quadrant.

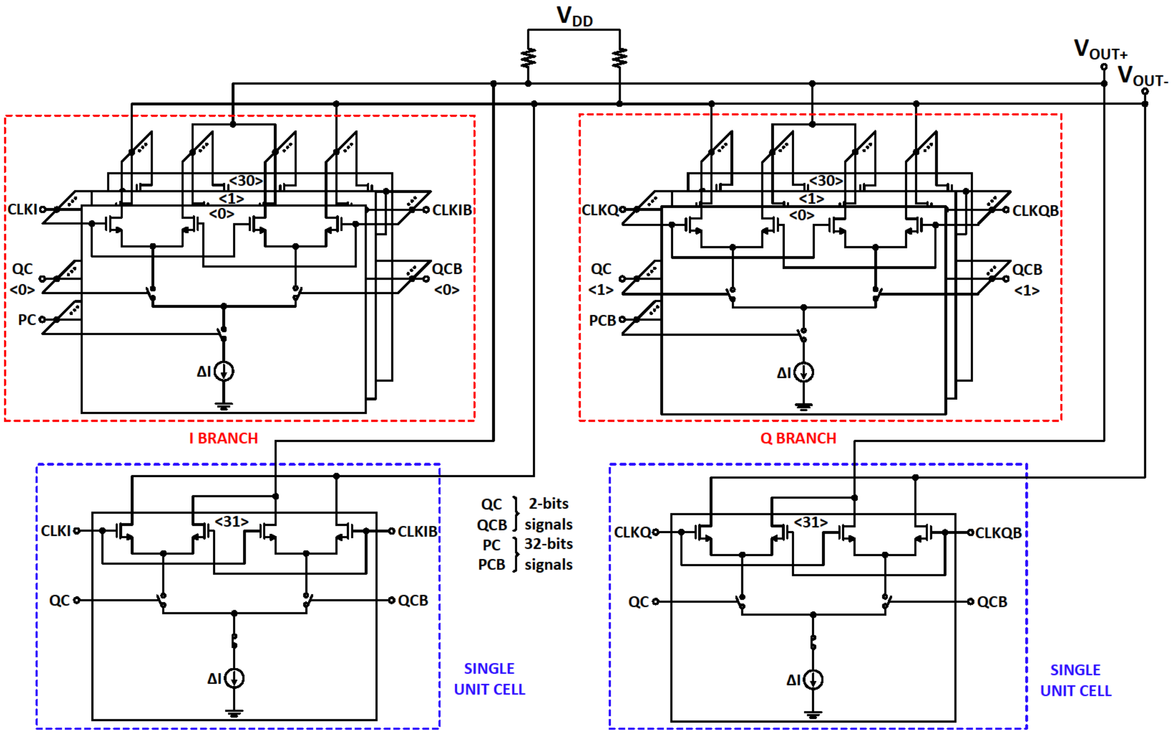
Before starting the design, it was necessary to review some architecture features. First, it is imperative to modify the unit cell in order to achieve any phase in any of the four quadrants, as illustrated in Fig. 9, where PC and its inverse PCB, control the phase, and QC and QCB control the quadrant. As well, a phase shifting issue usually appears with the use of the selected topology and it is depicted and highlighted with red in Fig. 8. This image shows an overlapping between the last phase in a quadrant (N) and the first one in the next quadrant (0). The issue is related to the thermometer-type phase control connected to PC and its inverse, PCB, shown in Fig. 9. For achieving the desired quadrant, QC and QCB allow mixing this quadrant upper and lower edge phases (two of the four input phases). To cross the quadrant, PC or PCB turn on more parallel unit cells, increasing the weight of the upper phase at the output, while the opposite control signal decreases the lower phase weight. With the conventional topology, at the quadrant edge, the upper phase has all the unit cells on its side turned on, being reflected at the output. Following this logic, the next quadrant first phase would be exactly the last one in the previous quadrant. This complication would lead us to lose 1 phase of resolution per quadrant. The addition of two always-on single unit cells prevents the previously mentioned overlapping from appearing. Now, the output phase will never be equal to any of the input phases, as depicted and highlighted with blue in Fig. 8.

Figure 8. Edge phase overlapping illustration.



In the selected topology, we use 32 unit cells in every branch in order to achieve the 32-phases-per-quadrant resolution. Seeking for symmetry, the methodology consists in designing one unit-cell and replicate it in all the architecture stages. The cell design can be divided into three main parts: switches, current mirrors, and input transistors.

Figure 9. Designed PI.



For the first one, it was carried out a technology characterization similar to that proposed in chapter 10 of [12]. We made a sweep with different transistor widths (W), minimum length (L = 180nm) and a fixed drain-source current to accomplish an on-resistance approximation. As expected, the resistance decreases with a larger W value, however, in terms of area, the use of a very large W is not optimal. After this analysis, we selected W = 10µm, as this value generates an on-resistance of 67.2Ω. Thus, a good switching performance compensates its impact on the area.

The design next step consists in selecting values for the unit cell current sources and the output resistances. As this circuit could have a large amount of parallel-stacked unit cells connected to the output nodes, the parasitic capacitance could be considerably high (hundreds of fF for Fig. 9). With this in mind, the resistance and the polarization current values should be as small as possible. The first to avoid a high time constant $\tau = RC$ and the second for saving power consumption. In order to accomplish these conditions, the selected values were R = 700Ω and ∆I = 60μA for the current sources. These values also allow obtaining an output DC voltage level close to $\frac{V_{DD}}{2}$, which prevents the output signal from saturating in V_{DD} or GND values during small-signal operation. The above values yield a starting point to the rest of the design.

For the current mirrors there are three considerations to take into account: in this application, we use a basic current mirror to reduce area and circuit complexity; using a device length larger than minimum, reduces the negative consequences of channel-modulation effect over the current copy rate [12]; and keeping the mirror transistors in saturation region improves the current copy rate [12]. For the copy transistors to operate in this region, it is necessary that $\mathrm{V_{DS}} \geq \mathrm{V_{DS,sat}}$ (in short-channel devices, $\mathrm{V_{DS,sat}}$ is not equal to $\mathrm{V_{GS}} - \mathrm{V_{th}}$ but depends on it).

With the help of the simulator, it is possible to select such a diode-connected-transistor size (W/L = 2μm/360nm) that the $\mathrm{V_{GS}}$ (781 mV used) is slightly larger than $\mathrm{V_{th}}$ (typically close to 600mV for the technology node used). This strategy, along with a high $\mathrm{V_{DS}}$ value (depends on the last design part) will lead the copy transistor to enter saturation region easily.

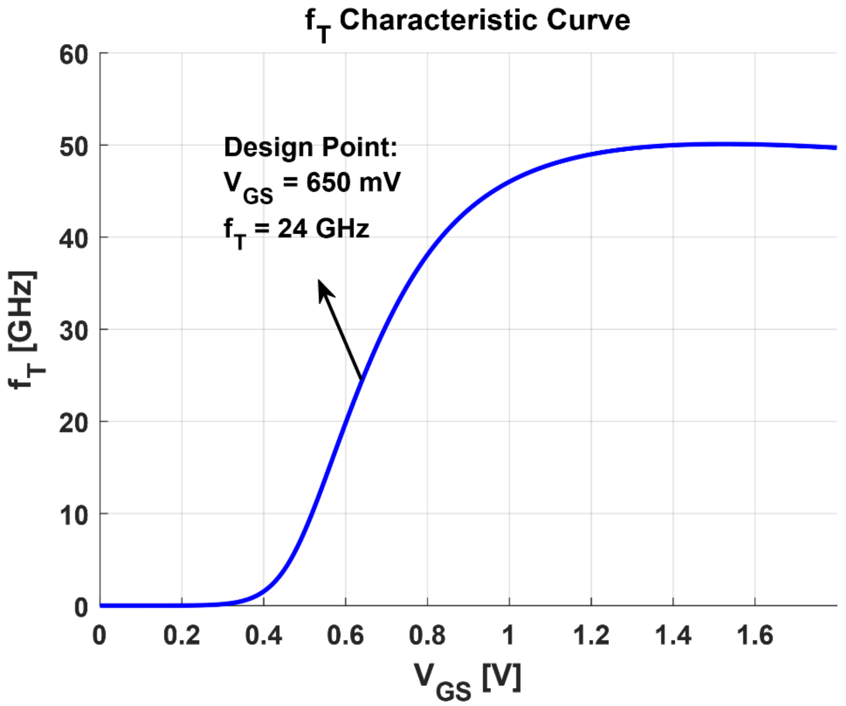
Regarding the last design part, Baker, in chapter 9 of [12], exposes the fT parameter for small-channel devices (L < 1μm), which refers to the transistor transition frequency from an amplifier to an attenuator:

$$\mathrm{f_T} \; \alpha \; \frac{\mathrm{V_{DS,sat}}}{L} \qquad (2)$$

Where $\mathrm{V_{DS,sat}}$ refers to the edge voltage between triode and saturation regions and L to the device length value. This relation allows concluding that, for a high-speed design, as is this case, the input transistors should have a small L (technology minimum) and a large $\mathrm{V_{DS,sat}}$; this latter means that the MOSFET enters the triode region earlier. However, in this particular circuit, maintaining the input transistors in this operating region becomes an issue. For the triode region, the transistor drain voltage must be small (close to the mirror copy transistor $\mathrm{V_{DS}}$, typically small for maintaining the input transistors on), which could imply two situations: a higher output resistance value or a higher unit cell polarization current. None of the above solutions is suitable, the first entails a larger area and a higher time constant in the output, reducing the circuit speed. The second could generate a very high power consumption as the number of unit cells in the circuit increases. Although these complications, simulator showed that this circuit also operates correctly when its input transistors are in the saturation region. With this in mind, it is important to know that the input signals (from a PLL), have a DC voltage component close to $\frac{V_{DD}}{2}$ (0.9V for this application), as these are rail-to-rail signals. Recalling the necessity of generating a high as possible $\mathrm{V_{DS}}$ voltage (the same source terminal voltage of the input transistor) for the copy devices in current mirrors, we must select an input transistor $\mathrm{V_{GS}}$ value greater than $\mathrm{V_{th}}$ and small enough to accomplish the mirror requirements. This transistor polarization point should also allow obtaining a high $\mathrm{f_T}$ parameter, since this is a high-speed design.

Fig. 10 marks the transistor polarization point selected for the design of this circuit. $\mathrm{V_{GS}}$ = 650mV allows obtaining an enough $\mathrm{V_{DS}}$ voltage (250mV) for the current mirror transistor to be operating in the saturation region. Despite the transistor $\mathrm{f_T}$ parameter value is not the highest possible, it is suitable for the device to operate at the required frequency, 1.25GHz.

Figure 10. f_T parameter characterization for the technology node transistors used.



Finally, the number of active unit cells define the input transistor V_{DS} voltage. This number will always be 33 because of the use of PC and its inverse, PCB, as the current mirrors control signals (when a bit of PC is in high level, the same bit in PCB is in low level). With this number, we are able to calculate the aforementioned V_{DS}voltage: $V_{DS} = V_{DD}$ (1.8V for this application) $-33 * \frac{\Delta I}{2} * R - V_{DS,mirror}$ (250mV) = 917mV. This value allows accomplishing the requirement of the input transistor to operate in the saturation region, which was discussed above.

In summary, the designed PI in Fig. 9 has a resolution of 32 bits per quadrant and can achieve phases in any of the four quadrants. The phase and quadrant are controlled by PC, PCB, QC, and QCB, respectively. PC and PCB are thermometer-type signals, which enable or disable the unit cells in the circuit by means of a switch.

B. CML-to-CMOS converter

With this circuit, we seek for the output signal to be CMOS-type through the following specifications for the output signal: rising and falling time less than 15% of the input signal period and duty cycle of 50% ± 2% of the input period. As well, for accomplishing CDR requirements, the operating frequency must be 1.25GHz.

The design of the chosen topology can be divided into three parts, the same highlighted in Fig. 11. The input amplifier is the most laborious section of this circuit, as it will be shown below. In order to obtain the strongest input DC level rejection, the capacitances value was set to 50fF, the smallest value that the 180nm technology node allows to build. Fig. 12 shows the amplifier frequency response, where a gain peak excels. Initially, the peak location was exactly in 1.25GHz (CDR operating frequency), needing a resistance value of 22kΩ. However, this value produced a very high $\tau = R*C$ and the circuit was not able to follow the input signal at the operating frequency. For this reason, we decided to lose some gain to achieve a higher speed, reducing the resistance value until 11kΩ. Furthermore, since this amplifier has a parasitic output capacitance, it was necessary to use five parallel-stacked inverters to reach a current value enough to charge this capacitor at the required speed.

Figure 11. Designed CML-to-CMOS.

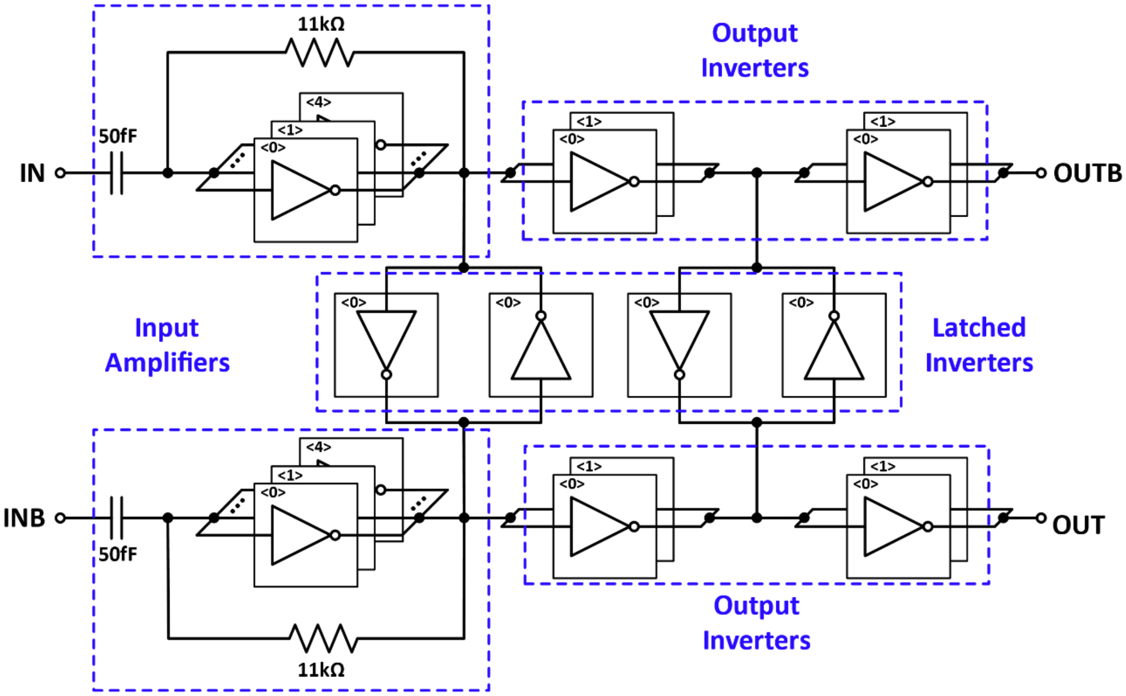
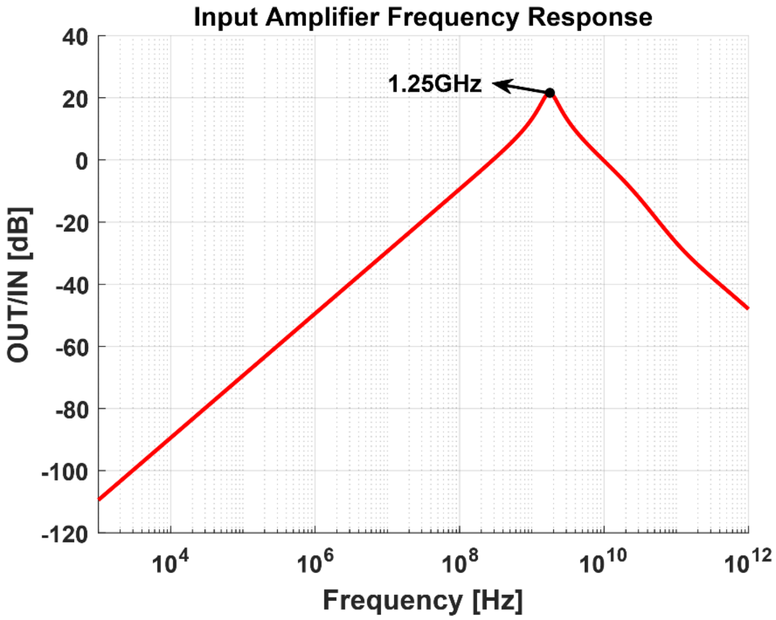


Figure 12. Frequency response of the CML-to-CMOS input amplifier.



Regarding the output and latched inverters, the simulator is a great help to observe the circuit behavior with a certain number of parallel-stacked inverter cells in these stages. Only one cell in latched inverters is able to maintain synchronized both the amplified signal and its inverse. On the other hand, the output inverters must be two parallel-stacked in order to make a correct driving to the circuit output load (as shown in section IV), which corresponds to a fan-out-four (FO4) inverter chain. The final design and all its features are depicted in Fig. 11.

3. RESULTS

Both circuits were implemented in a TSMC 0.18μm standard-logic CMOS technology. The nominal power supply is 1.8V, which corresponds to the digital supply of the used technology. PVT corners[1] validated the designed circuits, applying a maximum variation of +/- 10% for the supply voltage and -40°C to 125°C for temperature.

Fig. 13 shows the designed CML-to-CMOS layout. This image enables to appreciate that the use of the smallest capacitance value allowed by the 180nm technology node, as discussed in section III-B, is not only useful to perform a good DC input level filtering, but also for area optimization. In the layout process, we built symmetrical paths for the input signal and its inverse, which contributes to keep both signals synchronized. This layout covers an area of 1012 μm^2.

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[1] Corner simulations are reported using the following order: Process NMOS - Process PMOS - Process Capacitor/Resistor - Supply Voltage - Temperature; i.e., TTNNN indicates: Typical - Typical - Nominal - Nominal - Nominal.

Figure 13. Layout of the implemented CML-to-CMOS.

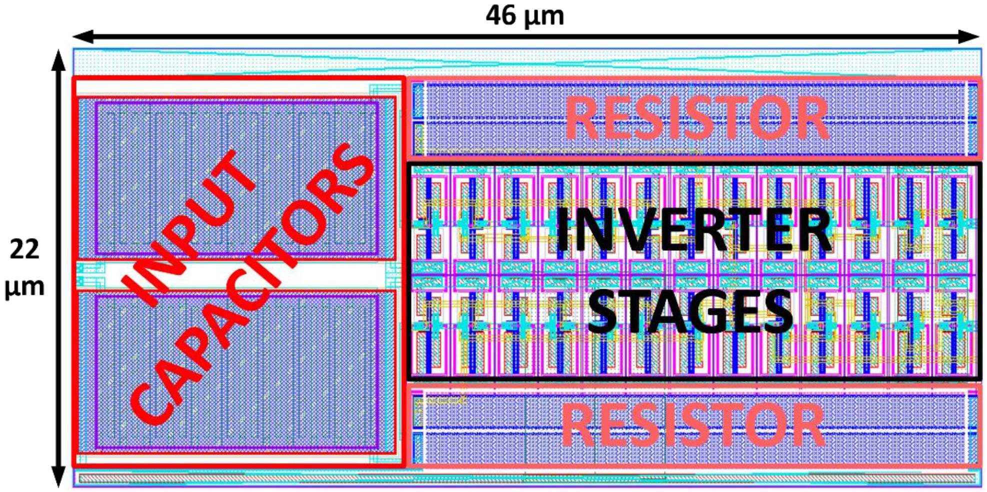


Fig. 14 depicts the input vs. output post-layout simulation for the CML-to-CMOS circuit, during about 4 input signal periods. This illustration allows observing a temporary behavior during the first period and a steady state from the second period onwards, which exposes a correct circuit functionality over PVT variations. The image also shows the four extreme corners: SSLLL, SSHHH, FFLLL, FFHHH, which usually disclose the most critical performance of circuits. The worst propagation delay case is 180.1ps, i.e., 22.5% of the input signal period, for SSHLH corner. The best case for this same variable is 22ps, i.e., 2.75% of the input signal period and appears in FFLHL corner, as expected. This corners analysis is useful to extract some additional data as follows: the rising time worst-case is 97.5ps and the falling time worst-case is 89.91ps; these values correspond to 12.1% and 11.2% of the input signal period, respectively. The duty cycle percentage worst cases can be also obtained, resulting in 48.42% and 51.19%. All these measurements allow verifying the accomplishment of the initial specifications.

Figure 14. Post-layout output waveforms of the designed CML-to-CMOS.

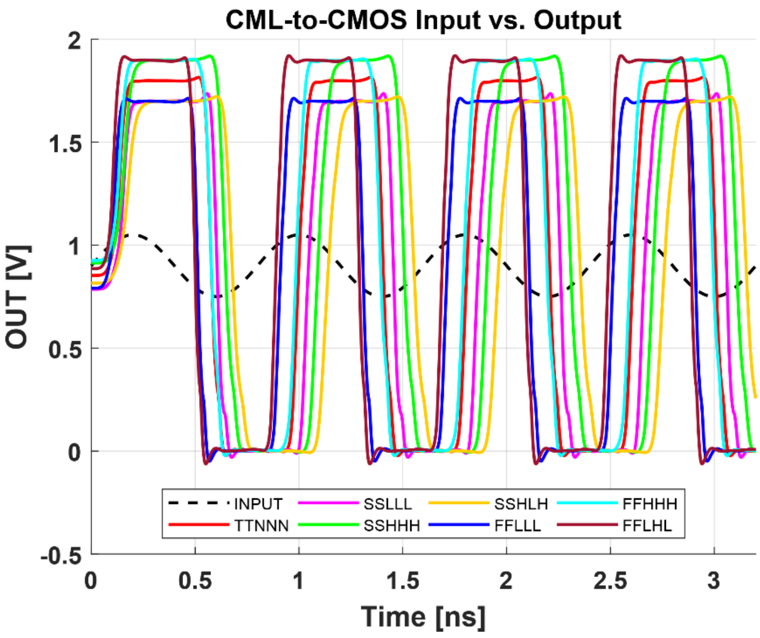


Fig. 15 presents the histogram of the designed CML-to-CMOS propagation delay time using Monte Carlo analysis. A mean value of about 80.4ps (10.1% of the input signal period) is obtained with a standard deviation less than 0.2% of the mean value. These calculations show that the circuit is very robust against random variations.

Figure 15. Propagation delay time histogram of the designed CML-to-CMOS, from Monte Carlo analysis.

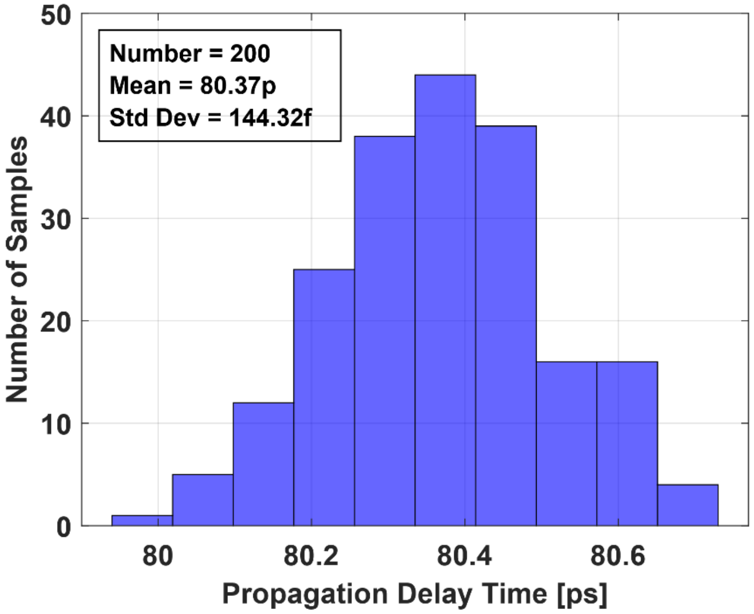
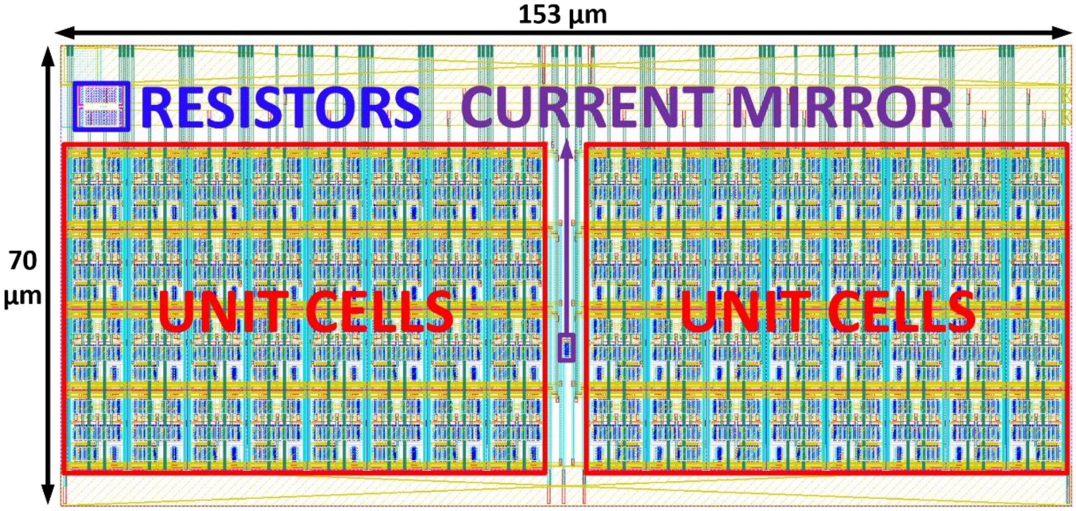


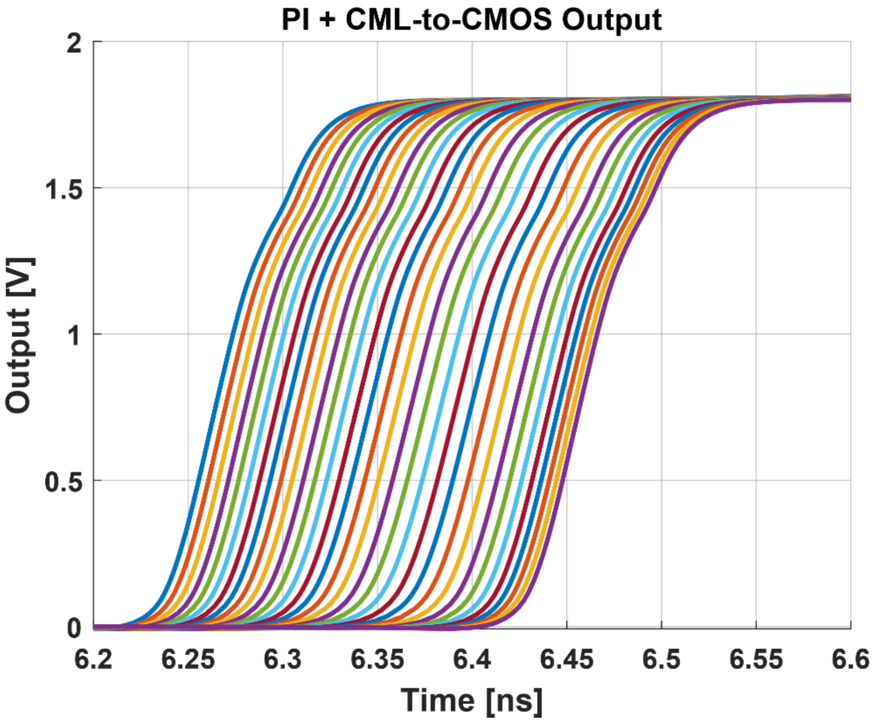
Fig. 16 depicts the PI layout. As this architecture is composed mainly of differential pairs, the symmetry plays a determining role in the correct circuit operation. Thus, the unit cells form two symmetrically-placed blocks and a central partition separates them. This partition allows distributing the input signal and its inverse in an equitable way for every unit cells block, further improving the circuit symmetry. Moreover, taking into account the high current consumption of this circuit, caused by a large number of parallel-stacked unit cells, it is very important to consider the necessary width of the paths for withstanding this current amount. The layout occupies a total area of 10710 μm^2.

Figure 16. Layout of the implemented PI.



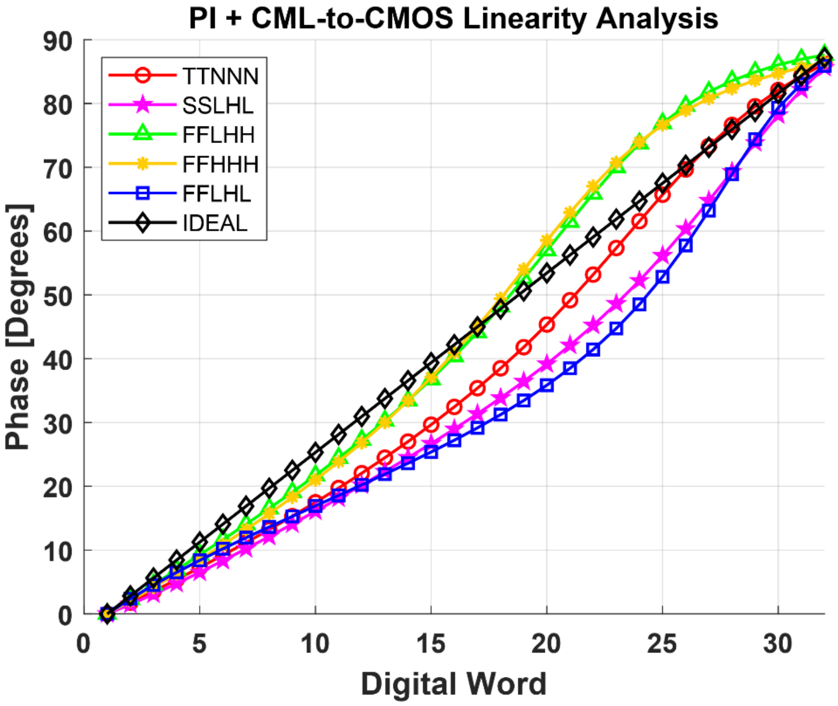
In Fig. 17, it is reported the typical case for the output voltage of the whole PI + CML-to-CMOS system all along one quadrant. Each one of the shown signals corresponds to a digital word, applied by PC and PCB signals. This code varies between 0 and 31, allowing a 32-phases-per-quadrant resolution. In the image, the time interval between the first and the last obtained phase is 193ps, which means a total phase shifting, with the 0-code signal as the reference, of roughly 87°. With these simulations it is also possible to measure the power consumption of every circuit: < 3.9mW for the PI and < 5.2mW for the CML-to-CMOS.

Figure 17. PI output after CML-to-CMOS stage, focused on rising transient, all along one quadrant.



Finally, it was performed an analysis in order to test the whole system (PI + CML-to-CMOS) linearity. Fig. 18 summarizes the two up and down worst-case results of this analysis across PVT variations, along with the typical and ideal case. The comparison of this latter case with the shown corners allows observing that the worst difference between trajectories takes place in FFLHL corner, as well as, that this difference corresponds roughly to 20°. Despite these nonlinearity issues, simulations show a behavior similar to the typical case in most of the corners, which makes this circuit appropriate for the present application.

Figure 18. Phase shifting linearity analysis.



4. SUMMARY

In this paper, a PI and CML-to-CMOS circuits for a CDR application are presented. A design methodology was proposed for each circuit, describing the path followed to obtain a functional system. A layout process, seeking area reduction, was performed. Simulation results over PVT and Monte Carlo variations for post-layout models reveal a correct performance for both circuits, within the industrial temperature range from -40◦C to 125◦C. The performance after coupling the two circuits was evaluated by a linearity analysis, making a comparison against the ideal behavior.

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ANNEX

Annex A. An All-Thin-Devices Level Shifter in Standard-Cell Format for Auto Place-and-Route Flow

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Abstract—This paper proposes a standard-cell format all-thin-devices level shifter suited for commercial digital-flow tools. Despite the fact that it is possible to find commercial level-shifter cells in standard-cell format, those cells require a mixed of thick- and thin-devices. The use of only thin-oxide transistors allows placing level shifters within thin-device based digital cells, optimizing area and place-and-route process. Due to the maximum voltage ratings of thin transistors, we adopted a switching technique to prevent high voltage differences between their terminals, avoiding a possible device breakdown. The proposed level shifter occupies an area of $156\mu m^2$ in a 0.18µm CMOS node.

I. INTRODUCTION

A current system-on-chip (SoC) typically uses multiple voltage domains to reduce power consumption and operate in different modes (e.g. sleep mode) [1]–[4]. In applications like internet-of-things (IoT), where power budget is limited, a SoC normally performs full processing during small time intervals and uses sleep mode in the remaining time to reduce consumption [5]. The power domain for blocks that can use this operating mode is isolated from the always-on domain as Fig. 1

exemplifies. Level shifters (LS) provide the interface among the power domains and ensure proper voltage levels for control signals.

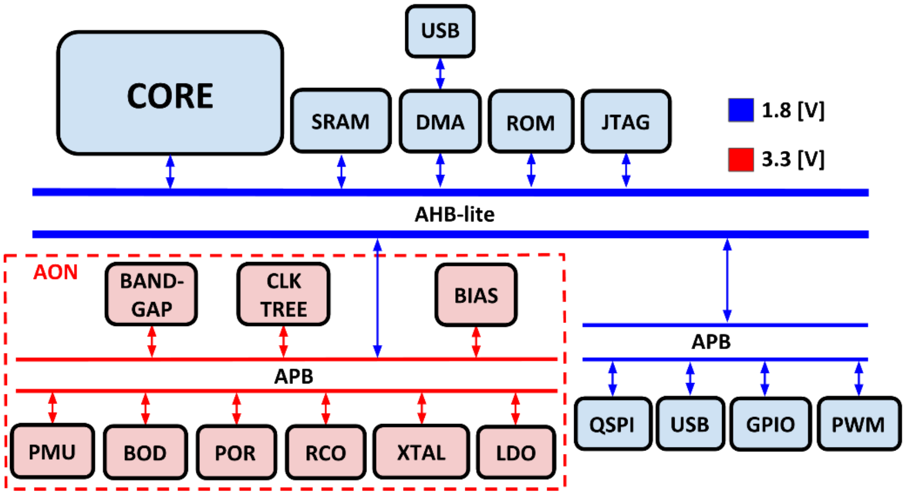

Fig. 1: Current system-on-chip typical architecture.

The digital domain (1.8V) shown in Fig.1 can be auto-placed by using a digital design flow. Synthesis and place-and-route tools optimize a full SoC placement and routing processes. The main constraint imposed by these tools is to have circuits in a standard-cell format, which enables an automatic placement. The issue of having non-standard-cell format is illustrated in the SoC of Fig. 2. Two main domains are communicated using LS in a non-standard-cell format, requiring to be hand-placed, spending a larger area in comparison with auto-placed standard-cells and implying additional manual work in the final sign-off of the chip.

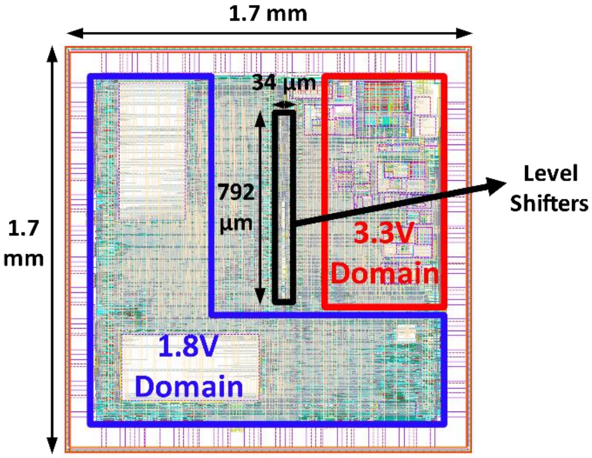

Fig. 2: Implementation of Fig. 1 scheme with two voltage domains coupled by non-standard-cell LS.

The design flow used in this work prefers only thin-oxide transistors in order to optimize area and routing. Thus, it is not well supported to use a typical LS with a multithickness approach as in Fig. 3 [6]. In this illustration, the thick transistors isolate high voltage nodes, avoiding a possible breakdown in the thin transistors. These thick devices cannot follow the grid specified for thin devices in a regular digital flow. Consequently, the layout does not follow a regular format.

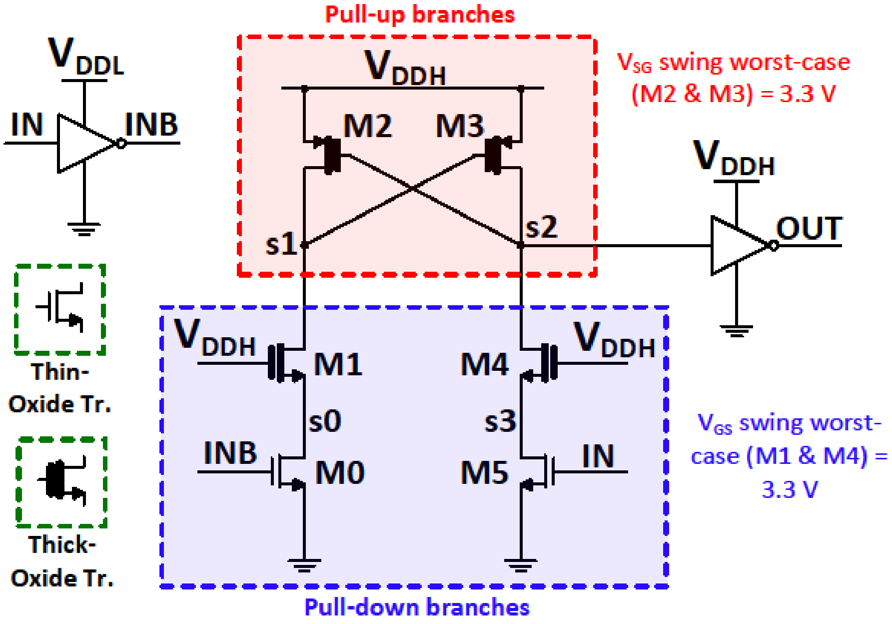

Fig. 3: Schematic of the classic LS.

Works with all-thin devices LS have been previously reported in [1], [7], where near-threshold supply voltage values are used. In [1], Lofti proposes an energy-efficient and wide-voltage-range LS, using only thin-oxide transistors. In that work, V_{DDL} and V_{DDH} values are 0.35V and 1.1V, respectively. This architecture is not an appropriate solution for the problem described in this section, in which V_{DDL} and V_{DDH} (1.8V to 3.3V) become larger and can cause problems with devices maximum voltage ratings.

We propose a novel LS architecture that enables its implementation in standard-cell format. The proposed LS can withstand larger power domain voltage differences using only thin-oxide devices with regular threshold-voltage.

II. PROPOSED ARCHITECTURE

Fig. 4 illustrates the proposed all-thin-devices LS, which enables to design the layout in a standard format. It is composed of two branches and two inverter stages. Both branches use a switching technique from [8], this reduces the high voltage stress and ensures thin transistors operate in a safe margin. The use of a current branch, based on [1], [7], [9] and highlighted in red, allows generating a current during every edge transition of the input signal. During a low-to-high one, the output branch copies the generated current to charge OUT node and produces the proper internal signals to cut off it and save power. In the opposite transition, this branch discharges OUT node using INB signal.

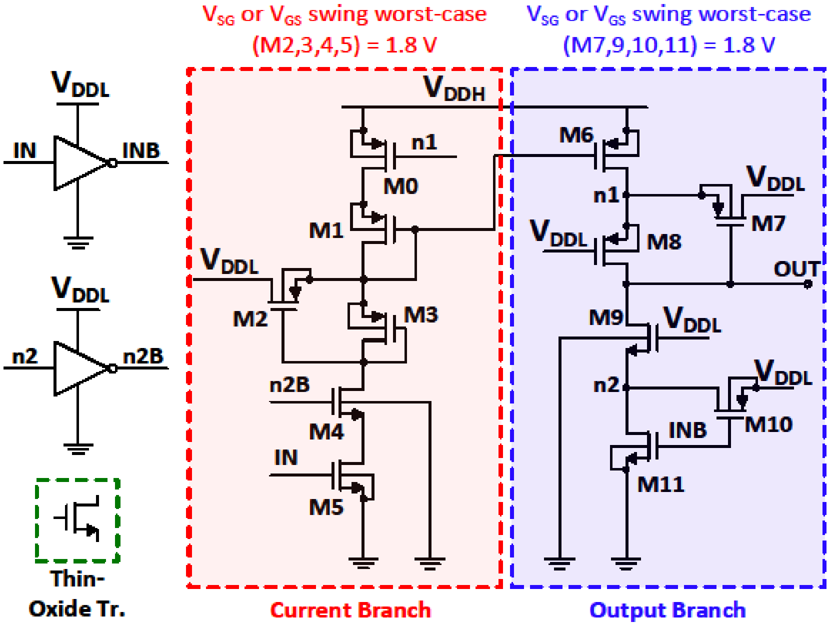

Fig. 4: Detailed schematic of the proposed LS.

The switching technique mentioned above is used with M7 and M10 transistors (Fig. 4), in the output branch. These devices charge and discharge n1 and n2 nodes to avoid high drain-to-source voltage differences in M6, M8, M9, and M11 transistors.

The M8 and M9 gates are connected to V_{DDL} rail for isolating n1 and n2 nodes from the large swing (0V to V_{DDH}) output node. In this branch, it is relevant to make an appropriate source terminal selection for M7 and M10 transistors in order to prevent forward biasing of their parasitic diodes. In addition, it is required to generate a voltage signal at the M6 gate terminal with 1) the same INB phase, 2) a swing that does not overcome the V_{SG} voltage limit. In view of these requirements, a current branch is expected, as depicted in Fig. 4.

To achieve the above conditions, the current branch uses IN as the main control signal, which allows to obtain the same INB phase at the M6 gate. This is important to prevent that the OUT node charge and discharge paths are activated at the same time, causing a short-circuit. For the second requirement, from a switched current source, this branch generates a voltage signal that roughly varies between V_{DDH} and V_{DDL}. This avoids a possible V_{SG} high voltage in M6. Also, it is important to make a good source terminal selection for M2 device due to the same reasons previously explained. For being able to cut off the current generation, M0 and M4 transistors are used as the current source shutdowns. These two switches are needed to isolate the M6 gate from V_{DDH} and GND when there is no current. Signals n1 and n2B control the gates of the switches, which ensures that the current source will only be active until OUT node achieves a stable state. M3 will act as a current limiter to control the current peak values in the source. Also, it will isolate the M6 gate from the M4 drain, since the latter can take a GND value and cause problems with V_{SG} voltage in M6. Finally, the M2 function is to keep a constant V_{DDL} voltage level in the M6 gate when the current source is powered down, during low-to-high transition. This will ensure a well-defined path for M6 polarization.

III. IMPLEMENTATION RESULTS

PVT corners[2] validated the proposed LS, applying a maximum variation of +/- 10% for both V_{DDL} and V_{DDH} and -40°C and 125°C for temperature. The input of the LS is a square-wave passed by a fan-out 4 (FO4) inverter chain and the output drives a FO4 inverter chain.

Figs. 5 and 6 show transient waveform for low-to-high and high-to-low transitions. V_{DDL} and V_{DDH} nominal values and input frequency were set to 1.8 V, 3.3 V and 1 MHz, respectively. The rising and falling output time characterization across corners, similar to that presented in [9], is shown in Fig. 5. For the worst case, the rise time is about 2.8ns and the fall time is 1ns, which corresponds to 0.28% and 0.1% of the input signal period, suggesting that the circuit can achieve a higher frequency operation. These results show that the worst case for rising and falling time coincides with the slow device corners. In this case, the devices lack driving capability to charge and discharge OUT node.

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[2] Corner simulations are reported using the following order: Process NMOS - Process PMOS - Supply Voltage - Temperature; i.e., TTNN indicates: Typical - Typical - Nominal - Nominal.

Fig. 5: Waveforms of the output voltage, focusing on rising and falling transients. Input rising and falling time = 0.1ns. WC = worst-case.

Transient response for the total current supplied by V_{DDH} across corners is presented in Fig. 6. Here, a current consumption measurement during the OUT node rising and falling edges is performed. The rising-edge peak is due to the current source and the mirror activation, in order to charge the OUT node all along the low-to-high transition. The falling-edge peak is generated because of the charging in the gate node for M6, which will turn off the current copy in the output branch. It can be appreciated that the time interval when there is a considerable current consumption is, roughly, 3.5 ns for both, low-to-high and high-to-low transitions, i.e., 0.35% of the input signal period. As expected, the worst current consumption corners are those with fast devices and higher supply voltage.

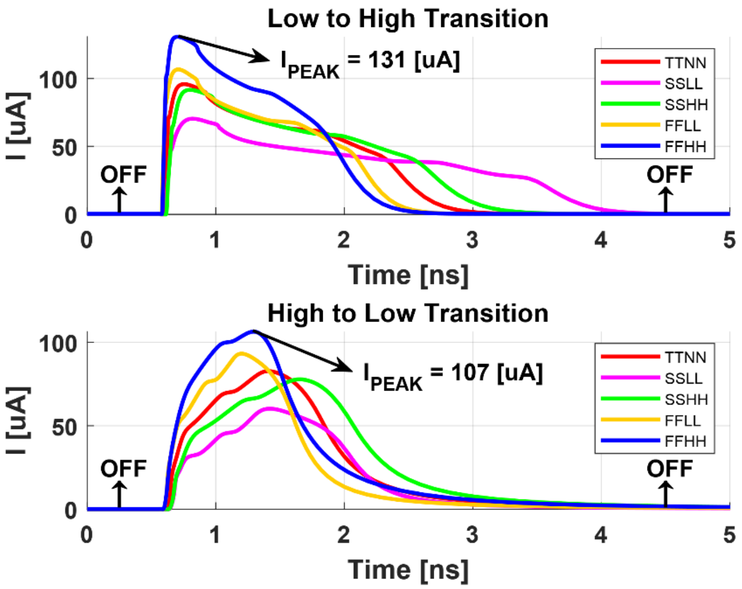

Fig. 6: Waveforms of current flowing in the circuit, focusing on rising and falling transients.

The proposed circuit was designed for working on V_{DDL} = 1.8V and V_{DDH} = 3.3V. Although that, we present a frequency characterization, also proposed in [4], [10]. To obtain the absolute maximum operating frequency, we made a sweep over V_{DDL} and V_{DDH} values and verified rail-to-rail functionality.

Fig. 7, presents a frequency analysis against V_{DDL} and V_{DDH} variations, keeping V_{DDH} - V_{DDL} relationship in a constant value. Under these conditions, a strong dependence between maximum operating frequency and V_{DDL} exists for V_{DDL} less than 1.4V, i.e. V_{DDH} less than 3.2V. This happens because the stacked transistors are operating near or in sub-threshold regimen, which makes them slower.

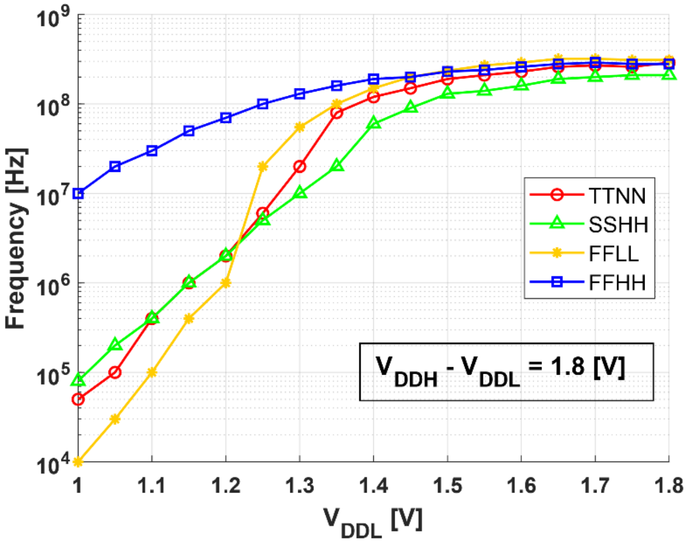

Fig. 7: Proposed LS maximum operation frequency for different V_{DDL} and V_{DDH} values.

Analyses for the maximum operating frequency varying V_{DDH} - V_{DDL} gap are depicted in Figs. 8 and 9. In the first case, V_{DDH} nominal value is constant and V_{DDL} nominal value is progressively decreasing to obtain a V_{DDH} - V_{DDL} sweep. In Fig. 9, on the contrary, V_{DDL} nominal value is constant and V_{DDH} varies. The image allows to detect a small difference in the maximum operating frequency, for both cases.

Fig. 8 shows the best and worst operating frequency cases, which correspond to, roughly, 300 MHz and 130MHz. In Fig. 9, a weak maximum operating frequency dependence on V_{DDH} - V_{DDL} is observed in four corners. Although this, for the SSLL corner, the figure allows appreciating that the maximum frequency, falls approximately one decade from 1.4V to 1.1V.

Fig. 8: Proposed LS maximum operation frequency for different V_{DDH} - V_{DDL} values, with a constant V_{DDH} value.

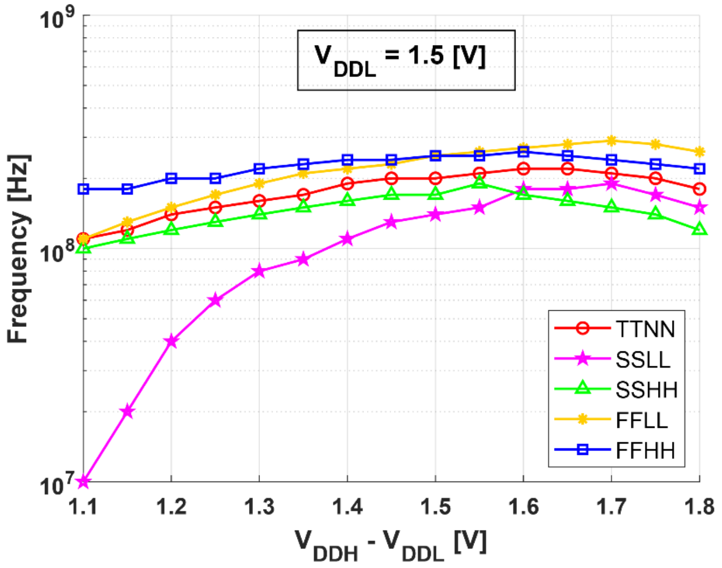

Fig. 9: Proposed LS maximum operation frequency for different V_{DDH} - V_{DDL} values, with a constant V_{DDL} value.

Energy and Delay analyses, were also performed and the results are summarized in Figs. 10 and 11 respectively. Fig. 10 shows the results for Energy-per-Transition

(EPT). For each corner, EPT exhibits low dependence on V_{DDH} - V_{DDL}, since the variability does not exceed 10% over all the gap, excepting the SSLL corner in which the variability reaches up to 18%. Worst case across all corners was 500fJ.

Fig. 10: Proposed LS low-to-high energy-per-transition for different V_{DDH} - V_{DDL} values, with a constant V_{DDL} value.

Fig. 11 shows the histogram of the proposed LS propagation delay time using Monte Carlo analysis. A mean value of about 1.2ns is obtained with a standard deviation less than 5% of the mean value, making this circuit robust against random variations.

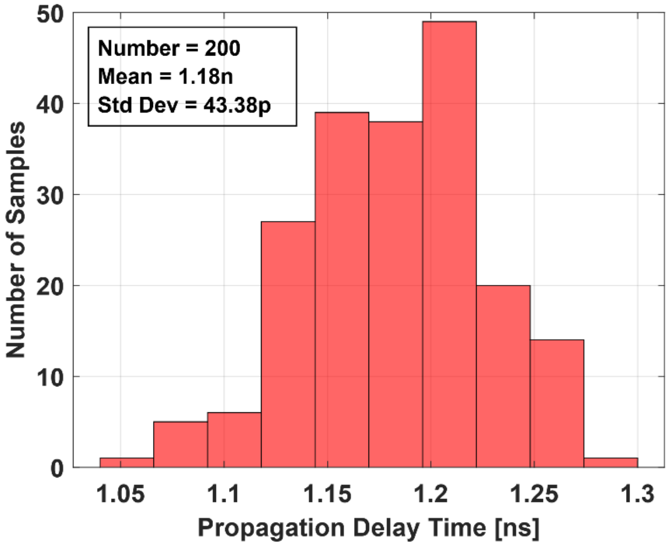

Fig. 11: Proposed LS propagation delay histogram from Monte Carlo variations.

Finally, Fig. 12 depicts the proposed LS layout in a standard-cell format. It is necessary to use 5 isolated N-wells because some of the PMOS devices have their bulks connected to different nodes. Searching for area reduction, the dimensions of the transistors used in this design are not larger than 500 nm. As result, the LS occupies an area of 156 μm^2.

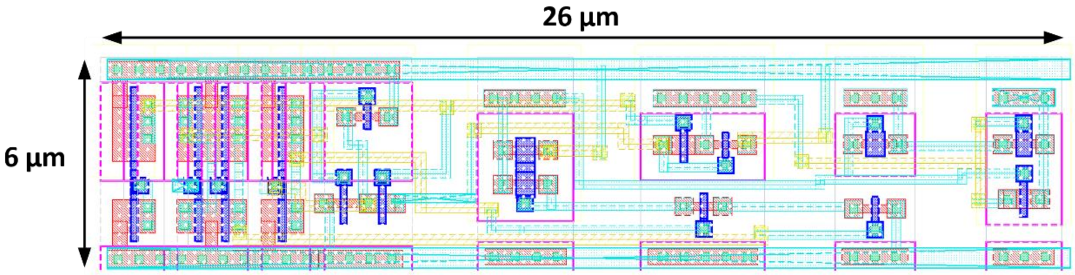

Fig. 12: Proposed LS layout view.

IV. CONCLUSIONS

In this paper, a level shifter has been presented, using a novel implementation with all-thin devices. This allows integrating the level shifter in a traditional digital design flow, without incurring in voltage rating violations. Maximum operating frequency and energy-per-transition with different supply voltage values were measured and analyzed. Finally, a layout process focused on digital-standard-cell requirements was implemented.

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