IMPLEMENTATION OF A DIGITAL LOW DROP-OUT REGULATOR WITH A SELF-GENERATED CLOCK IN A CMOS TECHNOLOGY

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Trabajo de Grado para optar al título de
Ingeniero Electrónico

Director
Elkim Felipe Roa Fuentes,
Philosophy Doctor.

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RESUMEN

TÍTULO: IMPLEMENTACIÓN DE UN REGULADOR DIGITAL DE BAJA CAIDA CON UN RELOJ AUTOGENERADO EN TECNOLOGÍA CMOS [*]

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PALABRAS CLAVE: BÚFER TRI ESTADOS, COMPARADOR, BAJA CAIDA, TECNOLOGÍA CMOS.

DESCRIPCIÓN:

Actualmente, en la mayoría de los sistemas en chip (SoC), se utilizan reguladores analógicos de baja caída (A-LDO) para suministrar los diferentes dominios de voltaje en el sistema. El problema con las aplicaciones de baja potencia es que (A-LDO) tienen una eficiencia reducida cuando la tensión de alimentación es baja. Una opción alternativa son los reguladores digitales de baja caída (D-LDO) debido a su bajo voltaje de funcionamiento, pero estos reguladores presentan un problema común debido a la respuesta lenta a eventos transitorios como caídas/subidas de tensión de alimentación. Una de las soluciones a este problema es aumentar la frecuencia de funcionamiento del D-LDO, lo que aumenta la velocidad de respuesta pero también aumenta el consumo de energía. El D-LDO con reloj autogenerado, es una solución que ataca este problema directamente, proporcionando un reloj de alta frecuencia solo cuando hay un evento de caída o aumento de voltaje de salida, pero en un estado estable , funciona con el reloj de frecuencia más baja externo al regulador. En este trabajo, proponemos implementar el DLDO del trabajo previo pero haciendo ajustes al diseño original, para que sea completamente sintetizable usando un área pequeña en un SoC. El diseño previo existente del trabajo previo, no cumplía con algunos aspectos que no permitían que se sintetizara completamente, este problema se aborda en este trabajo, ajustando los diseños de algunas celdas de la (D-LDO) mencionada, a un formato de celda estándar. Los resultados muestran una mejora en la respuesta a eventos transitorios utilizando un sistema sintetizable, en comparación con otras soluciones propuestas que utilizan un reloj permanente de alta frecuencia. El voltaje de salida cae 221.1mV con un paso de corriente de carga de 400ns de 1mA a 20mA (@ LOAD = 10pF).

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[*] Trabajo de grado

[**] Facultad de Ingenierías Físico-Mecánicas. Escuela de Ingenierías Eléctrica, Electrónica y Telecomunicaciones. Director: Elkim Felipe Roa Fuentes, Philosophy Doctor.

ABSTRACT

TITLE: IMPLEMENTATION OF A DIGITAL LOW DROP-OUT REGULATOR WITH A SELF-GENERATED CLOCK IN A CMOS TECHNOLOGY [*]

AUTHOR: JOAN MANUEL FLOREZ BONZA [**]

KEYWORDS: TRI-STATE BUFFER, COMPARATOR, LOW DROP-OUT, CMOS TECHNOLOGY

DESCRIPTION:

Currently, in most systems on chip (SoC), analog low-dropout (A-LDO) regulators are used to supply the different voltage domains in the system. The problem with low power applications is that (A-LDO) have reduced efficiency when the supply voltage is low. An alternative option are digital low dropout (D-LDO) regulators because of their low operating voltage, but these regulators present a common problem due to slow response to transient events such as supply voltage dips/surges. One of the solutions to this problem is to increase the operating frequency of the D-LDO, which increases the response speed but also increases the power consumption. The D-LDO with previous work self-generated clock, is a solution that attacks this problem directly, providing a high-frequency clock only when there is an event of drop or increase of output voltage, but in a steady-state, it works with the lower frequency clock external to the regulator. In this work, we propose to implement the DLDO of previous work but making adjustments to the original design, so that it is fully synthesizable using a small area in an SoC. The existing previous design of previous work, did not comply with some aspects that did not allow it to be fully synthesized, this problem is addressed in this work, adjusting the designs of some cells of the (D-LDO) mentioned, to a format of a standard cell. The results show an improvement in the response to transient events using a synthesizable system, compared to other proposed solutions that use a permanent high-frequency clock. The output voltage drops 221.1mV with a 400ns load current step from 1mA to 20mA (@ LOAD = 10pF).

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[*] Bachelor Thesis

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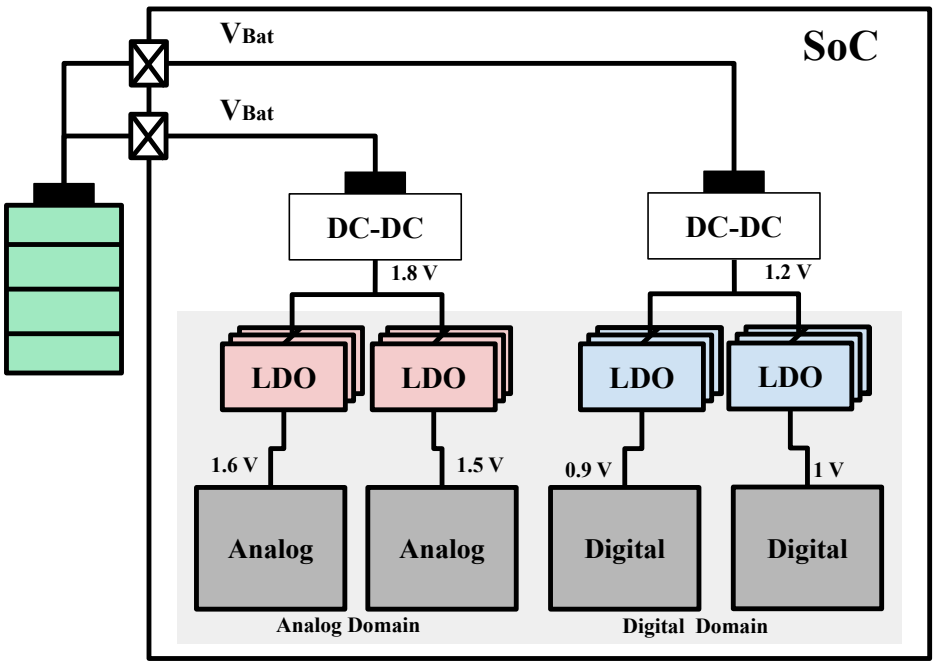
INTRODUCTION

Within a system-on-chip (SoC) there are different voltage domains, that is, there are several groups of circuits that each receive a different supply voltage as can be seen in Figure 1. This distribution allows you to disable parts of the system that are not necessary during a certain mode of operation, thus reducing power consumption. For certain applications it it is ideal for each circuit to correspond to a different voltage domain, so only those circuits that are necessary during a certain mode of operation would be used.

Analog low drop-out regulators (A-LDO), like the one depicted in Figure2(a), are currently used in most SoCs to supply the different voltage domains in the system. These regulators, having few components, occupy a little area, and they have a quick response to transient events because they are analog and the samples of the output signal is continuous. These pioneering A-LDOs exhibit a rapid transient response with low-level quiescent current (IQ)M. AKRAM, HONG W. y HWANG I. "Capacitorless Self-Clocked All-Digital Low-Dropout Regulator". En: *IEEE Journal of Solid-State Circuits* 54.1 (2019), págs. 266-276. DOI: 10.1109/JSSC.2018.2871039, high PSR, and high bandwidth Y. LU, KI W. y YUE C. P. "17.11 A 0.65ns-response-time 3.01ps FOM fully-integrated low-dropout regulator with full-spectrum power-supply-rejection for wideband communication systems". En: *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*. 2014, págs. 306-307. DOI: 10.1109/ISSCC.2014.6757446-Y.-S. YUK y col. "PSR Enhancement Through Super Gain Boosting and Differential Feed-Forward Noise Cancellation in a 65-nm CMOS LDO Regulator". En: *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 22.10 (2014), págs. 2181-2191. DOI: 10.1109/TVLSI.2013.2287282. Also, in some cases, no decoupling output capacitor J. GUO y LEUNG K. N. *A 6-μW Chip-Area-Efficient Output-Capacitorless LDO in 90-nm CMOS Technology*. in

IEEE Journal of Solid-State Circuits, vol. 45, no. 9, pp. 1896-1905, Sept. 2010, doi: 10.1109/JSSC.2010.2053859.-J. ZARATE ROLDAN y col. “A Capacitor-Less LDO With High-Frequency PSR Suitable for a Wide Range of On-Chip Capacitive Loads”. En: *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 24.9 (2016), págs. 2970-2982. DOI: 10.1109/TVLSI.2016.2527681 is required. Although conventional A-LDOs meet the requirements for voltage conversion for multiple voltage domains in an SoC, as in Figure 1, their performance decreases when the supply voltage is reduced. These regulators have the following drawbacks:

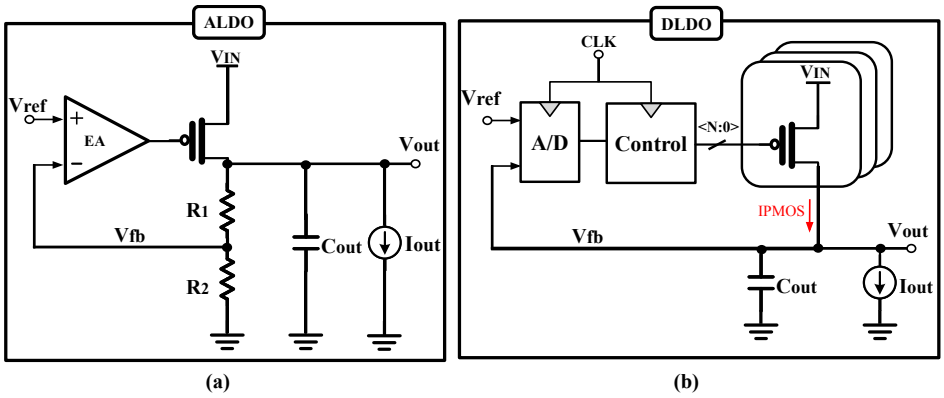
Figure 1. Block Diagram of the SoC Power Supply Network.



1. The performance of the regulator degrades when low input voltages are required, as it is difficult to achieve a high gain-bandwidth product in the error amplifier KUNDU y col. “A Fully Integrated Digital LDO With Built-In Adaptive Sampling and Active Voltage Positioning Using a Beat-Frequency Quantizer”. En: *IEEE Journal of Solid-State Circuits* 54.1 (2019), págs. 109-120. DOI: 10.1109/JSSC.2018.2870558.

2. The design of the error amplifier and the pass device is difficult to scale in terms of technology and specifications, for this reason, it can take several weeks To implemented this regulator in different technologies.

Figure 2. (a) Schematic of A-LDO. (b) Block Diagram of D-LDO.



There are some alternative options to solve these problems. One is to use digital low-dropout regulators (D-LDO) x. MA y col. “A 0.4V 430nA quiescent current NMOS digital LDO with NAND-based analog-assisted loop in 28nm CMOS”. En: *2018 IEEE International Solid - State Circuits Conference - (ISSCC)*. 2018, págs. 306-308. DOI: 10.1109/ISSCC.2018.8310306, like the one in Figure 2 (b). Digital LDOs have some advantages over their analog counterparts. The first, due to its ability to perform well at low operating voltages. A second, the ease with which these regulators can be scaled between technology nodes and specifications, that is, if they have the specifications that the regulator must meet, the circuit design can be obtained by performing some configurations. Both of these advantages come from the fact that analog circuits are now being replaced by digital cells, although, in the literature, there is not a single work with a true fully digital LDO implementation KUNDU y col., “A Fully Integrated Digital LDO With Built-In Adaptive Sampling and Active Voltage Positioning Using a Beat-Frequency Quantizer”. Even with these advantages, DLDOs are not without their drawbacks. DLDOs are conventionally slow or power-hungry

MA y col., “A 0.4V 430nA quiescent current NMOS digital LDO with NAND-based analog-assisted loop in 28nm CMOS”. A common problem with D-LDOs is the slow response to transient events, such as sudden changes in charging voltage. One of the solutions to this problem is to increase the operating frequency of D-LDO, which increases the speed of response to transient events but also increases power consumption.

For this problem, in G. ROMERO, RUEDA Luis E. y ROA Elkim. *A Digital Low-Dropout Regulator for Low-Supply Voltage Operation*. Universidad Industrial de Santander, 2019. they propose to use D-LDO with a self-generated clock, which only works with a high-frequency clock when the output voltage is outside the limits of the reference voltage, but when the regulator has stable output, it works with an external low-frequency clock. In this work, we propose to make the pertinent changes to the design that make it synthesizable for 180nm CMOS technology. As the purpose of this project is to improve the existing design of the D-LDO of Figure 2.1 of ROMERO, E. y Elkim, *A Digital Low-Dropout Regulator for Low-Supply Voltage Operation*, complying with the remaining requirements for its manufacture, the cells that compose it must be standard cells of the same library throughout the circuit.

In the previous work, ROMERO, E. y Elkim, *A Digital Low-Dropout Regulator for Low-Supply Voltage Operation* done in the OnChip research group, it was possible to arrive at a non-synthesizable solution, we propose the redesign of the cells that are not synthesizable and the generation of a Layout to make post-layout simulations and have a manufacturable design. In chapter II we explain the DLDO of ROMERO, E. y Elkim, *A Digital Low-Dropout Regulator for Low-Supply Voltage Operation*, how it works, and the cells that compose it. In chapter III the designs of the standard cells created are developed, the results obtained with the final design of the DLDO are described in chapter IV, and the conclusion in chapter V.

1. OBJECTIVES

1.1. GENERAL OBJECTIVES

- To implement a digital low drop-out (DLDO) regulator with a self-generated clock.

1.2. SPECIFIC OBJECTIVES

- To describe the behavior of the D-LDO digital circuit of previous work, using hardware description languages.
- To design and implement standard cells for the comparator and tri-state buffers.
- To implement the layout of the DLDO using the standard cells from the previous objective, and to perform post- layout simulations with extract parasites.

2. D-LDO WITH SELF-GENERATED CLOCK

The architecture proposed in ROMERO, E. y Elkim, *A Digital Low-Dropout Regulator for Low-Supply Voltage Operation*, has two feedback loops, one is the same loop of a conventional D-LDO in Figure 2 (b), which samples the output with an ADC, and then takes actions in cases of under-overshoot. The ADC is made up of 3 comparators, the first is the synchronous comparator based on NAND gates of Figure 2.2 in section A, this comparator samples the output every time the CLKp signal is on its rising edge, and it has two signals output, VCompF and Valid. The Valid signal indicates to the D-LDO Conter block that the VCompF output is ready to be sampled and VCompF is the signal that indicates whether Vout is equal to or different from Vref, in short, the COMPF comparator is responsible for the comparison between Vout and VREF. The TICH and TICL comparators are the threshold inverter comparators of the Figure 2.3 in section B, these are in charge of indicating when the Vout signal crosses the reference limits VREFH and VREFL, that is, when an overshoot or undershoot event. The VCompH and VCompL signals enable the FLIP-FLOP, which adds the G_inextF and G_inextR gains, which add to the D-LDO Counter count. This count tells how many pass-through devices are activated. The G_pre signal is an 8-bit signal that represents the count of the number of activated pass devices, which in this case are the Tri-State Buffer in Figure 2.4, section C, this signal is stored to reduce the delay of propagation between G pre and G <7: 0>, in this way metastability problems are avoided. Besides, the VCompH and VCompL signals activate the second feedback loop, which is the self-generated clock system, this system is in charge of generating a high-frequency clock signal and making the change from the external clock to the generated clock, in situations Undershoot and overshoot. As soon as the Vout signal stabilizes, the self-generated clock loop changes the clock, and the circuit returns to low power mode.

Figure 2.1. Proposed D-LDO Architecture in previous work.

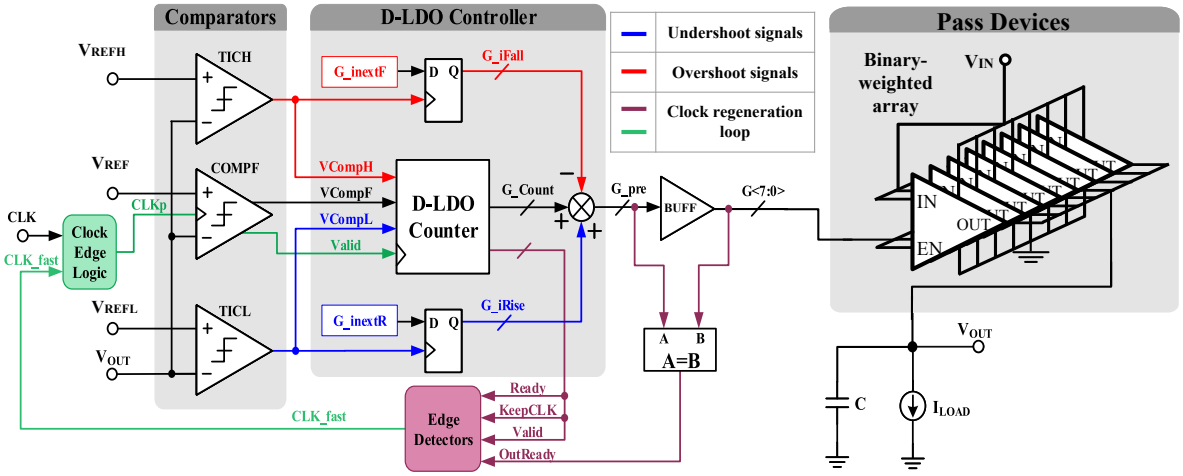
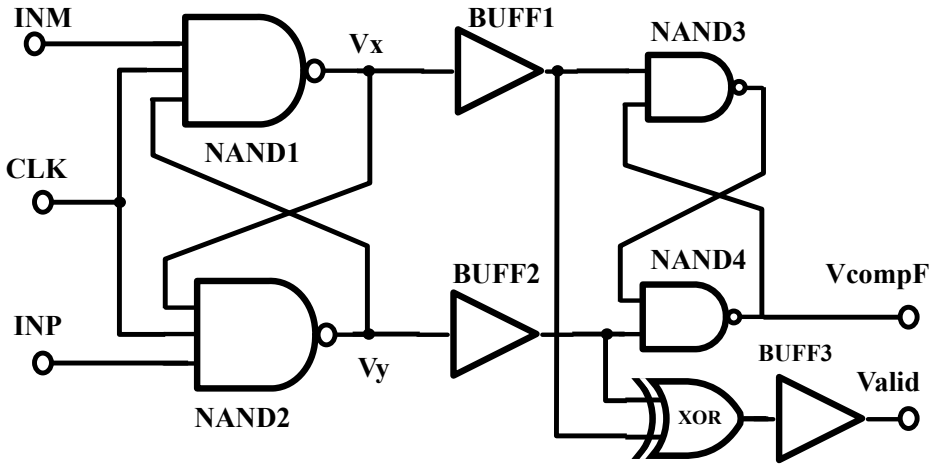


Figure 2.2. NAND-Based Clocked Comparator.

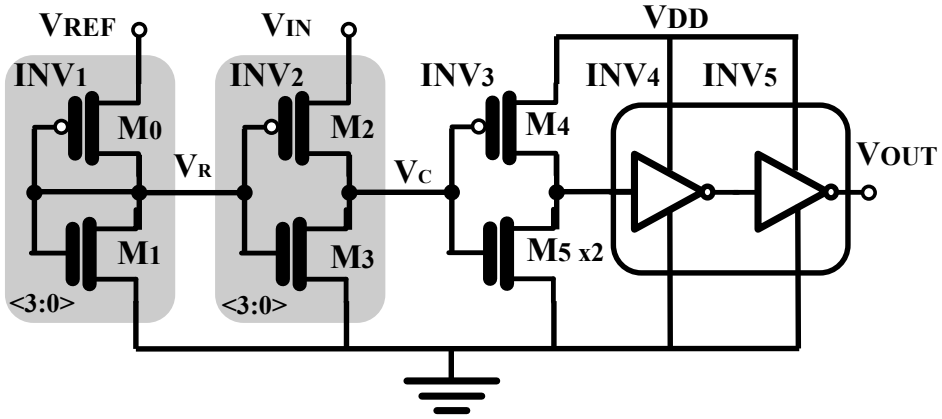


2.0.1. NAND-BASED CLOCKED COMPARATOR This work implements the idea of ROMERO, E. y Elkim, *A Digital Low-Dropout Regulator for Low-Supply Voltage Operation*, to adopt the NAND-based timed comparator of Figure 2.2, proposed by Weaver et al. S. WEAVER, HERSHBERG B. y MOON U. “Digitally Synthesized Stochastic Flash ADC Using Only Standard Digital Cells”. En: *IEEE Transactions on Circuits and Systems I: Regular Papers* 61.1 (2014), págs. 84-91. DOI: 10.1109/TCSI.2013.2268571, which was slightly modified by including an XOR gate for ge-

nerating a valid signal that indicates when the comparator's output is ready to be sampled. In the NAND-based clock comparator, when the CLK is low, the voltage at the Vx and Vy nodes is set to VDD. Here, Valid is low, and Vcomp keeps its previous state. Once CLK goes high, INP and INM start to unload nodes Vx and VY. These are also inputs to the 3-input NAND gates and thus bring Vx and Vy to their final states. For example, if INP is greater than INM, and CLK is high, Vy discharges faster than Vx, then Vy crosses the NAND1 threshold and sets Vx high; while Vy keeps dropping to GND. So VCompF is high and, seconds later (the BUFF3 delay), Valid is high.ROMERO, E. y Elkim, *A Digital Low-Dropout Regulator for Low-Supply Voltage Operation*.

2.0.2. THRESHOLD INVERTER COMPARATOR Several latest generation D-LDOs only use dynamic comparators as A/D converters Xiaofei Ma y col. "A 0.4V 430nA quiescent current NMOS digital LDO with NAND-based analog-assisted loop in 28nm CMOS". En: *2018 IEEE International Solid - State Circuits Conference - (ISSCC)*. 2018, págs. 306-308. DOI: 10.1109/ISSCC.2018.8310306. This is due to the potential static consumption potential of continuous comparators.ROMERO, E. y Elkim, *A Digital Low-Dropout Regulator for Low-Supply Voltage Operation* propose an improved model of the [open] logic-threshold triggered comparator (LTTC), called the threshold inverter (TIC) of Figure.2.3. The difference is that the (LTTC) of AJRAM M., HONG W. y HWANG I. "Fast Transient Fully Standard-Cell-Based All Digital Low-Dropout Regulator With 99.97 % Current Efficiency". En: *IEEE Transactions on Power Electronics* 33.9 (2018), págs. 8011-8019. DOI: 10.1109/TPEL.2017.2771942, works badly when one of the inputs is low and in the (TIC) of ROMERO, E. y Elkim, *A Digital Low-Dropout Regulator for Low-Supply Voltage Operation*, when the chassis number is low, the VOUT is inherently set to a high level, thus overcoming the startup problem ROMERO, E. y Elkim, *A Digital Low-Dropout Regulator for Low-Supply Voltage Operation*.

Figure 2.3. Threshold Inverter Comparator Schematic.

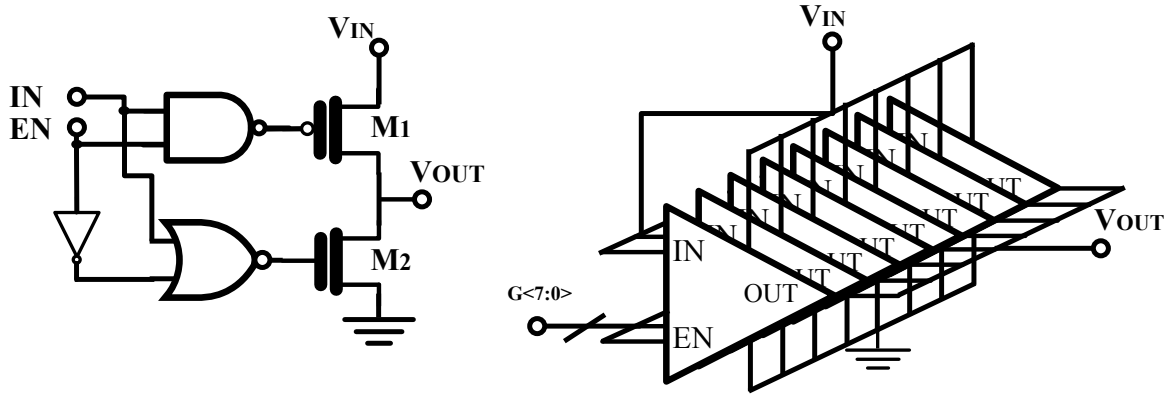


Another advantage of this design, which is based mainly on inverters, is that it allows the possibility of a synthesizable comparator. However, the (TIC) of ROMERO, E. y Elkim, *A Digital Low-Dropout Regulator for Low-Supply Voltage Operation* does not meet the conditions of a standard cell, both the dimensions of the transistors and their layout are typical of an analog block.

2.0.3. TRI-STATE BUFFER AS PASS DEVICES The pass-through devices are those that are responsible for creating a bridge between Vin and the load, those that are connected in parallel, usually in traditional D-LDOs such as M., W. e I., “Fast Transient Fully Standard-Cell-Based All Digital Low-Dropout Regulator With 99.97 % Current Efficiency” or KUNDU y col., “A Fully Integrated Digital LDO With Built-In Adaptive Sampling and Active Voltage Positioning Using a Beat-Frequency Quantizer”, use PMOS transistors NMOS. The downside to this is that it automatically makes the layout non-synthesizable. In ROMERO, E. y Elkim, *A Digital Low-Dropout Regulator for Low-Supply Voltage Operation*, they propose the use of the tri-state buffer of the Figure 2.4 (a), as a pas device, the main reason is that being a standard cell, it allows the design to be fully synthesizable, but also having 3 states, it is possible to keep the buffer off without the NMOS transistor consuming current from the

output, which is what would happen if inverters were used as pass-through devices. This is possible since in the situation where the EN input is low, the buffer output will be high impedance (hi-Z), regardless of the following of the IN value, but if the EN input is high, the state of the output depends on the state of the IN input, so in addition to using the Buffers as devices that increase the load current only by turning on the PMOS transistors and when you want to reduce it, only the PMOS are turned off, you can also control this current turning on the NMOS that decreases the current if necessary. These 3 states could increase the versatility of the circuit. In ROMERO, E. y Elkim, *A Digital Low-Dropout Regulator for Low-Supply Voltage Operation*, this option of turning on the M2 transistor was not contemplated and the IN input was connected directly to VIN, Figure 2.4 (b), which makes the BUFFERs controlled by the EN input which is connected to $G < 7 : 0 >$ and the output will have two states, high and hi-Z.

Figure 2.4. (a) Schematic of Tri-State Buffer. (b) Symbol of Tri-State Buffer.

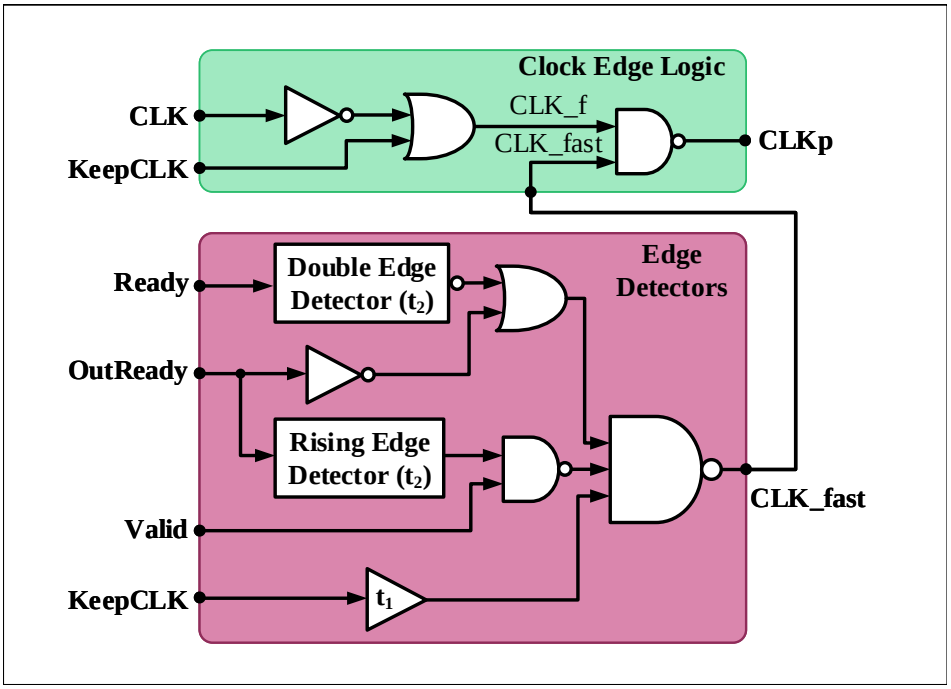


(a) (b)

2.0.4. CLOCK REGENERATION LOOP This section explains in detail the ROMERO, E. y Elkim, *A Digital Low-Dropout Regulator for Low-Supply Voltage Operation* autogenerated clock block, with the help of a timing diagram in Figure 2.5 that

shows the behavior of the circuit in an undershoot case. The generated layout is also observed. Edge Detectors and Clock Edge Logic:

Figure 2.5. Circuit diagram of Clock Edge Logic and Edge Detectors for Clock Regeneration.



The self-generated clock is the result of a feedback loop that creates failures in the input of the NAND-based comparator ROMERO, E. y Elkim, *A Digital Low-Dropout Regulator for Low-Supply Voltage Operation*. The equivalent circuit that can be seen in the Figure 2.5, is the self-generated clock, this is composed of two blocks, (Clock Edge Logic) that is in charge of changing the external clock, to the high-frequency clock and (Edge Detector) which is responsible for generating the glitches of the high-frequency clock.

The (Clock Edge Logic) block has two input signals, CLK which is the signal of the external low-frequency clock, and KeepCLK which is the signal in charge of enabling the high-frequency clock, since if it is a 0, the signal CLK_fast, will always be 1 and the CLK_f signal, it will commute for the external clock and in the opposite case,

CLK_f will always be 1 and the CLKp output only depends on the CLK_fast signal. The KeepCLK signal is high when VCompL or VCompH changes and resets when the controller enters a stable state.

The (Edge Detector) block creates glitches from the comparison of Ready and OutReady signals, the glitch is generated when one of these two signals settles and its duration is t2. Now, while VCompL or VCompH, KeepCLK is kept low and the moment Vout passes the limit of VREFH or VREFL, t seconds are counted later, KeepCLK enables the high-frequency clock and stays like that until the system reaches its stable state. The layout of this circuit is seen in the Figure 4.1, which includes standard cells pre-designed in 180nm CMOS technology, the area of the block is $757.068um^2$.

3. DESIGN AND IMPLEMENTATION USING STD CELLS

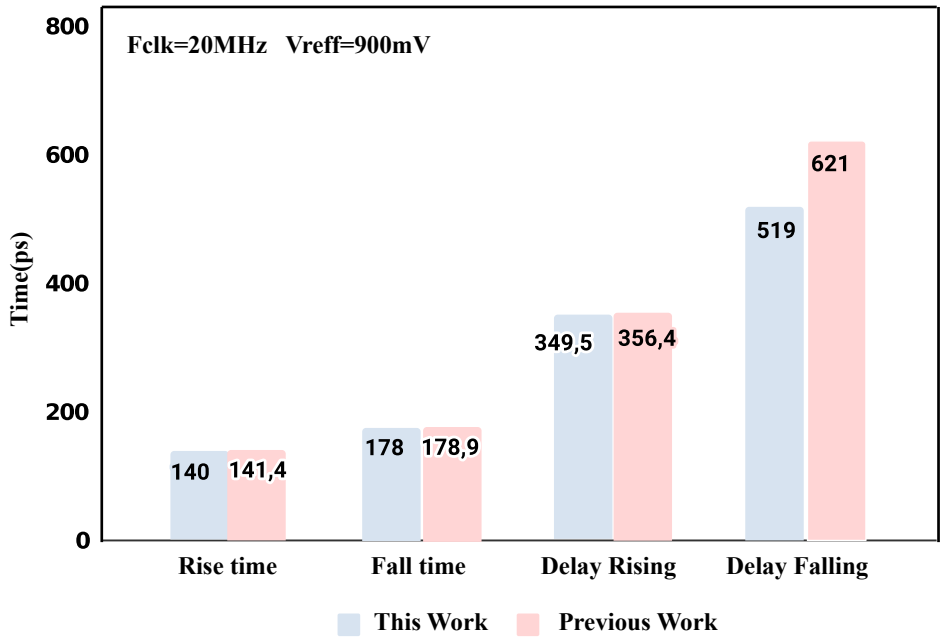
This section shows the techniques that were used to redesign the DLDO cells of ROMERO, E. y Elkim, *A Digital Low-Dropout Regulator for Low-Supply Voltage Operation* and the transitory results of each of the designed cells as well as the resulting layouts. The main problems we had when redesigning these cells were, when adjusting the dimensions of the transistors of the circuits, to comply with the regulatory widths of standard 9-track cells, preserving or improving the transient characteristics of the original cells. Also when making the layout of each cell it is necessary to comply with the standard cell layout format, this implies working with a specific size that limits the routing area in the cells.

3.0.1. NAND-BASED CLOCKED COMPARATORr Taking into account that the design of a circuit that is based on standard cell is easily portable from one technology to another. The objective is to design a comparator for a 9-tracks library. To begin with, the design of the comparator must be adjusted to be a standard cell, in ROMERO, E. y Elkim, *A Digital Low-Dropout Regulator for Low-Supply Voltage Operation* the NAND comparator does not meet the required conditions, if we look at the architecture of the NAND1 and NAND2 gates in Figure 2.2, they are NAND gates of 3 inputs, the dimensions of the NMOS transistors of these gates in ROMERO, E. y Elkim, *A Digital Low-Dropout Regulator for Low-Supply Voltage Operation* have twice the regulatory width (W) of a standard 9-track cell, due to this, the transistors were changed for two in parallel with a width almost half, which is equivalent to a transistor of the original size and the layout of the gates was made for a 9-track library.

The results obtained from this new design are an increase in speed and consumption, as shown in Figure 3.1, as well as the layout of the three-input NAND gate in

Figure 4.1 and the comparator as shown in Figure 4.1.

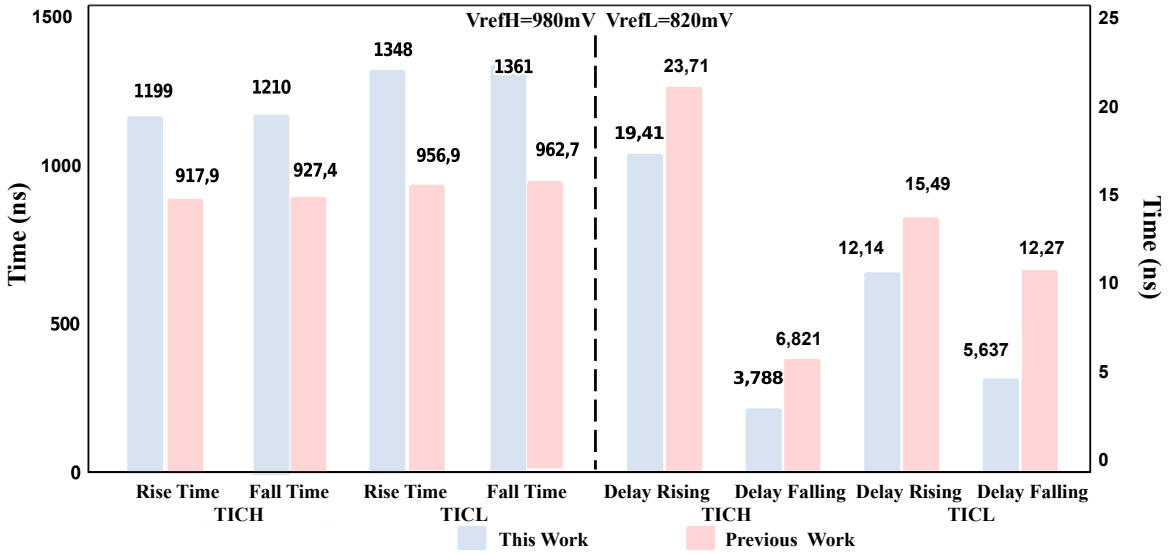
Figure 3.1. NAND Comparator Transient Parameters.



3.0.2. THRESHOLD INVERTER COMPARATOR The new comparator presents characteristics of a standard cell, this was achieved by changing the dimensions of the transistors in the Figure 2.3, the PMOS M0, M2 transistors originally had a width (W) of 2μm, but because the Maximum regulation width for a 9-track cell is 1.76 μm and to increase speed, we put 4 transistors in parallel each with a width of 1um, which is equivalent to a single transistor with a width of 4μm. Similarly, with the NMOS M1, M3 transistors to make them faster, 4 transistors were placed in parallel, with a width of 890nm each. The same was done with the NMOS M5 transistor, since its original width was 1.5μm, two transistors were placed in parallel with a minimum regulation width for a 9-track cell, which is equivalent to a slightly larger transistor. Regarding the M4 transistors, it was adjusted to the regulatory of 890nm. As a result, a comparator with a behavior similar to the original is obtained, faster in terms of Delay, but slightly slower in terms of rising and fall time, as seen in the Figure 3.2, and the layout of the

Figure 4.1 is obtained, with an area of $111\mu m^2$.

Figure 3.2. Threshold Inverter Comparator Parameters, Rise and Fall Time, Rise and Fall Delay, for Comparison of Upper and Lower Limit.



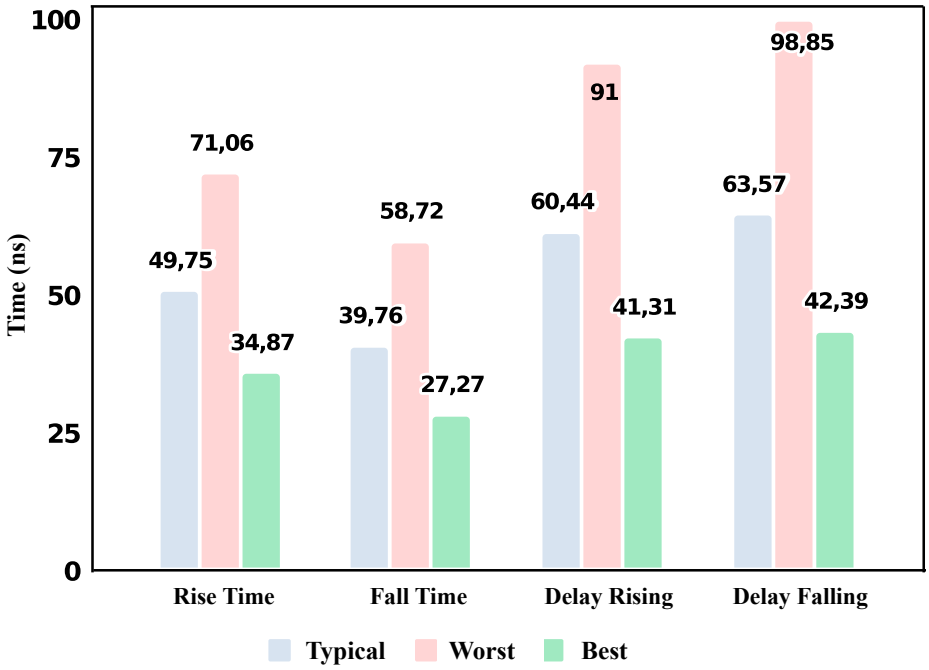
3.0.3. TRI-STATE BUFFER AS PASS DEVICES The problem addressed in this work is that the buffers in Figure 2.4 (b) do not have the characteristics of a standard cell, therefore it was necessary to fix their pitch to make a new layout, to be able to do automatic routing with Verilog code. The result is seen in the Figure 4.1, the layout has an area of $58.56\mu m^2$ and it is a Standard cell of 9 Tracks.

The results of the buffer consumption parameters are observed in Table 3.1 and b the transient characteristics are observed in Figure 3.3.

Table 3.1. Tri-State Buffer Consumption Parameters.

Parameter	**Consumption parameters**		
	Typical	Worst	Best
Input power	9,3nW	19,5nW	7,1nW
Average current	5,1nA	9,8nA	4,3nA
Peak current	7,1mA	8,0mA	6,2mA
Quiescent current	173,3pA	16,9nA	17,1pA

Figure 3.3. Tri-State Buffer Transient Parameters.



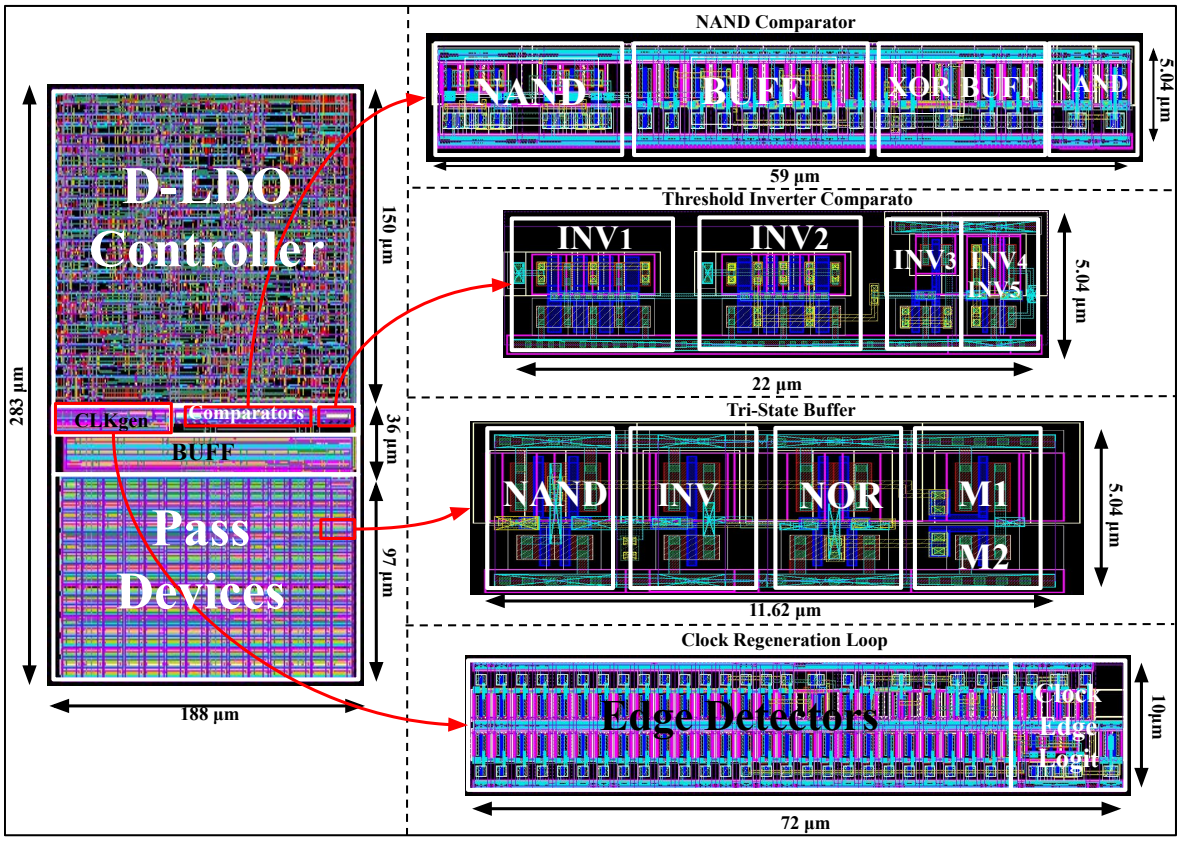
4. RESULTS

The advantage of the synthesizable design of the D-LDO is that it can be written in a hardware description code and can also scale between technologies. The code, instantiates the D-LDO controller code (dldo_sr) from ROMERO, E. y Elkim, *A Digital Low-Dropout Regulator for Low-Supply Voltage Operation*, along with the autogenerated clock block (dldo_clkgen), the A / D block (dldo_comp), the buffer bank (dldo_pass) and the BUFF block in figure ref proposed. These blocks use the standard designed cells and some cells of the TSMC18 technology used, in this way it is possible to do the automatic place and route using the Encounter tool and the .lef files of the standard cells created and the TSMC18 library.

Figure 4.1, shows the layout of the proposed D-LDO, which occupies an area of 0.053 mm^2 of which the majority is occupied by the $Pass\_devices$ block and the $DLDO\_Controller$. This Layout was generated following the digital flow and using the standard cells and Verilog code from the previous section. To use the cells made in the automatic routing, the files (.lef) of the cells were generated, with the abstract tool, later the automatic placement and routing were done with the Encounter tool, loading the files of the Verilog code of the section (IV) and files (.lef) of standard cells. Then the generated Layout was imported into Virtuoso.

The operation of the D-LDO for different situations is observed in Figure 4.2, where the simulation results are presented for a V_{IN} = 1.2V. Initially, the circuit is in SAR state, in this state it lasts 8 clock cycles to stabilize the output. Then the circuit is in a stable state (STEADY) so the V_{OUT}, oscillates between V_{REF}. Then in 1.5μs a load change is stimulated, which increases the current demand to the D-LDO with a rise time of 250s and as a consequence, there is a voltage drop in V_{OUT} which exceeds the limit of V_{REFL}. This activates fast recovery mode ({}$\_RISE$) and enables

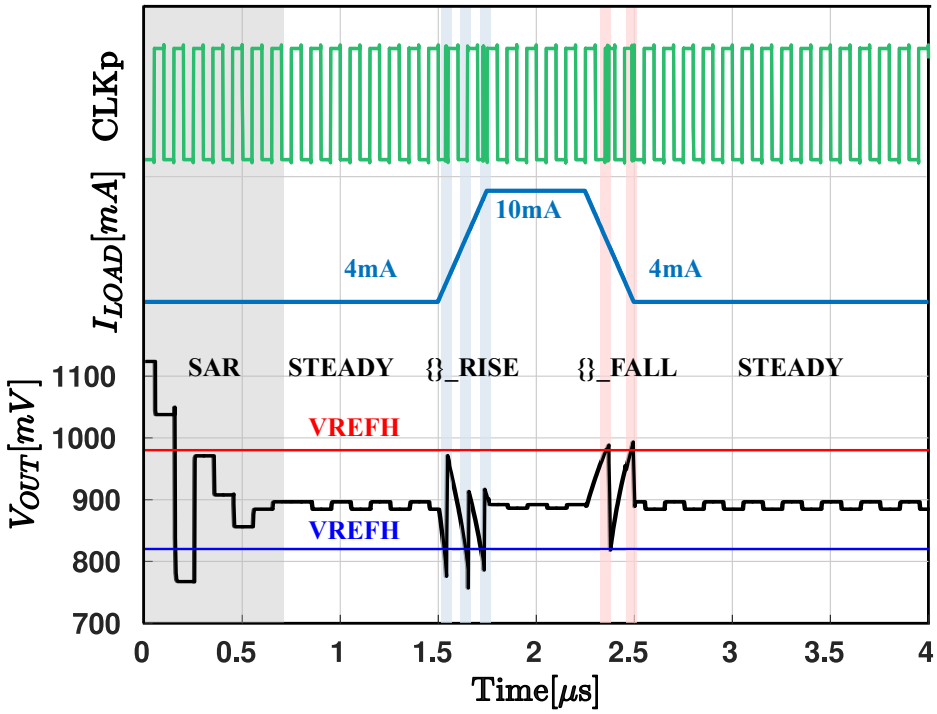
Figure 4.1. The layout of each block of the DLDO and the final integration.



the high-frequency clock that recovers V_{OUT} to its steady state. Once V_{OUT} is within the tolerance limits, the high-frequency clock is disabled and the low power mode returns with the external clock. At t = 2.75μs, there is a load change again, but in this case, there is a decrease in current demand with a fall time of 250s and as a consequence, we have an overshoot in V_{OUT}, which in this case passes the V_{REFH} limit and the fast recovery high mode ({}_$FALL$) is activated again. Quickly the circuit stabilizes V_{OUT} and the recovery mode fast is disabled again and will remain so as long as V_{OUT} does not exceed the limits of V_{REFL} and V_{REFH}.

In the Figure 4.3, the simulation results that describe the transient behavior of the D-LDO for different rise times of load current are observed, the test was carried out for a current variation of 19mA, ranging from 1mA to 20 mA and the rise times vary from

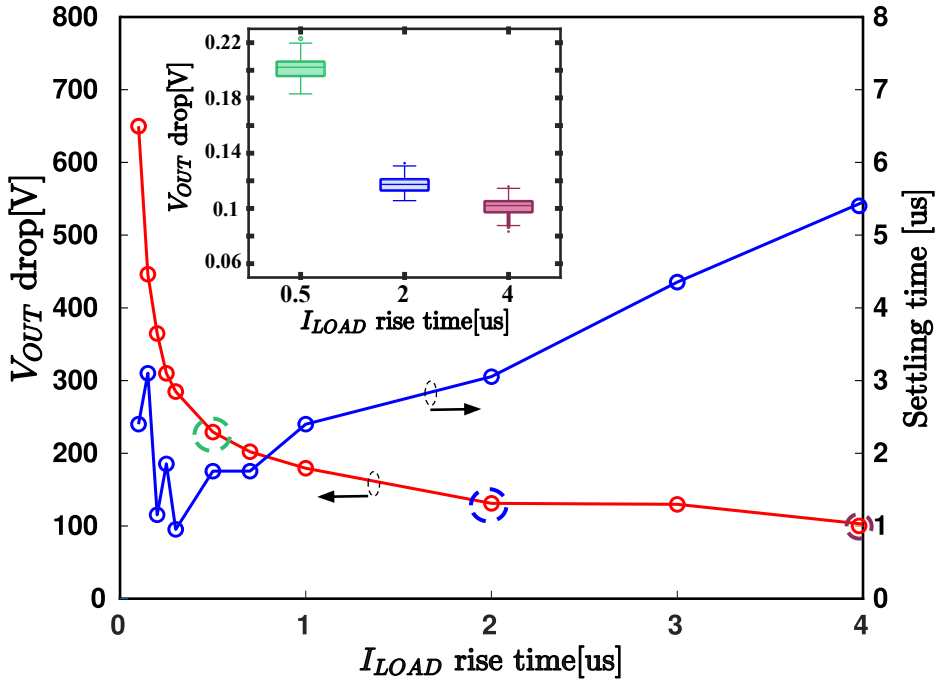
Figure 4.2. D-LDO Regulator Through Different Operating Modes.



100ns to 4μs(V_{IN}=1.2V, V_{OUT}=0.9V, ΔI_{LOAD}=19mA.). The average parameters are Settling time and voltage drop, in this way the limits of the D-LDO can be identified. To calculate the settling time, we used the same criteria as in ROMERO, E. y Elkim, *A Digital Low-Dropout Regulator for Low-Supply Voltage Operation*, the time that elapses since the start of the ramp, in this case, 1.5μs, and the time in which the variation of V_{OUT} does not exceed 5mV.

In the Figure 4.4, the charge regulation of D-LDO is observed. These results include the variations obtained by simulating the process and temperature corners. The presented simulations show that for a load current range of (100μA-20mA) with a V_{IN}, the load regulation in the typical case is 0.09 $\%/mA$. The error percentage of V_{OUT} corresponds to the difference between the mean value of V_{OUT} and V_{OUT}, this error is a characteristic of D-DLOs, since being digital, automatically introduce a quantization noise at the output of the regulator, it is also important to highlight the behavior

Figure 4.3. V_{OUT} Drop and Settling Time for Different I_{LOAD} Rise Times.



at low currents since this error is greater due to the computation of output devices when G is a small value, it affects more than when it is a considerably large value, which is observed in the typical curve, as shown look at the Table 4.2 *I_{LOAD} Rise Times=0.4μs,**I_{LOAD} Rise Times=1μs..

Table 4.2. Comparison of D-LDO Parameters.

Parameter	This Work Post Layout	Previous work
LDR	0.09 $\%/mA$	0.15 $\%/mA$
LNR	3 $\%/V$	2 $\%/V$
Settling time	0.751μs* | 2.4μs**	$\approx 2\mu$s * | >1μs**
V_{OUT} drop	221.1mV* | 180mV**	150mV* | <100mV**
Area	0.053 mm^2	0.029 mm^2

In the Figure 4.5, the operating frequency of the autogenerated clock is observed,

Table 4.1. State of the Art.

	Kundu, JSSC tr'19	**Akram, JSSC '19**	**Lee, JSSC '17**	**Nasir, JSSC '18**	**Previous work**	**This work****
Type	Digital	Digital	Digital	Hybrid	Digital	Digital
Process	65nm	65nm	**28nm**	130nm	180nm	180nm
V_{IN} [V]	**0.6-1.2**	0.7-1.2	1.1	1.1-1.2	1.2	1.2
V_{OUT} [V]	0.4-1.1	0.66-1.16	0.9	0.8-1.1	0.9	0.9
Max. I_{LOAD} [mA]	100	**235**	200	12	24	24
C_{LOAD} [pF]	40	Cap-less	23500	500	10	10
Load Reg	0.64	0.2	**0.11**	2.67	2.13	0.81
I_Q [μA]	100-1070	116-874	**110**	163	675-950	**25-304**
Max.C. Eff [%]	**99.0**	99.6	99.4	98.6	96.2	98.7
Area [mm^2]	**0.037**	0.069	0.021*	0.082*	0.029*	0.053*
FOM [ps]	**1.38**	N/A	9.57	184.4	2	2.4**

for different corners, the first two letters of the corner correspond to the speed of the transistors, F for fast, S for slow, and the last letter corresponds to the temperature status, H for high and L for low. The test was done with a load current change of 19mA, from 1m to 20mA, and a load current rise time of 250ns.

Line regulation was analyzed for different values of V_{IN} as shown in Figure 4.6, keeping I_{LOAD} constant at 10mA, for an input voltage variation from 1.05V to 1.5 V,the line regulation in the typical case is 3 $\%/V$. the comparison of the results obtained with those of the D-LDO of ROMERO, E. y Elkim, *A Digital Low-Dropout Regulator for Low-Supply Voltage Operation* are observed in Table 4.2.

In ROMERO, E. y Elkim, *A Digital Low-Dropout Regulator for Low-Supply Voltage Operation* he explains the behavior of D-LDO when V_{IN} is kept at a high value: for a constant load current when increasing V_{IN}, G must decrease to stabilize the system if G is a small value it is more sensitive to variations.

The figure of merit (FOM) calculation of the Table 4.1 was done with the equation 1 from Ma y col., "A 0.4V 430nA quiescent current NMOS digital LDO with NAND-

Figure 4.4. Load Regulation of the D-LDO.V_{IN}=1.2V

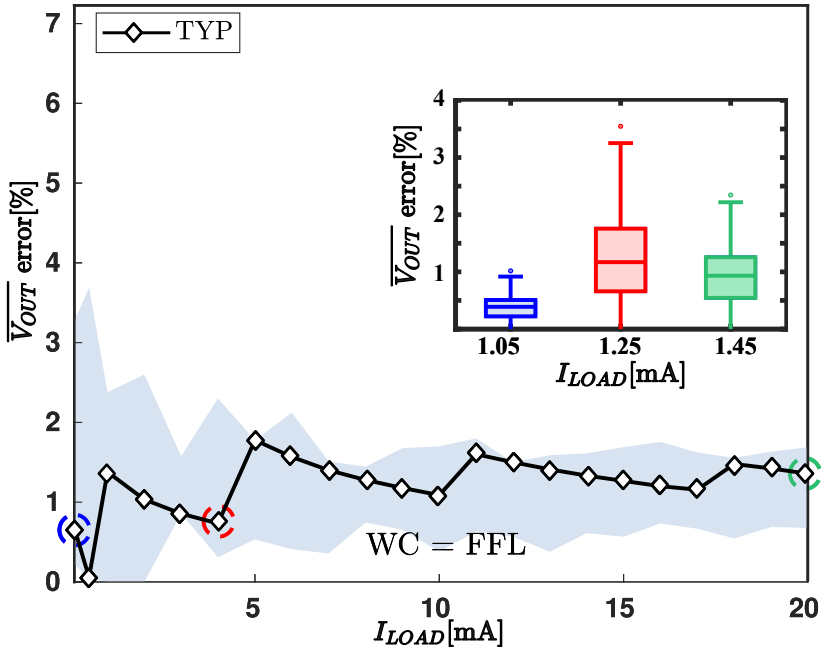
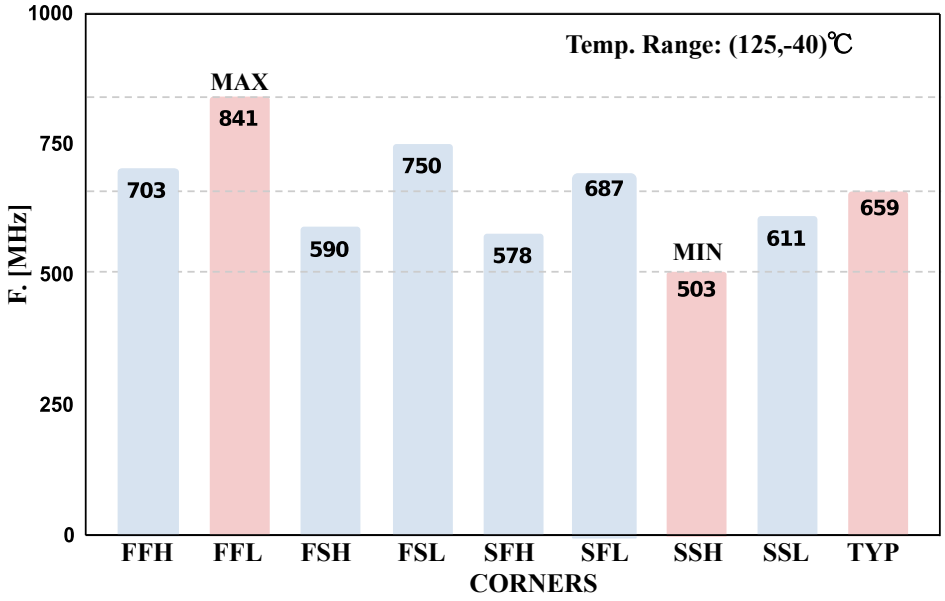


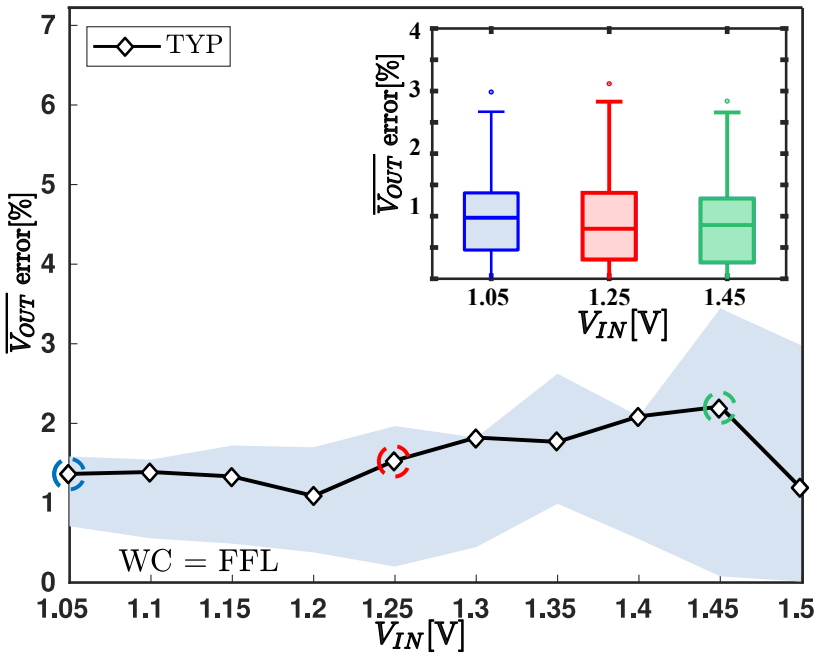
Figure 4.5. Operation frequency (CLK_fast).



based analog-assisted loop in 28nm CMOS".

$$FOM = \frac{C_{\text{LOAD}} \cdot V_{\text{OUT drop}} \cdot I_{\text{Q}}}{\Delta I_{\text{LOAD}}{}^2} \quad (1)$$

Figure 4.6. Line Regulation of the D-LDO.I_{LOAD}=10mA



5. CONCLUSION

The document presents the implementation of the standard cells and the layout of a D-LDO with a self-generated high-frequency clock with an operating frequency between (503-841)[MHz]. The final design features standard cells designed in 180nm CMOS technology that meet the characteristics of standard cells and are used to generate an automatic place and route using the Encounter tool. The final design load regulation is 0.9 $\%/mA$ and the line regulation is 3 $\%/V$. The circuit layout occupies an area of 0.053 mm^2. The transient response shows a voltage drop of 221.1mV, for a rise time of 400ns and a load current change of 19mA.

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