AN INTEGRATED RC OSCILLATOR WITH FREQUENCY TRIMMING TO DECREASE IMPACT OF SUPPLY VOLTAGE VARIATIONS

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RESUMEN

TÍTULO: AN INTEGRATED RC OSCILLATOR WITH FREQUENCY TRIMMING TO DECREASE IMPACT OF SUPPLY VOLTAGE VARIATIONS[*]

AUTORES: JULIÁN ARTURO ARENAS PEÑUELA[**]

PALABRAS CLAVE: Oscilador RC, Ajuste de frecuencia, Coeficiente de temperatura, Tiempo de establecimiento

DESCRIPCIÓN:

El presente artículo presenta un oscilador de relajación RC de frecuencia ajustable junto con sistema simple de calibración, fabricado en tecnología CMOS de 180nm. Esta arquitectura utiliza un amplificador de error con el fin de comparar la tensión de salida RC con una tensión de referencia interna. El consumo de potencia del oscilador es reducido gracias a un lazo de control auxiliar que desactiva el amplificador de error durante la mayor parte del periodo de oscilación. Dicho amplificador de error conmutado utiliza un Schmitt trigger con puntos de conmutación fijos en contraste con otras arquitecturas. El uso de un Schmitt trigger es menester debido a la necesidad de ajustar los puntos de conmutación a un valor cercano a la tensión de referencia y para permitir la carga completa del capacitor antes de un nuevo ciclo. Además, el diseño de la referencia interna garantiza robustez ante las variaciones de la tensión de alimentación al seguir a ésta de manera proporcional. El circuito propuesto consigue un coeficiente de estabilidad en tensión de ±0.5% sin la necesidad de un lazo de control para el ciclo útil del amplificador. La optimización del consumo de potencia, por lo tanto, pasa a centrarse en el diseño del Schmitt trigger debido a que éste se convierte en el bloque del sistema que más corriente estática consume. El oscilador ocupa un área de 0.055 mm2 con un consumo de potencia de 0.33µW@32.768kHz y 1.5µW@1.024MHz. Además, un tiempo de establecimiento de 220µSq@32.768kHz y 4.4µS@1.024MHz es conseguido.

[*] Proyecto de grado

[**] Facultad de Ingenierías fisicomecanica. Escuela de Ingenierías eléctrica, electrónica y de telecomunicaciones. Director Héctor Iván Gómez Ortiz,. Cordirector Elkim Felipe Roa Fuentes

ABSTRACT

TITLE: AN INTEGRATED RC OSCILLATOR WITH FREQUENCY TRIMMING TO DECREASE IMPACT OF SUPPLY VOLTAGE VARIATIONS*

AUTHOR: JULIÁN ARTURO ARENAS PEÑUELA**

KEYWORDS:.RC Oscillator, Frequency Trimming, Temperature Coefficient, Settling Time

DESCRIPTION:

This paper presents a wide-band RC relaxation oscillator with a low-complex frequency calibration, fabricated in 180nm CMOS technology. This architecture uses an error amplifier in order to compare the RC output voltage with an integrated reference. Power consumption is reduced thanks to an auxiliary power-down loop which turns-off the error amplifier during almost the whole oscillation period. This power-gated error amplifier uses a fixed threshold Schmitt trigger in contrast to a previous architecture. The usage of a Schmitt trigger is required in order to adjust the switching points close to the reference value and to fully charge the capacitance before a new cycle starts. Also, the integrated voltage reference behavior guarantees robustness against supply voltage variations by making the reference follow the supply. This makes the discharging time only dependent on the RC time constant value. The proposed circuit achieves a voltage stability of ±0.5% and low power operation without the need for a complex duty cycle control for the amplifier. Power consumption optimization focus on the Schmitt trigger as this circuit becomes the power-hungry block in the oscillation loop. The oscillator occupies an area of 0.055 mm^2 with a current consumption of 0.33µA@32.768kHz and 1.5µA@1.024MHz. Also, a start-up time of 220µSq@32.768kHz and 4.4µS@1.024MHz is achieved.

* Proyecto de grado

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INTRODUCTION

Traditional sensor monitoring paradigm has changed due to the pervasiveness of the internet of things (IoT) devices. A system-on-chip (SoC) for IoT applications can enter in sleep or deep sleep mode, rather than its normal operating scheme, by turning-off blocks outside the Always-on (AON) domain when SoC is obtaining data without processing. Furthermore, AON domain must have an ultra-low power consumption due to supply limitations such as battery supplied or harvesting systems[1]. In this restricted scenario, a reference clock must have an accurate and stable output frequency despite the strong supply voltage variations as well as different temperature conditions. In terms of frequency stability, crystal oscillators have better performance due to their high-quality factor. However, they imply integration challenges as having an off-chip element [2] [3]. Ring inverter-based oscillators are small area fully on-chip integrated, as their main core only relies on inverter cells. Nevertheless, PVT calibration is needed due to the reduction of the quality factor of the oscillator. To overcome the clock reference necessities, RC relaxation oscillators are preferred due to their integration facilities and high voltage and temperature stability [4]. Still, the challenge of the RC relaxation oscillator design relies mainly on the temperature dependence of the time constant τ because of the

[1] WANG J., GOH W. L., LIU X., and ZHOU J., "A 12.77-MHz 31 ppm/°C OnChip RC Relaxation Oscillator with Digital Compensation Technique," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 63, no. 11, pp. 1816–1824, 2016

[2] COUSTANS M., KRUMMENACHER F., KAYAL M., and TERRIER C., "A nA crystal - Less oscillator for internet of things," Proceedings of the 23rd International Conference Mixed Design of Integrated Circuits and Systems, MIXDES 2016, no. 1, pp. 136–139, 2016

[3] SAVANTH A., MYERS J., WEDDELL A., FLYNN D., and AL-HASHIMI B., "A 0.68nW/kHz supply-independent Relaxation Oscillator with 0.49%/V and 96ppm/°C stability," Digest of Technical Papers - IEEE International SolidState Circuits Conference, vol. 60, pp. 96–97, 2017

[4] Ibíd.

resistor elements [5]. Also, frequency oscillation is affected by active devices performance [6].

Despite the challenges of the RC relaxation oscillator design, different calibration methods such as temperature coefficient cancellation [7] and offset calibration [8] have been presented. However, they focus only to adjust the output frequency to a single value. Wide-band operation requires more attention to the delay of active elements, since their bandwidth needs to be enough to respond at higher frequencies; as well as passive tuning must guarantee a proper control to the time constant even with PVT variations.

This paper presents a wide-band 32.768kHz to 1MHz RC relaxation oscillator, frequency wide-band tuning as well as temperature compensation is performed automatically by a Finite State Machine (FSM). Voltage Independence is achieved by a voltage reference which varies proportionally to the supply. Also, power consumption is reduced to the minimum due to the bandwidth control of the active devices and an additional power-down control loop. Post-silicon performance of the oscillator is described in this paper as well.

General Objective: To design an RC oscillator in 180nm CMOS technology with an operation frequency between 33 kHz and 1 MHz, enabling frequency trimming to decrease the impact of supply voltage variations.

Specific Objectives:

- Design of the digital circuits that are needed for the control loop inside the oscillator.

[5] WANG J., GOH W. L., LIU X., and ZHOU J., Op. Cit.
[6] GURLEY C. ¨ uk, L. Pedal ¨ a, F. Sebastiano, and K. A. Makinwa, “A CMOS ` Dual-RC frequency reference with 250ppm inaccuracy from -45C to 85°C,” Digest of Technical Papers - IEEE International Solid-State Circuits Conference, vol. 61, pp. 54–56, 2018
[7] SAVANTH A., MYERS J., WEDDELL A., FLYNN D., and AL-HASHIMI B., Op. Cit.
[8] WANG J., GOH W. L., LIU X., and ZHOU J., Op. Cit.

- Design a voltage reference that allows a frequency that is robust against supply variations using the switching capacitor technique (SCR).
- To perform Monte Carlo and corners simulations to evaluate the performance of the oscillator.

Project Justification: Limited power budget available in IoT systems makes it a challenge to meet all specifications. Inside these restricted environments, digital systems require a low power clock source, such as current starved oscillators and RC oscillators. Design difficulty of these oscillator is increased due to inherent variations of active and passive devices that affect accuracy and frequency stability. RC relaxation oscillators are preferred because of frequency stability and accuracy compared to other topologies in the state of the art [9]. This project aims to fulfill the design of an RC relaxation oscillator that can provide a variable frequency and with strong performance against power supply variations.

[9] SAVANTH A., MYERS J., WEDDELL A., FLYNN D., and AL-HASHIMI B., Op. Cit.

1. RELAXATION OSCILLATOR ARCHITECTURE:

Figure 1: Proposed RC Relaxation Oscillator Circuit.

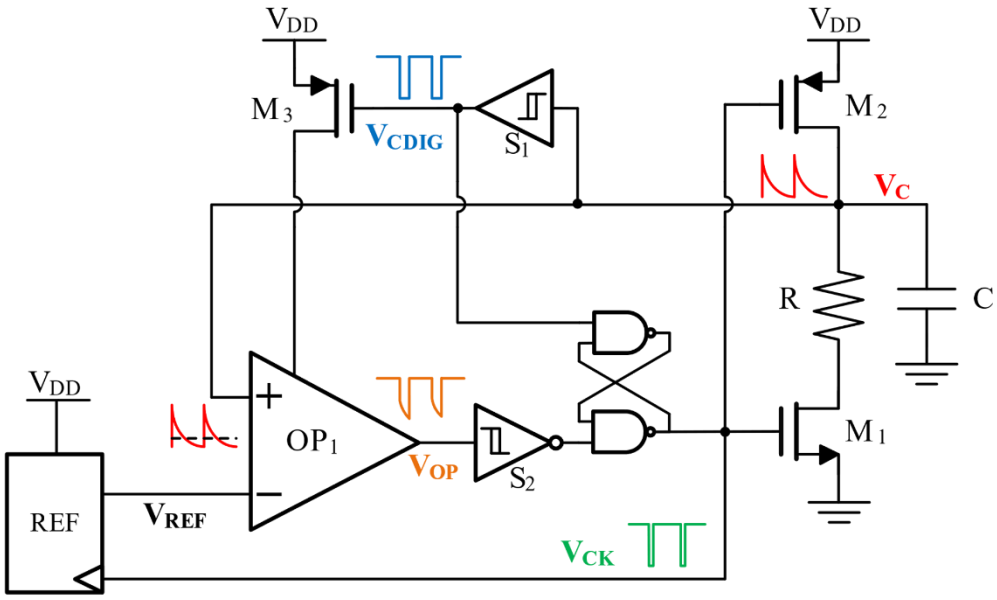
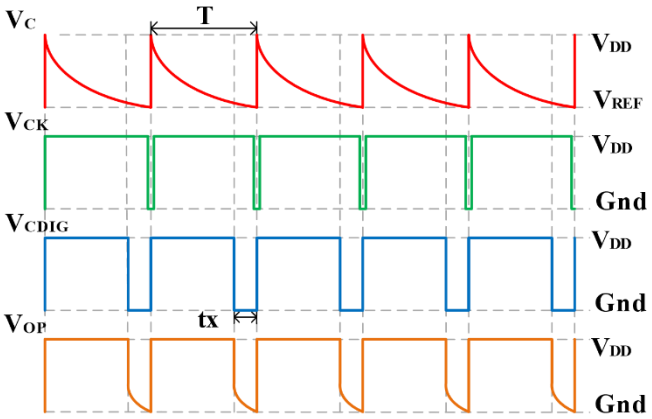


Figure 2. RC oscillator signals time diagram.



A regular relaxation oscillator uses an error amplifier to generate a pulse that charges and discharges an RC bank. The oscillator frequency depends on the capacitor discharge through the resistance and the comparison reference as Fig. 1 shows [10]. When V_{CK} is low, transistor M2 charges the capacitor. Once in this condition, V_C is higher than the voltage reference V_{REF} of the error amplifier (OP1), V_{CK} signal immediately becomes high after V_C becomes high. Then, the discharge process through the resistance starts and continues until V_C approaches to V_{REF}, turning V_{OP} to low, charging the capacitance and beginning the loop again.

The error amplifier only needs to operate when V_C is close to V_{REF} [11]. This feature enables the possibility to power-down the amplifier in the remaining cycle time. Hence, the Schmitt trigger (S1) has a switching point near to V_{REF}, activating the amplifier only when comparison is necessary. Fig. 2 illustrates the time diagram of the signals inside the oscillator. OP1 is active during a short time t_x generating the signal V_{OP}. For the rest of the cycle, V_{OP} is pulled-up to maintain V_{CK} in high. Also, Schmitt trigger (S2) has a switching point close to the supply in order to change its value only when OP1 is turned-off and prevent charging glitches. Once V_{OP} is low enough so V_{CK} turns M2 on, V_{CDIG} signal from (S1) turns-off the error amplifier. Finally, a NAND based latch matches the propagation delays between the direct loop and the power-down loop to avoid glitches.

Stability under different voltage and temperature conditions are desired features in a relaxation oscillator [12]. This architecture uses a switched capacitor-based voltage reference (SCR) to generate a reference proportional to voltage supply. V_{CK} charges and discharges the capacitor reference in order to generate approximately $V_{DD}/3$ at its output. An SCR is preferred rather than a resistance voltage divider because it

[10] SAVANTH A., MYERS J., WEDDELL A., FLYNN D., and AL-HASHIMI B., Op. Cit.
[11] Ibíd.
[12] GURLEY C. ¨ uk, PEDAL L. ¨ a, SEBASTIANO F., and MAKINWA K. A., “A CMOS ` Dual-RC frequency reference with 250ppm inaccuracy from -45C to 85°C,” Digest of Technical Papers - IEEE International Solid-State Circuits Conference, vol. 61, pp. 54–56, 2018

has a better temperature behavior, helping with temperature stability as well as saves static power consumption [13].

[13] SAVANTH A., MYERS J., WEDDELL A., FLYNN D., and AL-HASHIMI B., Op. Cit.

2. WIDE-BAND RCO CIRCUIT IMPLEMENTATION

Figure 3. RC oscillator implemented schematic.

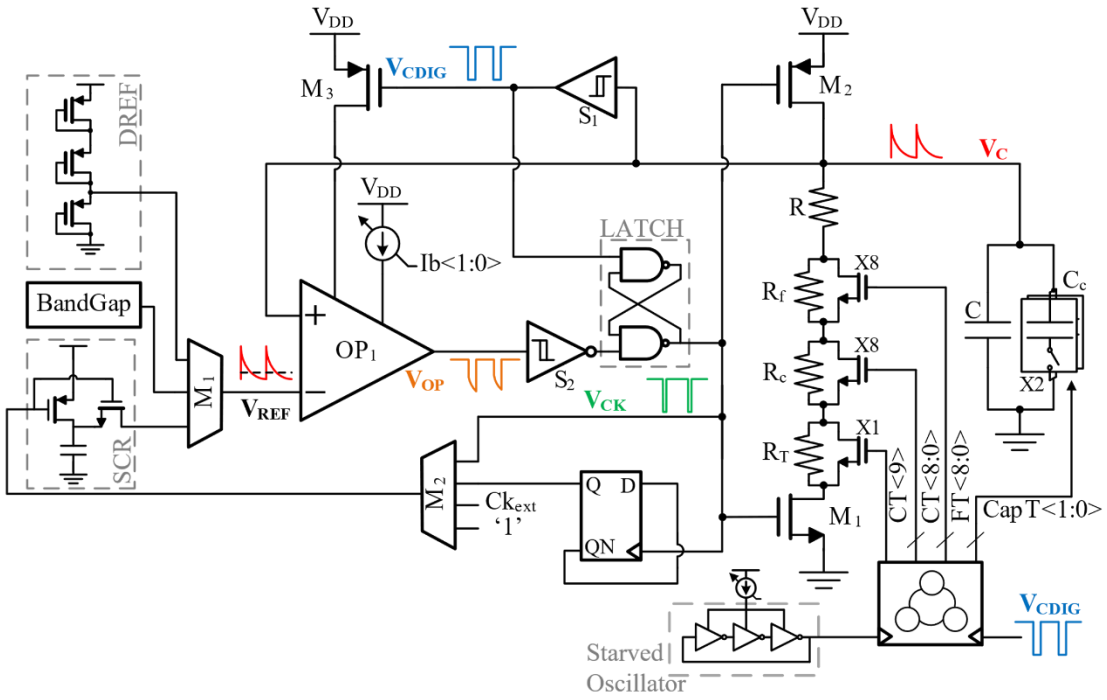


Figure 4: SCR and diode reference comparison.

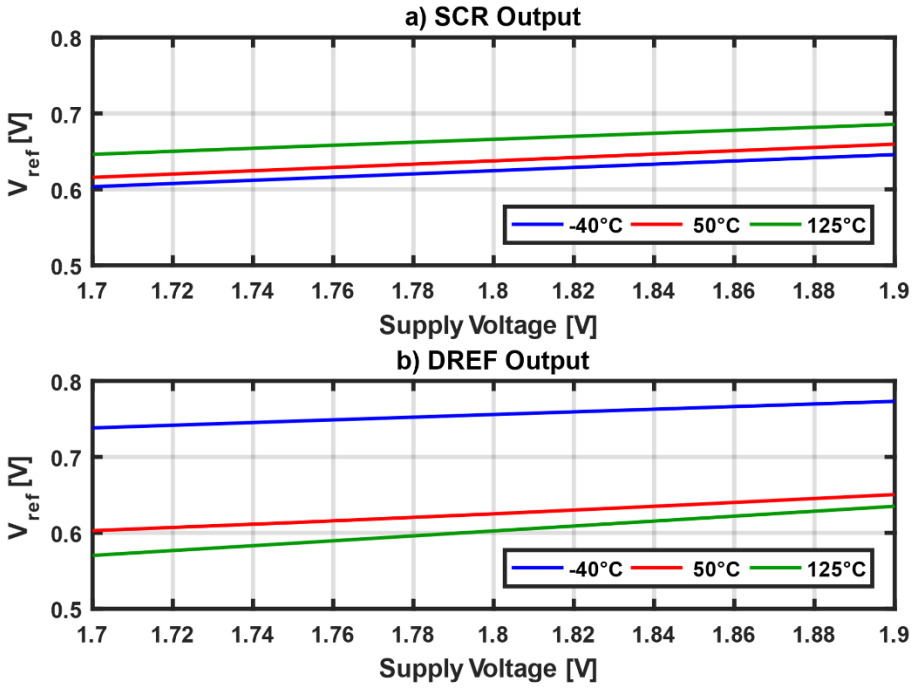


Figure 5: CMOS Schmitt trigger architecture.

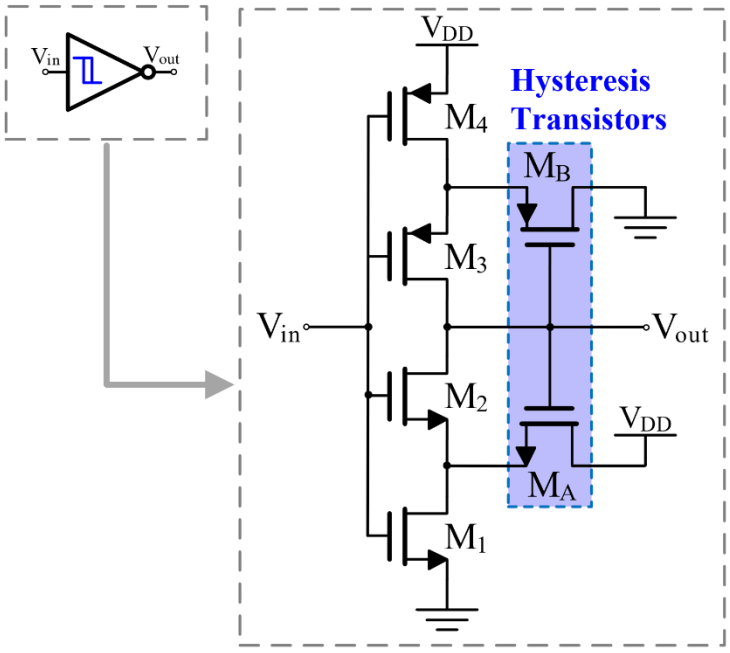


Figure 6: a) Simulation results of power consumption for different blocks at 32.768kHz. b) Simulation results of power consumption of different blocks at 1.024MHz.

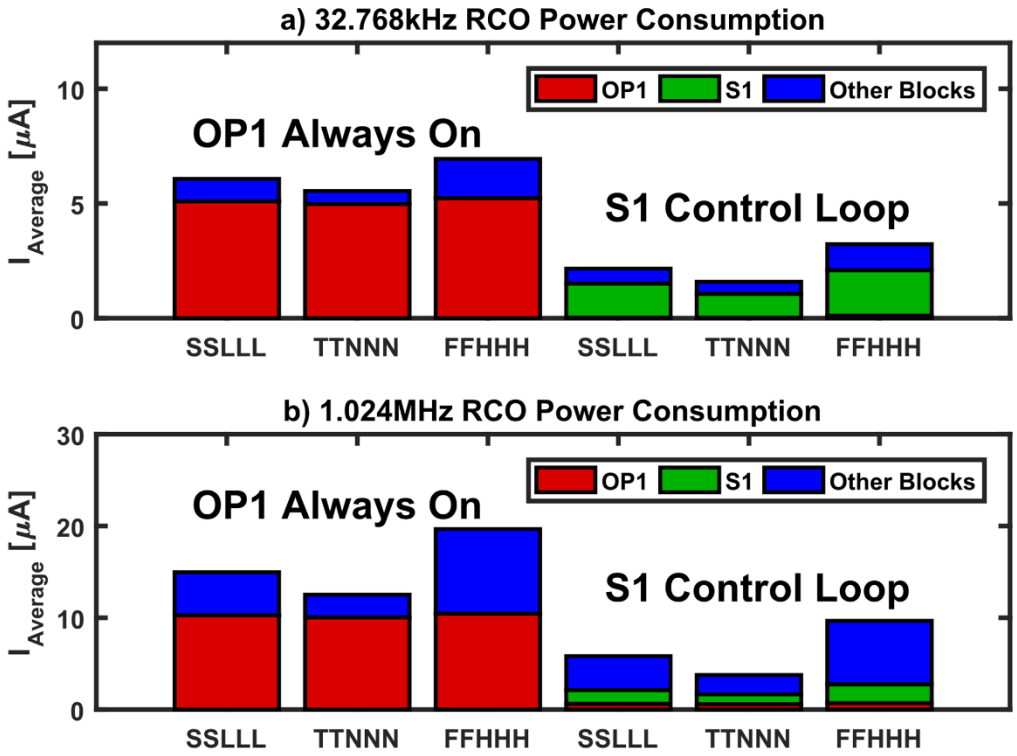


Fig. 3 shows the implemented system. Adding the wideband feature requires to have control of RC bank and OP1 bandwidth, avoiding any power consumption penalization. In addition, a finite state machine (FSM) provides autocalibration or manual control to fully verify the oscillator operation. However, the FSM design is out of the aims of this work. This section describes the implemented features including a discussion about power consumption optimization.

A. Error Amplifier Bandwidth Control

Propagation delay of the error amplifier directly affects the output frequency. This means that a high slew-rate and bandwidth performance are essential for the whole

system. However, power consumption increases as bandwidth does, needing more biasing current and, even with the power-down module, increasing the static consumption.

The implemented amplifier has a bandwidth control feature. As Fig. 3 shows, the digital word I_b varies the bias current turning-on and off digital controlled current mirrors. This digital tuning enables a current consumption less than 1µA at low frequency operation (kHz) but it also enables a higher frequency operation (MHz) by reducing propagation delay with the additional bias current.

B. RC Bank Tuning and Wide Band Operation

RC relaxation oscillator output frequency mainly relies in the time constant $\tau = RC$ [14]. However, resistance and capacitance variations across process and temperature deviate the RC time constant and the frequency as well. These variations affect temperature stability [15]. The proposed RC bank features three types of tuning, including resistance, capacitance, and a temperature coefficient tuning.

Fig. 3 shows the three resistance banks where R_f, R_c and R_T correspond to fine tuning, coarse tuning and temperature tuning respectively. Two 8 thermometer buses adjust the coarse and fine tuning, and an additional resistance control provides the temperature tuning. Temperature trimming is done by the cancellation of temperature coefficient of the resistors inside the oscillator. R_f and R_c banks are poly resistors and R_T are well resistors to help with temperature compensation. Temperature compensation is a major issue considering the resistance bank change over the frequency range. We address this issue by tuning the well resistor bank as well.

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[14] SAVANTH A., MYERS J., WEDDELL A., FLYNN D., and AL-HASHIMI B., Op. Cit.

[15] CAO Y., LEROUX P., COCK W. D., and STEYAERT M., "A 63,000 Q-factor relaxation oscillator with switched-capacitor integrated error feedback," Digest of Technical Papers - IEEE International Solid-State Circuits Conference, vol. 56, pp. 186–187, 2013

As the technology does not provide mim-capacitors, we implement a C bank with NMOS capacitors. This implementation occupies less area at the expense of increased sensitivity to process variations and leakage. In addition, a capacitance control enables a higher frequency range that only the coarse resistance step. Hence, two control bits provides different operation frequencies with a minimum value of 300fF for MHz range, and a maximum of 10pF for 32.768 kHz operation scheme.

C. Supply Voltage Robustness

The discharge time must be constant to ensure an invariant frequency. Assuming steady state, one period of the output waveform can be expressed by (1). Considering that the loop starts again when V_C is almost V_{REF}, (2) presents the relationship between the supply voltage and V_{REF}.

$$V_C(t) = V_{DD}(e^{-t/\tau}) \quad (1)$$

$$\frac{V_{REF}}{V_{DD}} = e^{-1/f\tau} \quad (2)$$

(2) reveals that, if OP1 compares with a constant reference under supply variations, the discharge time constant τ, and so the frequency will change over V_{DD} variations. V_{REF} must follow V_{DD} with a constant slope. A qualitative explanation is derived by considering that the comparison can occur after or before the expected time as the maximum value of V_C changes [16]. Therefore, the ideal voltage reference should be invariant to temperature and process but not to supply variations.

[16] SAVANTH A., MYERS J., WEDDELL A., FLYNN D., and AL-HASHIMI B., Op. Cit.

Savanth et. al. [17] proposes to use a switched capacitor-based reference (SCR) which emulates a resistor voltage divider. The advantage is that the SCR has better temperature coefficient, occupies less area and avoids any static current consumption. We add a diode reference (DREF), which works as a voltage resistor divider, and an external reference (Bandgap) as alternative options for debugging and comparison purposes. Bandgap reference design is out of the aims of this work.

Fig. 4 illustrates how the SCR presents a better behavior than DREF against temperature variations Bandgap reference is not compared because its output voltage does not vary with the supply. In Fig. 4a), the slope is almost constant with temperature and it is also proportional to voltage supply. Fig. 4b) shows how DREF experiments a considerable influence of temperature, changing the slope, losing proportionality to power supply and, therefore, altering the output frequency of the oscillator.

D. A closer look to the Schmitt Trigger

There are two Schmitt Triggers inside the oscillator loop. S1, which controls the power-down control module, and S2 that controls the RC charging and discharging scheme. Fig. 5 shows the CMOS Schmitt Trigger architecture. The hysteresis transistors control the operating points of M2 and M3, controlling both switching points. These thresholds points, seen from the output of view, are defined as:

$$V_{L2H} = \frac{V_{DD} - |V_{thp}|}{H+1} \qquad (3)$$

$$V_{H2L} = \frac{V_{DD} + GV_{thn}}{G+1} \qquad (4)$$

[17] Ibíd.

where H^2 and G^2 are W_BL_4/W_4L_B and W_1L_A/W_AL_1 respectively. (3) and (4) reveal the relationship and function of the Hysteresis transistors M_A and M_B. We designed S1 low-to-high switching point close to VREF value in order to turn on the error amplifier only during a short time of the whole period; implying an G value close to 1. Moreover, S2 high-to-low switching point must be close to the supply voltage to prevent a discharge glitch coming from OP1. This aspect relationship not only controls the switching points, but also define the static current of the Schmitt trigger. Since S2 input comes from a pulled-up wave, its power consumption is negligible. However, S1 receives V_C signal as its input, which generates static power consumption at low frequency operation. We oversize S1 transistors, leaving a considerable length in order to reduce power consumption without changing the switching points.

E. On the limits of power consumption

There are two main circuits that consumes most of the total current. The error amplifier and the Schmitt trigger (S1) that controls the amplifier power-down signal. Due to the control over amplifier operation, the current consumption in this circuit is less than 1µA over all process variations. Hence, the major part of the current corresponds to the Schmitt trigger where the slow slope of the RC discharge creates a large DC current.

Savanth et. al. [18] proposes an automatic control to Schmitt trigger threshold with the aim to optimize the amplifier power consumption. The control requires to estimate the time period of OpAmp operation and to adjust a variable threshold Schmitt trigger, also using it to adjust the frequency with pre-charged values of resistance tuning. In contrast, we use a fixed threshold Schmitt trigger, considering amplifier current is not the one limiting the power consumption We optimizes Schmitt trigger,

[18] Ibíd.

sizing it to reduce as much as possible the associated DC current. In addition, we evaluate robustness of the trigger threshold over process and temperatures variations, ensuring a proposer value for a precise comparison. Finally, we design the Schmitt Trigger in a way that the resulting amplifier average current plus Schmitt trigger average current is less than a half the full DC current of the amplifier.

Fig. 6 shows a power break-down of the oscillator when OP1 power control loop operates and when OP1 is always working. Fig. 6a) and Fig. 6b) show the power break-down at 32.768kHz and 1.024MHz respectively. For both operation frequencies, OP1 experiments the higher power consumption when is always on. When the power control loop operates, the OP1 power consumption is negligible compare to Schmitt trigger and other blocks. In addition, the behavior is consistent for both operation frequencies and across PVT variations[1].

3. MEASUREMENT AND SIMULATION RESULTS

Figure 7: Die micro-photograph and layout details of the proposed RCO.

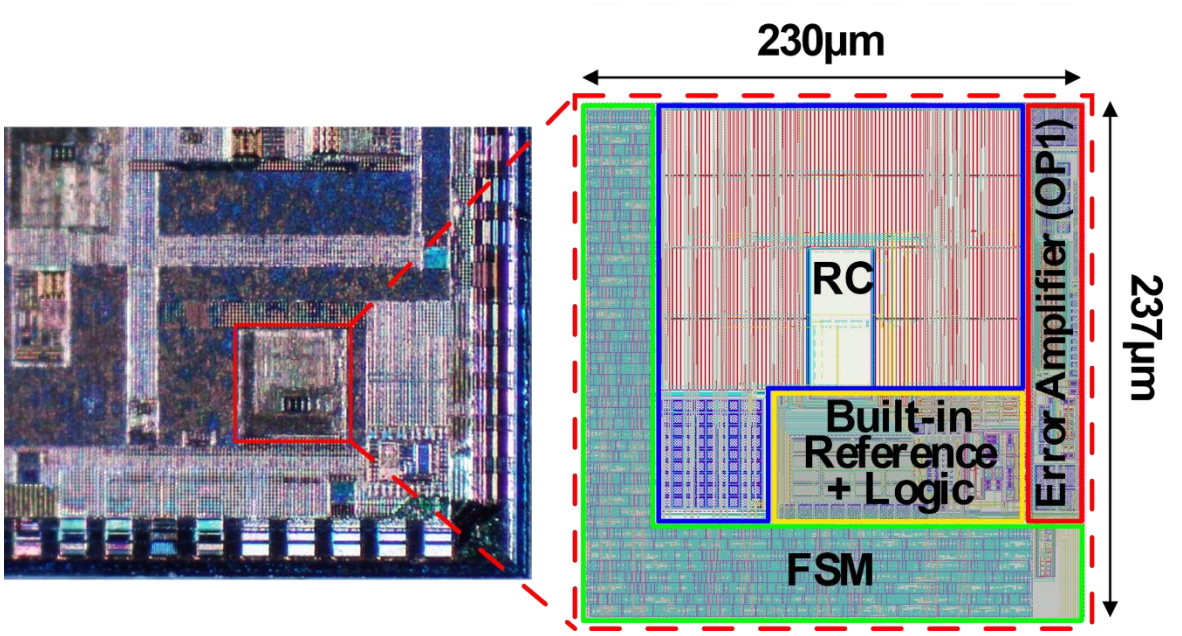

Figure 8: a) Corners simulation for typical and worst cases at 32.768kHz. b) Corners simulation results for typical and worst cases at 1.024MHz.

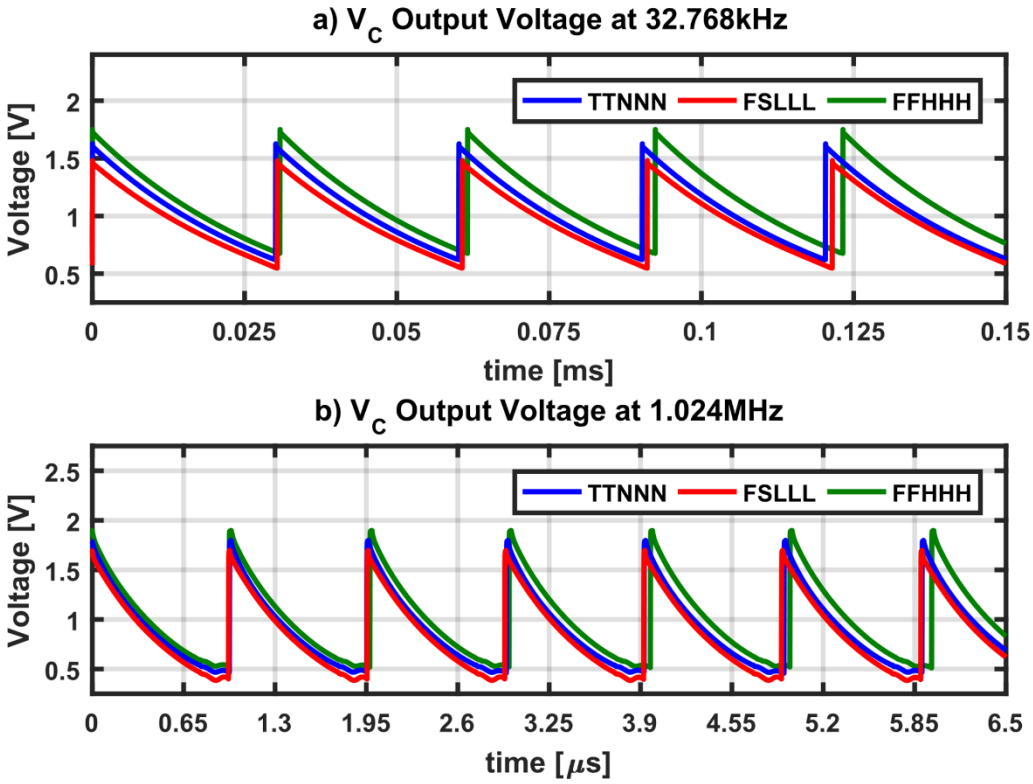

Figure 9: a) Montecarlo simulation for typical case at 32.768kHz. b) Montecarlo simulation for typical case at 1.024MHz.

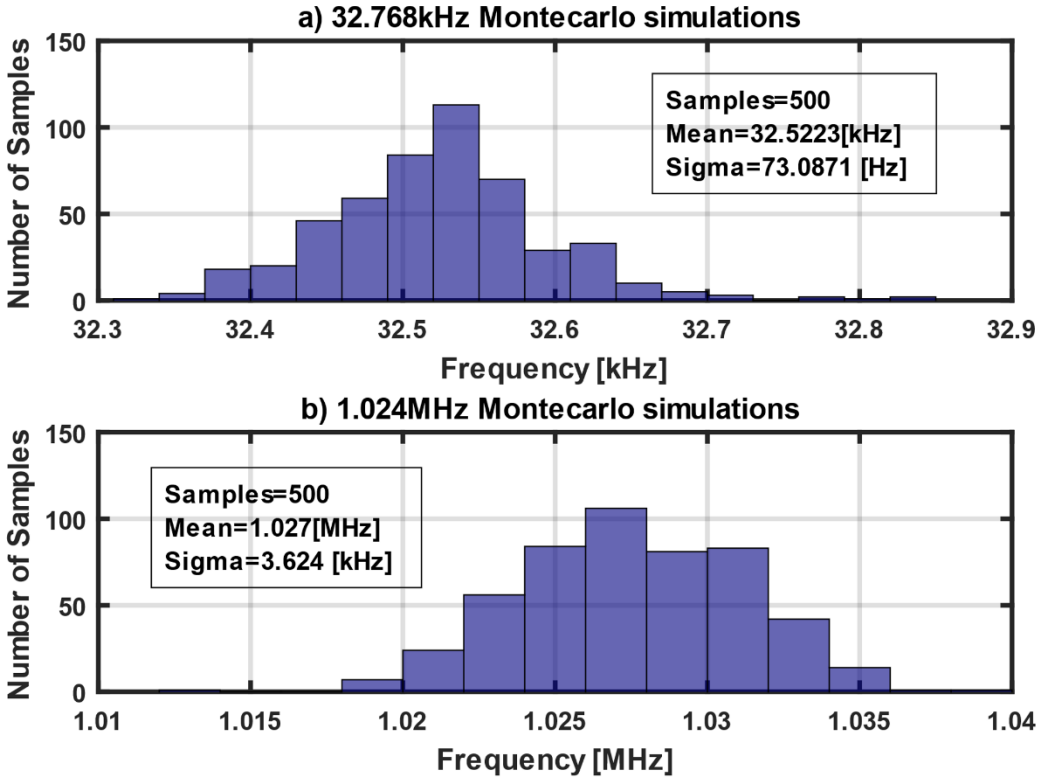

Figure 10: a) 32.768kHz free-running frequency against supply voltage. b) 1.024MHz free-running frequency against supply voltage.

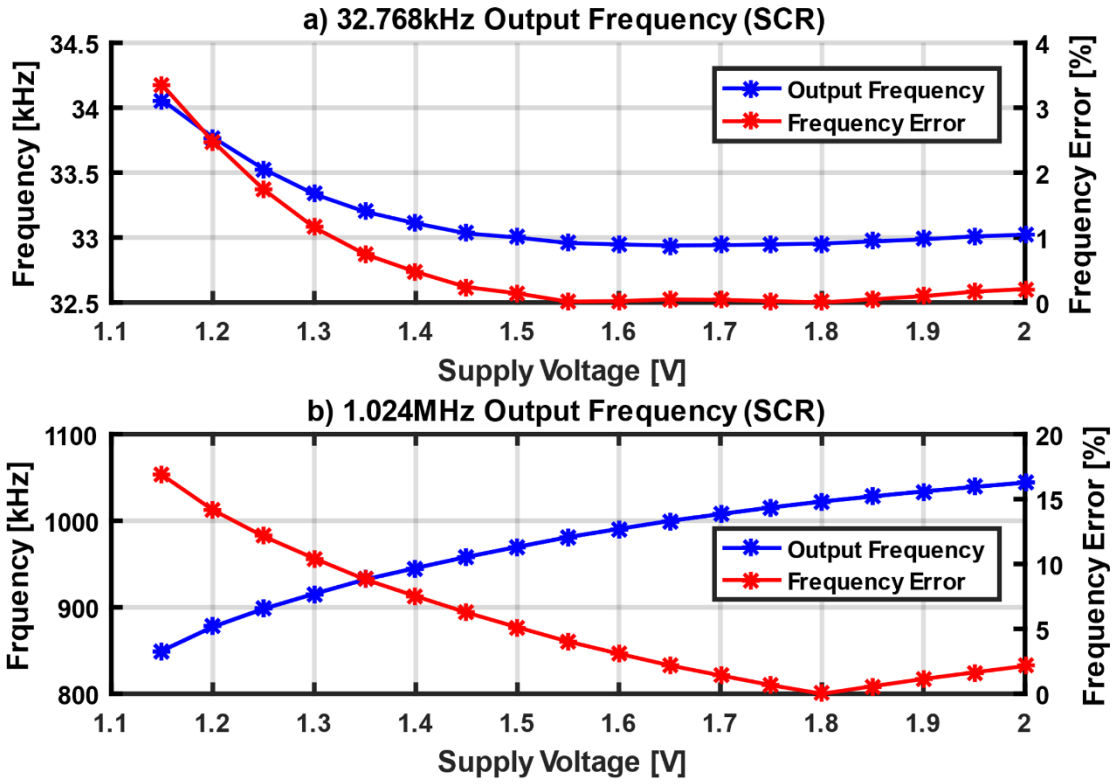

Figure 11: a) SCR measured results for 32.768kHz over temperature. b) DREF measured results for 32.768kHz over temperature.

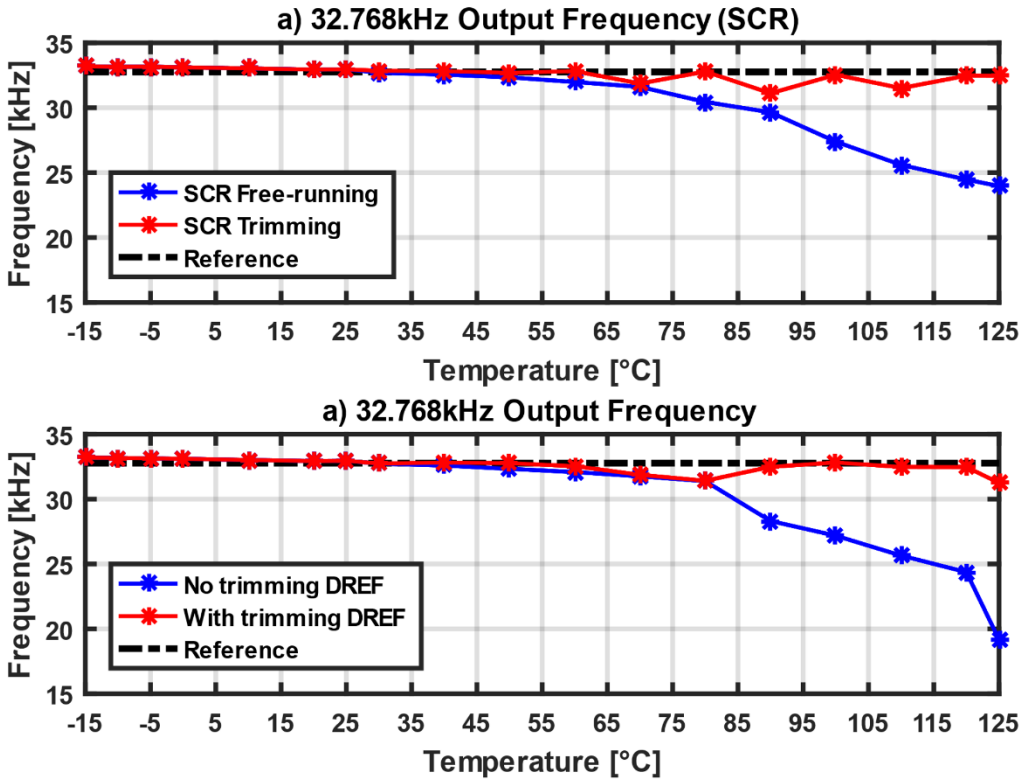

Figure 12: a) SCR measured results for 1.024MHz over temperature. b) DREF measured results for 1.024MHz over temperature.

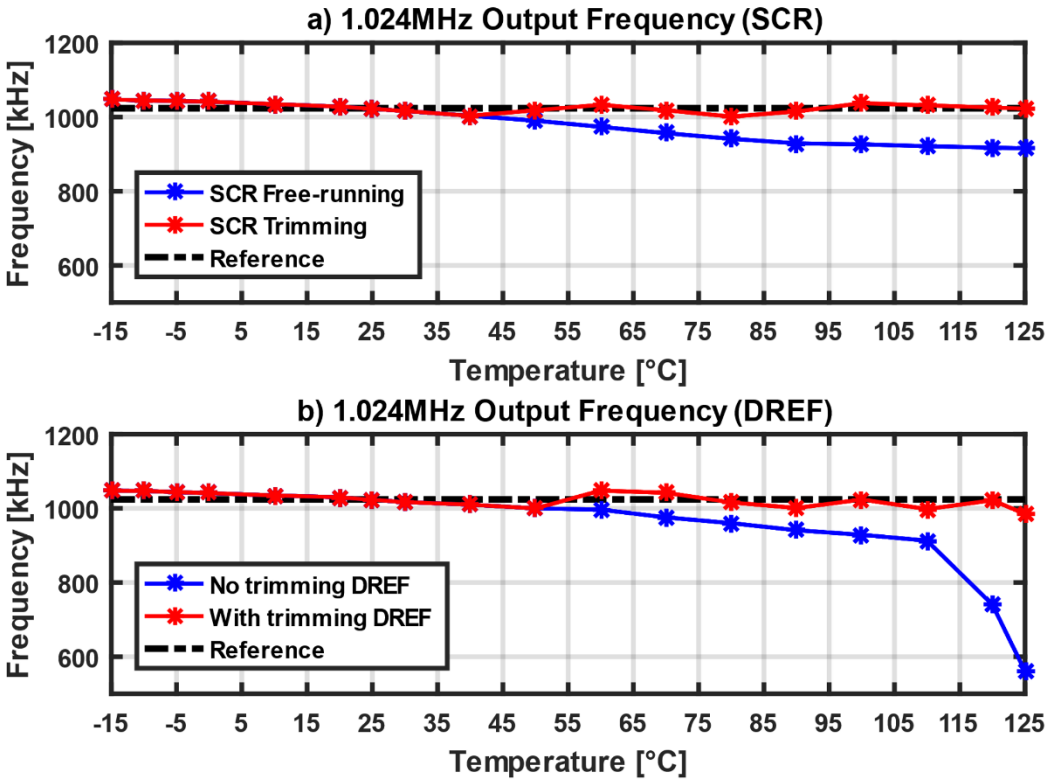

Figure 13: Measured settling time for 32.768kHz and 1.024MHz frequencies.

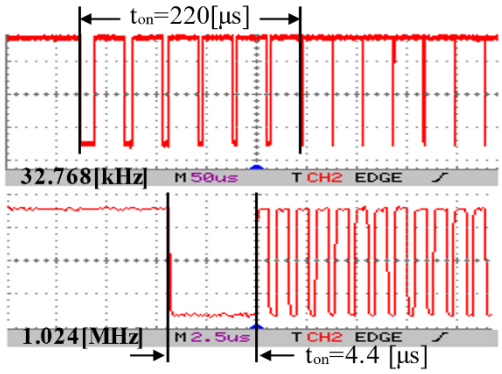

Table 1: Performance summary and comparison

		[19]	[20]	[21]	[22]	**This Work**
Tech (nm)		65	180	65	180	180
Power(µW)		0.92* 12**	750	98.4	43.2	0.33+@32.768kHz 1.5@+1.024MHz
Freq(kHz)		1350	8000	12600	14000	32.768-1024
Area(mm^2)		0.005	1.594	0.01	0.04	0.05
start-up Time (µs)		10	N.A.	N.A.	N.A.	220@32.768kHz 4.4@1.024MHz
start-up Energy (pJ)		120**	N.A.	N.A.	N.A.	72.64@32.768kHz 6.6@1.024MHz
T. Range (°C)		0 to 150	-45 to 85	0 to 80	-40 to 125	-15 to 125++
T. Coeff (ppm/°C)		96	3.85	8200	1900	68.57@32.768kHz 35.714@1.024MHz
V. Range (V)		0.9 to 1.9	1.7 to 2	1.1 to 1.5	1.7 to 1.9	1.1 to 2
V.Stab (%ΔT/V)		0.49	0.18	0.07	0.16	0.5@32.768kHz 10.23@1.024MHz
FOM (nW/kHz)		0.68* 8.89**	93.75	7.8	3.08	10.07+@32.768kHz 1.46+@1.024MHz

* Measured at 0.9V **Measured at 1.4V +Measured at 1.1V

++Simulation T.Range is from -40◦C to 125◦C

The RC oscillator is implemented in a 180nm CMOS GP technology. Fig. 7 shows the layout of the proposed oscillator. Moreover, Fig. 8 illustrates simulation results for the V_C output at worst frequency error corners and typical; guaranteeing a maximum error of 0.98% for all cases. Furthermore, Fig 9 shows the histogram, generated by Montecarlo analysis for both frequencies, where the frequency error is

[19] SAVANTH A., MYERS J., WEDDELL A., FLYNN D., and AL-HASHIMI B., Op. Cit.
[20] GURLEY C. ¨ uk, PEDAL L. ¨ a, SEBASTIANO F., and MAKINWA K. A., Op. Cit.
[21] CAO Y., LEROUX P., COCK W. D., and STEYAERT M. Op. Cit.
[22] TOKUNAGA Y., "An On-Chip CMOS Relaxation Oscillator with Power Averaging Feedback Using a Reference Proportional to Supply Voltage.," pp. 404–406, 2009

0.67% and 1% over 3σ for 32.768 kHz and 1.024MHz respectively. This section also shows post-silicon measurement results for voltage and temperature stability for 32.768kHz and 1.024MHz, and a comparison with state-of-the-art relaxation oscillators as well.

A. Post-silicon voltage stability

Savanth et. al. [23] designs a variable threshold Schmitt trigger which is controlled by a FSM to provide better voltage stability. In contrast, we design a robust Schmitt trigger which threshold is always greater than reference voltage over process and environmental variations. The design is optimal at 32.768kHz, achieving a similar voltage stability as in [24] without the need for a complex control. Fig. 10 shows the results for 32.768kHz and 1.024MHz varying the voltage supply from 1.1 to 2 V. Fig 10a) shows the stability for 32.768kHz where frequency error is less than ±1% for voltage over 1.5V. For voltage supply values less than 1.5 V the SCR reference loses the proportionality, hence, increasing the frequency variation. Fig. 10b) shows a similar behavior for 1.024MHz but with higher variation due to the optimization of threshold at 32.768kHz. However, frequency variation is still near to ±1% from 1.7 to 1.9 volts.

B. Post-silicon temperature stability

As the capacitance of the RC bank is NMOS based, variations over temperature increases comparing to a mim-capacitor implementation. We measure oscillator performance from -15 to 125 ◦C for 32.768kHz and 1.024MHz and using SCR and DREF references. Fig. 11 shows the performance at 32.768kHz at free running and after frequency tuning. The increased sensitivity to temperature mitigates with the tuning feature. Frequency error at high temperatures reduces after tuning, resulting

[23] SAVANTH A., MYERS J., WEDDELL A., FLYNN D., and AL-HASHIMI B., Op. Cit.
[24] Ibíd.

in an average error less than 0.96 %. As expected, DREF reference presents a higher sensitivity under temperature variations.

C. *Post-silicon Transient Behavior and State-of-the-Art Comparison*

Fig. 13 shows a captured transient behavior after activation of the oscillator. Due to a power down condition, the oscillator output establishes in V_{DD} with a steady current about 300nA at 25 ◦C. Once the oscillator activates, settling time for low and high frequency operation corresponds to 220µs and 4.4µs respectively. Table I shows better temperature and voltage coefficients coming from this work, while guaranteeing wideband operation. Also, area is reduced to its minimum even with the absence of mim-capacitors on the design technology.

4. SUMMARY

This paper demonstrated a wide-band relaxation oscillator with robust behavior under voltage supply variations. A Schmitt trigger-based power control loop optimizes error amplifier energy consumption, making the Schmitt trigger the power-hungry block. The oscillator achieves energy efficiency by proper sizing of the Schmitt trigger. Due to the slow slope at Schmitt trigger input, the circuit achieves better efficiency at high frequency. Measurement post-silicon results prove wideband operation in a range of 32.768kHz to 1.024MHz with a power consumption of 0.33µA and 1.5µA respectively. The circuit is fabricated in a 180nm CMOS technology occupying an area of 0.5mm2 and achieving a voltage stability of 0.5%@32.768kHz**.**

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