ON-CHIP POWER SUPPLY VOLTAGE LEVEL MONITORING CIRCUIT.

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RESUMEN

Título: Circuito de monitoreo de voltaje de alimentación On-Chip[1]

Autor:
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Palabras Clave: Monitor de voltaje, Tensión de alimentación, POR, BOD, Circuito integrado, Microelectrónica.

DESCRIPCIÓN

Dentro del grupo de investigación ONCHIP se están desarrollando proyectos de doctorado diseñando circuitos analógicos y digitales como parte de un SoC (*System On Chip*). Uno de los circuitos fundamentales en un SoC es un circuito de monitoreo de voltaje, el cual se encarga de cumplir funciones de inicialización (Al momento de encendido del chip el voltaje en él no es constante) y protección del chip ante caídas de voltaje inesperadas. Este documento presenta el diseño y validación mediante simulaciones (con variaciones de temperatura y proceso) de un circuito de *power on reset* con capacidad de detección de *brown out* a nivel *on-chip* implementado en tecnología CMOS 180nm. El presente diseño (consiste en 4 bloques, el núcleo principal, dos selecciones de nivel y un inversor) ofrece una solución sencilla al problema de *power on* y *brown out reset*, además de la posibilidad de implementación en circuitos *always on* gracias a la facultad de selección de niveles de *brown out.* Además, dos bloques de este diseño pretenden ser implementados como parte del grupo de circuitos *always on* de la segunda versión del micro controlador desarrollado por el grupo de investigación ONCHIP, ocupando un área activa de 84μm x 46μm con un consumo en estado estacionario de 40μA en el peor de los casos.

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[1] Trabajo de Grado

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ABSTRACT

Title: On-chip power supply voltage level monitoring circuit[1]

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Key Words: Voltage monitor, Power supply, POR, BOD, System On Chip, Microelectronics.

DESCRIPTION

Within ONCHIP research group PhD projects designing analog and digital circuits are being developed as part of a SoC (System on Chip). One of the fundamental circuits in a SoC is a voltage monitoring circuit, which is responsible for fulfilling initialization functions (At the time the chip is turned on, the voltage in it is not constant) and protection of the chip from unexpected drops in voltage. This document presents the design and validation through corners simulations (with temperature and process variations) of an on chip power on reset with brown out detection capability circuit implemented on a 180nm CMOS technology. The actual design (consisting of 4 blocks, the main core, two level selectors and a group of inverters) offers a simple solution for the problem of power on and brown out reset, besides the possibility of implementation on always on circuits due to the faculty of selectable brown out reset levels. In addition, as an extension of the project, two blocks of this design pretend to be implemented as part of the always on group of circuits for the second version of the ONCHIP's microcontroller occupying 84μm x 46μm of active area with a static current consumption of 40μA in the worst case.

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[1] Bachelor Thesis

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GENERAL OBJECTIVE

Design of an on-chip voltage level monitoring circuit in 180nm CMOS technology

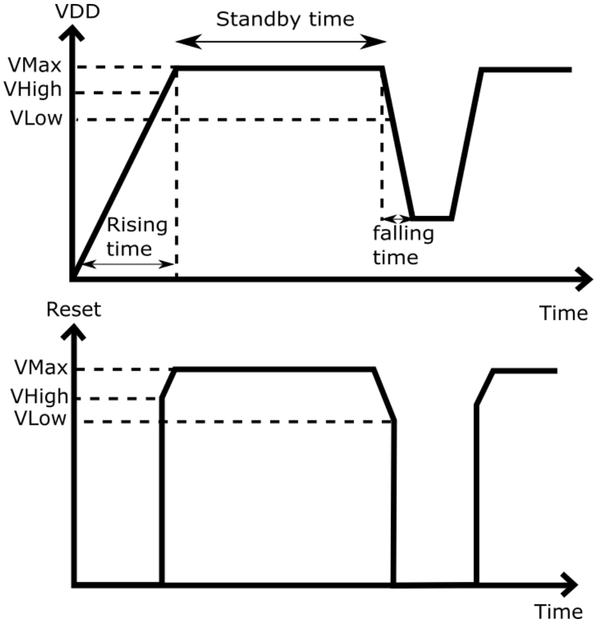
SPECIFIC OBJECTIVES

- Design of a circuit whose current consumption in steady state with active BOD is less than 50μA.
- Reaction to a Brown-out event less than 250μs.
- Different selection possibilities for the Brown-out level (Programmability).

INTRODUCTION

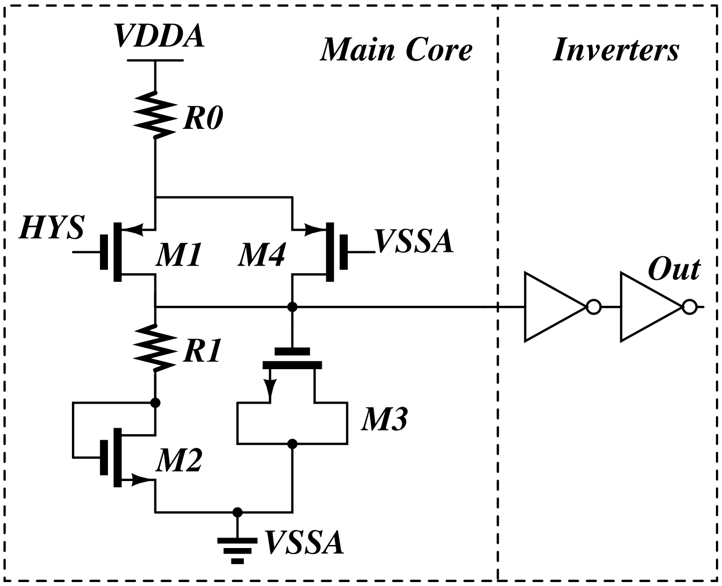
Within ONCHIP's Research group PhD projects designing analog and digital circuits are developed as part of a SoC. A SoC (System on Chip) is the grouping of all the components of an electronic system in a integrated circuit. One of the circuits that composes a SoC is a power supply voltage monitoring circuit, that meets two important applications. First one is POR (Power-on Reset), that is responsible for generating a reset signal during the rise time of the power supply, which is necessary in many digital circuits to define a known initial state, avoiding data corruption and, in turn, an undesired behavior in the SoC; this signal must keep the circuit in reset state until the power supply reaches a minimum voltage level at which this circuits can operate correctly [2]. On the other hand, during normal operation of the SoC it is possible that the supply voltage drops below a level at which the circuits can operate correctly, moving them away from a known value. This event is known as a Brown-out. One of the most common causes is a sudden increase in regulator load. Therefore, in order to avoid unexpected activity and corruption of the data in the core of the system, a BOD (Brown-out Detector) generates a Reset signal to the SoC. Figure 1. shows a representative behavior of the power supply in time with a brown-out event and the desired reset signal. Here, Vmax represents its steady-state value, VHigh, the value where the POR signal shuts off and Vlow, the value where the BOD signal turns on (active low) due to the brown-out event.

Figure 1: Power supply Ramp with brown-out event and Reset signal.



One of the challenges that SoC designers have is energy saving. One way to achieve a consumption reduction is offering different functionalities, which in turn are reflected in a reduction in the number of circuits that remains on. In [2], [7], [4], [6] different proposals that aim to solve the problem of POR and BOD are presented. These architectures present a single level of BOD, this in many applications can be a disadvantage. For example, if the SoC is working at a low power operation level and suddenly changes to working at full power, this sudden change generates a drop in the supply voltage, which if it exceeds the threshold of the BOD, it will immediately place SoC in the reset state, even if the system can operate at this voltage. Another disadvantage is the reduction in the useful life of the batteries, preventing operation in modes that support a voltage below the BOD threshold.

Figure 2: Prior Art.

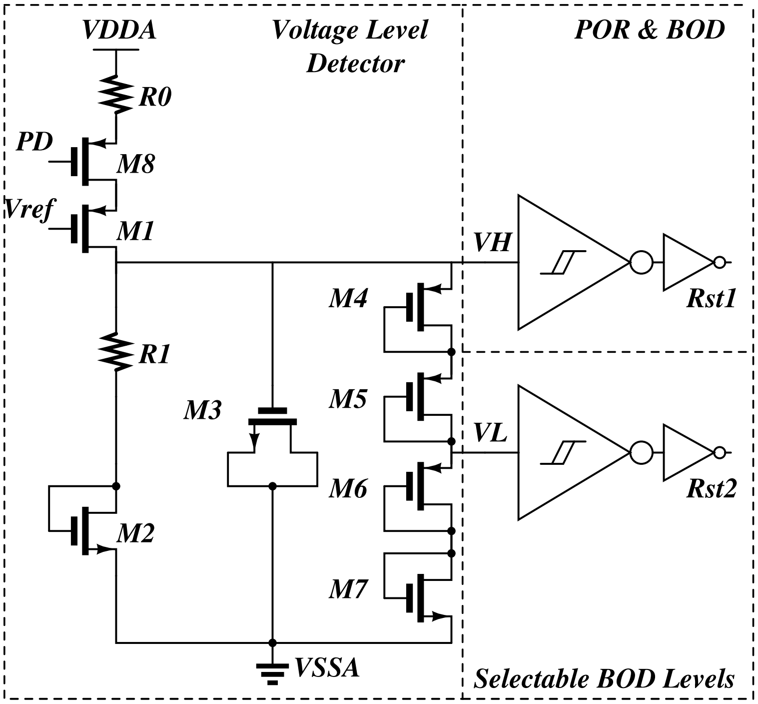


Zolfaghari in [7], presents a simple solution for POR and BOD shown in figure 2. Although a reference input is shown, both (POR and BOR) happen at the same level, also, if a different level is desired, another voltage reference is needed. A POR with BOD capability circuit is designed giving possibility of POR and BOR at different levels with the possibility of threshold selection for giving different levels of power supply operation with a unique voltage reference source.

Chapter 1
PROPOSED ARCHITECTURE

Figure 3 shows the architecture proposed in this work, it is composed by 4 different blocks, the main core which is a voltage level detector, two Schmitt triggers and two inverters. The main core consists of two resistors R_0 and R_1, a PMOS transistor M_1 with its gate connected to V_{ref}, which is a voltage reference signal (which can be delivered by a bandgap reference, or any other voltage reference), an NMOS M_2 in diode connection, a MOS capacitor M_3, and a group of PMOS and an NMOS transistors (M_4 - M_7) connected as a diode.

Figure 3: Proposed architecture for POR with BOD capability.



1.1 OPERATION PRINCIPLE

The operation of the circuit is as follows: At first, when the power is switched on, the supply voltage VDDA rises up as a function of time, and transistor M_1 remains off until its source-gate voltage (V_{GS}) overpasses its threshold voltage (V_{th}); as M_1 is off, the current through the resistor is negligible, so the source voltage of M_1 would be VDDA and its gate voltage would be V_{ref}. M_1 turns on when VDDA$>V_{ref}+V_{th}$. At this point the MOS cap is discharged so VH and VL are 0V, then at the buffers out it will be 0V as well. When VDDA overpasses $V_{ref}+V_{th}$, M_1 turns on and a current starts to flow through R_1, the MOS-capacitor M_3 and the CMOS branch, so V_H and V_L starts to rise. V_L is given by a group of diode-connected MOSFETs used as voltage divider with its bodies connected to source. When V_H overpasses the high trip of the Schmitt trigger it switches from high to low turning on the reset signal.

1.2 VOLTAGE LEVEL DETECTOR DESIGN

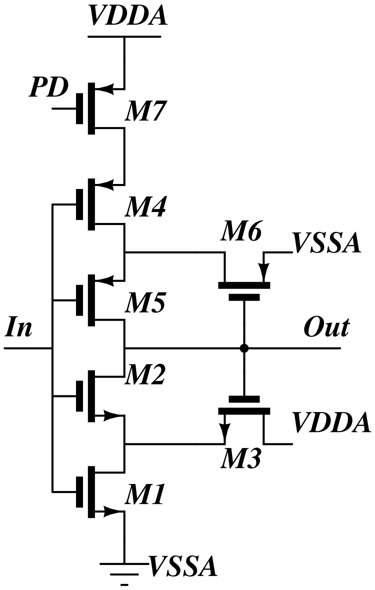
The steady-state current consumption is determined mostly by the R_0, M_1, R_1, M_2 branch. The aspect ratio of M_1 and R_0 can be determined by setting a nominal current consumption in steady-state and selecting a desired value of the voltage on the capacitor at this moment. Selecting a high V_H point, allows a bigger gap between the value of V_{High} and V_{Low} in the Schmitt trigger and so a high POR level. In this case, V_H which is M_1 drain voltage (V_D) is high enough to set M_1 in triode, so the value of R_0 and the aspect ratio of M_1 can be calculated using PMOS triode drain current.

$$I_D = \frac{1}{2}Kn'\frac{W}{L}(V_{GS2} - V_{th})^2 \tag{1.1}$$

Something similar is done for R_1 and M_2, using Kirchoff's law, and matching the current trough M_1 and M_2 (which is the NMOS saturation drain current), as a low current consumption CMOS voltage divider was implemented.

$$I_D = Kp'\frac{W}{L}[(V_{SG1} - |V_{th}|)V_{SD} - \frac{1}{2}V_{SD}^2] \tag{1.2}$$

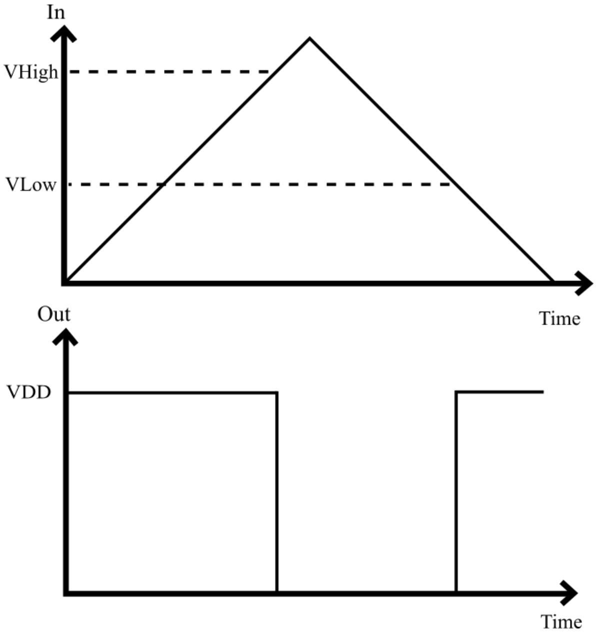
Figure 4: Standar Schmitt trigger.



1.3 SCHMITT TRIGGER DESIGN

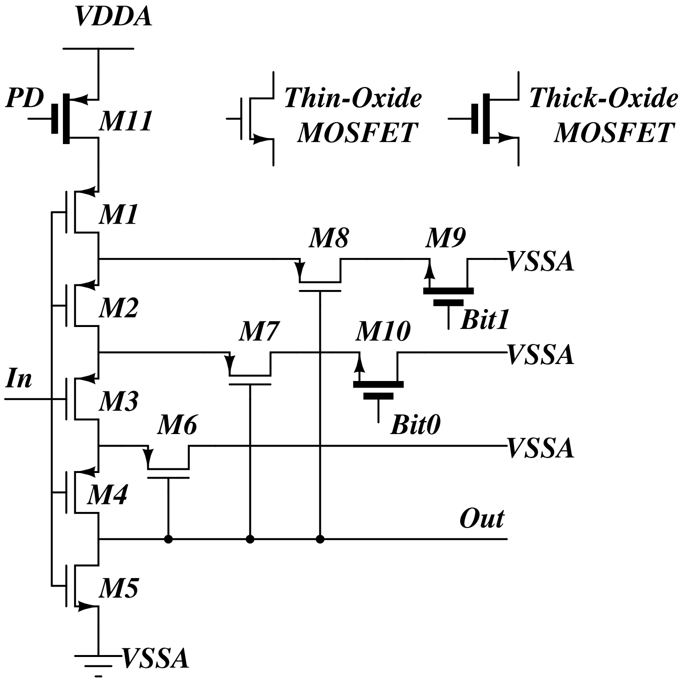
The Schmitt Trigger shown in Figure 4 is designed as a solution for different POR and BOD level, which has the behavior shown in Figure 5.

Figure 5: Schmitt trigger output.



Also, there was an interest on programmability of this last one. Wu in [5], presents a solution for selectable trip points. A preliminary design with three different levels was implemented. In this application VDDA is not a constant value but a falling ramp, causing that V_H falls too. Due to constant time of the RC, V_H falls slower than VDD, so gap between both signals increases as function of time. This difference is used for setting the trip point knowing the value of the supply and the input at the wanted BOD level. This preliminary design was made with thick-oxide MOSFETs because of the 3.3V supply, which restricted the wanted BOD levels, due to its threshold voltage. Figure 6 shows the Schmitt trigger designed in this work with thin-oxide MOSFETs (M_1-M_8) considering its lower threshold voltage compared to the thick-oxide ones, with its input to V_L which is a voltage divider from V_H, this with the idea of increasing the gap between supply and input. Both Schmitt triggers were designed following [1].

Figure 6: Schmitt trigger-based design for variable BOD levels.



The high trip point of the Schmitt trigger can be calculated as follows:

$$\frac{k_1}{k_3} = \left(\frac{VDD - V_{Hi}}{V_{Hi} - V_{TN}}\right)^2 \tag{1.3}$$

where $k_i = 0.5(\mu C_{ox})(W/L)_i$. The low trip point is set using:

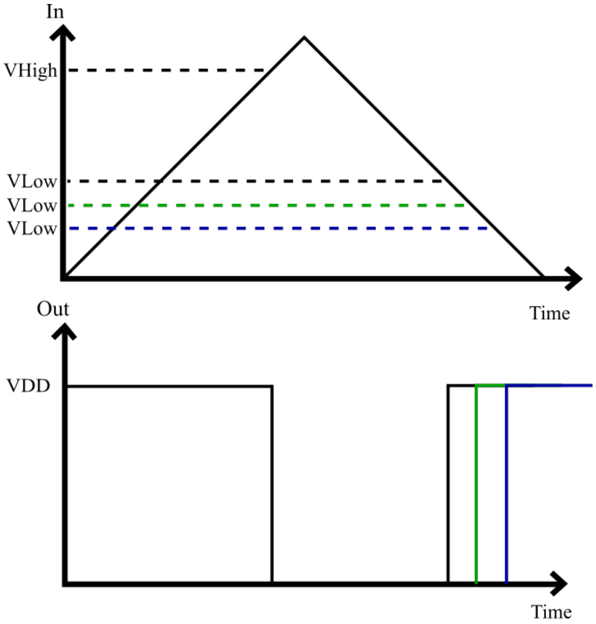
$$\frac{k_4}{k_6} = \left(\frac{V_{Li}}{VDD - V_{Li} - |V_{TP}|}\right)^2 \tag{1.4}$$

The level selection is configured using 1.4. but in this case, for example, if the first level is wanted, bits selection will be 00, thus, M_9 and M_{10} will be off, so k_4 must be the equivalent transistor between M_1, M_2 and M_3. The equivalent transistor can be calculated knowing that it is a self-cascode composite transistor. Its aspect ratio is given by:

$$\left(\frac{W}{L}\right)_{eq} = \frac{m}{m+1}\left(\frac{W}{L}\right)_1 = \frac{1}{m+1}\left(\frac{W}{L}\right)_2 \tag{1.5}$$

The same procedure can be applied for the other two configurations (10, 11). As result, Schmitt trigger shown in Figure 6 has the behavior shown in Figure 7

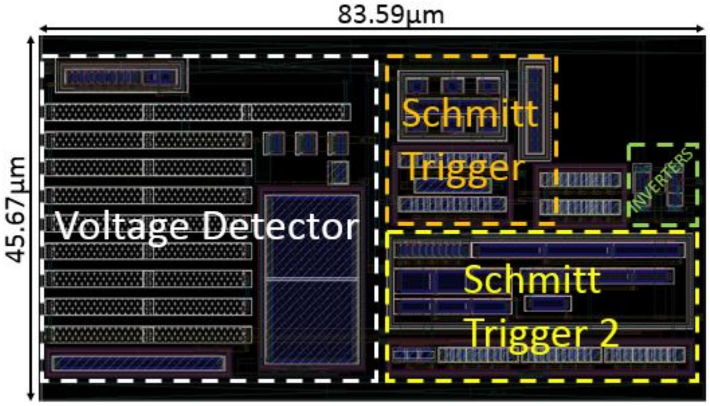
Figure 7: programable Schmitt trigger output.



Chapter 2
POST-LAYOUT RESULTS

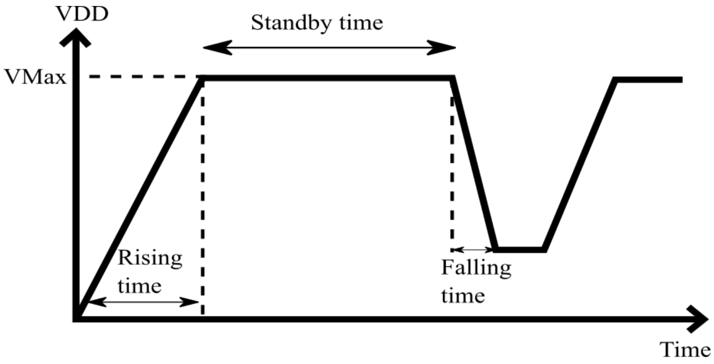
2.1 SIMULATION CONDITIONS

Figure 8: Proposed Layout for the circuit.



The proposed layout for the circuit is shown in Figure 8.

Figure 9: VDD Behavior with brown-out event



The design was tested with corners simulations. VDD was configured in order to have a behavior like the one shown in figure 9 with the following conditions:

Table 1: Simulation Conditions.

Parameter	Conditions	
VDD	23V/ms, -23V/ms for 100us	2.3V/ms, -2.3V/ms for 1ms
Temperature	-40 , 50 , 125	-40 , 50 , 125
NMOS	Slow, Fast	Slow, Fast
PMOS	Slow, Fast	Slow, Fast
Resistors	Low, High	Low, High

2.2 SIMULATION RESULTS

The circuit was extracted at 50°C and submitted to the test bench, figure 10 shows power-on reset signal for 1ms rising time of VDD through different corners with this extracted circuit, VDD is shown as a red line, black lines are different corners, and the blue one is the nominal corner.

Figure 10: post-layout's POR signal for 100μs VDD rising time.

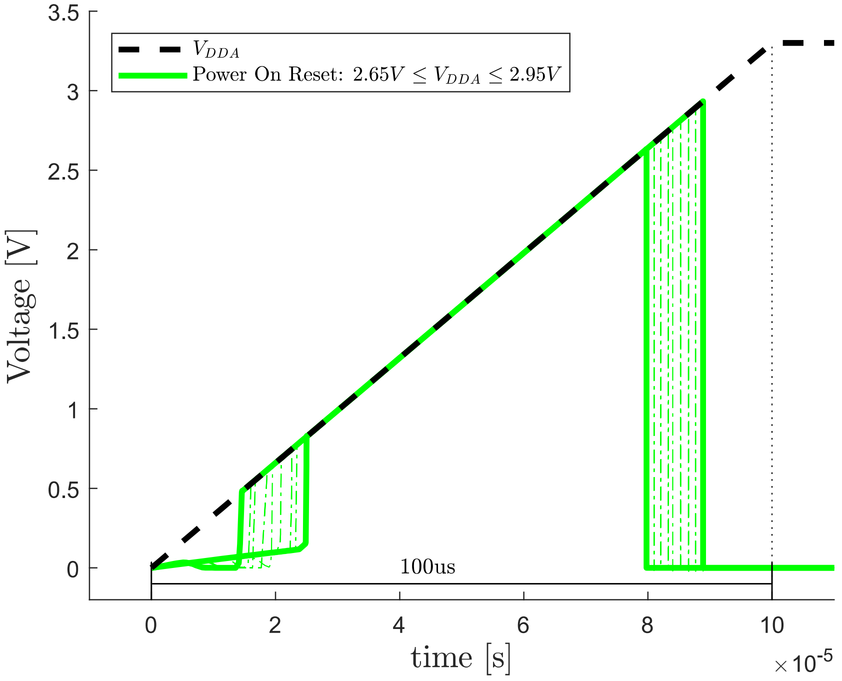


Figure 11 shows the different levels at which the reset becomes active at a 100μs falling time of VDD (Brown-out event),where thin lines show the excursion trough corners simulation, while thicker lines represents nominal values for each configuration, Table 2 presents simulation results for Power-on reset, different brown-out levels and current consumption of the entire circuit showing minimum, nominal and maximum value.

Figure 11: post-layout's BOD signals for different Bit configuration (BC) and 100μs VDD falling time.

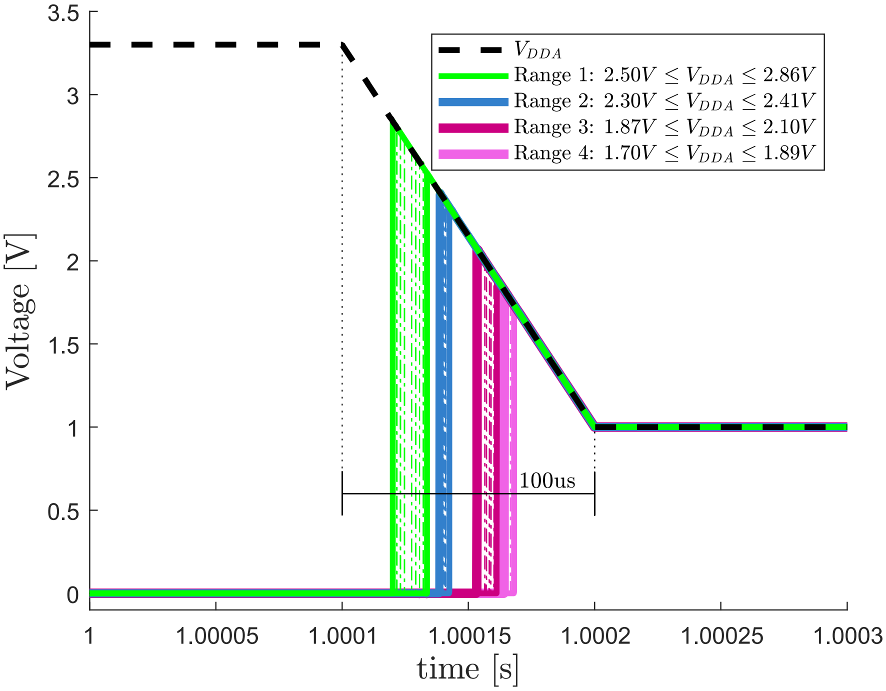


Table 2: Simulation Results.

Parameter	Description	Min	Nom	Max	Unit	Cond.
POR	100μs rising time	2.65	2.78	2.95	V	
	1ms rising time	2.6	2.74	2.92	V	
BOD	100μs rising time	2.54	2.67	2.85	V	BC=xx
		2.25	2.27	2.39	V	BC=00
		1.82	1.83	1.93	V	BC=10
		1.66	1.66	1.76	V	BC=11
	1ms rising time	2.57	2.7	2.87	V	BC=xx
		2.36	2.41	2.46	V	BC=00
		1.9	1.98	2.26	V	BC=10
		1.74	1.8	2.16	V	BC=11
IDD$_{SC}$	Static current consumption	13.67	17.15	23.73	μA	BC=00
		18.62	23.10	32.03	μA	BC=10
		24.38	29.6	40.03	μA	BC=11
IDD$_{PD}$	Static current after POR with active Power Down	0.22	0.37	2	nA	

Chapter 3
STAND-ALONE POR APPLICATION

The Voltage level detector and the Schmitt trigger alongside a variable voltage reference source designed inside the research group by a PhD student, were tested in a stand alone POR circuit that can be seen in figures 12 and 13, which will be manufactured as part of the second version of ONCHIP's microcontroller. Results for different rising times as well as current consumption for this circuit are consigned in Table 3

Figure 12: Layout of stand-alone POR for ONCHIP's project with active are of 83μm x 68μm.

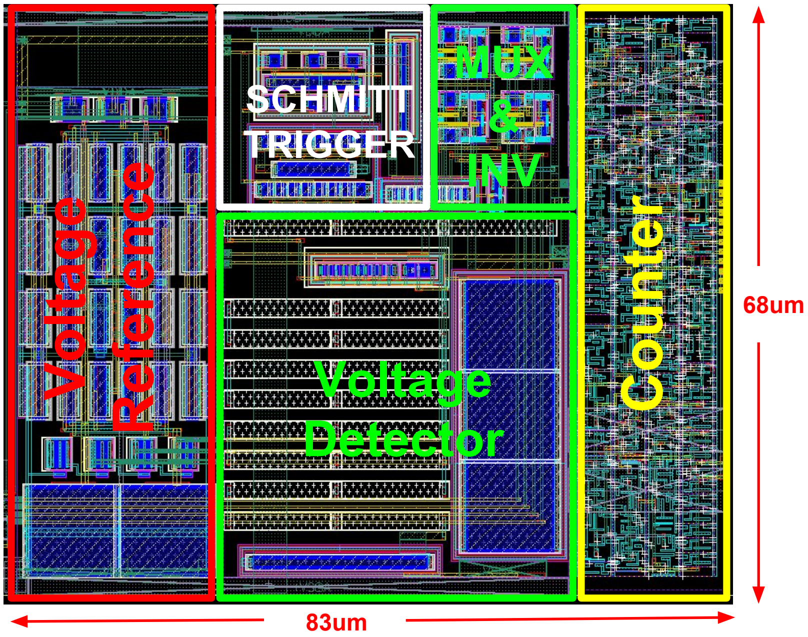


Figure 13: Proposed architecture for stand-alone POR.

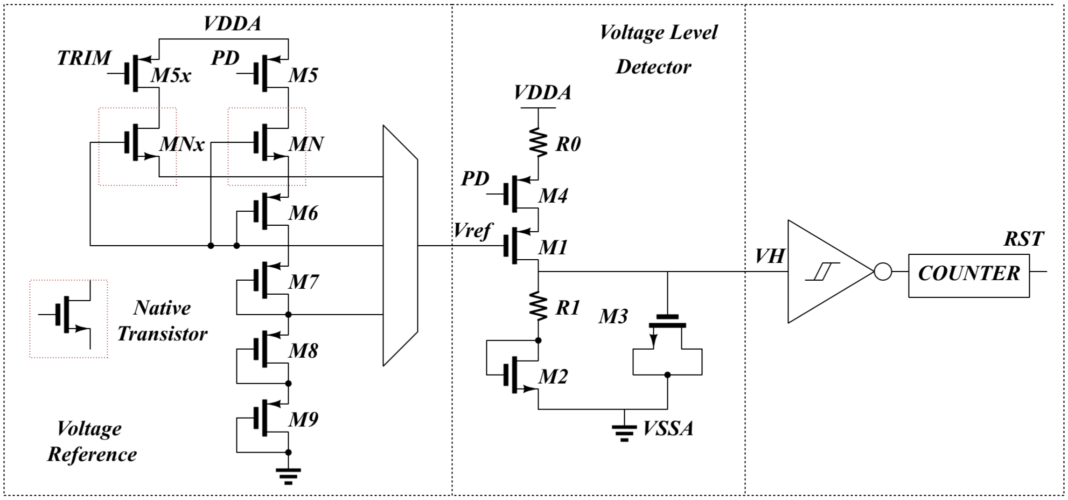


Table 3: Simulation Results of stand-alone POR.

Parameter	Description	Min.	nominal	Max.	Unit	Conditions
POR	1μs rising time	2.032	2.304	2.678	V	Vref(3)
		1.782	1.949	2.081	V	Vref(2)
		1.851	2.239	2.407	V	Vref(1)
	10μs rising time	1.701	1.952	2.602	V	Vref(3)
		1.377	1.46	2.02	V	Vref(2)
		1.365	1.621	1.773	V	Vref(1)
	100μs rising time	1.621	2.093	2.449	V	Vref(3)
		1.206	1.448	1.973	V	Vref(2)
		1.106	1.356	1.511	V	Vref(1)
	1ms rising time	1.531	2.239	2.333	V	Vref(3)
		1.078	1.803	1.861	V	Vref(2)
		0.806	1.209	1.348	V	Vref(1)
	50ms rising time	1.799	2.231	2.5	V	Vref(3)
		1.112	1.79	1.958	V	Vref(2)
		2.89m	0.853	1.473	V	Vref(1)
IDD_{SC}	Static current Consumption	4.708	6.965	11.33	μA	
IDD_{PD}	Supply current after POR with active Power Down	0.164	9.68	640.7	nA	

CONCLUSIONS

An on-chip power on reset circuit with selectable brown-out detection has been designed in a 180nm CMOS technology, the results show a fast POR and a BOD response, with less than 400mV excursion and a current consumption of less than 50μA in the worst case. The possibility of different BOD levels allows this design to be part of always-on circuits. An active area of 84μm x 46μm was used. In addition to this design a stand-alone POR circuit was implemented with integrated voltage reference signal with the capacity of tracking and respond to a VDD ramp up to 1μs rising time with an active area of 83μm x 68μm

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