A DIGITAL LOW-DROPOUT REGULATOR FOR LOW-SUPPLY VOLTAGE OPERATION

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RESUMEN

TITULO: Regulador de Baja Caída de Tensión para Aplicaciones de Bajo Voltaje[*].

AUTOR: Gabriel Steven Romero Rondón [**]

PALABRAS CLAVE: Regulador de baja caída de tensión, regulador de tensión con lógica digital, comparadores, reloj autogenerado, celdas digitales estándar

DESCRIPCIÓN

Las aplicaciones de sistemas integrados o sistemas en chip (SoC) con limitaciones en el presupuesto de energía requieren que sus circuitos trabajen a la mínima tensión de alimentación posible. SoC típicos utilizan reguladores de baja caída de tensión (LDO) analógicos, pero el amplificador de error en un LDO analógico implica que la tensión mínima de entrada tiene que ser mayor. Los LDO digitales (D-LDO) han surgido como una alternativa para la conversión de voltaje debido a que pueden operar a tensiones más bajas que sus contrapartes analógicas. Sin embargo, los D-LDOs poseen un bajo desempeño ante eventos transitorios, como caídas de tensión. Para mejorar esta respuesta transitoria, algunas soluciones proponen incrementar de forma indiscriminada la frecuencia de operación del D-LDO, pero esto aumenta significativamente el consumo de potencia. Para atacar este vínculo entre la velocidad y el consumo de potencia, en este trabajo se propone un LDO completamente digital que implementa un reloj autogenerado. El D-LDO propuesto se compone únicamente de celdas digitales estándar, esto permite que el diseño sea escalable en cuanto a proceso, voltajes de entrada y voltajes de salida. Los resultados obtenidos demuestran mejoras en la respuesta transitoria cuando se comparan con soluciones previas que utilizan una frecuencia externa de reloj similar a la utilizada en este diseño. La salida de este circuito cae 150mV cuando ocurre un salto de corriente que va desde 1mA hasta 20mA en un tiempo de 400ns (@CLOAD = 10pF) y exhibe una eficiencia máxima de corriente de 96.2%. El regulador propuesto ocupa un área de 0.029mm^2 en una tecnología estándar CMOS de 180 nanómetros.

[*] Proyecto de grado

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ABSTRACT

TITLE: A Digital Low-Dropout Regulator for Low-Supply Voltage Operation[*].

AUTHOR: Gabriel Steven Romero Rondón [**]

KEYWORDS: Low-dropout regulator, continuous comparator, dynamic comparator, self-generated clock, standard cells

DESCRIPTION

System-on-chip (SoC) applications with limited power budget require circuits to work at their minimum operating supply voltage. Typical SoC utilizes analog low-dropout (ALDO) regulators as its voltage converter, but the error amplifier in the A-LDO entails a higher constraint in the lowest supply voltage. Digital low-dropout (D-LDO) regulators have emerged as an alternative voltage converter due to their lower operating-voltage limit. However, D-LDOs have demonstrated poor response during transient events, such as voltage drops. To enhance the transient response, common solutions indiscriminately increase the D-LDO operating frequency, leading to higher power consumption. To address the power-speed trade-off, we propose a fully-digital LDO implementing a self-generated clock. The proposed D-LDO is composed exclusively by digital standard cells, this feature enables the voltage and process scalability of this design. Our results show transient response improvements compared to prior solutions utilizing similar external-clock frequencies. The output voltage drops 150mV with a 400ns load current step from 1mA to 20mA (@CLOAD = 10pF) and exhibits a maximum current efficiency of 96.2%. The proposed regulator occupies an area of 0.029mm^2 in a 180-nm CMOS standard technology. This fully-standard cell design can be replicated in order to meet the different specifications for ultra-fine-grained applications in SoCs implemented in different technologies

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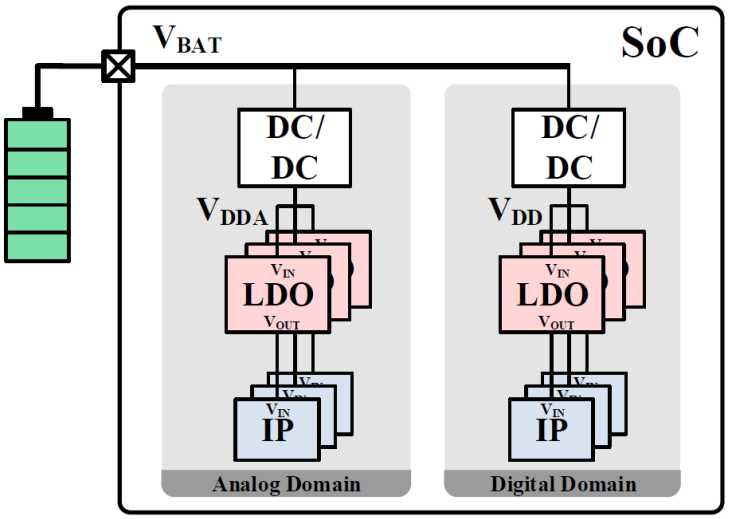
INTRODUCTION

Energy efficiency is one of the most relevant constraints in battery-powered applications, such as internet-of-things (IoT). Modern solutions to power saving problems exploit the dynamic power consumption (*P*) dependence on the supply voltage (*V*): $P \propto V^1$. Multiple voltage domain strategies properly scale the supply voltage to achieve power-saving without affecting circuits with high-yield requirements. Fig. 1 represents the power distribution in a system-on-chip (SoC) with several voltage domains. Without loss of generality, a battery supplies the SoC. As shown, a set of low-dropout (LDO) regulators establishes the supply voltage of each intellectual property (IP) circuit at a value lower than V_{DD} or V_{DDA}.

Figure 1. Multiple voltage domains achieved by several LDOs in an SoC.

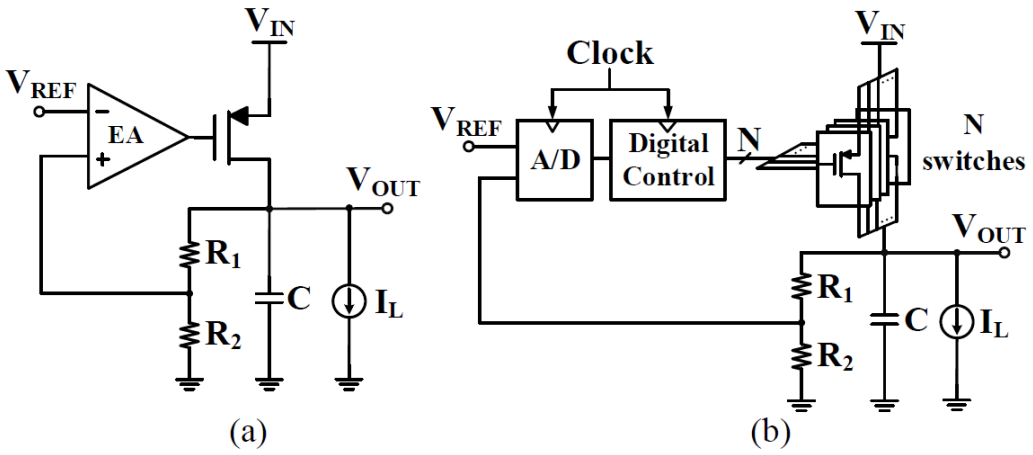


Although conventional analog LDO (A-LDO) regulators meet the requirements for voltage conversion in multi-voltage-domain approaches, their performance drops

[1] RABAEY J. M., CHANDRAKASAN A. P., and BORIVOJE, N. *Digital integrated circuits: a design perspective*. PHI Learning Private Limited, 2013

when the input voltage is scaled down. Fig. 2 (a) depicts a typical circuit representation of an A-LDO. An error amplifier (EA) drives the PMOS transistor gate to achieve the desired output voltage. The EA driving capability relies upon its high gain, which directly depends on the supply voltage value. Achieving a high gain becomes more difficult as VIN decreases. Then, a low-gain EA impacts adversely on the stability margin and response time of A-LDOs [2]. Digital LDO (D-LDO) regulators, broadly represented in Fig. 2 (b), are an emerging solution to address the mentioned issues. In D-LDOs, the EA is replaced by an analog-to-digital (A/D) converter and a digital controller. The possibility of using low voltage A/D converter topologies and low voltage digital controllers entails that D-LDOs are more suitable for low supply voltage operation. Besides, the usage of a digital core adds two relevant features: easier programmability and process scalability. Hence, D-LDOs design is more flexible, and it can be effortlessly replicated.

Figure 2. (a) Conventional A-LDO architecture. (b) Typical block diagram of D-LDO.



[2] KUNDU S., LIU M., S. WEN *et al.*, "A Fully Integrated Digital LDO With Built-In Adaptive Sampling and Active Voltage Positioning Using a Beat-Frequency Quantizer," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 1, pp. 109–120, Jan 2019

However, conventional reported D-LDOs are either slow or power-hungry [3]. This trade-off exists because DLDOs need higher clock frequencies for a fast drop/overshoot response. The high-frequency clock causes a significant growth in power consumption, decreasing the efficiency of the regulator.

Recent literature reports significant progress in overcoming the power-speed trade-off in D-LDOs by adding an analog loop in parallel to the digital logic [4] [5] [6] [7]. Nevertheless, these approaches increase the design difficulty and lose the process scalability feature. In [8], Huang et al. overcome the speed difficulty by switching to a high-frequency clock during under/overshoot events. However, this design still requires a fast-external clock that operates continuously. Thus, the power losses of the regulator are still considerable. Another promising way to address the power-speed trade-off consists of generating the clock inside the D-LDO. Kundu et al. [9] propose a voltage-controlled oscillator (VCO) as A/D converter. The VCO is used in such a way that the frequency intrinsically increases when the output voltage is far from the desired value. However, this D-LDO consumes a high amount of power due to the power-starving VCOs. Following a similar idea, Akram et al. [10] proposed a self-clocked D-LDO, but their system relies on comparators that respond slowly to voltage variations. This problem can lead to stability issues within the regulator.

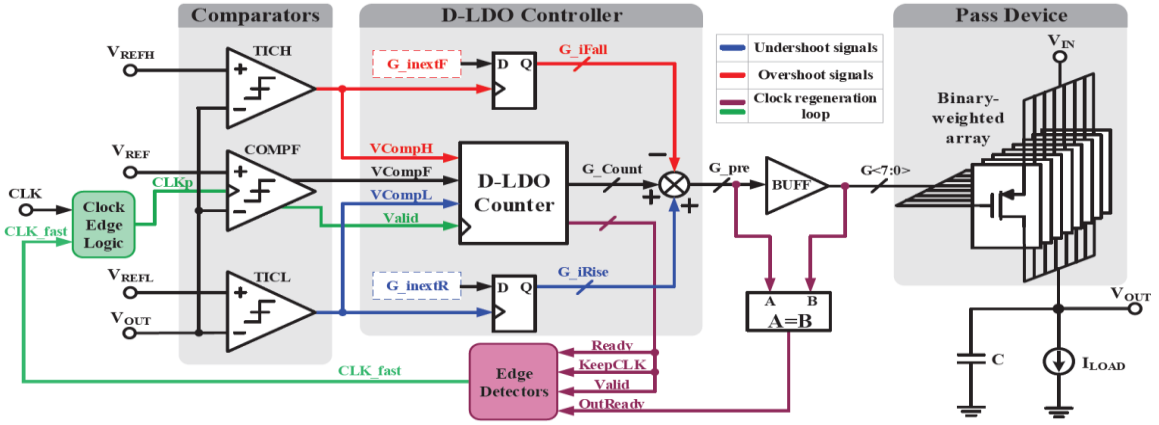
[3] MA X., LU Y., MARTINS R. P. et al., "A 0.4V 430nA quiescent current NMOS digital LDO with NAND-based analog-assisted loop in 28nm CMOS," in 2018 IEEE International Solid - State Circuits Conference- (ISSCC), Feb 2018, pp. 306–308
[4] Ibíd.
[5] HUANG M., LU Y., S. U et al., "An Analog-Assisted Tri-Loop Digital Low-Dropout Regulator," IEEE Journal of Solid-State Circuits, vol. 53, no. 1, pp. 20–34, Jan 2018
[6] NASIR S. B., SEN S., and RAYCHOWDHURY A., "Switched-Mode-Control Based Hybrid LDO for Fine-Grain Power Management of Digital Load Circuits," IEEE Journal of Solid-State Circuits, vol. 53, no. 2, pp. 569– 581, Feb 2018
[7] WANG X. and MERCIER P. P., "A Charge-Pump-based Digital LDO Employing an AC-Coupled High-Z Feedback Loop Towards a sub-4fs FoM and a 105,000x Stable Dynamic Current Range," 2019
[8] HUANG M., LU Y., SIN S. et al., "A Fully Integrated Digital LDO With Coarse Fine-Tuning and Burst-Mode Operation," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 63, no. 7, pp. 683–687, July 2016
[9] KUNDU S., LIU M., S. WEN et al., Op. Cit.
[10] AKRAM M. A., HONG W., and HWANG I., "Capacitorless Self-Clocked All- Digital Low-Dropout Regulator," IEEE Journal of Solid-State Circuits, vol. 54, no. 1, pp. 266–276, Jan 2019

In this paper, a fully-digital LDO is implemented using only standard-cells. We counteract the power-speed trade-off by using a self-generated clock that works only in voltage drop/overshoot events. The self-generated clock considers the critical path of the D-LDO logic before creating a new clock edge. In this way, the regulator avoids metastability states during its operation. Besides, for breaking the dependence on the external clock frequency, an event-driven logic is used. All the circuits comprising the regulator are synthesizable, which implies that the circuit can be represented by a hardware description language (HDL).

1. D-LDO PROPOSED ARCHITECTURE

The proposed D-LDO architecture (Fig. 3) includes two feedback loops. The main loop resembles the typical D-LDO block diagram of Fig. 2 (b), where V_{OUT} is connected to an A/D converter. In the proposed D-LDO, the A/D converter consists of three voltage comparators. Once in the digital domain, the D-LDO controller adjusts its output according to the discretized V_{OUT}. The purpose of the main loop is turning on the appropriate number of transistors in the pass device for providing the corresponding load current while maintaining V_{OUT} close to the desired voltage (V_{REF}). The second loop corresponds to the clock regeneration loop. The signals composing this loop are particularly relevant when V_{OUT} is far from V_{REF}. In that event, this loop generates a high-frequency clock for fastly recover V_{OUT} back to V_{REF}. Once V_{OUT} approaches V_{REF}, the regulator works at the frequency of the external clock (CLK) again.

Figure 3. Proposed D-LDO architecture.



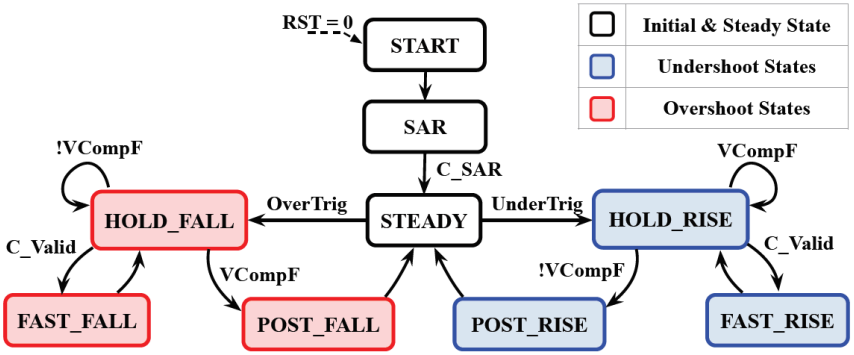
In the main loop, D-LDO architecture includes three voltage comparators. COMPF is a NAND-based clocked comparator (section II-A) responsible for the comparison between V_{OUT} and V_{REF}. After the rising edge of CLKp arrives, Valid signal indicates

when the output of the comparator is ready to be sampled. TICH and TICL are threshold inverter comparators (section II-B). They respond when V_{OUT} crosses V_{REFH} and V_{REFL}, to enable the fast recovery mode of the regulator. For the target application V_{REFH} = 980mV, V_{REF} = 900mV and V_{REFL} = 820 mV.

The controller and the pass device are also part of the main loop of the regulator. In the controller, the D-LDO Counter comprises a Finite State Machine (FSM) that determines the operating mode of the regulator. The external D-Flip-Flops are used when V_{OUT} is out of the boundaries set by V_{REFL} and V_{REFH}. G_pre is the 8-bit output of the controller; this signal is buffered for reducing the propagation delay between G_pre and G<7:0>. Finally, the value of G establishes the number of turned-on devices in the pass device.

Fig. 4 depicts the state diagram of the FSM in the proposed D-LDO. The states START, SAR and STEADY correspond to the start-up and the steady-state operation of the regulator. During these operating modes, the external clock controls the comparator, and the circuit works in low-power mode. Also, the states that represent the fast recovery mode in an under- shoot event are {HOLD, FAST, POST}_RISE, while the states for an undershoot event are {HOLD, FAST, POST}_FALL.

Figure 4. State diagram of the FSM in the D-LDO Counter.



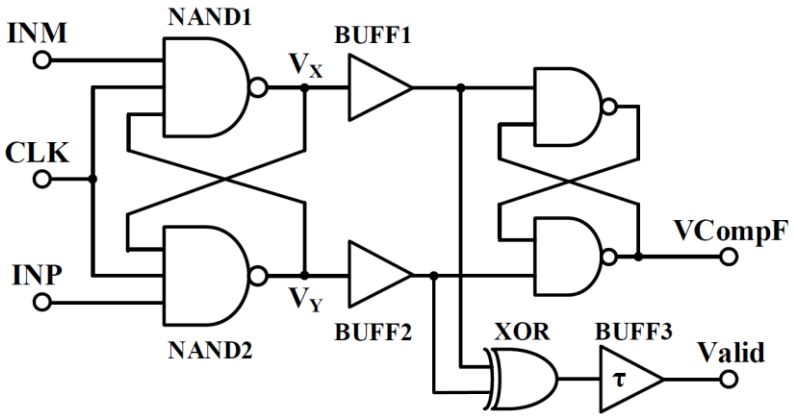
During the SoC start-up sequence, the FSM is set to START state. At the next rising edge of Valid signal, the D-LDO begins its SAR mode. In the SAR state, D-LDO logic implements a successive approximation algorithm that searches for the appropriate digital word (G<7:0>). The application of the algorithm takes eight clock cycles because each bit of the 8-bit controller establishes after each cycle. Then, C_SAR goes high, and the regulator starts its steady-state operation. During STEADY state, the D-LDO Counter output increases or decreases by one according to VCompF value. If VcompF is low, the controller turns off one transistor, if VcompF is high, then it must turn on one transistor.

Hitherto, the digital word G<7:0> is controlled only by the D-LDO Counter, but once an undershoot (overshoot) event occurs, the response of the comparator sets the value of G_iRise (G_iFall) to G_inextR (G_inextF). G_inextR and G_inextF are calculated in a way that the change in G<7:0> counteracts the voltage variation in the output and tries to set it at the reference value again. Besides, the edge of VCompL (VCompH) sets the FSM input UnderTrig (OverTrig) to high and enables the clock regeneration loop. At the next clock edge, the FSM goes to HOLD state. In this state, the FSM resets the external D-Flip-Flops and the value of G_Count is updated, so G_pre remains constant. The purpose of the reset is giving the full control of G<7:0> to the D-LDO Counter. While in HOLD state, if VCompF is low (high), the regulator has successfully recovered, then, the FSM goes to POST state. Conversely, if VCompF is held constant, the FSM stays in HOLD state until the counter output, C_Valid, is high. This counter avoids fast changes in the D-LDO since V_{OUT} has to settle to its final value. Thus, the D-LDO logic waits for a specific number of clock edges before adding (or subtracting) G_inextR (G_inextF) to G_Count again; this operation occurs in FAST state. After performing a new change in G_Count, the FSM returns to HOLD. The loop between these two states continues until VCompF changes, and the FSM goes to POST state. This state is useful for resetting several signals. After one Valid edge, the FSM returns to STEADY state and keeps working in low-power mode.

1.1 NAND-BASED CLOCKED COMPARATOR

A digital standard cell is a predefined block that has fixed size and functionality, for instance, a NAND gate [11]. The layout of a standard-cell is designed with standard locations of V_{DD} and GND. Hence, the design is easily portable from one technology to another. In this context, we adopt the NAND-based clocked comparator of Fig. 5, proposed by Weaver et al. [12]. The current design also includes an XOR-gate for the generation of Valid signal that indicates when the output of the comparator is ready to be sampled.

Figure 5. NAND-based clocked comparator.



In the NAND-based clocked comparator, when CLK is low, the voltage at nodes V_X and V_Y is set to V_{DD}. Here, Valid is low, and VCOMP holds its previous state. Once CLK goes high, INP and INM start discharging nodes V_X and V_Y. These voltages are also inputs of the 3-in NAND gates to form a latch and get V_X and V_Y to their final states. For instance, if INP is higher than INM, and CLK is high, V_Y discharges faster than V_X, then, V_Y crosses the threshold of NAND1 and sets V_X to high; while V_Y

[11] KAHNG A. B., LIENIG J., MARKOV I. L. et al., VLSI physical design: from graph partitioning to timing closure. Springer., 2011, pp. 12–14

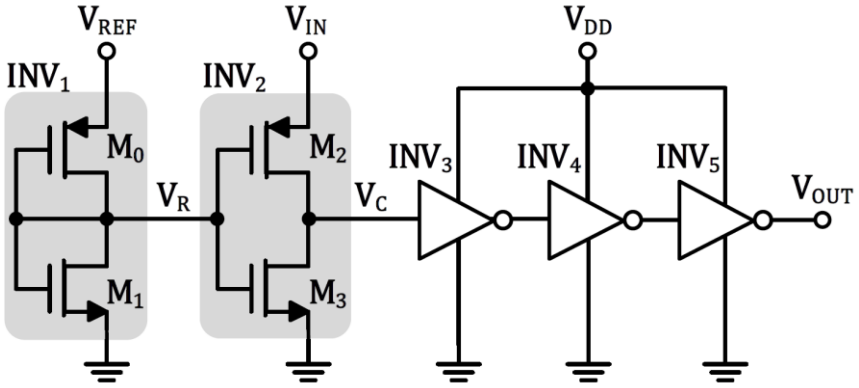
[12] WEAVER S., HERSHBERG B., and MOON U., “Digitally Synthesized Stochastic Flash ADC Using Only Standard Digital Cells,” IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 61, no. 1, pp. 84–91, Jan 2014

keeps falling to GND. Then, VCompF is high and, τ seconds later (the delay of BUFF3), Valid is high.

1.2 THRESHOLD INVERTER COMPARATOR

Several state-of-the-art D-LDOs only use dynamic comparators as their A/D converter [13]. The main reason for avoiding continuous comparators is due to their static power consumption. Recently, based on [14], Abrar et al. [15] proposed a logic-threshold-based comparator. However, their comparator performs poorly when one of the inputs is low. To overcome this issue, we propose the threshold inverter comparator (TIC) of Fig. 6. In this case, when V_{IN} is low, V_{OUT} is intrinsically set to high, thus, overcoming the start-up issue. The usage of the TIC as the continuous comparator significantly reduces the design complexity and enables the possibility of a synthesizable comparator.

Figure 6. Modified threshold inverter comparator.



[13] MA X., LU Y., MARTINS R. P. et al., Op. Cit.
[14] TANGEL A. and CHOI K., "The CMOS Inverter as a Comparator in ADC Designs," Analog Integrated Circuits and Signal Processing, vol. 39, no. 2, p. 147155, 2004
[15] AKRAM M. A., HONG W., and HWANG I., "Fast Transient Fully Standard- Cell-Based All Digital Low-Dropout Regulator With 99.97% Current Efficiency," IEEE Transactions on Power Electronics, vol. 33, no. 9, pp. 8011–8019, Sep. 2018

The operating principle of the proposed comparator relies on the V_{SG} of transistor M_2. When V_{IN} is higher than V_{REF}, transistor M_2 is turned on and V_C is set to V_{IN}, then, the output inverters set V_{OUT} to GND. In contrast, when V_{IN} is lower than V_{REF}, M_2 is turned off and M_3 sinks V_C to GND; then, V_{OUT} is established to V_{DD}.

From [16], the voltage at node V_R corresponds to a scaled version of V_{REF}.

$$V_R = \frac{V_{REF} + \left(\sqrt{\frac{\beta_{n1}}{\beta_{p0}}} \cdot V_{THN_1} - V_{THP_0}\right)}{1 + \sqrt{\frac{\beta_{n1}}{\beta_{p0}}}} \quad (1)$$

Where $\beta_n = \mu_n \cdot C_{OX} \cdot \frac{W}{L}$ and $\beta_p = \mu_p \cdot C_{OX} \cdot \frac{W}{L}$

The switching point of INV_2 occurs when V_R equals V_C. In such case, V_R is also defined by equation (1) but with the appropriate variables for INV_2. These two equations of V_R can be solved for finding the value of V_{IN} that changes the comparator output. Under the assumption that the aspect ratio between NMOS ($M_{1,3}$) and PMOS ($M_{0,2}$) transistors is the same in both inverters, solving both for V_{IN} results in (2).

$$V_{IN} = V_{REF} + V_{THN_1}\sqrt{\frac{\beta_{n1}}{\beta_{p0}}} - V_{THN_3}\sqrt{\frac{\beta_{n3}}{\beta_{p2}}} + \Delta V_{THP} \quad (2)$$

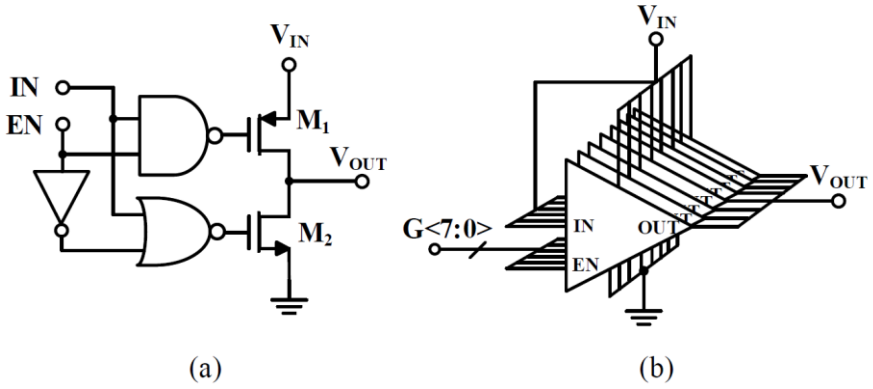
Where $\Delta V_{THP} = V_{THP_2} - V_{THP_0}$ Equation (2) suggests that inverters INV_1 and INV_2 should be the same size and the same V_{TH} to reduce the offset of the comparator.

[16] BAKER R. J., *CMOS: circuit design, layout, and simulation*. IEEE Press, 2010, pp. 331–335

1.3 TRI-STATE BUFFER AS PASS DEVICE

Traditional D-LDOs employ either NMOS or PMOS transistors as their pass device. However, the usage of non-standard format devices opposes to one of the main advantages of D-LDOs: the ease of portability. Then, it would be useful if a standard cell gate could serve as the pass device. The first idea would be to use one of the most basic gates: the CMOS inverter. But, in the inverter, if the PMOS transistor is turned off, then the NMOS transistor inevitably turns on and sinks current from the output. The need for a third state between high and low leads to the tri-state buffer (Fig. 7 (a)). If EN is low, then the buffer output is high impedance (hi-Z) regardless of the value of IN. When EN is high, IN turns on either M_1 or M_2 and the output is connected to V_{IN} or GND.

Figure 7. (a) Tri-state buffer schematic. (b) Buffers connected as pass devices in D-LDO.



The implementation of this buffer as the pass device has two significant advantages: First, the D-LDO design is now fully synthesizable and easily portable. Second, the transistor M_2 can be used when required. For instance, when the load current decreases, instead of only turning off the PMOS transistors, the NMOS transistors can be accordingly turned on to counteract the load current decrease. In this version of the D-LDO, the second advantage of the tri-state buffers is not exploited. Thus,

for switching the output of the buffers from high to hi-Z, they are connected to G<7:0> as Fig. 7 (b) shows.

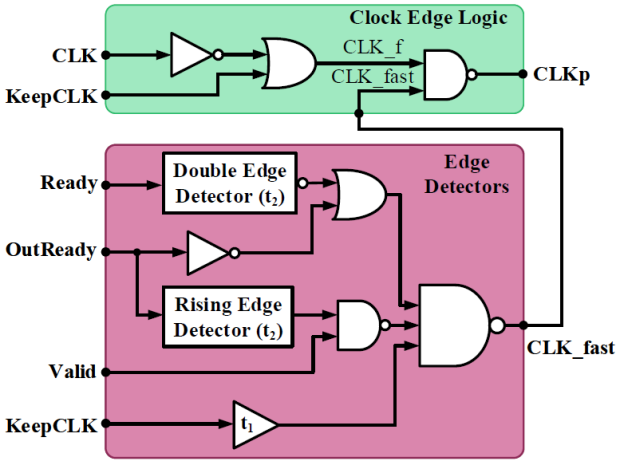
2. CLOCK REGENERATION LOOP

This section focuses on the details of the blocks comprising the clock regeneration loop. A timing diagram describes the behavior of the clock regeneration loop during fast recovery mode. We also theoretically explain how to calculate the values of the gain in fast recovery mode (G_inextF and G_inextR) for improving the transient response while avoiding instability.

2.1 EDGE DETECTORS AND CLOCK EDGE LOGIC

The self-generated clock is the result of a feedback loop that creates glitches at the input of the NAND-based comparator. Fig. 8 presents the two main blocks of the clock regeneration loop. These blocks are in charge of creating glitches (Edge Detectors) and switching between the external clock and the self-generated clock (Clock Edge Logic).

Figure 8. Circuit diagram of Clock Edge Logic and Edge Detectors for clock regeneration.

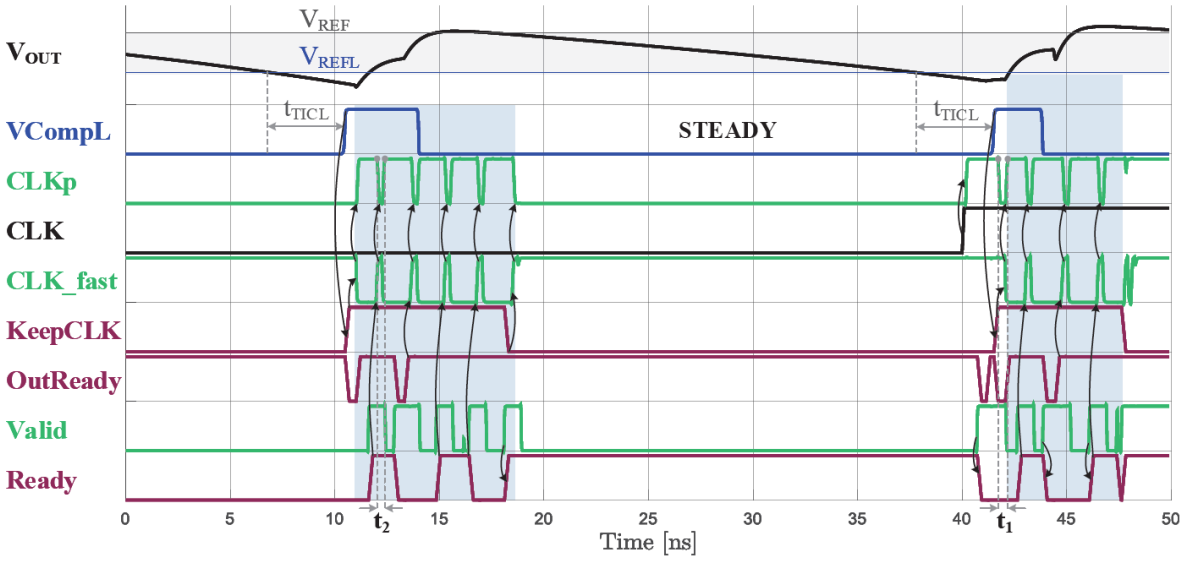


The glitches are generated considering the critical path of the D-LDO. The signal Ready corresponds to the output of a T-Flip-Flop in the D-LDO Counter. On the other hand, OutReady is the output of a comparator between G_pre and G. The Edge Detectors block uses Ready and OutReady to create a glitch when the last of these signals settles. In this way, the regulator avoids metastability in the digital controller. The duration of the glitch generated by Ready or OutReady is t_2, during this time, CLKp is low, and the NAND comparator is reset.

A significant feature of Clock Edge Logic is the ability to boost the frequency of CLKp regardless of the CLK signal value. The signal KeepCLK is high when either VCompL or VCompH changes and is reset when the FSM is in POST_STATE. KeepCLK filters the value of the external clock, and the result is the signal CLK_f. The delay applied to KeepCLK (t_1) in the Edge Detectors creates a glitch that stimulates the NAND comparator.

Fig. 9 depicts the waveforms of the clock regeneration loop during an undershoot event. While the circuit is working in steady-state mode, KeepCLK is low, maintaining CLK_fast in a high state; hence, CLKp has the same form of the external clock (CLK). t_{TICL} seconds after V_{OUT} gets below V_{REFL}, VCompL rises and sets KeepCLK to high. Then, t_1 seconds after the rising edge of KeepCLK, CLKp is high. The positive edge of CLKp triggers the NAND-based comparator. Once the output of the comparator is established, the rising edge of Valid toggles the signal Ready. Then, because OutReady is high, the double edge detector sets CLK_fast high for t_2 seconds. This glitch is enough for generating a new rising edge of CLKp, triggering the NAND-based comparator again.

Figure 9. Timing diagram of clock regeneration signals in fast recovery mode.



In the next cycle, the critical path corresponds to the OutReady signal. When Ready toggles, the double edge detector output goes low, but, due to OutReady being low, the glitch does not propagate to CLK_fast. Instead, the glitch is generated when OutReady is high. Due to Valid being high, the rising edge detector keeps CLK_fast high for t_2 seconds. In the end, this glitch creates a new rising edge of CLKp.

When V_{OUT} recovers to V_{REF}, the FSM sets KeepCLK at low; in that case, CLK controls CLKp again. Fig. 9 also depicts the situation when the undershoot is detected while CLK is high. Once KeepCLK goes high, the signal CLK_f holds CLKp low for t_1 seconds. Then, CLK_fast sets CLKp to high, and the comparator responds to CLKp with a rising edge of Valid. The clock regeneration loop works until V_{OUT} recovers. When KeepCLK goes low, the external clock is not filtered anymore, and the regulator works in low power mode.

2.2 CALCULATION OF G_INEXTR AND G_INEXTF

A meaningful advantage of D-LDOs is that they suffer fewer stability issues than their analog counterparts [17]. However, when the sampling frequency increases, the loop stability tends to decrease [18]. Due to the high-frequency self-generated clock, the gain in the fast recovery mode has to be carefully selected. This gain is related to the values of G_inextR and G_inextF.

From section II-C, we recall that the output current of the D-LDO flows through an array of transistors like M_1 of Fig. 7 (a). Then, the following equation defines the voltage at node VOUT:

$$V_{OUT} = V_{IN} - \frac{I_{LOAD}}{G \cdot \Omega_u} \tag{3}$$

Where Ω_u is the conductance of a single transistor, and *G* is the number of turned-on devices. Given that all the turned-on transistors work in the triode region, the unit conductance (Ω_u) corresponds to:

$$\frac{\partial I_D}{\partial V_{SD}} = \Omega_u = \beta_P \cdot (V_{OUT} - V_{THP}) \tag{4}$$

When the D-LDO Counter is working in steady-state mode, G is toggling between two different values, namely, *Gss* and G*ss* + 1. Then, for instance, if VCompL goes high, it means that V_{OUT} has changed at least to 820mV (the value of V_{REFL}). From

[17] LEE Y., QU W., SINGH S. et *al.*, "A 200-mA Digital Low Drop-Out Regulator with Coarse-Fine Dual Loop in Mobile Application Processor," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 1, pp. 64–76, Jan 2017

[18] SALEM L. G., WARCHALL J., and MERCIER P. P., "20.3 A 100nA-to-2mA successive-approximation digital LDO with PD compensation and sub-LSB duty control achieving a 15.1ns response time at 0.5V," in *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, Feb 2017, pp. 340–341

combining equations (3) and (4), the minimum value of I_{LOAD} that could have caused such voltage drop is:

$$I_{LOADmin} = Gss \cdot \beta \cdot (V_{IN} - 0.82)(0.82 - V_{THP}) \quad (5)$$

Similarly, the combination of equations (3) and (4) leads to the value of G that could get V_{OUT} back to 900 mV.

$$G = \frac{I_{LOADmin}}{\beta \cdot (V_{IN} - 0.9)(0.9 - V_{THP})} \quad (6)$$

Where $G = Gss + G\_inextR$. Finally, replacing equation (5) in (6) leads to the relation between G_inextR and Gss:

$$G\_inextR = 0.12 \cdot Gss \quad (7)$$

The same analysis is performed with G_inextF, which leads to:

$$G\_inextF = 0.19 \cdot Gss \quad (8)$$

For scaling *Gss* as in equations (7) and (8), we used bit shift multiplication as described in [19]. This method makes the multiplication less accurate but faster.

In this way, we increase the stability of the regulator by ensuring that the gain is not enough for making V_{OUT} overcome V_{REFH}. Thus, the loop has not enough gain for producing an oscillation outside the boundaries fixed by V_{REFL} and V_{REFH}.

[19] MAINI A. K., *Digital electronics: principles, devices and applications*. J. Wiley, 2007, pp. 58–62.

3. RESULTS

Fig. 10 shows the layout of the blocks comprising the D-LDO regulator. This circuit occupies an area of 0.029mm^2. The core of the D-LDO (FSM and Datapath) consumes most of the regulator area. The layout was implemented following the digital design flow, using only standard-cells for the blocks in the regulator.

Figure 10. Layout of the proposed D-LDO.

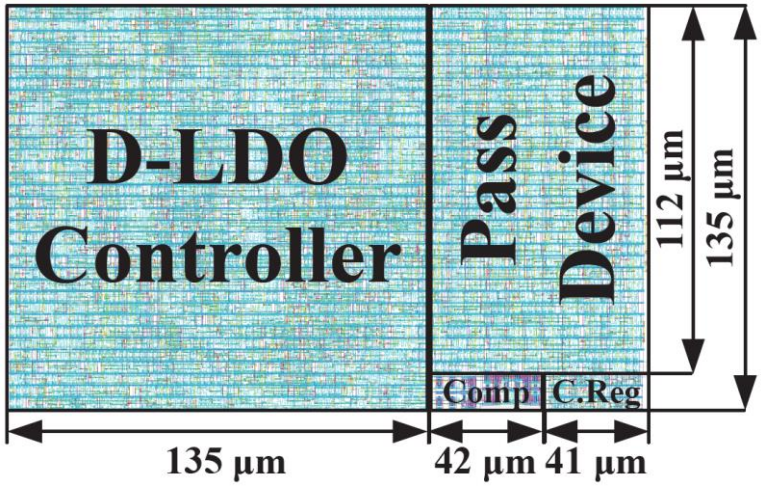


Fig. 11 shows the simulation of the D-LDO transient behavior if V_{IN}=1.2V. The circuit begins in the SAR operating mode since the regulator starts in a reset state. After eight CLKp cycles, the regulator reaches the steady-state. Once in steady-state mode, V_{OUT} toggles around V_{REF}. After 1.5μs, I_{LOAD} starts increasing, causing a drop in V_{OUT}. When V_{OUT} crosses V_{REFL}, the fast recovery mode is enabled and continues until the output voltage is higher than V_{REF}. Due to the 250ns rise time of I_{LOAD}, V_{OUT} gets below V_{REFL} several times. Each time, the clock regeneration loop responds by boosting the frequency of CLKp from 20MHz to 800MHz. When the ramp finishes, the regulator keeps working in the steady-state mode. Then, at 2μs, I_{LOAD} decreases to 4mA with a fall time of 250ns. During this event, V_{OUT} reaches V_{REFH} twice and the

fast recovery logic returns V_{OUT} back to V_{REF}. Finally, the output of the regulator is within the boundaries set by V_{REFL} and V_{REFH}, and then the regulator works in steady-state mode.

Figure 11. D-LDO regulator through different operating modes.

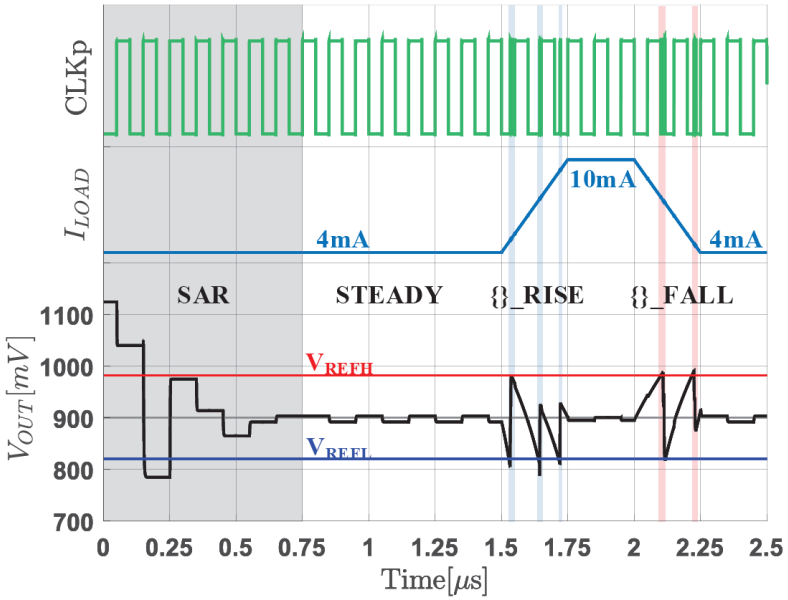
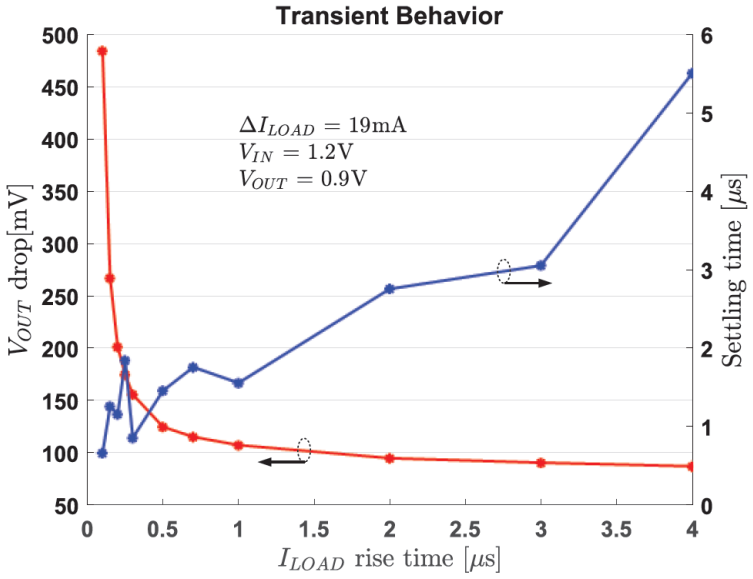


Fig. 12 depicts the transient behavior of the D-LDO for different rise times of I_{LOAD}. In this test, the initial current is set to 1mA, while the final current is 20mA. For each rise time condition, V_{OUT} drop and the settling time are measured. The purpose of measuring the transient behavior is to identify the speed limits of the regulator. When the I_{LOAD} rise time is below 400ns, the voltage drop is above 150mV. On the other hand, when the rise time is higher than 1μs, V_{OUT} does not get below 800mV.

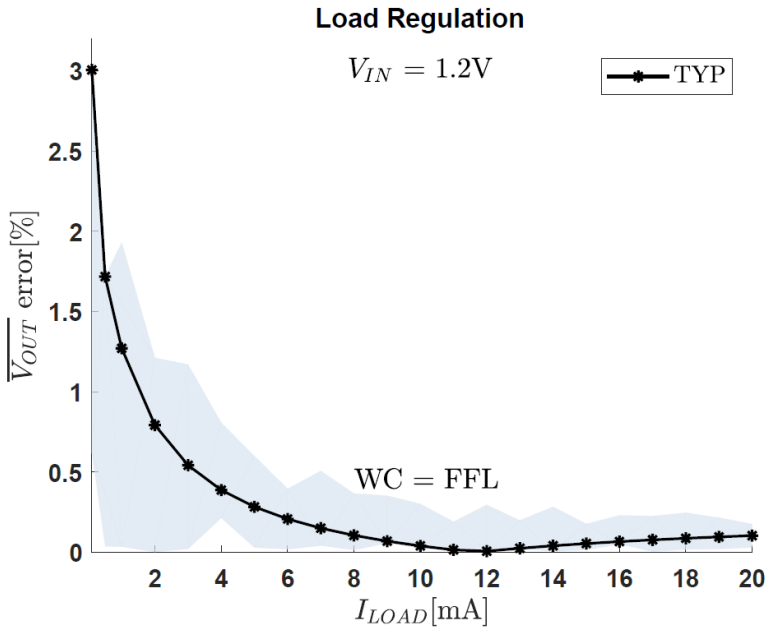
Figure 12. V_{OUT} drop and settling time for different I_{LOAD} rise times.



The settling time is the time elapsed since the I_{LOAD} ramp starts to the time when V_{OUT} error is less than 5mV. We affirm that the output voltage is settled when it enters the 5mV window because once V_{OUT} enters this zone (while I_{LOAD} is 20mA), the output ripple is irrelevant compared to the 5mV boundaries.

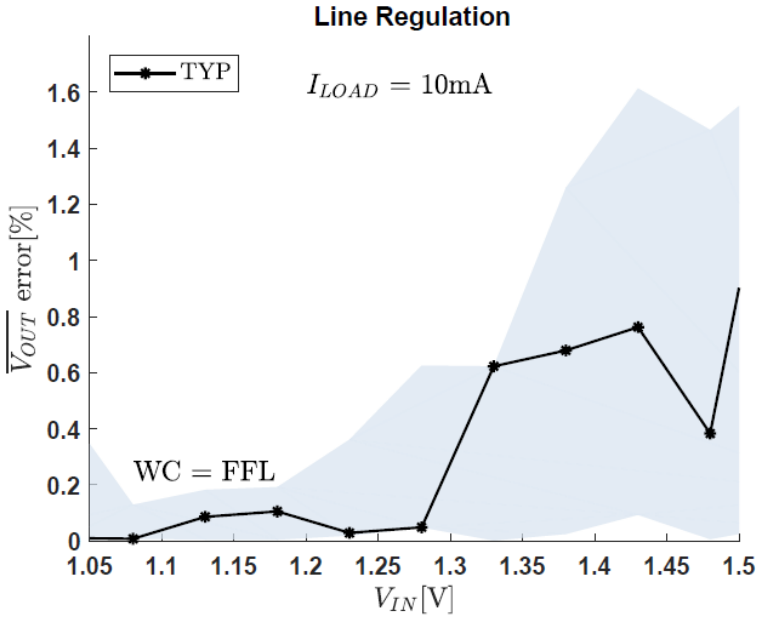
Fig. 13 presents the load regulation of the proposed D-LDO. Load regulation is measured through process and temperature corners, low temperature corners correspond to -40°C while the high temperature is 125◦C. V_{OUT} error corresponds to the relative error of the mean value of V_{OUT}. The load regulation of the typical case through the operating range of the regulator (100μA - 20mA) is 0.15 %/mA. The behavior at low currents corresponds to an intrinsic feature of D-LDO regulators. Equation (3) indicates that the output voltage is more sensible to G variations when G is low rather than when G is high.

Figure 13. Load Regulation of the D-LDO.



The results of the line regulation through corners are presented in Fig. 14. In the line regulation test, the load current is fixed to 10mA. For this condition of I_{LOAD}, the minimum input voltage is 1.05V. The line regulation of the typical case, when V_{IN} ranges from 1.05V to 1.5V, is 2 %/V. Equation (3) explains the behavior of the circuit when V_{IN} is high: If the load current is constant and V_{IN} increases, the value of G has to decrease for maintaining V_{OUT} close to V_{REF}. If G is small, V_{OUT} is more sensible to the variation of G.

Figure 14. Line Regulation of the D-LDO.



4. CONCLUSIONS

In this paper, we presented a fully-digital D-LDO that includes a clock regeneration technique for enhancing the transient behavior without the need for a higher external-clock frequency. The layout of the cells was implemented in a 180-nm CMOS standard technology. The load regulation corresponds to 0.15 %/mA while the line regulation is 2 %/V. The transient response shows a voltage drop of 150mV with a 19mA current step and 400ns rising edge.

BIBLIOGRAPHY

AKRAM M. A., HONG W., and HWANG I., “Capacitorless Self-Clocked All- Digital Low-Dropout Regulator,” IEEE Journal of Solid-State Circuits, vol. 54, no. 1, pp. 266–276, Jan 2019.

AKRAM M. A., HONG W., and HWANG I., “Fast Transient Fully Standard- Cell-Based All Digital Low-Dropout Regulator With 99.97% Current Efficiency,” IEEE Transactions on Power Electronics, vol. 33, no. 9, pp. 8011–8019, Sep. 2018.

BAKER R. J., CMOS: circuit design, layout, and simulation. IEEE Press, 2010, pp. 331–335.

HUANG M., LU Y., S. U et al., “An Analog-Assisted Tri-Loop Digital Low-Dropout Regulator,” IEEE Journal of Solid-State Circuits, vol. 53, no. 1, pp. 20–34, Jan 2018.

HUANG M., LU Y., SIN S. et al., “A Fully Integrated Digital LDO With Coarse Fine-Tuning and Burst-Mode Operation,” IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 63, no. 7, pp. 683–687, July 2016.

KAHNG A. B., LIENIG J., MARKOV I. L. et al., VLSI physical design: from graph partitioning to timing closure. Springer., 2011, pp. 12–14.

KUNDU S., LIU M., S. WEN et al., “A Fully Integrated Digital LDO With Built-In Adaptive Sampling and Active Voltage Positioning Using a Beat-Frequency Quantizer,” IEEE Journal of Solid-State Circuits, vol. 54, no. 1, pp. 109–120, Jan 2019.

LEE Y., QU W., SINGH S. et al., “A 200-mA Digital Low Drop-Out Regulator with Coarse-Fine Dual Loop in Mobile Application Processor,” IEEE Journal of Solid-State Circuits, vol. 52, no. 1, pp. 64–76, Jan 2017.

MA X., LU Y., MARTINS R. P. et al., “A 0.4V 430nA quiescent current NMOS digital LDO with NAND-based analog-assisted loop in 28nm CMOS,” in 2018 IEEE International Solid - State Circuits Conference- (ISSCC), Feb 2018, pp. 306–308.

MAINI A. K., Digital electronics: principles, devices and applications. J. Wiley, 2007, pp. 58–62.

NASIR S. B., SEN S., and RAYCHOWDHURY A., “Switched-Mode-Control Based Hybrid LDO for Fine-Grain Power Management of Digital Load Circuits,” IEEE Journal of Solid-State Circuits, vol. 53, no. 2, pp. 569– 581, Feb 2018.

RABAEY J. M., CHANDRAKASAN A. P., and BORIVOJE, N. Digital integrated circuits: a design perspective. PHI Learning Private Limited, 2013.

SALEM L. G., WARCHALL J., and MERCIER P. P., “20.3 A 100nA-to-2mA successive-approximation digital LDO with PD compensation and sub-LSB duty control achieving a 15.1ns response time at 0.5V,” in 2017 IEEE International Solid-State Circuits Conference (ISSCC), Feb 2017, pp. 340–341.

TANGEL A. and CHOI K., “The CMOS Inverter as a Comparator in ADC Designs,” Analog Integrated Circuits and Signal Processing, vol. 39, no. 2, p. 147155, 2004.

WANG X. and MERCIER P. P., “A Charge-Pump-based Digital LDO Employing an AC-Coupled High-Z Feedback Loop Towards a sub-4fs FoM and a 105,000x Stable Dynamic Current Range,” 2019.

WEAVER S., HERSHBERG B., and MOON U., “Digitally Synthesized Stochastic Flash ADC Using Only Standard Digital Cells,” IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 61, no. 1, pp. 84–91, Jan 2014.