OPTIMIZATION OF A CRYSTAL OSCILLATOR DESIGN FOR A 28 NM SOC IMPLEMENTING START-UP TIME REDUCTION

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Degree work presented as a requirement to qualify for the title of Electronic Engineer

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2024

To our family and friends.

And to our team, with whom we started and finished this amazing journey.

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I want to thank my family, especially my grandmother, my parents, and my siblings, as I could not have reached where I am without them. Thank you for all the trust and support you have given me throughout my life.

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To everyone who was part of this wonderful journey, thank you from the bottom of my heart.

- Sergio Oliveros.

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To all of you, thank you from the bottom of my heart.

- Andrés Tarazona.

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RESUMEN

TÍTULO: OPTIMIZACIÓN DEL DISEÑO DE UN OSCILADOR DE CRISTAL PARA UN SOC DE 28 NM IMPLEMENTANDO REDUCCIÓN DEL TIEMPO DE ARRANQUE [*]

AUTORES: ANDRÉS LEONARDO TARAZONA MORENO
SERGIO SEBASTIÁN OLIVEROS SEPÚLVEDA [**]

PALABRAS CLAVE: OSCILADOR DE CRISTAL, TIEMPO DE INICIO, DAL, CMOS, SOC.

DESCRIPCIÓN:

Este trabajo presenta una investigación sobre el diseño y optimización de un oscilador de cristal en tecnología CMOS de 28 nm para su implementación en un System-on-Chip (SoC), que está en desarrollo por el grupo de investigación OnChip. Se aborda específicamente el desafío de reducir el tiempo de arranque de este tipo de osciladores, característica crucial en aplicaciones de baja potencia.

Debido al alto factor de calidad del cristal utilizado en el oscilador, el tiempo de arranque del circuito suele ser considerablemente largo, típicamente en órdenes de cientos de milisegundos. Este tiempo de arranque prolongado se ve influenciado por la resistencia negativa (R_N) y el ruido interno asociado del oscilador. Para abordar este desafío, el proyecto se enfoca en la implementación exitosa de la técnica de ajuste dinámico de carga (DAL).

La técnica DAL aprovecha el reloj generado por el oscilador para lograr un control automático de la capacitancia de carga del circuito. Inicialmente, se establece una capacitancia de valor bajo para aumentar la resistencia R_N y, como consecuencia, reducir significativamente el tiempo de arranque del oscilador y la energía requerida para el inicio. Una vez la amplitud de la señal generada es considerada suficiente, la capacitancia se ajusta gradualmente y se establece en un valor mayor, determinado para funcionar indefinidamente. Esta estrategia no solo optimiza el rendimiento del sistema, sino que también

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promueve una mayor eficiencia energética, lo que tiene importantes implicaciones para el diseño y la implementación de sistemas electrónicos de baja potencia.

Los resultados obtenidos incluyen un aumento del 210% en la velocidad del sistema y una reducción del consumo de energía de inicio de un 62.45%, los cuales tienen el potencial de contribuir significativamente en el desarrollo de sistemas electrónicos de baja potencia.

ABSTRACT

TITLE: OPTIMIZATION OF A CRYSTAL OSCILLATOR DESIGN FOR A 28 NM SOC IMPLEMENTING START-UP TIME REDUCTION [*]

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SERGIO SEBASTIÁN OLIVEROS SEPÚLVEDA [**]

KEYWORDS: CRYSTAL OSCILLATOR, START-UP TIME, DAL, CMOS, SOC.

DESCRIPTION:

This paper presents research on the design and optimization of a crystal oscillator in 28 nm CMOS technology for implementation in a System-on-Chip (SoC), which is under development by the OnChip research group. It specifically addresses the challenge of reducing the start-up time of this type of oscillator, a crucial feature in low-power applications.

Due to the high quality factor of the crystal used in the oscillator, the circuit's start-up time is typically considerably long, usually in the order of hundreds of milliseconds. This prolonged start-up time is influenced by the negative resistance (R_N) and associated internal noise of the oscillator. To address this challenge, the project focuses on the successful implementation of the Dynamic Load Adjustment (DAL) technique.

The DAL technique leverages the clock generated by the oscillator to achieve automatic control of the circuit's load capacitance. Initially, a low-value capacitance is set to increase the resistance R_N and, consequently, significantly reduce the oscillator's start-up time and the energy required for start-up. Once the amplitude of the generated signal is deemed sufficient, the capacitance is gradually adjusted and set to a higher value, determined to operate indefinitely. This strategy optimizes the system's performance and promotes greater energy efficiency, which has significant implications for the design and implemen-

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[*] BSc Thesis

[**] Facultad de Ingenierías Físico-Mecánicas. Escuela de Ingenierías Eléctrica, Electrónica y de Telecomunicaciones. Advisor: JAVIER FERNEY ARDILA OCHOA

tation of low-power electronic systems.

The results obtained include a 210% increase in system speed and a 62.45% reduction in start-up energy consumption, which have the potential to contribute significantly to the development of low-power electronic systems.

INTRODUCTION

A crystal oscillator is a circuit that uses a piezoelectric crystal (typically quartz) to generate an output signal at a defined frequency, primarily determined by the resonance frequency of the crystal. Oscillators play a critical role in a wide range of electronic systems, providing a stable clock signal as a reference for other chip components. These clock signals must be robust against fluctuations in process, supply voltage, and temperature (PVT) while maintaining their stability over extended periods.

One of the challenges in oscillator design is reducing the start-up time, which represents the period required for the oscillator to stabilize after being powered on. A shorter start-up time is highly desirable in low-power applications, resulting in faster response times and, in some cases, reduced energy consumption during start-up.

Several techniques have been developed to reduce the start-up time of oscillators and adapted to different application fields. The main focus of this project is to implement a dynamically adjusted load (DAL) technique to optimize the design of a 28 nm CMOS crystal oscillator for a System-on-Chip (SoC).

The OnChip research group aims to advance the development of the microelectronics industry in Colombia. This project is part of the development of a 28 nm technology-based SoC, composed of various electronic modules.

1. PROJECT OVERVIEW

1.1. MOTIVATION

This project aims to implement a technique for reducing stabilization time in a crystal oscillator, designed to deliver a 32.768 [kHz] sinusoidal reference signal. The circuit creation process begins with the design of the crystal oscillator in 28 nm CMOS technology, followed by the implementation of the DAL technique. This oscillator is intended to be integrated with other undergraduate projects into a System-on-Chip (SoC), currently under development by members of the OnChip research group.

This project provides a valuable opportunity to develop analog and digital design skills by applying a methodology that follows the design flow, from transistor sizing to circuit layout development. This experience meets academic objectives and contributes to personal and professional aspirations.

1.2. OBJECTIVES

1.2.1. General objective To optimize the design of an oscillator in 28 nm technology by implementing a startup reduction technique.

1.2.2. Specific objectives

- To implement a methodology for the design and optimization of a crystal oscillator considering energy efficiency.
- To study the mechanisms and strategies for startup time reduction found in the literature.
- To perform oscillator layout design and post-layout validation.

1.3. OSCILLATOR OPERATING PRINCIPLES

Crystal oscillators use quartz crystal's piezoelectric effect to operate. When metal electrodes enclose the quartz crystal and an alternating voltage is applied across them, the crystal mechanically deforms at a specific frequency related to its structure and physical dimensions. This mechanical deformation generates an alternating electric field that induces a damped sinusoidal signal in response. If an external circuit feeds back this signal, it is possible to maintain it over time.

A quartz crystal resonator can be represented as the simplified equivalent circuit shown in Figure 1. The crystal operates like a series RLC circuit. The inductance L_s is equivalent to the crystal mass; the capacitance C_s represents the crystal elasticity and R_s accounts for the heat losses. Additionally, we must add a parallel capacitance C_p, representing parasitic capacitances and those generated by the two plates employed for the crystal pins [1].

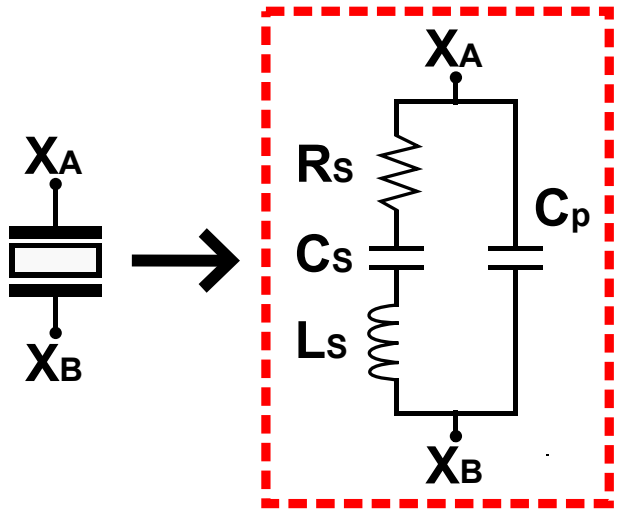

Figure 1. Quartz crystal modeling.

[1] Guillermo GONZALEZ. *Foundations of oscillator circuit design*. eng. Artech House microwave library. Boston: Artech House, 2006.

1.3.1. Circuit analysis By performing a frequency sweep for the magnitude of the equivalent impedance of the crystal observed in Equation 1, it is possible to identify two critical peaks in Figure 2. The first one is due to the interaction between the capacitor Cs and the inductance Ls, creating a series resonance circuit. This point is called the series resonance frequency fs, where the crystal impedance is minimum. After this point, when the frequency is higher than fs the impedance behavior is inductive. At the moment when the inductance Ls and the capacitor Cp form a parallel LC tank, the impedance reaches its maximum point, thus obtaining the parallel resonance frequency fp.

$$Z(s) = \frac{s^2 L_s C_s + s R_s C_s + 1}{s(C_s + C_p)(s^2 \frac{L_s C_s C_p}{(C_s + C_p)} + s \frac{R_s C_s C_p}{(C_s + C_p)} + 1)} \tag{1}$$

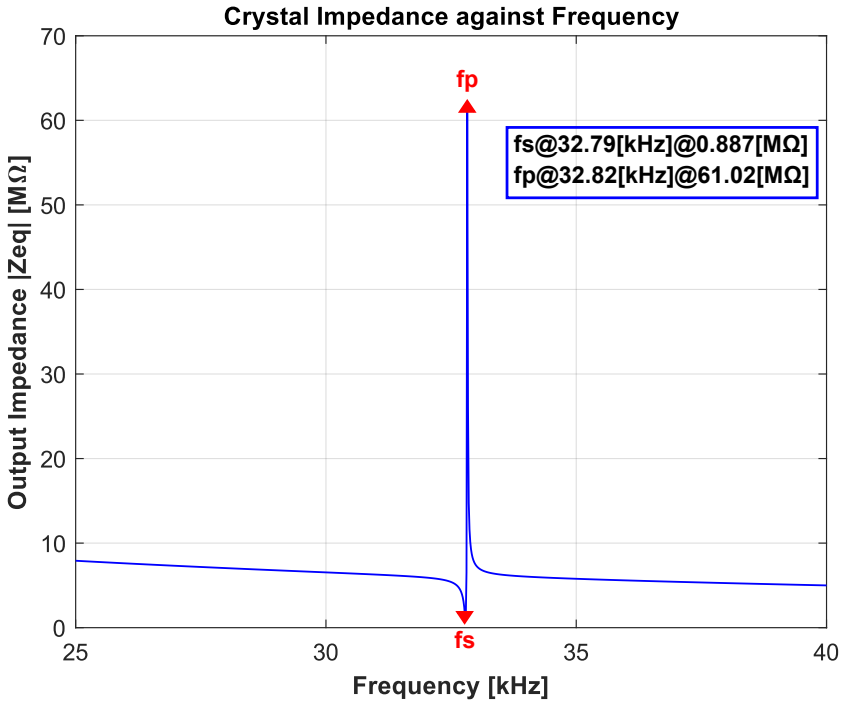

Figure 2. Crystal impedance against frequency.

Various topologies exist for crystal oscillators, including the Colpitts and Santos oscillators. However, in both cases, one of the crystal pins is grounded, posing an issue due to potential parasitic capacitance introduced in parallel with the crystal. Consequently, the Pierce Oscillator is commonly preferred, despite requiring two pins for crystal connection. Hence, the Pierce Oscillator configuration serves as the fundamental topology for analysis. Operational slightly above the series resonance frequency, the Pierce Oscillator's phase shift alone is inadequate to sustain oscillation, necessitating the addition of load capacitances.

The analysis of this circuit begins with determining the series resonance frequency based on the crystal modeling:

$$f_s = \frac{1}{2\pi\sqrt{L_s C_s}} \tag{2}$$

where f_s is the series resonance frequency of the crystal, L_s and C_s are respectively the series inductance and capacitance of the crystal model. The quality factor of the crystal is also determined:

$$Q = \frac{1}{2\pi f_s C_s R_s} \tag{3}$$

These parameters are characterized and can be obtained from the datasheet of the crystal model used. In addition, series capacitance and inductance can be related in terms of resonance frequency and quality factor.

$$C_s = \frac{1}{2\pi f_s R_s Q} \tag{4}$$

$$L_s = \frac{R_s Q}{2\pi f_s} \tag{5}$$

When the crystal is in a state of series resonance (considering only the RLC circuit), the resulting impedance reduces to the series resistance R_s.

When designing a crystal oscillator, some specific criteria must be considered. To analyze this, we start from the topology of the Pierce oscillator, shown in Figure 3.

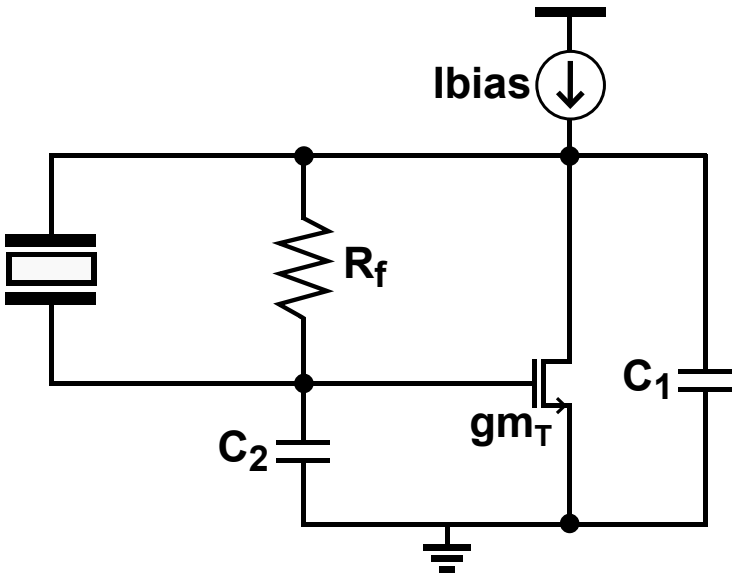

Figure 3. Simplified schematic diagram of a Pierce oscillator.

To make a circuit maintain an oscillation, it is possible to use the Barkhausen criterion, which has two fundamental principles. The first one says that the loop gain of the oscillator must be equal to 1. Otherwise, the oscillation deteriorates or increases to infinity. The second principle mentions that the phase shift must be 360 degrees to produce positive feedback. The above parameters require an active device, which achieves the minimum gain criterion by canceling the real part of the impedance. The imaginary part will determine the oscillation frequency [2]. Figure 4 shows the equivalent circuit used to analyze the oscillator:

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[2] Willy SANSEN. "Design of crystal oscillators". In: *Analog Design Essentials*. Boston, MA: Springer US, 2006, pp. 677–709. DOI: 10.1007/0-387-25747-0_22.

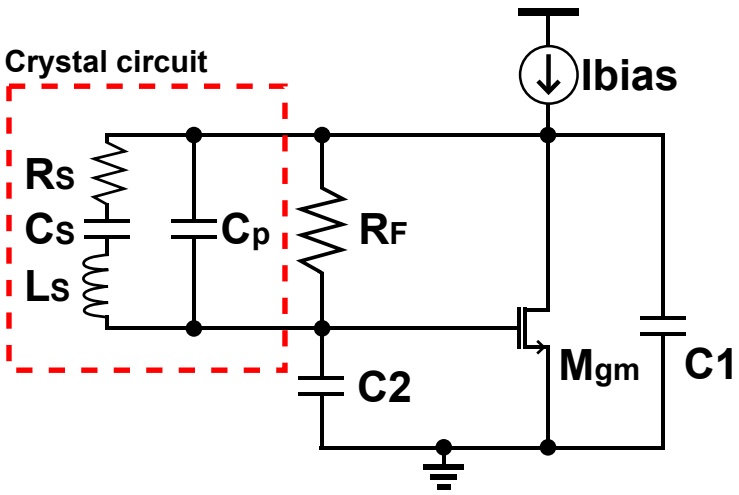

Figure 4. Circuit analyzed.

The purpose of this analysis is to calculate the impedance of the active circuit to determine a minimum impedance expression to ensure circuit oscillation. First, an analysis using Thevenin's theorem is made to obtain the equivalent impedance of the active part of the circuit without taking R_f into account, as shown in Figure 5.

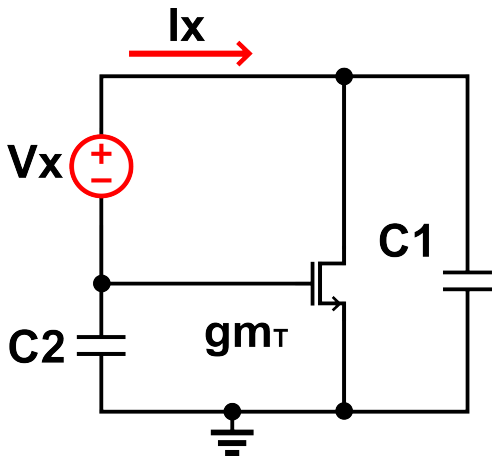

Figure 5. Equivalent resistance of a Pierce oscillator.

The resulting expression is as follows:

$$Z_{eq} = \frac{V_x}{I_x} = \frac{1}{j\omega C_1} + \frac{1}{j\omega C_2} - \frac{gm}{\omega^2 C_1 C_2} \tag{6}$$

To ensure the oscillations are maintained, the real part of the equivalent impedance must be greater than or equal to the value of the crystal's series resistance R_s.

$$R_s \leq \frac{gm}{C_1 C_2 w^2} \tag{7}$$

As mentioned above, the value of R_s is already defined. Hence, for a fixed load, the main design parameter is gm, referred to as gm_{crit} because it is the minimum value necessary to maintain the oscillations.

After establishing a baseline design condition, the analysis incorporates the effects of parasitic capacitances, as shown in Figure 6. This analysis enables a more accurate determination of the circuit impedance:

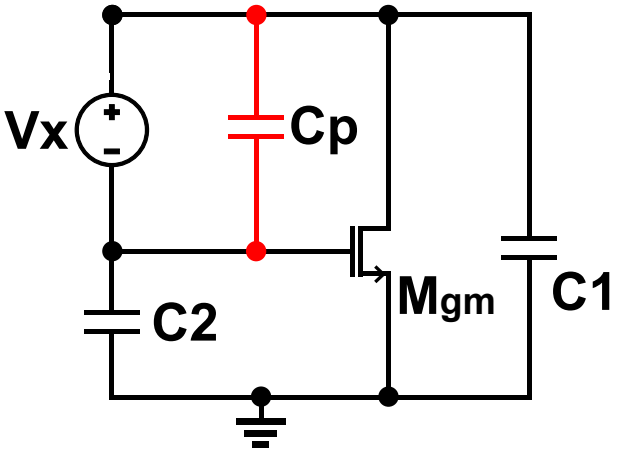

Figure 6. Circuit adding C_p.

Where:

$$Re\{Z_{eq}\} = R_N = \frac{-gmC_1C_2}{(gmC_p)^2 + \omega^2 (C_1C_2 + C_2C_p + C_1C_p)^2} \tag{8}$$

On the other hand, by analyzing the equivalent impedance of the series RLC circuit, which represents the crystal equivalent circuit, and the R_f resistance in parallel, it is

possible to obtain the new R_s resistance.

$$Re\{Z_{crystal}\} = \frac{R_f\left[4p^2 + C_s^2 R_s\left(R_f + R_s\right)\omega^2\right]}{4p^2 + C_s^2\left(R_f + R_s\right)^2\omega^2} \tag{9}$$

Where p represents the pulling factor.

To simplify this expression, two conditions were considered:

$$C_s^2\left(R_f + R_s\right)^2\omega^2 >> 4p^2 \tag{10}$$

and:

$$R_f >> R_s \tag{11}$$

Using these conditions, the given expression of the crystal resistance can be reduced to:

$$RE\{Z_{crystal}\} \approx R_s \tag{12}$$

Furthermore, it is possible to derive an extra condition:

$$C_s^2 R_s\left(R_f + R_s\right)\omega^2 >> 4p^2 \tag{13}$$

From Equations 11 and 13, a requirement for the value of R_f can be obtained:

$$R_f >> \frac{4p^2}{C_s^2 R_s \omega^2} \tag{14}$$

With the more comprehensive expression of the circuit impedance shown in Equation 8, and after knowing that the equivalent impedance of the RLC circuit in parallel with R_f equals R_s, it becomes possible to establish a relationship between these impedance equations. This is achieved by applying the condition $|R_N| \geq R_s$ to derive an expres-

sion that characterizes the circuit resistance ($|R_N|$) using the other circuit parameters.

To better understand the behavior of R_N in terms of gm, Figure 7 shows a polar diagram. This semicircle starts on the imaginary axis for gm equal to zero and ends on this same axis for an infinite gm. The vertical line through the semicircle delineates the minimum negative resistance required to maintain the oscillations, i.e., at this point, the resistance exactly offsets the value of R_s.

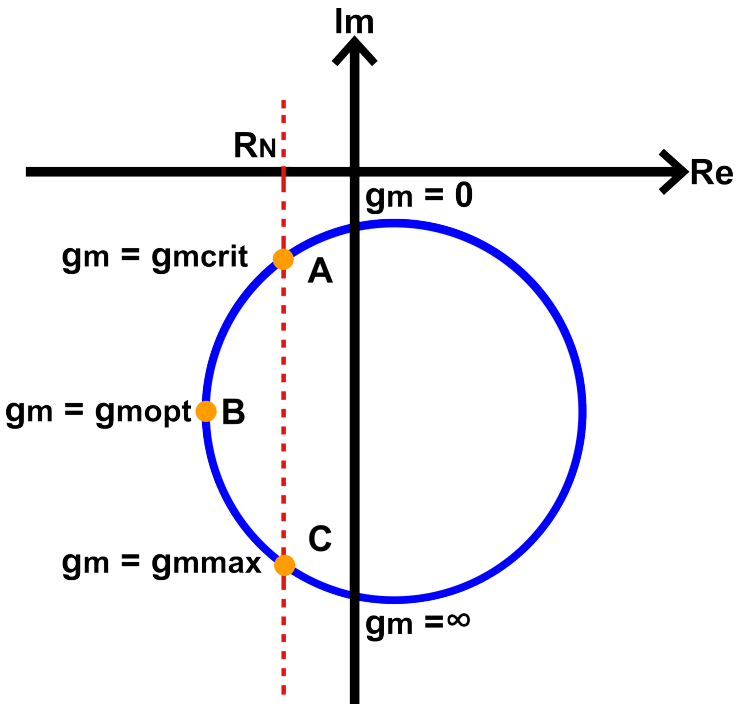

Figure 7. Polar diagram of R_N in terms of gm.

Figure 7 reveals three critical points: A, B, and C. Point A refers to the first time, the value of gm causes the negative resistance to reach the minimum value needed (gm_{crit}). Point B shows the maximum value the negative resistance can reach by increasing gm where $gm = gm_{opt}$. In the case of point C, if gm continues to increase, it again reaches the minimum value of the negative resistance. Even so, this point does not meet the condition of phase stability because, at higher gm, the instability of the

circuit increases [3].

On the other hand, the start-up time depends on the crystal parameters and the negative resistance of the active circuit [4]. In this way, it is possible to discern that as long as one has a higher R_N resistance, the oscillation onset time decreases, so point B is the best point of choice to achieve a considerably lower onset time through an affordable gm. The start-up time will be discussed in more detail in later sections.

Finally, to obtain a small pulling factor, C_1 and C_2 must be large enough; usually, C_1 equals C_2.

1.4. TOPOLOGY

It is necessary to define the components needed to build the oscillator driver. To better understand the topology used, the system will be divided into the following parts: bias, core, amplification, start-up, and boost [5]. It is possible to observe these blocks in Figure 8.

1.4.1. Bias Power must be provided to the transistors in all branches to ensure proper circuit operation. A separate power supply ($BIAS$) is incorporated to mitigate susceptibility to voltage, temperature, and process (PVT) variations. This supply gene-

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[3] E.A. VITTOZ, M.G.R. DEGRAUWE, and S. BITZ. "High-performance crystal oscillator circuits: theory and application". In: *IEEE Journal of Solid-State Circuits* 23.3 (1988), pp. 774–783. DOI: 10.1109/4.318.

[4] A. RUSZNYAK. "Start-up time of CMOS oscillators". In: *IEEE Transactions on Circuits and Systems* 34.3 (1987), pp. 259–268. DOI: 10.1109/TCS.1987.1086137.

[5] S. LEAL. "Crystal Oscillator Design for Energy-Constrained Systems in Standard CMOS 28nm Technology". Universidad Industrial de Santander, 2022.

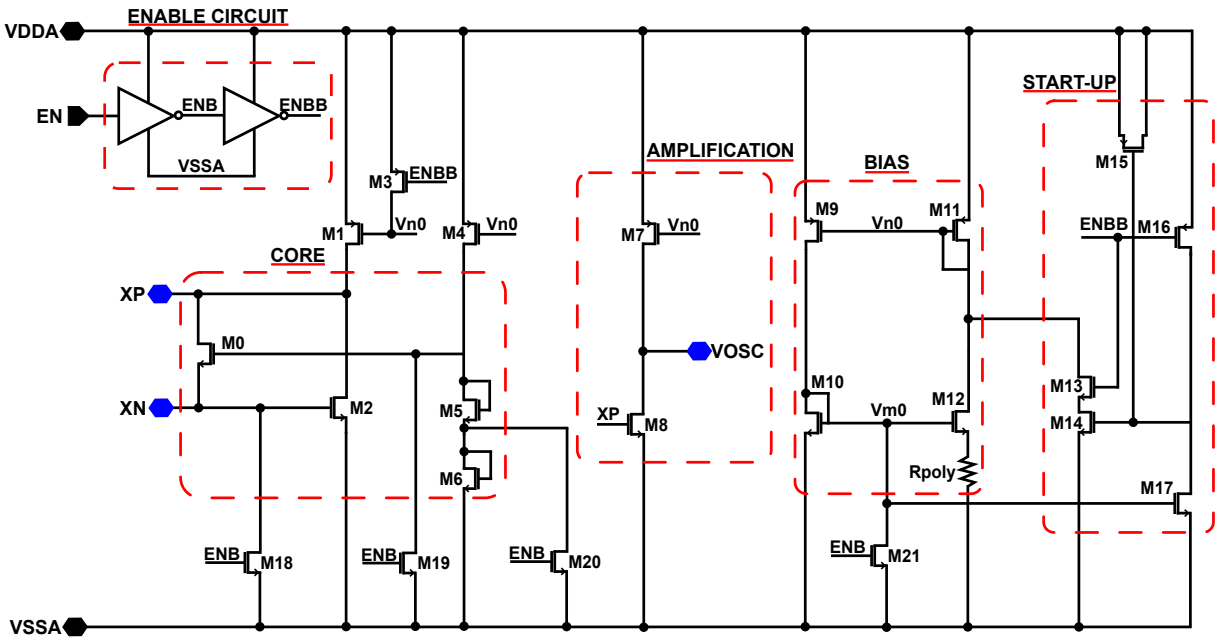

Figure 8. Topology used for the oscillator driver.

rates a robust reference current replicated in multiple circuit branches. Additionally, the design incorporates a polysilicon resistor ($Rpoly$) for a dual purpose: first, to reset the ratio between the reference current and the output current, and second, to stabilize the circuit nodes against thermal fluctuations [6].

1.4.2. Core The core of the circuit is constructed using a Pierce topology with specific modifications. Transistor M_0 determines the negative resistance of the circuit, biased by the series configuration of two transistors, M_5 and M_6, arranged as diodes. It is crucial to guarantee critical M_2 transconductance value (gm_{crit}) to keep the oscillations stable. Notably, the resistance value (R_f) generated by M_0 must be high, on the order of Megaohms.

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[6] Behzad RAZAVI. *Design of Analog CMOS Integrated Circuits*. 1st ed. USA: McGraw-Hill, Inc., 2000.

1.4.3. Amplification Since the range of variation in the output of the crystal pins does not reach sufficiently high levels, it is necessary to amplify the signal using a conventional common source amplifier, allowing the original signal to transform into a "rail to rail" signal capable of covering all the available amplitude.

1.4.4. Bias start-up A circuit with a shutdown signal (ENB) controls the idle or restart state of the bias circuit. When the shutdown signal is activated, the current source nodes are set to potentials VDD and VSS, respectively, thus interrupting the current flow to the reference circuit. The circuit returns to regular operation when the ENB signal turns off. In addition, a capacitor is incorporated to prevent unwanted discharge due to current leakage. When the ENB signal is high, M_{13} is off and M_{16} is on, so the voltage at the gate of M_{14} becomes VDD and turns on. The current through M_{13} is zero because it is in series with M_{14}. Node $Vn0$ will be at VDD, so there will be no current in the reference circuit and M_{17} will be off. Now, in case ENB is turned off, M_{16} is turned off and M_{13} is turned on. Because $Vm0$ is at VSS, M_{17} will be off and the voltage at the gate of M_{14} will remain at VDD, so M_{14} will be on. With M_{13} and M_{14} turned on, the inrush current starts to flow from $Vn0$, which generates a current flow in $M9$ and M_{11}. With this process, a current flow to M_{10} and M_{12} will start. Finally, the inrush current is turned off when M_{14} is turned off again through the influence of node $Vm0$ on the gate of transistor M_{17}.

1.4.5. Enable circuit This stage consists of two inverters used to amplify the power-down signal coming from outside the circuit. This process decreases the transition time on both the rising and falling edges of the ENB and $ENBB$ signals.

1.5. PERFORMANCE MEASURES

In addition to start-up time, a crystal oscillator must generate a robust signal with low noise at a defined power supply. Therefore, several parameters determine the oscillator performance in these areas:

1.5.1. Output frequency (f_{out}) This frequency primarily depends on the crystal used and the circuit load capacitance. The output signal frequency should remain stable and robust against supply voltage and temperature variations.

1.5.2. Phase noise (PN) Represents short-term phase variations in the output signal. A common way to measure phase noise is by observing in the spectrum the ratio between the carrier power and the signal noise power within a bandwidth of 1 [Hz] at a specific offset from the carrier:

$$\mathcal{L}_{fm}[dBc/Hz] = P_{noise}[dBm/Hz] - P_{carrier}[dBm] \tag{15}$$

Phase noise is expressed in dBc, which indicates how many decibels the noise of the carrier signal is at a certain offset. This parameter is produced by thermal, shot, and flicker noise [7].

1.5.3. Pulling factor (p) This parameter indicates the difference between the signal oscillation frequency and the mechanical resonant frequency of a quartz crystal [8]. The following is a simplified expression for calculating the pulling factor of a signal:

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[7] A. HAJIMIRI and T.H. LEE. "A general theory of phase noise in electrical oscillators". In: *IEEE Journal of Solid-State Circuits* 33.2 (1998), pp. 179–194. DOI: 10.1109/4.658619.

[8] Ming DING et al. "A Low-Power Fast Start-Up Crystal Oscillator With an Autonomous Dynamically Adjusted Load". In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 66.4 (2019), pp. 1382–1392. DOI: 10.1109/TCSI.2018.2880282.

$$p = \frac{\omega - \omega_s}{\omega_s} \approx \frac{C_s}{2\left(C_p + C_L\right)} \tag{16}$$

Where ω is the output angular frequency, ω_s is the crystal angular resonance frequency, C_s is the series crystal capacitance, C_p is the parasitic capacitance, and C_L is the oscillator load capacitance.

It is also possible to express the pulling factor in parts per million (ppm), which can be calculated as an error expression:

$$p\,[ppm] = \frac{|f_{desired} - f_s| * 10^6}{f_{desired}} \tag{17}$$

Where $f_{desired}$ is the ideal oscillation frequency and f_s is the crystal resonance frequency.

1.5.4. Load capacitance (C_L) This capacitance is one of the most crucial design parameters for crystal oscillators as it significantly affects the oscillator output frequency, start-up time, output signal amplitude, and pulling factor. Typically, the load capacitance values are provided by the model of the quartz crystal used.

$$C_L = \frac{C_{1(2)}}{2} \tag{18}$$

Where $C_{1(2)}$ are the capacitances connected to each pin of the quartz crystal.

1.5.5. Drive level (DL) This refers to the maximum power dissipation allowed in the crystal and is determined by the oscillator circuit. The drive level must be low because an excess of energy applied to the crystal can alter its equivalent series resistance and cause distortions in the generated signal, increasing noise in the resulting frequency. Moreover, maintaining a high drive level can also physically damage the crystal, so it

is desirable to keep it low to avoid shortening its lifespan.

The drive level equals the multiplication of the RMS current passing through the crystal and the RMS voltage between its ports.

$$DL = I_{XO_{RMS}} V_{XO_{RMS}} \tag{19}$$

1.5.6. Start-up time (t_{Start}) This refers to the time it takes for the oscillator to reach the steady state once it is turned on. Equation 20 shows an expression to estimate the start-up time [8]:

$$T_{Start} = \frac{2L_s}{|R_N| - R_s} \ln\left(\frac{0.9\omega C_T VDD}{|I_{M(0)}|}\right) \tag{20}$$

Where:

$$C_T = \frac{C_1 C_2}{C_1 + C_2} + C_p \tag{21}$$

$|R_N|$ is the circuit's negative resistance, L_s and R_s are the series inductance and capacitance of the quartz crystal, and $I_{M(0)}$ is the amplitude of the initial motional current.

1.5.7. Steady-state power (P_{ss}) Represents the average power consumed by the oscillator when it reaches a steady state. This parameter equals the average of the power consumption in a steady-state period:

$$P_{ss} = \frac{1}{t_{sim} - t_{start}} \int_{t_{start}}^{t_{sim}} I_{Driver} * VDD \tag{22}$$

Where t_{start} is the start-up time and t_{sim} is the evaluation time.

1.5.8. Start-up energy (E_{st-up}) It refers to the energy the oscillator requires to reach a steady state:

$$E_{st-up} = \int_{0}^{t_{start}} I_{Driver} * VDD \tag{23}$$

Start-up energy is a crucial parameter in low-power and communications systems due to the need to turn circuits on and off constantly. The constant activation and deactivation imply that the startup process occurs repeatedly, which increases the importance of minimizing the energy required to reach a stable state.

1.6. STATE OF THE ART

In 1988, a study related to the analysis of crystal oscillator designs [9], covered some fundamental variables and criteria that must be considered when designing an oscillator. Years later, in 2016, researchers introduced an ultra-low power crystal oscillator (XTAL) circuit designed for generating a 32.768 [kHz] clock source [10]. Implemented in 130 nm CMOS technology, the circuit occupies a compact area of 0.0625 [mm^2] while boasting an impressive temperature stability of 1.85 [ppm/C].

In 2017, a publication [11] introduced a PLL-assisted crystal oscillator utilizing a current-switching phase detector (PD) with an intrinsic 90° phase offset for IoT applications.

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[9] E.A. VITTOZ, M.G.R. DEGRAUWE, and S. BITZ. "High-performance crystal oscillator circuits: theory and application". In: *IEEE Journal of Solid-State Circuits* 23.3 (1988), pp. 774–783. DOI: 10.1109/4.318.

[10] Aatmesh SHRIVASTAVA, Divya AKELLA KAMAKSHI, and Benton H. CALHOUN. "A 1.5 nW, 32.768 kHz XTAL Oscillator Operational From a 0.3 V Supply". In: *IEEE Journal of Solid-State Circuits* 51.3 (2016), pp. 686–696. DOI: 10.1109/JSSC.2015.2512382.

[11] Yu ZENG et al. "A 1.7nW PLL-assisted current injected 32KHz crystal oscillator for IoT". in: *2017 Symposium on VLSI Circuits*. 2017, pp. C68–C69. DOI: 10.23919/VLSIC.2017.8008551.

The PLL ensures accurate pulse injection timing into the XO, sustaining oscillation at only 100mV amplitude and ensuring robust operation across Process, Voltage, and Temperature (PVT) variations. This technique achieves high energy injection efficiency and avoids using power-hungry amplifiers. The measured power consumption is 1.7 [nW] at room temperature, with operation demonstrated from -20 ℃ to 80 ℃ and across three corner wafers. The comparison table provided demonstrates a 2x power reduction compared to other works. However, this work boasts a start-up time of less than 10 [ms], a 3000-fold improvement over previous works. Furthermore, the proposed approach does not require calibration and exhibits robust operation across process corners.

In 2019, a research [8] presented a study focused on reducing stabilization time for a 24 [MHz] crystal oscillator through dynamic load capacitance adjustment. Initially, this study considers some advantages and disadvantages of using methods to increase $|R_N|$ and frequency injection methods. To implement the proposed technique, this study employs a clock detector to monitor the amplitude and frequency of the generated signal, along with a state machine and a digital switch enable system, responsible for increasing circuit load over time.

In 2020, a publication [12] introduced 32 [kHz] crystal oscillators operating with only a 60 [mV] supply. Two implementations, utilizing a Schmitt trigger circuit for two different crystals, were designed and experimentally characterized. The power consumptions of the oscillators are 2.26 [nW] and 15 [nW], and the temperature stabilities achieved are 62 [ppm] (25-62 ℃) and 50 [ppm] (5-62 ℃), respectively. The study also measured

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[12] Mariana SINISCALCHI, Fernando SILVEIRA, and Carlos GALUP-MONTORO. “Ultra-Low-Voltage CMOS Crystal Oscillators”. In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 67.6 (2020), pp. 1846–1856. DOI: 10.1109/TCSI.2020.2971110.

the dependence on the supply voltage of current consumption, fractional frequency, start-up time, and oscillation amplitude. Furthermore, the study provides design guidelines for using a Schmitt trigger as an amplifier in crystal oscillator applications, and the experimentally characterized amplifiers demonstrate competitive performance with the lowest reported supply voltage of 60 [mV].

In 2021, a publication [13] synthesized and compared different techniques to reduce the stabilization time of a crystal oscillator, categorizing them into two groups: Energy injection, involving injecting energy into the crystal before oscillations begin, and RN-boosting, involving increasing $|R_N|$ by varying gm or C_L. Additionally, it is possible to include inductive loads in parallel with the load capacitance.

In 2022, an undergraduate project [5] addressed the design of a crystal oscillator in 28 nm CMOS technology intended for high-speed systems. The designed oscillator operates at 32.74 [kHz] with an error of less than 1%. Despite having a considerable start-up time, the XO design focuses on achieving superior frequency accuracy. However, the startup time measurement involved activating the circuit with an enable signal and comparing it to the turn-on time when the circuit is permanently active. This difference in start-up conditions revealed significant variation in startup time, highlighting the importance of understanding and controlling this critical parameter in XO design.

1.7. DESIGN SPECIFICATIONS

Table 1 lists the design specifications for the crystal oscillator. These specifications are the starting point of the design process; through their analysis, it is possible to perform

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[13] Ka-Meng LEI, Pui-In MAK, and Rui P. MARTINS. "Startup Time and Energy-Reduction Techniques for Crystal Oscillators in the IoT Era". In: *IEEE Transactions on Circuits and Systems II: Express Briefs* 68.1 (2021), pp. 30–35. DOI: 10.1109/TCSII.2020.3040419.

a parameter extraction and know the key variables to create a circuit that meets the established requirements.

Table 1. Main XTAL design specifications.

Parameters	Units	Design Target			Comments
		Min	Typ	Max	
V_{DDA}	V	1.6	1.8	2.0	-
I_{VDD}	μA	-	-	1	-
f_{out}	kHz	-	32.768	-	-
$Pulling\ factor$	ppm	-	*TBS	-	-
C_L	pF	3.7	-	12	Final load capacitance
DL	nW	-	30	-	-
t_{Start}	ms	-	-	300	Without calibration strategy
PN	dBc	-	*TBS	-	-
P_{ss}	μW	-	*TBS	-	-
E_{st-up}	nJ	-	*TBS	-	-

*TBS: to be simulated.

2. DAL TECHNIQUE

2.1. DAL OPERATING PRINCIPLE

The start-up process of the oscillator illustrated in Figure 9 involves two stages. Initially, during the transient state immediately after powering on the circuit, the output signal begins oscillating and gradually increases in amplitude. Subsequently, the system reaches the steady state, where the signal stabilizes, maintaining its peak-to-peak amplitude and frequency. In this stable state, the signal becomes robust enough to serve as a clock signal for the other circuit blocks.

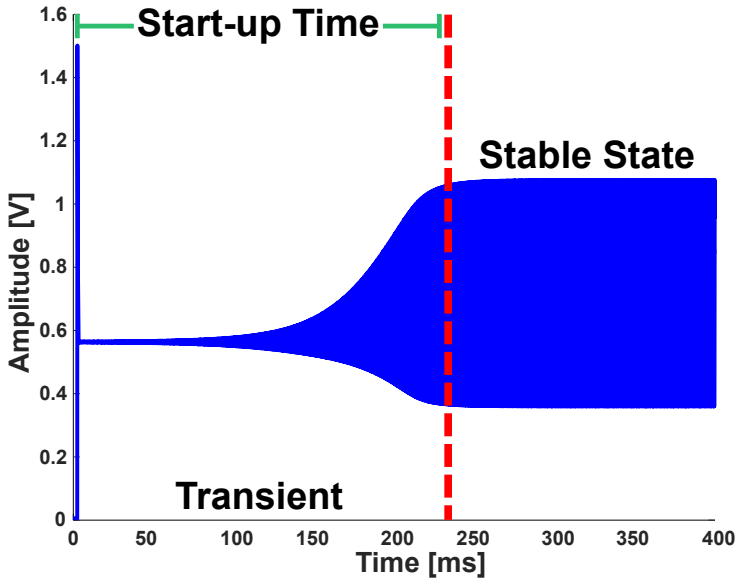

Figure 9. XTAL time response.

The oscillator start-up time indicates the time required for the oscillator to reach steady state. This time depends on several factors, including the quality factor of the crystal used, the oscillation frequency, the internal noise at start-up, and the equivalent resistance seen by the quartz crystal (negative resistance). It is important to note that

the initial stimulus to start oscillating comes from the circuit's internal noise, and the signal growth occurs through the positive feedback provided by the oscillator feedback network. Furthermore, at an overall level, the oscillator operation relies on the ability of the quartz crystal to maintain a stable resonant frequency in response to applied signals.

With a defined output frequency, crystal models with quality factors on the order of tens of thousands and considering that frequency injection techniques may introduce susceptibilities to PVT variations [8], it is considered that the most effective parameter for reducing the startup time of the oscillator is the negative resistance $|R_N|$. As addressed in the following sections, $|R_N|$ depends mainly on the transconductance of the main transistor (gm), the angular oscillation frequency (ω), and the circuit load capacitance (C_L).

Therefore, at least two design parameters are available to improve the oscillator start-up time: C_L and gm. Increasing gm generally involves increasing the current flowing through the transistor, causing an increase in the total power of the circuit, which is one of the main limitations in circuit design, especially in low-power applications. On the other hand, varying the circuit's load capacitance allows increasing $|R_N|$ and, consequently, reducing the oscillator start-up time. Increasing $|R_N|$ through C_L means there is no need to set a high gm, so the circuit current can be low to decrease power consumption. Additionally, optimizing a circuit for shorter start-up times leads to energy start-up values close to optimal [8]; in other words, optimizing the circuit start-up time through this method also reduces start energy.

Decreasing the load capacitance increases the pulling factor, which represents the difference between the frequency of the output signal and the desired frequency. How-

ever, this disadvantage does not impact the final circuit's performance. As explained later, the small capacitance is only present during a portion of the circuit's transient state.

Figure 10 shows the implementation of the DAL technique, which implies the design of six types of blocks that complement the oscillator:

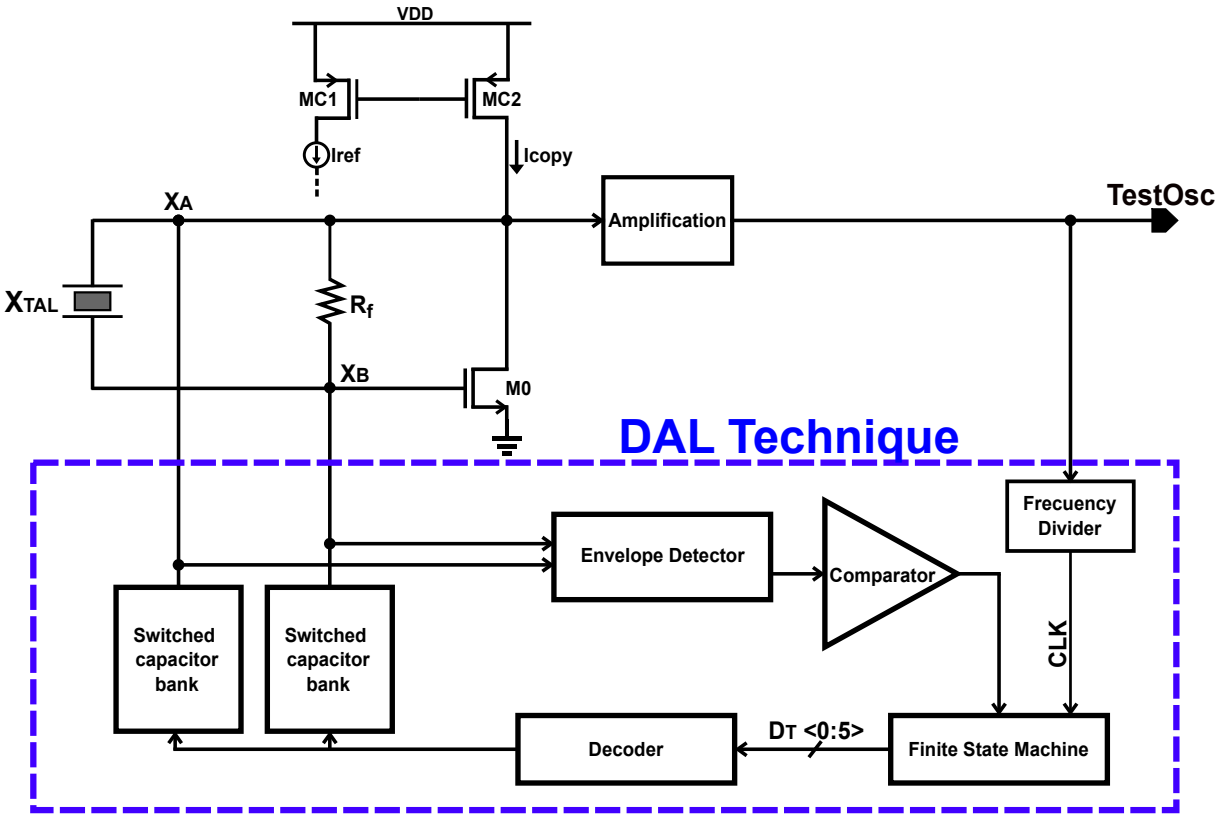

Figure 10. Oscillator with DAL technique.

- **Envelope detector:** This circuit performs the function of identifying the waveform envelope of the oscillator output signal.
- **Comparator:** This block compares the amplitude of the signal provided by the envelope detector with a reference signal, which is set to a voltage value close to the signal amplitude when it is in its steady state. Once the comparator is triggered, its output signal remains high indefinitely.
- **Frequency divider:** This block is in charge of reducing the operating speed of the digital logic to prevent abrupt changes in the output signal caused by the increase in load capacitance. This divider receives the oscillator clock signal as input and provides an output signal with a quarter of the original frequency, as this frequency avoids sudden drops in output signal amplitude.
- **Finite state machine:** This FSM performs the function of a 6-bit counter, responsible for controlling the gradual increase in the system's load capacitance. By generating each of the possible combinations with the 6 bits of the counter, the FSM triggers the closure of each of the 64 switches in the capacitor bank. The FSM starts with all bits low and, after counting, keeps all bits high indefinitely.
- **Decoder:** This block is responsible for receiving the six output bits from the FSM and transforming them into 64 activation signals, tasked with closing switches that connect capacitors in parallel in the capacitor bank.
- **Capacitor bank:** This work uses two capacitor banks connected to the crystal ports. These banks aim to allow the gradual increase of the oscillator load capacitance. Each capacitor bank contains 64 capacitors connected in parallel. Each capacitor is connected in series with switches, which gradually close as the decoder sends activation signals.

The behavioral operation of the dynamic load adjustment technique involves initially setting the circuit load capacitance to be smaller than the planned load capacitance, resulting in an increase of $|R_N|$. As the negative resistance of the circuit increases, the start-up speed also increases, causing the oscillation signal to rise quickly, as seen in Figure 11 (a). Once the amplitude of the signal measured by the envelope detector is considered sufficiently large (near to steady state), the comparator sets its output signal high, activating the FSM and starting the 6-bit count. These bits enter the decoder and generate the activation signals for each switch, gradually connecting the capacitors and thus increasing the circuit load capacitance, Figure 11 (b). Each digital block operates at one-quarter of the oscillator output frequency provided by the frequency divider.

Once the process is complete, the capacitor bank behaves as the total load capacitance of the circuit, as shown in Figure 11 (c). Establishing the total C_L improves the pulling factor and makes the circuit more robust against disturbances. This allows to take advantage of the benefits of having a small load capacitance during the transient phase while avoiding its negative consequences when reaching the steady state.

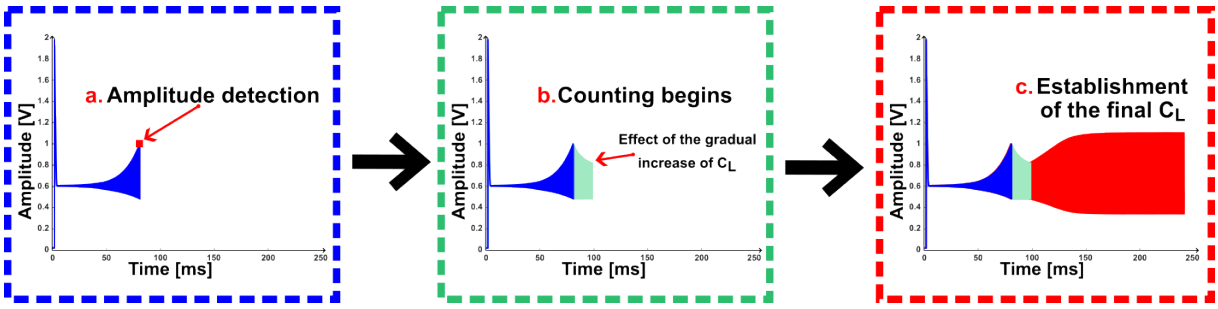

Figure 11. Effects of the implementation of the technique over time.

2.2. DAL TECHNIQUE ANALYSIS

To analyze the behavior of the magnitude of the resistance of the active part of the circuit, it is possible to rewrite equation 8:

$$|R_N| = \frac{gmC_1C_2}{(gmC_p)^2 + \omega^2 (C_1C_2 + C_2C_p + C_1C_p)^2} \tag{24}$$

Where:

$$C_{1(2)} = 2C_L \tag{25}$$

and:

$$C_{1(2)} \gg C_p \tag{26}$$

Taking equations 25 and 26, and substituting it into 24, it is possible to obtain a more simplified expression for the resistance to be calculated:

$$|R_N| \approx \frac{gm}{(2\omega C_L)^2} \tag{27}$$

Looking at the equation 27, it can be noted that the resistance of the active part of the circuit is directly proportional to the transistor transconductance and inversely proportional to the square of the circuit's load capacitance. Therefore, decreasing the oscillator's load capacitance is deemed a better strategy to increase $|R_N|$.

Starting from the simplified expression and equation 7 we can estimate a new critical gm:

$$gm_{crit} \approx R_S (2\omega C_L)^2 \tag{28}$$

Increasing $|R_N|$ by modifying the load capacitance has two main advantages: a quadratic increase of $|R_N|$, and the reduction in the energy required to reach the circuit's steady state.

2.3. CHOICE OF INITIAL LOAD CAPACITANCE

For this work, a 1.5 [pF] capacitance was selected as the initial load capacitance, since this value allows one of the largest differences of $|R_N|$ compared to the final C_L. On the other hand, a 3.7 [pF] was chosen as the final load. The final load capacitance values allowed for the crystal model used can be obtained from its datasheet, indicating that C_L can be 3.7, 4.4, and 6 [pF]. The minimum possible value was selected to reduce the final size of the circuit layout.

By analyzing the expression of $|R_N|$ in Equation 24, it is possible to determine the point where the magnitude of $|R_N|$ reaches its maximum with a given gm.

$$gm_{opt} = \omega \left(C_1 + C_2 + \frac{C_1 C_2}{C_p} \right) \tag{29}$$

At this optimum point, achieving the shortest start-up time is possible. Figure 12 compares the magnitude of $|R_N|$ achieved by varying the gm of the transistor for two different load capacitances.

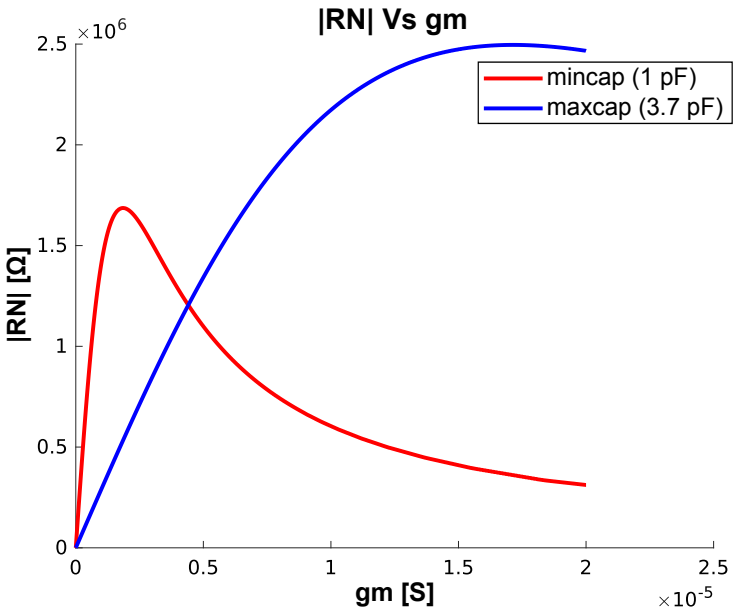

Figure 12. $|R_N|$ Vs gm with fixed capacitances of 1 and 3.7 [pF].

From this figure, it can be seen that with a lower load capacitance, it is possible to achieve a higher magnitude of $|R_N|$ at a lower gm. For the selection of the initial load capacitance, two criteria are used. The first is that the largest difference of $|R_N|$ can be reached concerning the 3.7 [pF] capacitance. The second criterion is that the required R_f resistance is obtainable with the transistor designed to function as a resistor, since it is designed to be in weak inversion, it is difficult to ensure that the resistance value is maintained in the face of PVT variations.

The analysis of Equation 24 allows determining that the largest difference in $|R_N|$ is obtained when setting C_L close to 1 [pF]. To corroborate this behavior, various simulations were conducted with the designed oscillator, varying its load capacitances. These tests established that the shortest start-up time is achieved with capacitances between 1 and 1.7 [pF].

When evaluating the magnitude differences between these capacitances, it was confirmed that with a capacitance of 1 [pF] it is possible to obtain a greater difference of $|R_N|$. However, for this capacitance, a R_f value of approximately 76 [$M\Omega$] is required, obtained from Equation 14, which is difficult to reach and maintain against PVT variations.

Continuing the analysis, a load capacitance of 1.5 [pF] was chosen. Although it has a smaller difference in $|R_N|$ magnitudes, it requires a R_f resistance of approximately 46 [$M\Omega$], which is feasible for implementation. This comparison is shown in Figure 13.

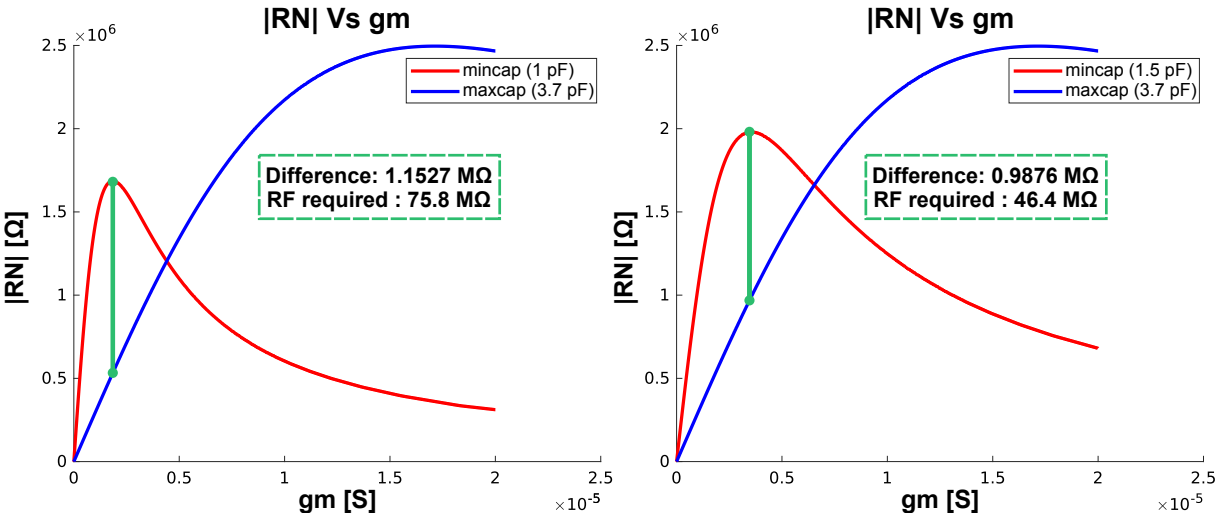

Figure 13. Comparison of $|R_N|$ Vs gm with load capacitances of 1 and 1.5 [pF].

3. CIRCUIT IMPLEMENTATION

To determine the design flow, it is necessary to examine the circuits that make up the DAL technique. For easier interpretation, the block diagram is displayed again in Figure 14. This figure illustrates how the signal is processed by an envelope detector, which activates the comparator and starts the digital logic, gradually increasing the load capacitance.

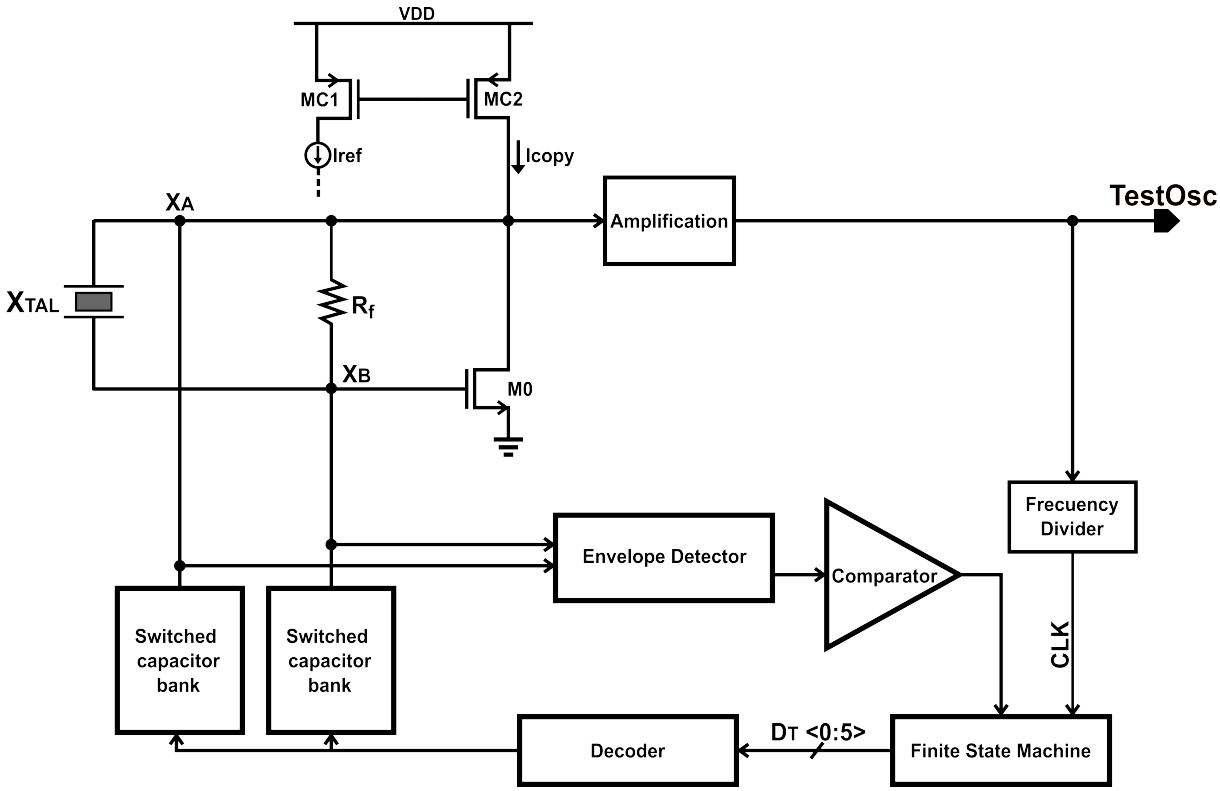

Figure 14. DAL technique diagram.

3.1. DAL BLOCKS DESIGN

3.1.1. Envelope detector The envelope detector continuously monitors the X_A and X_B signals to observe their behavior, focusing only on the amplitude of the crystal's signal. The output of this block serves as input to the comparator, allowing it to detect a specific voltage required for the technique's operation. Figure 15 shows the detector's topology, which uses a pseudodifferential architecture to suppress common mode variations. Thus, the X_A and X_B inputs correspond to the two crystal pins.

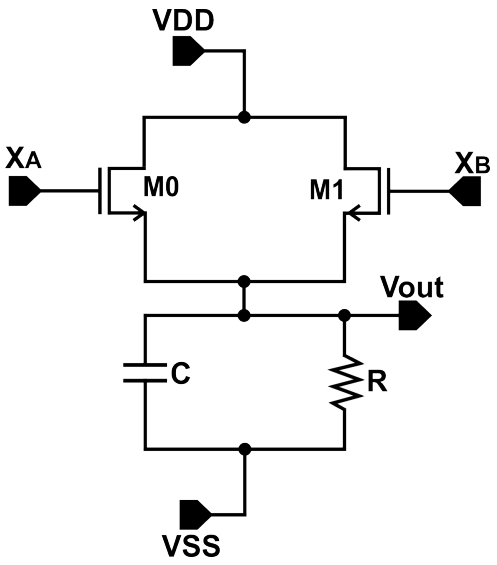

Figure 15. Envelope detector topology.

A capacitance in parallel to a resistor is required to operate the envelope detector. The capacitance is charged and discharged according to the input signal, thus following its envelope. The value of these devices determines a specific time constant τ, which is essential so that the charging and discharging process is fast enough but not too slow. If a τ value is too high, the detector will have a slow response to variations in the signal, so it will not follow the wave. If τ is set too low, the detector follows the changes in the input signal but introduces unwanted noise. The following criterion serves to determine the minimum available time constant:

$$\frac{1}{w_c} << RC \tag{30}$$

Where:

$$w_c = 2\pi f_c \tag{31}$$

f_c is the input frequency to the detector, which, in this case, corresponds to the oscillation frequency at one of the crystal pins, so it has a value of 32.768 [kHz].

Equation 30 serves to select the capacitance value and the resistance value. Since the oscillation frequency is known, the resulting criterion is as follows:

$$4.857x10^{-6} << RC \tag{32}$$

As equation 32 shows, fulfilling this condition requires a considerable product capacitance resistance. Due to the above, it is not advisable to use these real devices since their size is usually too large, which would considerably affect the chip size. To deal with this problem, transistors can work as capacitances and resistances. Figure 16 illustrates the result of this.

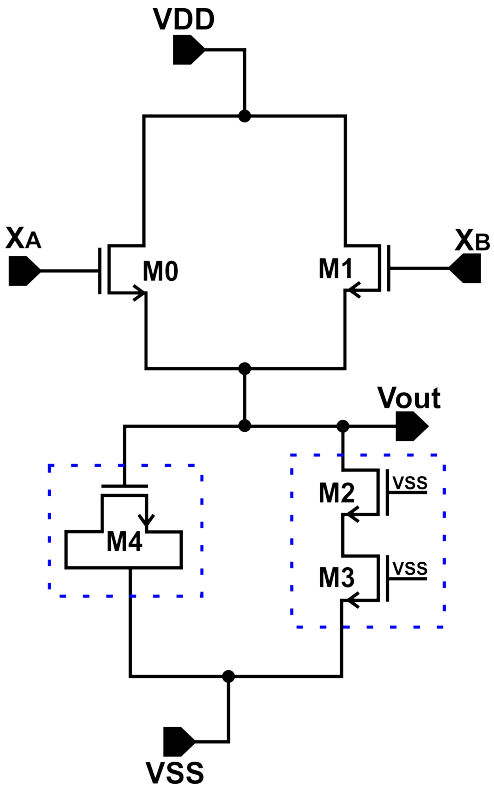

Figure 16. Envelope detector in CMOS technology.

Transistor M_4 is connected in capacitor mode, while transistors M_2 and M_3 form a resistance in this branch. The voltage variation at the V_{out} node is taken into account to determine the capacitance and resistance values. Therefore, two tests are performed to determine whether these values meet the established criteria (Figure 17).

In the case of test A, a DC voltage source feeds the circuit with the maximum and minimum value that V_{out} node can reach. The analysis extracts the value of current flowing through the M_2-M_3 branch, thus obtaining an expression for the minimum resistance and the maximum resistance, as seen in Equations 33 and 34, reached by the circuit.

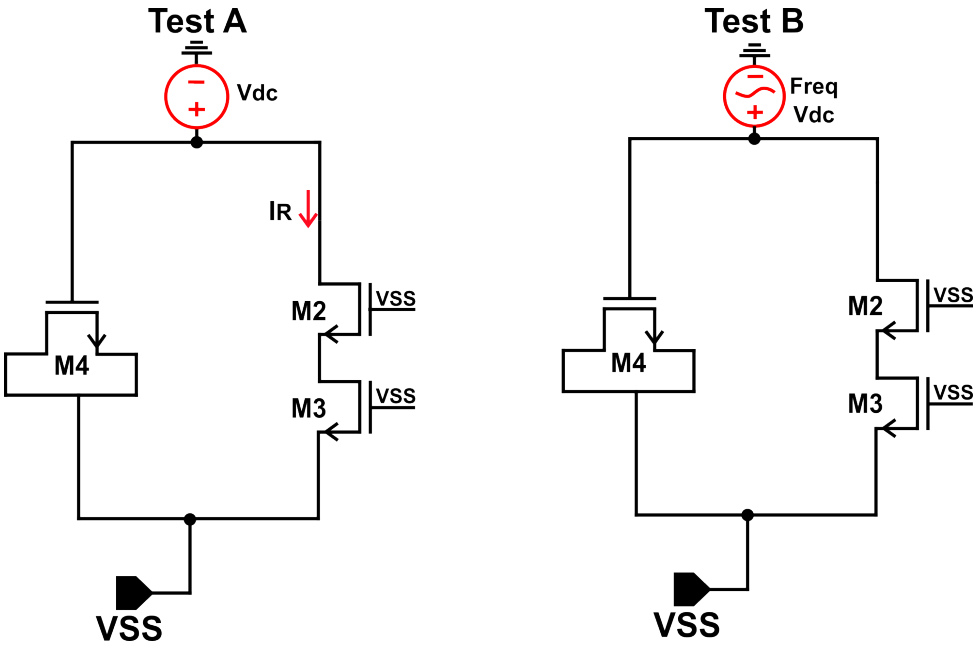

Figure 17. Tests to obtain capacitance and resistance.

$$R_{min} = \frac{Vdc_{min}}{I_{res}} \tag{33}$$

$$R_{max} = \frac{Vdc_{max}}{I_{res}} \tag{34}$$

In the case of test B, an AC voltage source feeds the circuit with the maximum and minimum values that V_{out} node can take. At the same time, a frequency is defined for this signal. A frequency sweep is performed to calculate the system's capacitance through the signal's phase shift. The capacitance value is extracted for both voltage cases, thus obtaining the circuit's minimum and maximum capacitance.

Table 2 shows the results of the resistance and capacitance values, as well as the minimum and maximum τ. In both cases, the τ meets the criteria from Equation 30, so the detector meets the conditions to follow the signal correctly. Additionally, it is important to mention that the obtained capacitance values underwent verification by

comparing them with the C_{gs} Vs V_{gs} curve from the transistor characterization.

Table 2. Calculations for τ.

	Components	
	R [GΩ]	C [fF]
Min	89.49	136.8
Max	162.5	223.1
τ[ms]	12.24	36.25

3.1.2. Comparator The comparator is necessary to implement the start-up time reduction technique because it is responsible for triggering the operation of the FSM, thus allowing the gradual change of capacitance. This device constantly compares with an external reference value. The reference of the comparator is 98% of the oscillator's stable state amplitude. After crossing this point, the comparator output goes high. It is important to note that this maximum value gets extracted after the envelope detector processes the oscillation wave. Figure 18 displays the topology of the comparator. This topology incorporates a high gain stage that converts the output signal to a rail-to-rail signal using an inverter at the output. The comparator operates with an external current source of 1 [μA].

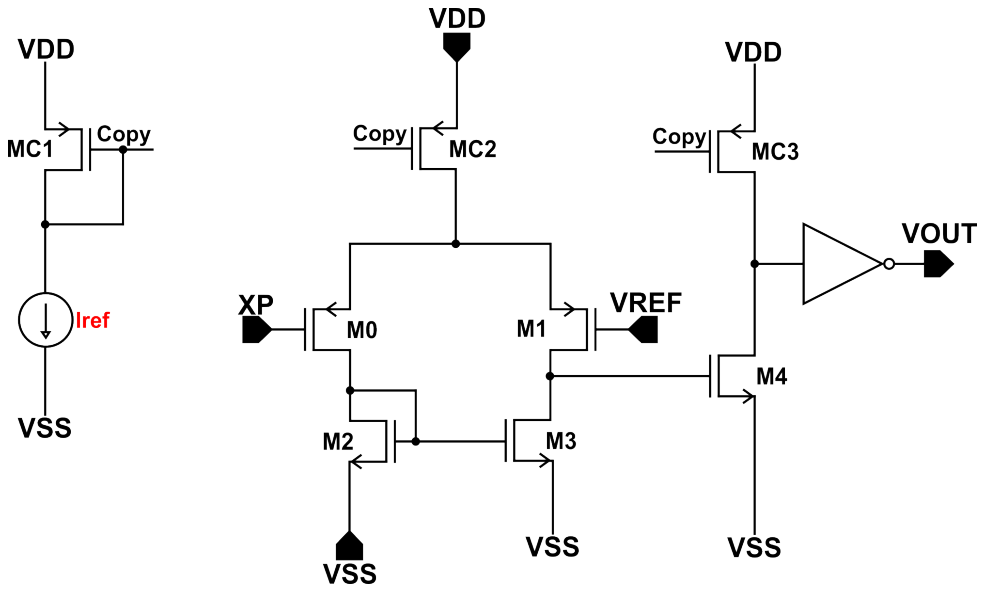

Figure 18. Comparator topology.

3.1.3. Latch To prevent the FSM from turning on and off while the load is being adjusted, the comparator's output is maintained high by using a latch. When a high voltage enters the latch, it holds it indefinitely, regardless of whether the input changes again. The latch operates through two inverters in opposition (Figure 19), such that when the circuit receives the first high value, the 'feedback' inverter holds this output high indefinitely, regardless of what value the input takes again. The final topology is visible in Figure 20.

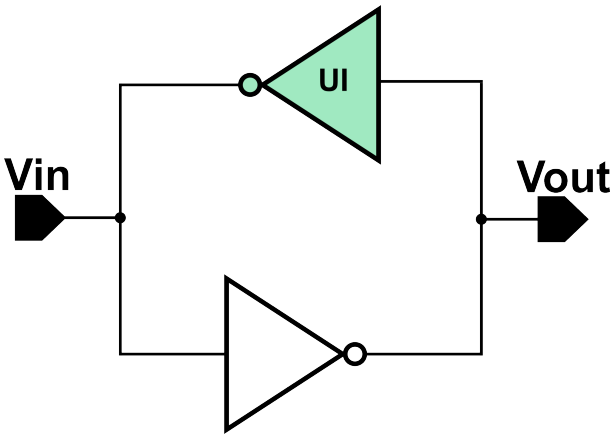

Figure 19. Latch scheme.

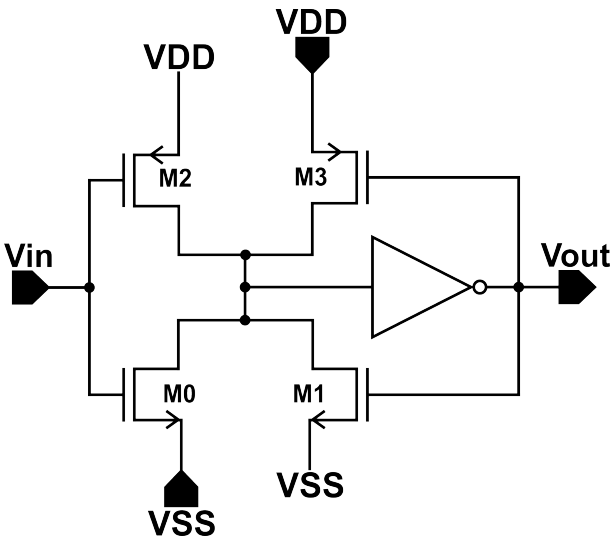

Figure 20. Latch topology.

3.1.4. Digital logic This work's digital logic comprises six types of logic gates: buffers, NOT, NAND, AND, OR, and XOR. These logic gates, shown in Figure 21, are built from the transistor level and are used to develop all the sequential logic of the system.

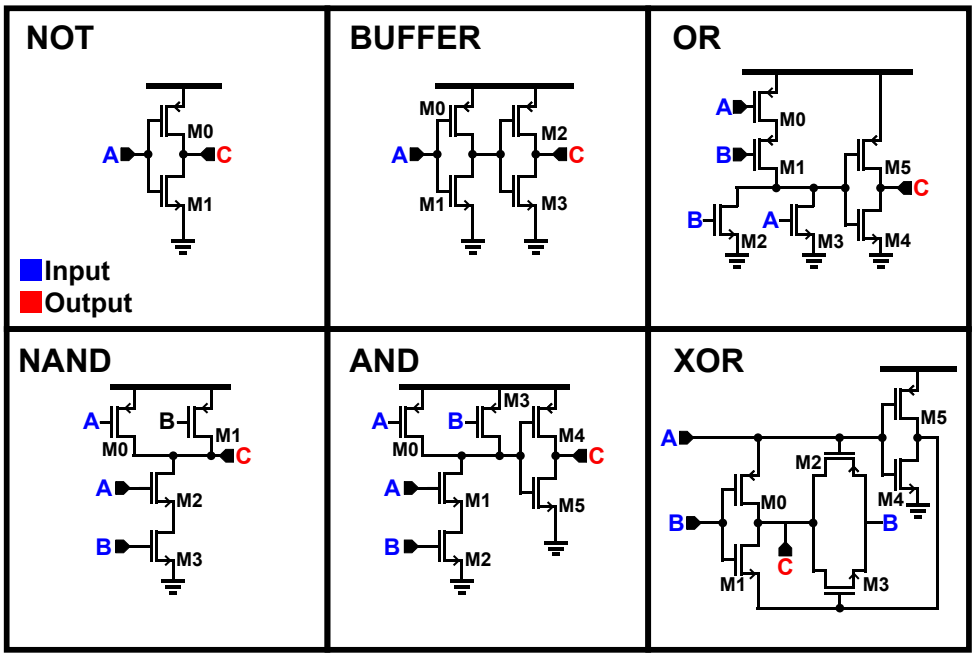

Figure 21. Schematics of the implemented logic gates.

The design of the gates is based on the dimensions of the inverter created to generate the NOT gate. The criterion used is based on obtaining symmetrical voltage transfer characteristics and equal driving capability in both directions, for which $K_N(W/L) = K_P(W/L)$ is sought while seeking to maintain reduced sizes [14].

$$\frac{\mu_n}{\mu_p} = \frac{W_p}{W_n} \tag{35}$$

Another element present is the master-slave D-type flip-flop, which is created by connecting two D-type latches in series and inverting the input of one of them [15], as shown

[14] Adel S. SEDRA and Kenneth C. SMITH. *Microelectronic Circuits*. fifth. Oxford University Press, 2004.

[15] J. S. Baligar YOGITA HIREMATH Akalpita L. Kulkarni. "DESIGN AND IMPLEMENTATION OF SYNCHRONOUS 4-BIT UP COUNTER USING 180NM CMOS PROCESS TECHNOLOGY". in: *International Journal of Research in Engineering and Technology* 03 (05 2014). DOI: 10.15623/ijret.2014.0305149.

in Figure 22. This configuration allows obtaining a digital memory that updates its output every time there is a falling edge at its input.

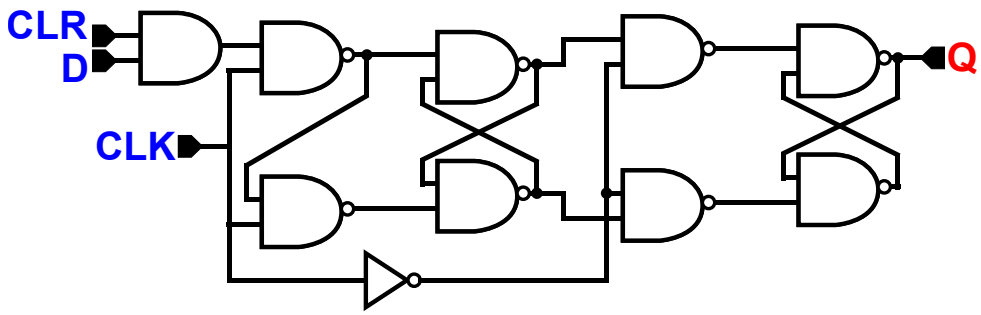

Figure 22. D-type flip-flop.

The implemented flip-flop has a reset logic created with an AND gate at the input so that if the CLR signal is set low, the flip-flop sets its output low on the next clock edge and remains so until CLR is high again.

3.1.5. Frequency divider As mentioned in the unit 2.1 this work implements a frequency divider to reduce the operating speed of the system, in this case, the designed divider delivers at the output a quarter of the original frequency. This block consists of two cascaded flip-flops with the inverted output fed back, as illustrated in Figure 23.

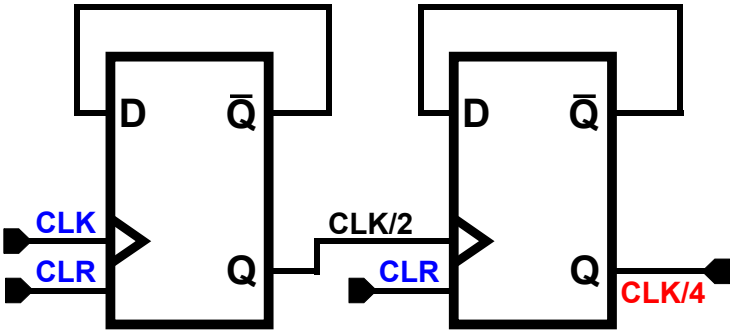

Figure 23. 4X frequency divider.

Frequency division favors having a smoother transition in load capacitance changes. Since this capacitance affects the output signal amplitude, it is preferable to have a gradual transition to avoid abrupt changes in the amplitude of the final clock signal.

3.1.6. Finite-state machine The state machine functions as a 6-bit counter, which serves as input for the decoder and the subsequent activation of the load capacitors. The designed FSM has three states: an idle state where all bits are low, a counting state, and an idle state with all bits high.

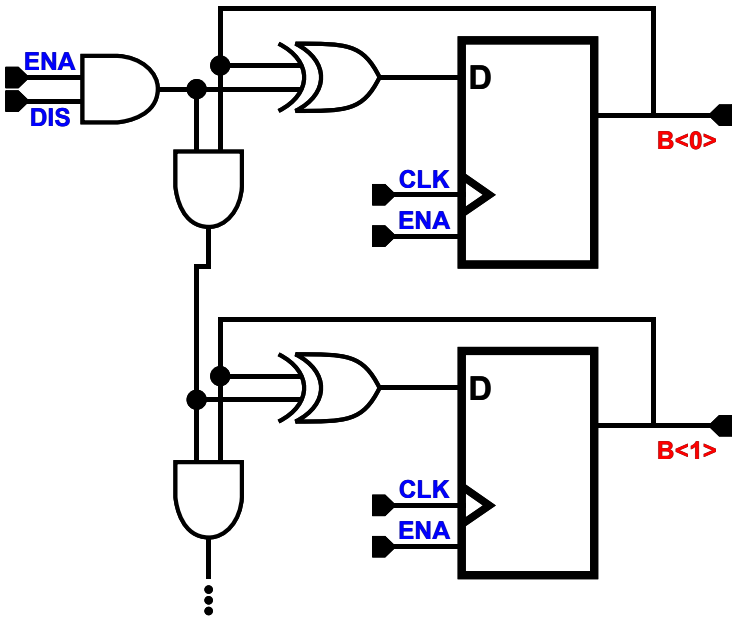

Figure 24. 6-bit synchronous counter.

Figure 24 shows part of the schematic of the 6-bit synchronous counter, constructed using flip-flops, AND, and XOR gates [15]. In addition to this counter, the FSM includes digital logic for counting activation, and a stop logic, shown in Figure 25, so that once all the bits are high, the system maintains its value.

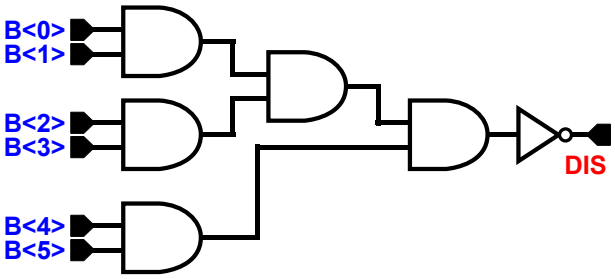

Figure 25. FSM stop logic.

3.1.7. Decoder The decoder designed is a 6 to 64-bit decoder, which has the function of closing the switches included in the capacitor bank to allow the gradual increase of the total load capacitance of the oscillator.

This module uses thermometer decoding, as shown in Figure 26. In this case, the decoding converts the decimal number N representing the bit string at the input into $N + 1$ switches that remain closed at the output.

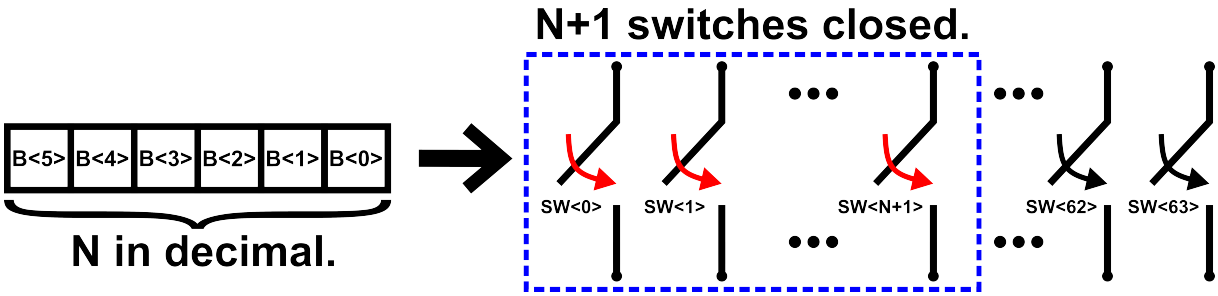

Figure 26. 6 to 64-bit decoder.

The decoder outputs are set high gradually, as the input counter increases the bits from 0 to 63 are set high in that order. The circuit design for this decoder starts with the construction of the truth table for each of its outputs and the simplification of each of the Boolean functions using Karnaugh maps.

The state of the decoder depends on its input, so once the FSM remains in the final standby state, all decoder outputs will remain high. Furthermore, once a bit is set high, it remains in this state indefinitely, allowing the load capacitance value to be set.

3.1.8. Capacitors bank The capacitor bank is the module in charge of increasing the circuit's load capacitance. This system has a bank of 64 capacitors connected in parallel, which have a series transistor working as a switch so that as these switches are closed, each of the connected capacitors contributes to increasing the load capacitance.

Figure 27 shows a representation of the capacitor bank implemented.

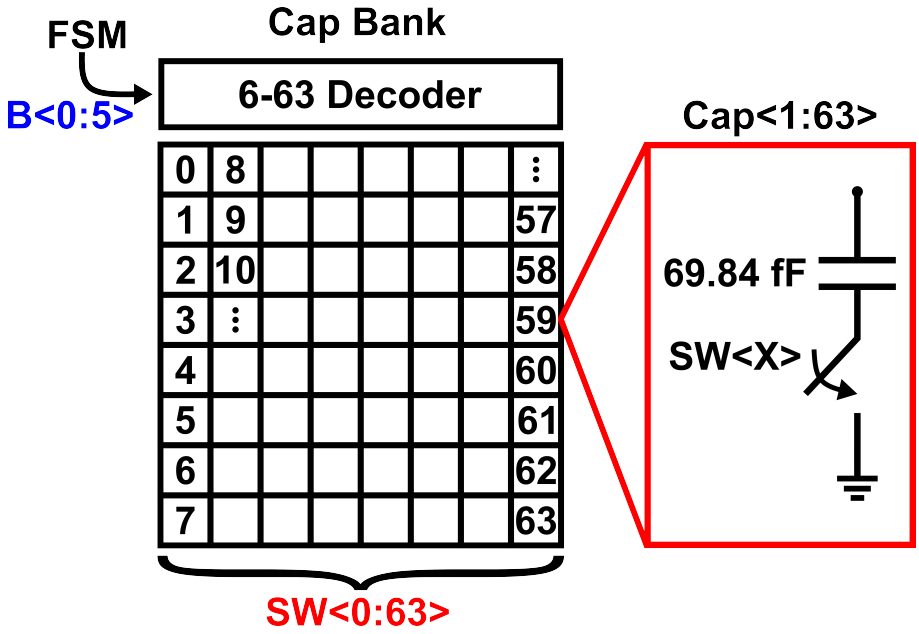

Figure 27. Capacitors bank. Image taken and modified from DAL work [16].

The main capacitor of this bank has the initial load capacitance of the circuit (1.5 [pF]) and is in a branch that is always active. When the FSM starts to operate, each branch starts to be enabled, until reaching the final load capacitance (3.7 [pF]). The remaining 63 capacitors have the same value, obtained by dividing the missing load capacitance by the total number of capacitors available to distribute the load.

4. RESULTS AND DISCUSSION

Figure 28 shows the schematic created to perform the simulations. The test includes the oscillator driver, the blocks of the DAL technique, and a representation of the conditions that subject the circuit when it is manufactured and integrated into a chip, such as electrostatic protection circuits (ESDP) and the wire bond model, which are the connections between an integrated circuit and its packaging. It is pertinent to note that the inclusion of ESD and wire bond elements in the test setup serves to bring the circuit's behavior closer to reality. Incorporating ESD protection circuits is crucial as it mirrors the adverse effects of electrostatic discharge events that can occur during handling and operation, which can potentially damage the circuit. Similarly, modeling the wire bond connections is essential as they introduce parasitic elements and can affect signal integrity, reliability, and overall performance in real-world applications. Therefore, simulating these aspects in the test environment is paramount for accurately evaluating the circuit's behavior and ensuring its robustness in practical scenarios.

In previously mentioned works, such as the implementation of the DAL technique [8] and the design of a crystal oscillator [9], the physical effects of ESD protections and wirebond are not explicitly contemplated. While the results obtained in this work include them through the testbench.

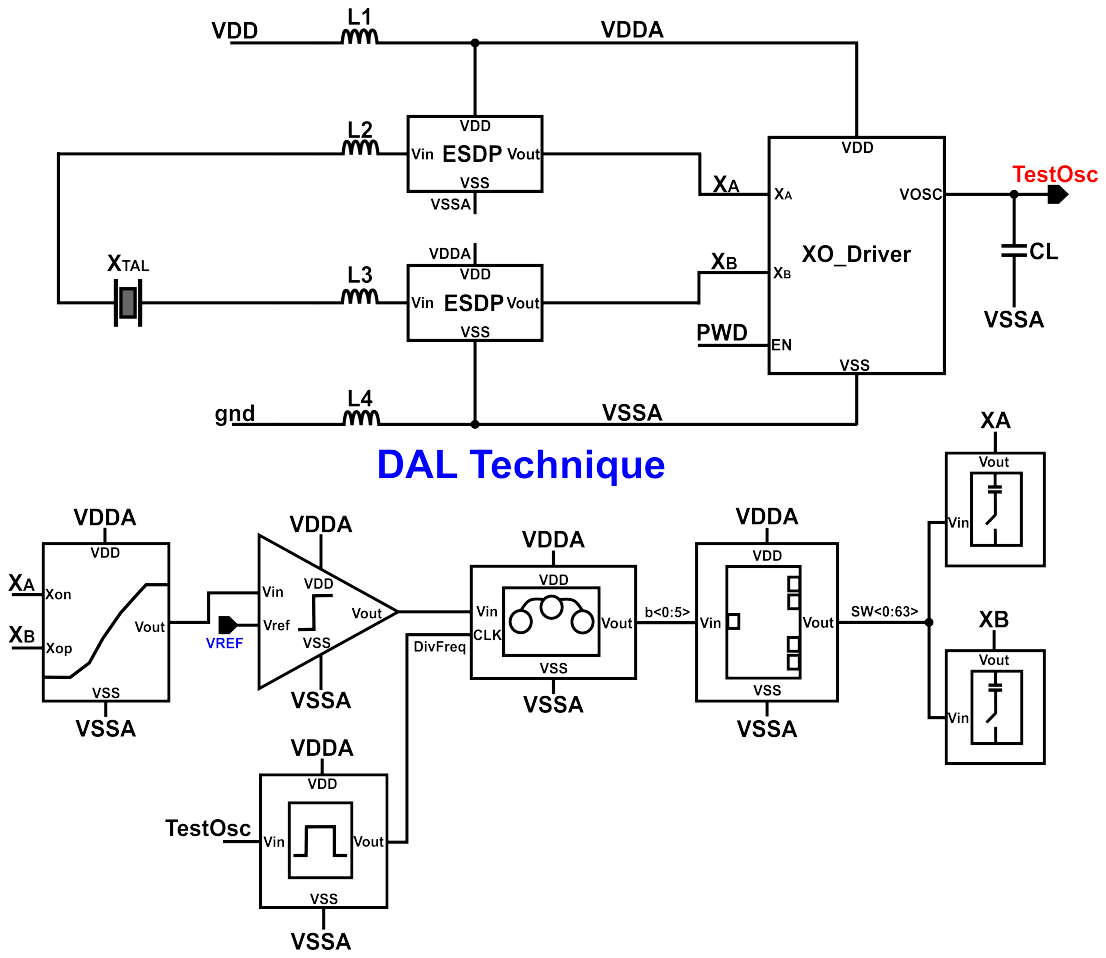

Figure 28. Testbench.

4.1. DEVICE SIZING

This section shows the final dimensions of each element in the oscillator circuit and complementary blocks.

4.1.1. Oscillator's driver The dimensions of the oscillator's driver shown in Figure 8 are detailed in Table 3. The size indicated in the W/L box corresponds to the dimensions of a single finger, the letter P represents the number of parallel transistors and S represents the number of transistors in series.

Table 3. Final dimensions for the oscillator's driver.

Name	W/L [um/um]	P	S
M_0	2/0.15	3	1
M_1	0.6/2	2	2
M_2	0.3/2	1	2
M_3	2/1	1	1
$M_{4,7}$	0.6/2	1	2
M_5	0.6/0.4	10	1
M_6	0.6/0.4	4	1
M_8	0.27/1.5	1	2
$M_{9,11}$	0.6/2	2	2

Name	W/L [um/um]	P	S
M_{10}	0.4/2	20	1
M_{12}	0.4/2	30	1
$M_{13,14}$	2/1	1	1
M_{15}	0.3/0.3	1	1
M_{16}	2/0.3	1	1
M_{17}	2/1.05	1	1
$M_{18,19}$	2/0.35	1	1
$M_{20,21}$	2/0.35	1	1
R_{poli}	2/9.8	1	18

4.1.2. Envelope detector The dimensions of the envelope detector, shown in Figure 16, are detailed in Table 4.

Table 4. Final dimensions for the envelope detector.

Name	W/L [um/um]	P	S
M_0	0.27/2	2	1
M_1	0.27/2	2	1
M_2	0.27/2	1	1
M_3	0.27/2	1	1
M_4	1.335/2	12	1

4.1.3. Comparator The dimensions of the comparator in Figure 18 are detailed in Table 5.

Table 5. Final dimensions for the comparator.

Name	W/L [um/um]	P	S
M_{C1}	0.27/0.15	1	1
M_{C2}	0.27/0.15	1	1
M_{C3}	0.27/0.15	1	1
M_0	0.27/0.15	2	1
M_1	0.27/0.15	2	1
M_2	0.27/0.15	1	1
M_3	0.27/0.15	1	1
M_4	2/0.15	1	1

4.1.4. Latch The dimensions of the latch in Figure 20 are detailed in Table 6.

Table 6. Final dimensions for the latch.

Name	W/L [um/um]	P	S
M_0	2/0.15	2	1
M_1	2/0.15	4	1
M_2	2/0.15	2	1
M_3	2/0.15	2	1

4.1.5. Logic gates The dimensions of the logic gates shown in Figure 21, that form the digital logic, are detailed in Table 7.

Table 7. Final dimensions for each logic gate.

Name	W/L [um/um]	P	S
NOT			
M_0	1.35/0.15	1	1
M_1	0.62/0.15	1	1
Buffer			
$M_{0,2}$	1.35/0.15	1	1
$M_{1,3}$	0.62/0.15	1	1
OR			
$M_{0,1}$	1.35/0.15	2	1
$M_{2,3}$	0.62/0.15	1	1
M_4	0.62/0.15	1	1
M_5	1.35/0.15	1	1

Name	W/L [um/um]	P	S
NAND			
$M_{0,1}$	1.35/0.15	1	1
$M_{2,3}$	0.62/0.15	1	1
AND			
$M_{0,3,4}$	1.35/0.15	1	1
$M_{1,2}$	0.62/0.15	2	1
M_5	0.62/0.15	1	1
XOR			
$M_{0,2,5}$	1.35/0.15	1	1
$M_{1,4}$	0.62/0.15	2	1
M_3	0.62/0.15	1	1

4.1.6. Capacitors bank The dimensions of the basic elements in the capacitors banks, shown in Figure 27, are detailed in Table 8.

Table 8. Final dimensions for the basic elements of the capacitors bank.

Name	W/L [um/um]	P	S
M_0	2/2	1	1
C	2/2	8	1
C_{CAP}	1/2	732	1

4.2. START-UP RESULTS

To evaluate the circuit, two main tests were performed, the first with a load capacitance of 3.7 [pF], and a test with the oscillator implementing the proposed technique. To define the stabilization time, the criterion of 98% was used. It is desired to compare the results of both cases to determine the effectiveness of the implemented technique. The results obtained are shown below.

Figure 29 illustrates the results obtained for a load capacitance of 3.7 [pF]. The circuit must operate with this capacitance in steady state. In all cases, a comparison will be made. The stabilization time obtained was 232 [ms] in nominal simulation (50 ℃). This time was used as a reference to evaluate the effectiveness of the implemented technique.

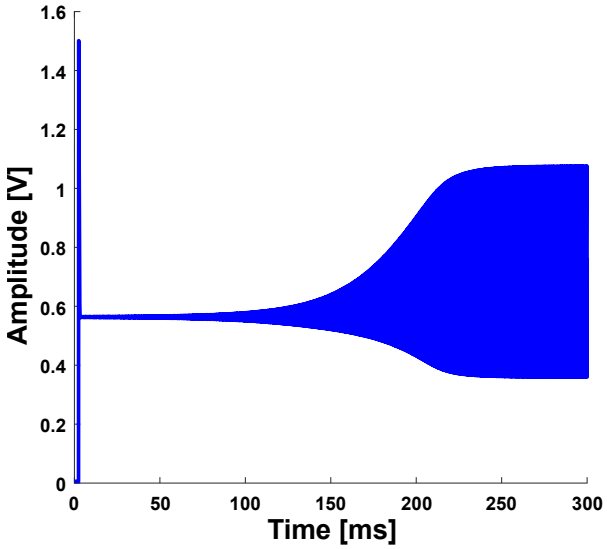

Figure 29. Oscillator time response measured in XA pin with $C_L = 3.7[pF]$.

Figure 30 shows the results when implementing the DAL, which transitions from small to large load capacitance.

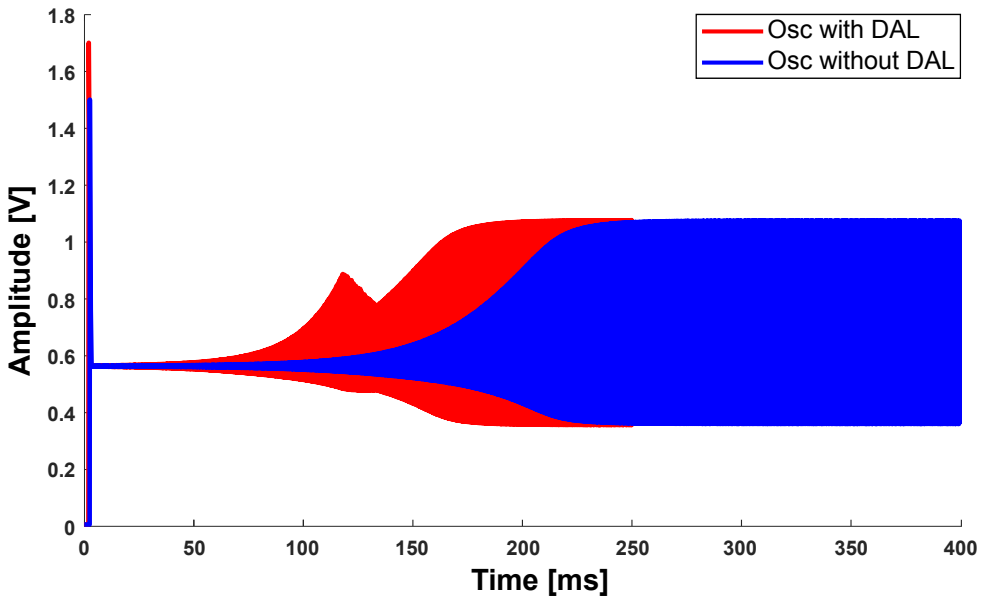

Figure 30. Comparison between oscillator without DAL and with DAL under nominal conditions.

Figure 30 shows the circuit behavior with DAL implementation, generating a stabilization time of 137.7 [ms]. The signal waveform graph illustrates that the waveform changes upon the transition of C_L. Additionally, the signal amplitude depends on the load capacitance used, with lower load capacitance resulting in higher signal amplitude.

Initially, the output amplitude of the circuit is high since it has a capacitance of 1.5 [pF]. Then, when the DAL is activated, the output voltage transitions to look like the waveform in Figure 29. Comparing the settling time results with a C_L of 3.7 [pF] and the DAL, the circuit without DAL is 68.48% slower.

4.3. CORNERS

Simulations were conducted with variations in process, supply voltage, and temperature (PVT) to test the designed circuit. Variations with minimum and maximum voltages of 1.6 and 2 [V], respectively, were performed. For temperature, values of -40 and 80

[℃] were taken. Finally, process variations involved testing fast and slow NMOS and PMOS transistors and their possible combinations. The PVT results for the crystal oscillator are shown in Table 9.

Table 9. Corners results with and without DAL technique.

Parameter	**WITHOUT DAL**			**WITH DAL**		
	Min	**Max**	**Typ**	**Min**	**Max**	**Typ**
I_{VDD} [μA]	0.789	1.609	1.416	0.77	1.548	1.41
f_{out} [kHz]	32.75	32.752	32.752	32.75	32.76	32.76
DL [nW]	11.62	108.3	25.43	10.6	80.2	24.3
t_{Start} [ms]	218.4	375.4	232	127.4	216.5	137.7
P_{ss} [μW]	1.278	3.219	2.548	1.27	3.2	2.51
E_{st-up} [nJ]	248.9	924	744	125	342	271
$Pulling\ factor$ [ppm]	15.26	15.26	15.26	15.2	15.2	15.2

As can be seen in Table 9, the current specification is not met. This is because the amplitude of the crystal's sinusoidal signal depends on the load capacitance and the current flowing through the circuit. Therefore, with a defined load capacitance, the current had to be adjusted to obtain a relatively large wave amplitude so that, when considering variations in PVT, the signal reaching the comparator always exceeds the reference value set to activate the digital logic.

Figure 31 presents the waveform results for DAL corners:

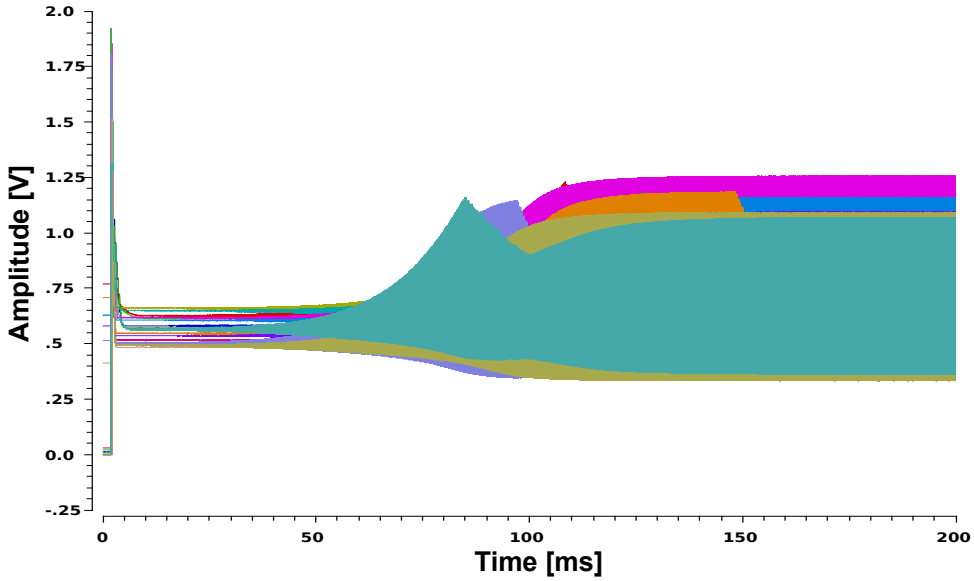

Figure 31. DAL test under PVT.

From these simulations, the maximum settling time was 216.5 [ms], occurring at VDD of 1.6 [V], temperatures of 80 [℃], and transistors with low Vth.

The results in Table 9 show a significant improvement in the startup time t_{Start} when applying the DAL technique compared to the oscillator without DAL. The percentage advantage is 41.7% for the minimum value, 40.65% for the typical value, and 42.33% for the maximum value. These percentages demonstrate the effectiveness of the DAL technique in reducing the start-up time under different conditions, which is crucial for applications requiring fast stabilization of the oscillator. In addition to this significant improvement in start-up time, the circuit achieves a reduction in power consumption in the start-up state of 63.6%. This optimization is achieved without compromising the output frequency accuracy, which remains close to the target of 32.768 [kHz], with a pulling factor of 15.2 [ppm], equivalent to the oscillator without DAL. On the other hand, the steady-state consumption is similar between the two cases. Overall, the

circuit demonstrates that it is possible to achieve substantial improvements in start-up time and energy efficiency without deteriorating other critical parameters, which is a significant result in crystal oscillator development.

4.4. MONTECARLO

A Montecarlo analysis was performed with 500 samples per parameter, the results are shown below:

Table 10. Montecarlo results without DAL technique and 3.7 [pF] load capacitance.

Parameter	**Mean**	σ
I_{VDD} [uA]	1.419	128.4 [nA]
f_{out} [kHz]	32.75	0.724 [Hz]
DL [nW]	35.21	9.509 [nW]
t_{Start} [ms]	277.6	45.49 [ms]
P_{ss} [uW]	2.554	231.2 [nW]
E_{st-up} [nJ]	712.5	117.76 [nJ]
$Pulling\ factor$ [ppm]	18.47	22.11 [ppm]

4.5. LAYOUT

Figure 32 shows the circuit layout, which consists of eight blocks. Each block was designed to achieve a square shape in the final layout.

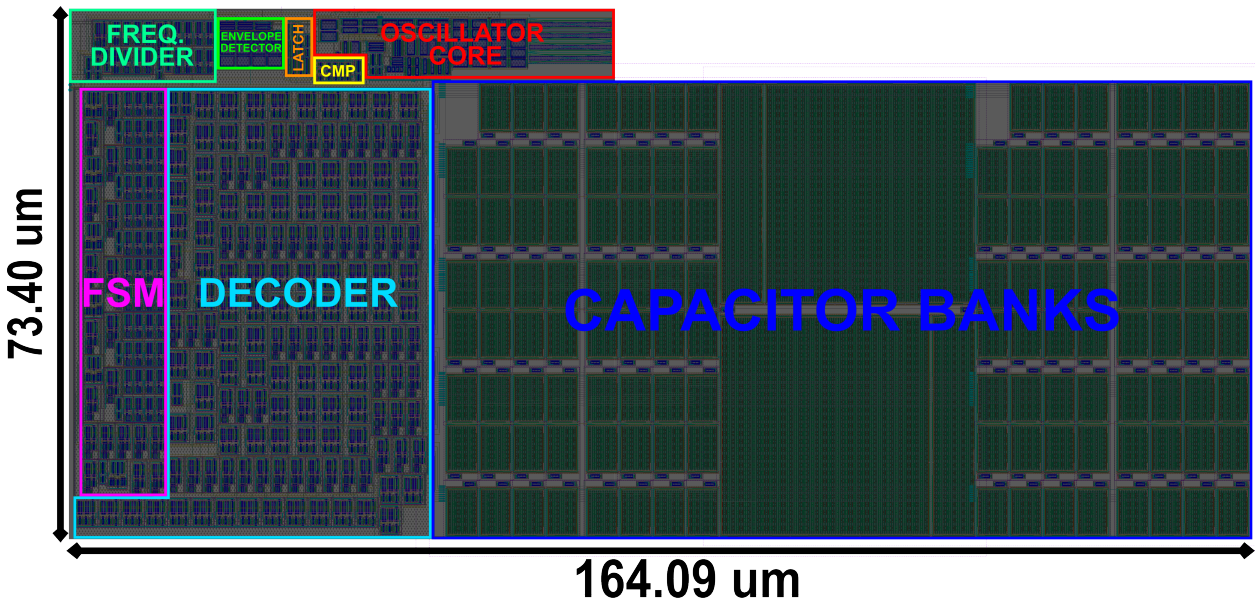

Figure 32. Layout.

For the layout, several considerations were taken into account:

- Metal selection: A convention was established to use even metal layers for horizontal connections and odd layers for vertical connections. Additionally, the use of layers was mostly limited up to metal 3 to facilitate layout connections when integrating the circuit into a larger system.
- Use of interdigitated and common centroid techniques: These techniques were employed to improve transistor matching. These circuits require symmetry for optimum performance, especially in components such as the comparator input pair and the current mirrors for the oscillator driver. Dummy transistors were also strategically added to maintain symmetry and reduce unbalance in the circuit.

- Symmetrical routing: It was used primarily in analog circuits to minimize noise, improve signal integrity, and reduce mismatches since high accuracy and stability are required. It also seeks to reduce the effects of parasitic capacitances.

4.6. POST-LAYOUT

Post-layout simulations were conducted to verify that parasitic capacitance effects do not impact the circuit's performance. These simulations covered all corner cases evaluated in Section 4.3. Two instances were assessed: the oscillator with a capacitance of 3.7 [pF] and the oscillator with the DAL implementation. The results are summarized in Table 11.

Table 11. Post-Layout corners results with and without DAL technique.

Parameter	**WITHOUT DAL**			**WITH DAL**		
	Min	**Max**	**Typ**	**Min**	**Max**	**Typ**
I_{VDD} [μA]	1.205	1.821	1.821	1.221	1.672	1.614
f_{out} [kHz]	32.65	32.76	32.75	32.68	32.73	32.72
DL [nW]	9.236	70.18	60.23	147.9	949.3	250.6
t_{Start} [ms]	262.5	445.4	284.8	130.2	210.5	135.7
P_{ss} [μW]	2.169	3.278	3.278	2.198	3	2.9
E_{st-up} [nJ]	632.6	1186	940.5	328.4	437.4	353.2
$Pulling\ factor$ [ppm]	2.833	3091	2.833	760	2170	900

From these results, an increase in startup time without DAL is observed, with values ranging from 262.5 [ms] to 445.4 [ms], whereas in pre-layout simulations (Table 9), the values ranged from 218.4 [ms] to 375.4 [ms].

Additionally, there are differences in energy consumption values between pre-layout and post-layout. For example, in Table 9, the minimum energy consumption without DAL is 248.9 [nJ], while in post-layout, a minimum value of 632.6 [nJ] is observed, an approximate increase of 250%.

Regarding output frequency, the results show a slight variation between pre-layout and post-layout. In both cases, the output frequency stayed within a narrow range. In post-layout, the worst output frequency result occurs at 32.65 [kHz], leading to a pulling factor of 3091 [ppm], the largest error observed.

With the DAL technique implemented, current consumption is higher in post-layout, with a minimum of 1.221 [μA] compared to 0.77 [μA] in pre-layout. The output frequency remains within a narrow range in both scenarios, but Table 11 reveals greater variation, resulting in a typical pulling factor error of 900 [ppm].

The start-up times vary between 130.2 [ms] and 210.5 [ms], which is similar in pre-layout and post-layout. This indicates that although the oscillator without the DAL experiences a significant worsening of the start-up time, implementing the technique ensures that these times will not tend to vary. These results suggest parasitic capacitances can significantly affect circuit performance, reducing efficiency and increasing power consumption. However, it is worth noting that the reduction in start-up time and initial energy meets the specifications and improves the results of the oscillator without the DAL technique.

4.7. RESULTS COMPARISON AGAINST OTHER WORKS

Table 12 compares the results obtained with this design and works where oscillators of similar frequencies are designed. One of these results is a previous undergraduate thesis conducted by a member of the OnChip research group in 2022. Another work in the table is the main reference work, designed for a 24 MHz oscillator. In this case, the percentage reduction in start-up time obtained is used as the comparison criterion.

Table 12. Results comparison.

	This work	**Previous Work**[17]	**DAL Work**	**Low-Voltage XTAL**	**PLL-Assisted XTAL**	**0.3 V Supply XTAL**
Process	28 nm CMOS	28 nm CMOS	90 nm CMOS	130 nm CMOS	55 nm DDC	130 nm CMOS
$VDD\ [V]$	1.8	1	1	0.06-0.1	0.4-0.8	0.3-0.9
$I_{VDD}\ [\mu A]$	1.614	-	-	-	-	-
$f_{out}\ [kHz]$	32.72	32.74	24000	32.768	32.768	32
$C_L\ [pF]$	1.5-3.7	3.7	10	12.5	-	6
$DL\ [nW]$	250.6	-	-	-	-	-
$t_{Start}\ [ms]$	135.7*	200	0.2**	13000	8	31000
$P_{SS}\ [\mu W]$	2.9	1.536	95	0.015	0.0017	1.5
$E_{st-up}\ [nJ]$	353.2	26.48	38	-	-	-
$Pulling\ factor\ [ppm]$	900	-	-	-	-	-
$PN\ [dBc/Hz]$ @$1KHz$	-101.5	-98.53	-	-	-	-

*2.1X reduction.

**6X reduction.

In the context of the final design, which focuses on developing a crystal oscillator integrating the DAL technique, significant advancements have been achieved. The circuit

without the DAL functionality has an initial energy consumption of 940.5 [nJ], reducing to 353.2 [nJ] with the DAL active, representing a reduction of 2.66 times that of a circuit without applying the technique. In addition, the steady-state consumption is 2.9 [uW], corresponding to the average power consumed by the oscillator with the final load capacitance of 3.7 [pF].

In the case of the previous work[17], it operates with a supply voltage of 1 [V], while the circuit of this project operates with a VDD of 1.8 [V], which implies an increase in power consumption. For this reason, the initial energy of the previous work is lower than that obtained in this project. A similar situation happens with jobs involving a lower supply voltage, in tens or hundreds of millis, such as PLL-Assisted XTAL or Low Voltage XTAL.

Regarding frequency accuracy, the oscillator reaches a frequency of 32.72 [kHz] compared to the 32.74 [kHz] of the previous work, remaining close to the target of 32.768 [kHz]. Based on this measure, the achieved pulling factor is 900 [ppm]. In the case of the DAL Work, an oscillator of 24 [MHz] is used and for the low voltage works, an exact frequency of 32.768 [kHz] is achieved. In addition, the implemented circuit shows less influential phase noise at the output frequency concerning previous work, with a difference of approximately 3 [$\frac{dBc}{Hz}$].

Finally, the main focus of the project is reducing startup time. The current work achieved a stabilization time of 135.7 [ms], signifying an almost 2.1X reduction comparing the circuit without the DAL technique. The stabilization time achieved is 64.3 [ms] shorter compared to the previous work, which is 47.3% slower. In addition, the stabilization time obtained is generally superior to the low supply voltage work, as these are not focused on obtaining fast stabilization times. It's worth noting that startup time can

vary significantly depending on different applications, and the method of determining it is an important factor to consider. In this case, the circuit receives an enable signal after 1 [ms], meaning the crystal nodes are initially uncharged. This information is not explicitly mentioned in the other papers.

5. CONCLUSIONS AND FUTURE WORK

5.1. CONCLUSIONS

Through the analysis and application of the DAL technique to increase $|R_N|$ varying the oscillator's load capacitance, it was possible to implement a system capable of significantly reducing both the start-up time and start-up energy of the circuit. We achieved an effective reduction in start-up time, with a 2.02X reduction observed in the worst-case scenario and a 1.92X reduction in the energy required for clock signal establishment.

Starting from a thorough research of the state of the art, various strategies were explored to reduce the start-up time in crystal oscillators, identifying inherent limitations such as the trade-off between start-up time and circuit output frequency accuracy. Among the techniques investigated, the dynamically adjusted loading (DAL) method was highlighted for its ability to optimize start-up time by gradually varying the circuit's load capacitance. This approach enables the oscillator to start with a specific capacitance that progressively increases, contributing not only to the reduction of the start-up time but also to improving the accuracy of the steady-state oscillation frequency and the initial energy reduction of the circuit.

Thanks to the techniques of interdigitated layout, common centroid, and symmetry search, variations in circuit performance parameters were reduced during post-layout validation. This ensured that although parameters worsened in some cases, they still met the specified requirements.

Furthermore, the implementation of the DAL technique reduces the worsening effects on the oscillator start-up time during post-layout simulations. It was observed that although the oscillator stabilization time worsened, once the DAL technique was implemented, these times did not show significant variations compared to pre-layout simulations.

The selected criterion for the initial load capacitance was based on finding the largest difference in $|R_N|$ while considering feasible values of R_f. This method offered clear guidance on the best C_L value to use in the circuit. The aim was to approach the optimum value to maximize the reduction in startup time and energy.

The value of resistance R_f was one of the main limiting factors when selecting the initial load capacitance of the circuit. Although the selected capacitance of 1.5 [pF] required a resistor value close to the considered limit, it was achievable, and the time reduction was successfully implemented.

5.2. FUTURE WORK

- Explore tuning techniques to calibrate the circuit parameters after fabrication. These parameters may include the load capacitance or the polysilicon resistor used in the self-bias. These techniques allow adjustments to the oscillator design to improve its performance and accuracy, especially regarding start-up time and frequency stability.
- Investigate and optimize specific parameters of the DAL method to improve its start-up time performance. This could include exploring different capacitance variation profiles and control strategies to adapt to different operating conditions. Also, it is possible to redesign the blocks that make up the DAL technique to optimize the circuit area.

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