# DEVELOPMENT OF A CMOS 28 NM DIGITAL STANDARD CELL LIBRARY

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FACULTAD DE INGENIERÍAS FÍSICO-MECÁNICAS
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*Dedicated to Jorge Ramón, a great person, teacher, engineer and most of all, Friend.*

I would like to thank to all the people I've ever met, because a man is made of his experiences and his experiences are a product from mankind, but not even the biggest paper or the all the words ever known are enough to share how grateful I am.

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-CP

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David Uriel Rodríguez Cárdenas

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## RESUMEN

**Titulo:** Diseño de una Librería de Celdas Estándar en Tecnología CMOS de 28nm[‡]

**Autores:** **CARLOS ANDRÉS PÉREZ LÓPEZ**
**DAVID URIEL RODRÍGUEZ CÁRDENAS**[‡ ‡]

**Palabras Clave:** 28nm, CMOS, compuerta lógica, flip-flop, síntesis, ASIC, celda estándar.

**Descripción:**

Se desarrolla una librería de celdas estándar con la tecnología del estado-del-arte de 28 nanómetros para ser utilizada en un ambiente académico. Esta librería incluye un conjunto de celdas básicas que representan compuertas lógicas tales como las NOT, NAND y NOR. Cada una de estas compuertas lógicas se presenta en distintos tamaños, múltiplos de configuración más básica presentada. Cada una de estas presentaciones es capaz de manejar un valor distinto de carga. Entre las demás celdas se encuentran tres *flip-flops*, estos incluyen un *flip-flop pass-gate* tradicional y dos flip-flops de alta velocidad. Estos dos últimos *flip-flops, los cuales son* el *True Single Phase Clock (TSPC)* y el *Strong Arm (SA) flip-flop*, pueden operar a frecuencias que superan los 11GHz y presentan tiempos de hold y de setup tan bajos como 3.88 pico segundos y 9.35 pico segundos respectivamente. Se realizó la representación de layout para cada una de las celdas, donde cada una cumple con las reglas de diseño de la tecnología CMOS de 28nm y adicionalmente con pautas para el diseño de celdas estándar. Se muestra el consumo en área del layout de los distintos *flip-flops* para un mejor contraste en cuanto a esta característica. Finalmente, se presenta la síntesis de un circuito *PRBS Generator (Pseudo Random Bit Sequence)* a manera de ejemplo para un mejor entendimiento del uso de la metodología de celdas estándar y se muestra un esquema del PRBS y el layout del mismo.


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## ABSTRACT

**Title:** Development of a CMOS 28 nm Digital Standard Cell Library[‡]

**Authors:** **CARLOS ANDRÉS PÉREZ LÓPEZ**
**DAVID URIEL RODRÍGUEZ CÁRDENAS[‡ ‡]**

**Keywords:** 28nm, CMOS, logical gate, flip-flop, synthesis, ASIC, standard cell.

**Description:**

A Standard Cell library developed in the state of the art CMOS 28 nanometer technology to be used in an academic environment is presented. This library includes a set of basic cells that represent logic gates such as the NOT, NAND and NOR gates. Each one of these logic gates is presented in multiples of its base design, and each version of the gate is capable of handling different amounts of load. The other cells include a traditional pass-gate based and two high speed flip-flops. The last two flip-flops are a True Single Phase Clock and a Strong Arm flip-flop. These high speed flip-flops are able to operate with maximum frequencies over 11GHz and they present hold times as low as 3.88 ps and setup times as low as 9.35 ps. A layout representation was made for each cell in compliance with the design rules of the CMOS 28nm technology in use and the cell's design guidelines as well. The area consumption of the flip-flop's layouts is shown. Finally, a PRBS generator is presented as a synthesis example by using standard cells for better understanding of the use of the standard cell's methodology. A scheme and the layout of the PRBS circuit is shown.


[‡] Bachelor degree

# INTRODUCTION

A standard cell library is the abstraction layer between a logical design coded in Hardware Description Language (HDL) and the physical layout of a circuit. Although both, the logical design and the psychical layout are responsible of the design performance, the characteristics such as maximum frequency and power consumption relies directly on the physical layout of the library[1].

Standard cells are designed following the rules of a manufacturing technology, in other words the library is not dependent upon the application design, and as a result a single library can be used as an instrument to synthesize multiple designs. Consequently a demand for commercial standard cell has risen. The commercial standard cell libraries offer different characteristics used in different applications and manufacturing technologies. In such market as the one of standard cells, intellectual property (IP) protection is a matter of interest. Therefore the library license cost restricts their access to general public[2]. On the case of academic use of libraries, limitations are higher and the range of technologies, applications and methods of implementation available are reduced as well[3].

Serious disadvantages had been described in the past about large standard cell libraries[4]. Therefore, it is of interest to develop a small standard cell library focusing on essential logical gates and basic flip-flops. In addition upgrades to existing cell specific gates or further circuits can be added on demand at any time. The advantages of having own standard cell library in a state of the art technology can benefit the CIDIC group, allowing full access to the library to add additional cells and to optimize the present ones in order to be used in future projects. Hence the production of a standard cell library desirable option over the acquisition of a commercial license.

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[1] DAS, B. and ONODERA, H. Area-efficient reconfigurable-array-based oscillator for standard cell characterization, Circuits, Devices Systems, IET [online], vol. 6, no. 6, Nov 2012 [cited 2015-11-10], pp. 429–436. Available from IEEE Xplore digital library.

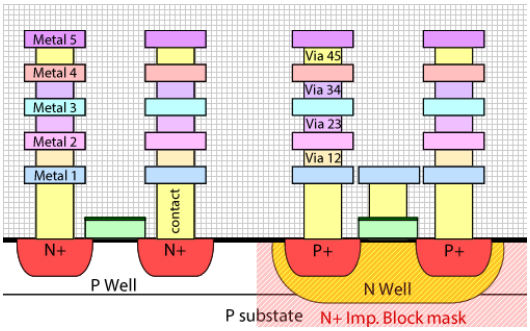
[2] GRAD, J. and STINE, J. A standard cell library for student projects, in Microelectronic Systems Education, 2003. Proceedings [online]. 2003 IEEE International Conference on, June 2003 [cited 2015-11-10], pp. 98–99. Available from IEEE Xplore digital library.

[3] DONG S., HA JOS, B. and PERRY, J. Developing Standard Cells for TSMC 0.25 um Technology with MOSIS DEEP Rules, Virginia Tech, Tech. Rep. [online], 02 2002 [cited 2015-11-10]. Available from internet http://www.vtvt.ece.vt.edu/tutorial/references/tech_report.pdf

[4] GUAN, B. and SECHEN, C. Large standard cell libraries and their impact on layout area and circuit performance, in Computer Design: VLSI in Computers and Processor, 1996. ICCD '96. Proceedings [Online]. 1996 IEEE International Conference on, Oct 1996 [cited 2015-11-10], pp. 378–383. Available from IEEE Xplore digital library.

# 1 28 NANOMETER CMOS TECHNOLOGY

FIGURE 1 28NM TECHNOLOGY CROSS SECTION




The proposed standard cell library is based on the state of the art 28nm technology. The 28nm technology is optimized for wired applications that require high performance while maintaining a low power consumption; moreover, the total area of a device may be drastically reduced as a consequence of the already reduced size of transistors that the technology offers, whose minimum gate length is 30nm -Compared to its predecessor, the 40nm foundry technology, which was introduced by TSMC in 2008-.

The 28 nm technology allows to design using transistors with channel length down to 30 nanometers, Such channel length dimensions implies a rise in the leakage currents by direct tunneling, this is mitigated by using a high dielectric constant -high K- metal as gate dielectric, which can provide higher capacitance values than the previous gate dielectric -SiO2 (silicon dioxide)-[5].

The use of a state of the art technology implies a raise in the production cost per area unit; nonetheless, this production cost raise is overcome by the benefits of the technology itself, which include the area reduction per design, due to the higher density of components; a better performance; lower parasitic capacitance values; and a higher frequency range.

## 1.1 TECHNOLOGY CHARACTERISTICS

The 28nm technology in use is a five metal layer technology driven by a nominal value of 0.85 Volts, it allows to design using transistors sized down to a minimal channel length and width of 30 and 40 nanometers respectively. Transistors of multiple threshold voltages ($Vt$)

[5] HEYNS M., BECKX S. , BENDER H. Scaling of high-k dielectrics towards sub-1nm eot, in VLSI Technology, Systems, and Applications[Online], 2003 International Symposium on, 2003 [cited 2015-11-10], pp. 247–250. Available from IEEE Xplore digital library.

-low, regular and High are available as well. A graphical description of the 28nnm foundry technology can be seen in Figure 1.

**FIGURE 2 NFET CHARACTERIZATION**

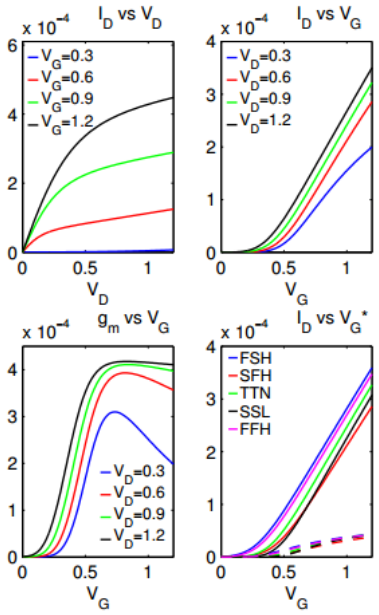
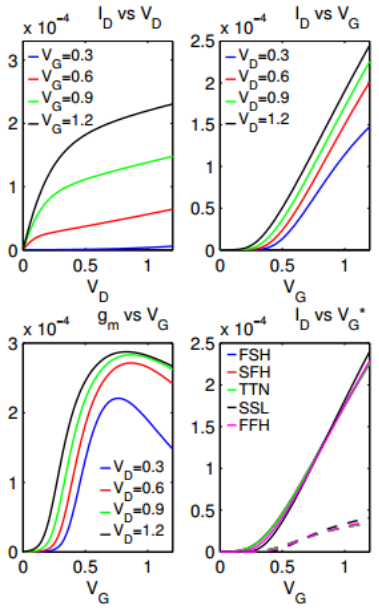



**FIGURE 3 PFET CHARACTERIZATION.**




The characteristic curves associated to regular $Vt$ N type MOSFETs can be seen in Figure 2 and the curves for regular $Vt$ P type MOSFETs can be seen in Figure 3 The top-left graph in Figure 2 and Figure 3 shows the behavior of the transistor's drain current versus a variable $Vd$ ($Id$ vs $Vd$) for different cases of gate voltage ($Vg$). The graph displays triode and saturation regions of the MOSFET.

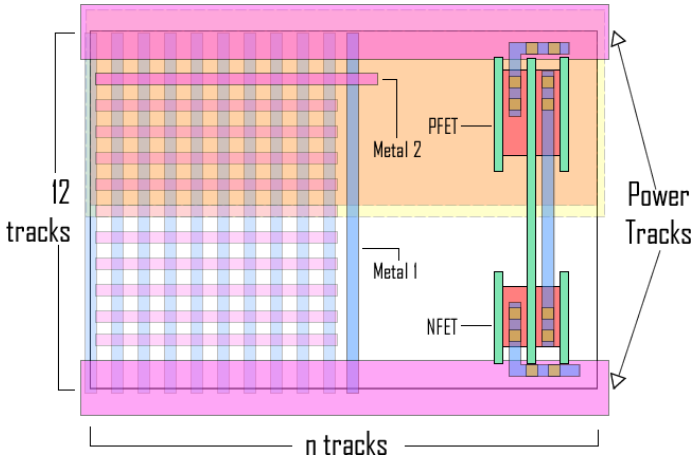
The top-right graph shows the behavior of the drain current versus a variable value of gate voltage (Id vs Vg) for different cases of drain voltage ($Vd$). The value of the MOSFET's threshold voltage is calculated by applying a straight line extrapolation in the linear zone of the graphic ( $0.7[V] < V_g < 0.9[V]$). There is an associated response of $0.4700[V]$ and $0.4657[V]$ Threshold Voltage for the N and P transistors respectively.

The bottom-left graph shows the transconductance (Gm) of the MOSFET versus a variable gate voltage (Vg), and it's obtained by deriving the top-right graph respect to Vg for different cases of$Vd$. The bottom-right graph from Figure 2 and Figure 3 shows the results of a PVT environment analysis, which comprehends corner cases such as variable voltage

and temperature conditions; and transistor mismatches, with the purpose of characterizing the MOSFET's susceptibility to a behavior change under variable conditions.

# 2 THE STANDARD CELL METHODOLOGY

FIGURE 4 STANDARD CELL LAYOUT VIEW




Cell based design methodologies were developed with the purpose of improving prototyping and chip area efficiency. Among these methodologies, the standard cell based one is the most widely used methodology for ASICs (Application Specific Integrated Circuits) design. This methodology uses a set of different pre designed standardized cells, and each cell maps a high level component -such as a logic gate- into a circuit layout -the cell's geometric characteristics-. These cell layouts can be interconnected in order to describe a larger circuit (Each cell may be used more than once); for example, the layout representation of a latch circuit can be described by interconnecting the layouts of two NAND gates.

When a set of standard cells are designed under the same technology, design rules and guidelines, they are called a standard cell library. A library is used to synthesize into layout a circuit described in HDL, this circuit is composed of an array of cells interconnected (by a process called routing) which can be instanced multiple times on the circuit. Since the array of standards cells, as a group, they need to be designed to satisfy the technology rules and, in addition to having enough space to allow the routing process to interconnect the cells without compromising area consumption.

The use of standard cells is highly beneficial to digital design flow. For example it is possible to use a single standard cell library in multiple projects; and the standardization of the cells allows automated tools to take care of the circuit's routing with a better handling of computational resources. These benefits turn each library into a high value IP.

Since a standard cell library is a high value intellectual property, using a commercial library becomes very difficult due to the licenses cost. In addition, the developer doesn't have full control over the cells that belong to these commercial libraries; therefore, in most cases it becomes viable to develop an owned standard cell library. By owning the standard cell library, the developer has full control on the number, type and layout of the cells; and consequently, possibilities like expanding the library to cover new applications, review and improve each cell capabilities are available.

- *Scope selection:* In order to develop a functional set of standard cells, the designer must first focus on the scope of the library in terms of its characteristics. With this in mind the cells first topologies can be chosen. The first topologies added to a standard cell library are usually logic gates and flip flops. If a circuit or array is going to be used many times in a project, a standard cell can be dedicated to it.
- *The Schematic Design:* The topology of a selected circuit is simulated using the transistor's models for the used technology. These simulations are made considering several operating conditions, known as corners, and the transistor's sizes are tuned for the final design in order to ensure the application requirements are met.
- *The Layout Design:* The layout view is the definition of the schematic circuit's geometrical characteristics. During this definition, implants, wells, metals and polysilicon layers are placed in order to shape the transistors and the circuit itself. The layout design is restricted by a set of rules, which are defined by the technology and sometimes by the manufacturer. For example, the minimum space between two metal tracks. During the layout step of the design flow, the developer defines the cells' standard characteristics, such as the cells' height.
    - *Metals:* The 28nm foundry technology has 5 available metal layers, which can be used to realize the ASIC's layout routing. Every metal layer has an associated set of design rules to be followed. The first two metal layers, from now on referred to as Metal 1 and Metal 2, are the ones used for the basic routing of the gates. Specifically, Metal 1 is used to route the gate and locate all input and output pins, while Metal 2 is mainly used for supply and ground tracks. The proposed library has two 0.22um wide horizontal Metal 2 tracks, separated by a 1,182um gap. One of these tracks is connected to the supply voltage and the other one is connected to the ground voltage of the circuit.
    - *Standard Cell's height:* The proposed standard cell library has a defined cell's height of 12 Metal 2 tracks (resulting in a cell's height equal to 1,402um). This height is measured by taking into account the minimum gap between 0.05um wide metal 2 tracks and the minimum gap between $Vdd$ or ground metal 2 track and an adjacent 0.05um wide metal 2 track. Metal 2 routing is only used when necessary since automated routing tools use this layer in

order to be able to access the cell's input and output pins, which are connected to metal 1 wires.

  - *Standard Cell's width:* The width of a standard cell has to be a multiple of the minimum width of a metal 1 track, which is 0,05um. Due to this requirement, the width of a standard cell is defined by the next multiple value of a metal 1 track. By applying these requirements, automated tools can optimize the use of resources for routing. A physical analogue of the schematic circuit is made by setting the location of wells, implants, polysilicon and metal by following guidelines that ensure the standardization of cells hence the compatibility between them in the synthesis process, reducing the capacitance as well and optimizing the routing spaces.

- *The Layout and schematic comparison:* A layout versus Schematic (LVS) comparison process is used to determine if the physical design on the layout corresponds to the topology on the schematic.
- *The parasitic extraction and simulation:* The final step on the development of a single standard cell involves a parameters extraction, which includes the many parasitic capacitances and resistors that result from the layout design. After these parameters are extracted, they're added to the simulation setup in order to make a post-layout simulation including the effects of the characteristics and setup of materials. A feedback is then realized between the layout creation and the post layout simulation steps, in order to check that application requirements are met.
- *The Library Synthesis:* After all cells are finished, the library and simulation data are synthesized, resulting on a library file that the application designer can use.

# 3 THE DESIGNED STANDARD CELL LIBRARY

TABLE 1 CONTENTS OF THE LIBRARY

| | |
|---|---|
| Flip -flop | DFFRE<br>SAFFRE<br>TSPCFFRE |
| Inverters | INV1x, INV2x, INV4x, INV8x |
| Primitive Gates | NAND1x, NAND2x<br>NOR1x, NOR2x |
| Fillers | Fill tie<br>MOSCAP |

The proposed library includes a total of thirteen cells listed in table I , which are divided into o categories called ”Static Cells” and ”Dynamic Cells”. The standard cells are categorized as follows:

## 3.1 STATIC CELLS

The static cells category includes static behavior logic gates, which means the output value of the logic gate is the result of the Boolean function it represents. Moreover, an inverter based D Flip Flop is added to this category. The cells included to this category are mentioned below:

### 3.1.1 NOT Gate

FIGURE 5 NOT GATE SCHEMATIC

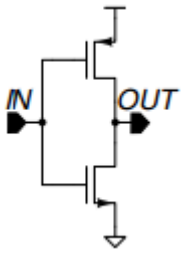



TABLE 2 NOT GATE SUMMARY

| INV | 1x | 2x | 3x | 4x |
|---|---|---|---|---|
| Max. Freq. | $14.8Ghz$ | $12.8Ghz$ | $13.6Ghz$ | $13.0Ghz$ |
| R.O. Delay | $12.20ps$ | $14.31ps$ | $13.96ps$ | $14.32ps$ |
| F.O. Delay | $13.23ps$ | $14.10ps$ | $13.83ps$ | $15.24ps$ |

The NOT gate is a single input, single output logic circuit whose output is the inverted logic value of the input. It is formed by a PMOS pull up transistor and a NMOS pull down transistor. Both transistors share a gate connection and a drain connection, as shown in Figure 5.

### 3.1.2 NAND Gate

FIGURE 6 NAND GATE SCHEMATIC

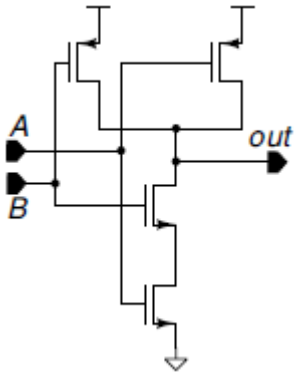



TABLE 3 NAND GATE SUMMARY

| NAND | 1x | 2x |
|---|---|---|
| Max. Freq. | $9.2GHz$ | $10.1hz$ |
| R.O. Delay | $13.064ps$ | $11.959ps$ |
| F.O. Delay | $20.901ps$ | $20.488ps$ |

The NAND or Negative AND gate is a logic circuit whose output is a logic low voltage only when all inputs are a logic high voltage. In any other case, the NAND gate's output is a logic high voltage. The main advantage of NAND gates is that it is possible to implement any Boolean function with a combination of them. The schematic of the NAND gate shows four transistors. The NMOS transistors act as a series pull down net, which fully activates when inputs A and B are have a high logic voltage. The PMOS transistors tie the output node to $Vdd$ when either A or B are 0. The NAND gate's schematic is shown in Figure 6.

### 3.1.3 NOR Gate

FIGURE 7 NOR GATE SCHEMATIC

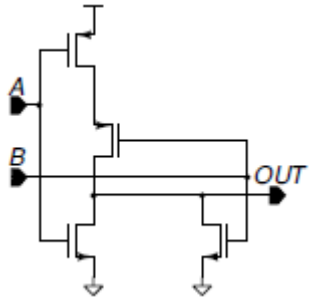



TABLE 4 NOR GATE SUMMARY

| NOR | 1x | 2x |
|---|---|---|
| Max. Freq. | $7.4GHz$ | $10.4Ghz$ |
| R.O. Delay | $25.27ps$ | $20.477ps$ |
| F.O. Delay | $25.20ps$ | $19.611ps$ |

The NOR or Negative OR gate is a logic circuit whose output is a logic high voltage only when all inputs are a logic low voltage. In any other case, the NOR gate's output is a logic low voltage. The main advantage of NOR gates is also that it is possible to implement any

Boolean function with a combination of them. The NOR gate's schematic gate shows four transistors. The NMOS transistors tie the output node to ground whenever any input is a logic 1 and the PMOS transistors can only tie the output node to $Vdd$ if both inputs A and B are a logic low. The NOR gate's schematic is shown in Figure 7.

### 3.1.4 Pass-Gate Based D Flip Flop

FIGURE 8 DFFRE SCHEMATIC

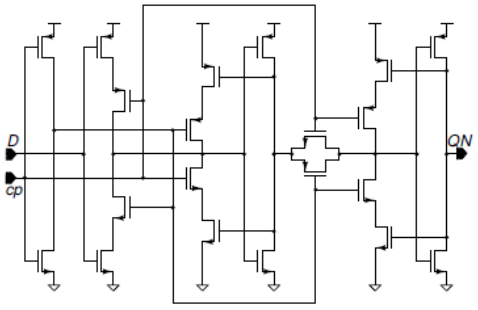



TABLE 5 DFFRE SUMMARY

| DFFRE | | LAYOUT | |
|---|---|---|---|
| Max. Freq. | $11.3GHz$ | Cell's Width | $2.60um$ |
| Hold Time | $61.40ps$ | Cell's Height | $1.402um$ |
| Setup Time | $18.79ps$ | Total Area | $3.645um^2$ |
| R.O. Delay | $37.14ps$ | Used Rails | 1 |
| F.O. Delay | $40.670ps$ | | |

The pass gate based flip- flop is a fully inverter based which uses a pass gate, the clock controls a set of latched inverters in order to charge the data on the flip flop when clock is not on rising edge and to hold the data and deliver it to a holding circuit while on rising edge. The data is delivered to the holding circuit by a pass gate connected to the clock and the negated clock, while the data is not updated the holding circuit will feedback itself to maintain the data.

### 3.1.5 Fill Tie

A Fill Tie is a cell that only contains PMOS body to $Vdd$ and NMOS body to $Vss$ connections. It is necessary to use a fill tie cell when developing a standard cell based design, since the gates themselves don't have a body connection. The fill tie is a compact cell, and can be used as many times as necessary in order to allow a better body connection to large circuits or arrays.

### 3.1.6 MOS Cap

A MOS Cap is a cell designed to add a capacitance between $Vdd$ and $Vss$ with the purpose of stabilizing DC signals.

### 3.1.7 Tie Up and Tie Down

The NMOS transistors gate oxide is a thin and sensitive layer which sometimes needs to be tied to $Vdd$ or$Vss$, depending on the logic level. But being tied up directly to Vdd or Vss implies that an unwanted behavior on the supply voltage may be harmful for the transistor's gate. In order to protect these transistors' gates, Tie Up and Tie Down cells are used. These cells replace the transistor's gate direct connection to either $Vdd$ or $Vss$ and instead they are connected to a fill tie cell.

## 3.2 DYNAMIC CELLS

The Dynamic Cells category includes Flip Flop circuits which show a dynamic behavior due to the use of temporarily stored information in some of the circuit's nodes as pre-charge operation. The cells included to this category are mentioned below.

### 3.2.1 True Single-Phase Clock Flip-flop

FIGURE 9 TSPC SCHEMATIC

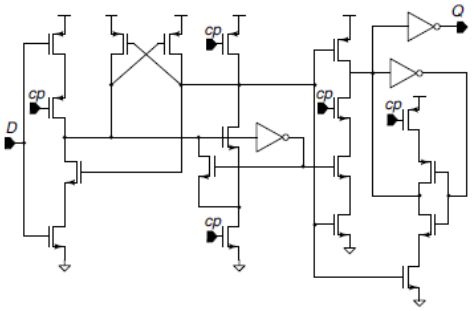



TABLE 6 TSPC SUMMARY

| TSPC | | LAYOUT | |
|---|---|---|---|
| Max. Freq. | $13.5GHz$ | Cell's Width | $6.169um$ |
| Hold Time | $3.88ps$ | Cell's Height | $3.803um$ |
| Setup Time | $19.38ps$ | Total Area | $17.375um^2$ |
| R.O. Delay | $40.851ps$ | Used Rails | 2 |
| F.O. Delay | $31.41ps$ | | |

The true single phase clock static contention free flip-flop proposed in[6], from now TSPCFF which aims to a lower hold and setup times by using a non-delayed clock to act on the transistors effective in the critical path. The TSPCFF is composed from 4 sections, a first one which as a not gate when Clock is low, a second one which holds the data on high clock and deliveries the data on rising edge to a third section called the keeper which holds the data received and finally passing the data to an unbalanced not gate that adjusts rise and fall times as cleans the signal. TSPCFF advantages other flip flop designs on reducing hold time, reduced power consumption and by being voltage-scalable.

[6] KIM, Y., JUNG W., LEE I., DONG, Q., HENRY M., SYLVERSTER D. and BLAAUW D. 27.8 a static contention-free single-phase-clocked 24t flip-flop in 45nm for low-power applications, in Solid-State Circuits Conference Digest of Technical Papers (ISSCC) [Online], 2014 IEEE International, Feb 2014 [cited 2015-11-10], pp. 466–467. Available from IEEE Xplore digital library.

### 3.2.2 Strong Arm Flip-flop

FIGURE 10 SAFF SCHEMATIC

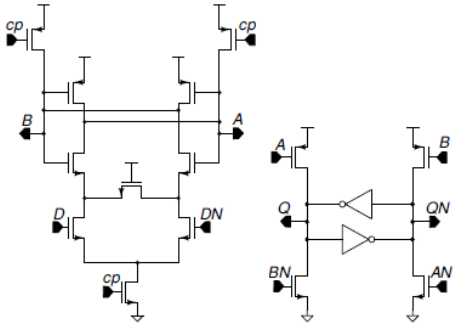



TABLE 7 SAFF SUMMARY

| SAFF | | LAYOUT | |
|---|---|---|---|
| Max. Freq. | $18.3GHz$ | Cell's Width | $16.30um$ |
| Hold Time | $6.45ps$ | Cell's Height | $7.01um$ |
| Setup Time | $9.35ps$ | Total Area | $11.263um^2$ |
| R.O. Delay | $37.14ps$ | Used Rails | 5 |
| F.O. Delay | $31.217ps$ | | |

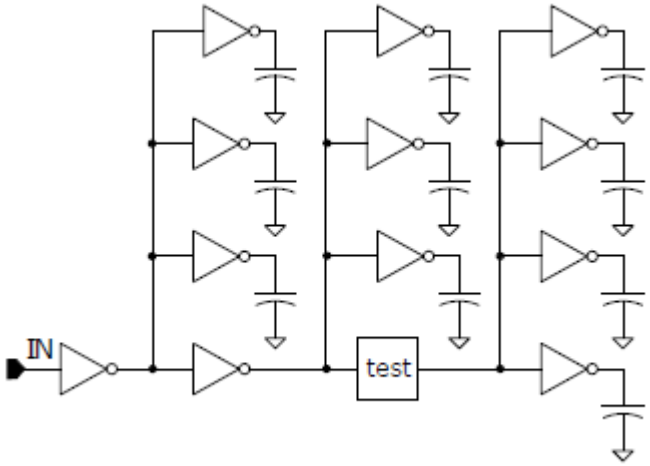
The strong arm latching comparator proposed in Figure 10, from now on referred to as SAFF (strong arm flip flop) is a widely used circuit which has the ability to regenerate small signals into one of its two stable states -$Vdd$ or $Vss$- and consuming no power when in one of these states. The latched comparator is by definition a symmetric circuit, which means it shouldn't have any unbalances[7]. These unbalances do exist on real applications, and they are presented as mismatch. This mismatch mostly affects the input transistors pair, since they are acting as amplifiers. Due to these mismatch unbalances, an amplified offset voltage is generated in the circuit, and thus, the circuit will regenerate the input into one of the stable states. The higher this offset is, the higher chance that the circuit regenerates an undesired signal and delivers a wrong output[8].

[7] KAWAI N., TAKAYAMA S., MASUMI J., KIKUCHI N., ITOH Y., OGAWA K., UGAWA A., SUZUKI H. and TANAKA Y. A fully static topologically compressed 21-transistor flip-flop with 75% power saving, in Solid-State Circuits Conference (ISSCC) [Online], 2014 IEEE Asian, Nov 2013 [cited 2015-11-10], pp. 117–120. Available from IEEE Xplore digital library.

8 ABIDI A. and XU H. Understanding the regenerative comparator circuit, in Custom Integrated Circuits Conference (CICC) [Online], 2014 IEEE Proceedings of the, Sept 2014 [cited 2015-11-10], pp. 1–8. Available from IEEE Xplore digital library.

# 4 SIMULATION RESULTS

FIGURE 11 FANOUT-OF-FOUR SIMULATION SETUP




All simulations were made through a fan out (FO) setup. When in a FO setup, a frequency sweep was run in order to determine each gate's maximum frequency. Afterwards, the gate's characterization was made while operating at maximum frequency. A Fan-Out 4 (FO4) simulation setup is presented in Figure 11.

## 4.1 NOT GATE

FIGURE 12 NOT GATE AT 14.79GHZ

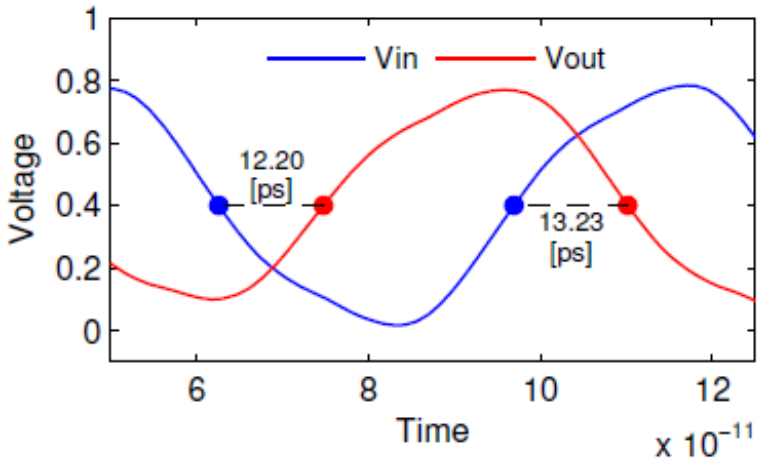
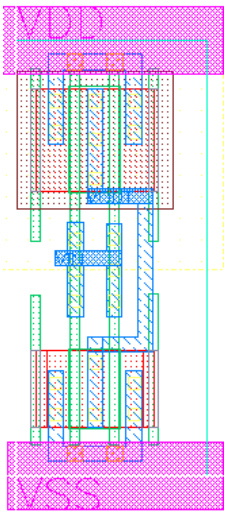


FIGURE 13 NOT GATE LAYOUT




The NOT gate, shown in Figure 5, is obtained with one PMOS and one NMOS transistor, and it was simulated with a FO4 setup. Initially, a first simulation was focused on determining the most useful size ratio between the NMOS and PMOS transistors' channel width. This size ratio had to result in a balanced delay response between the gate's input and output, which means the delay between a rising input and the output; and the delay between a falling input and the output should be as similar as possible. This way, it was guaranteed that the PMOS and NMOS transistor's pull strength (pull up and pull down, respectively) was as well balanced. Once both PMOS and NMOS transistors' channel width was determined, a second simulation was run, involving a frequency sweep and resulting in the determination of the gate's maximum frequency. The second simulation was repeated for different transistor's multiplier values and the multiplier for which the gate exhibited the higher peak of maximum frequency was chosen as the NOT gate 1X. Once these steps were followed, NOT gates 2X, 4X and 8X were defined by escalating the 1X NOT gate's configuration, in order to get NOT gates with a higher load capability. The characterization of a basic NOT1x cell can be seen at **¡Error! No se encuentra el origen de la referencia.** and its layout view at Figure 13, all developed NOT gates can be seen in Table 2.

## 4.2 NAND GATE

FIGURE 14 NAND GATE AT 8.26GHZ

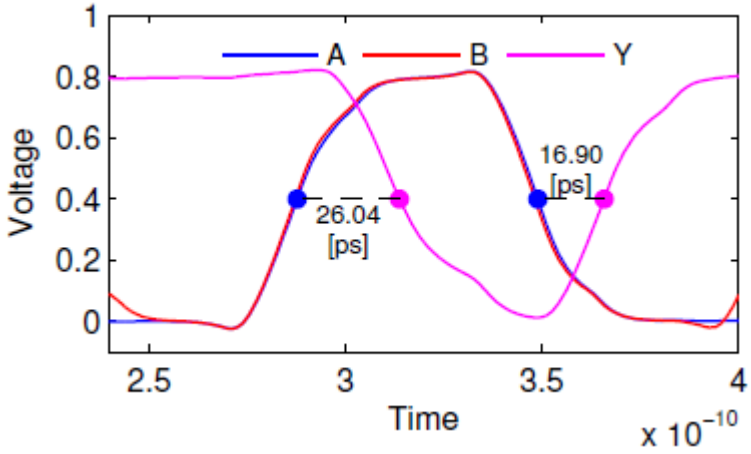
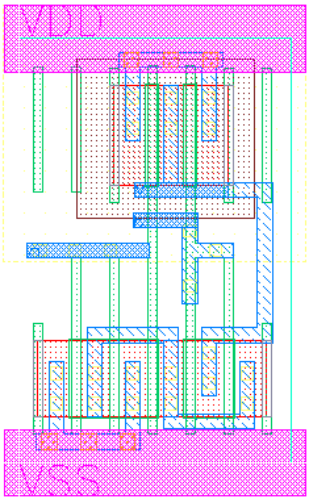



FIGURE 15 NAND GATE LAYOUT




Initially, the parallel pair of PMOS transistors showed more strength when pulling the output up to $Vdd$ than the series NMOS pair pulling the output node to ground, as a consequence of the resistance seen from the output node towards both paths. Consequently, the number of fingers of the NMOS transistors were raised in order to give more strength to the NMOS pair when pulling the output to ground; and as a consequence, improving the high frequency performance of the gate. The characterization of the NAND1x gate can be seen at Figure 14, its layout at Figure 15 and the resulting characteristics of all the NAND cells at Table 3.

### 4.3 PASS-GATE BASED D FLIP-FLOP

FIGURE 16 DFFRE AT 11.3GHZ

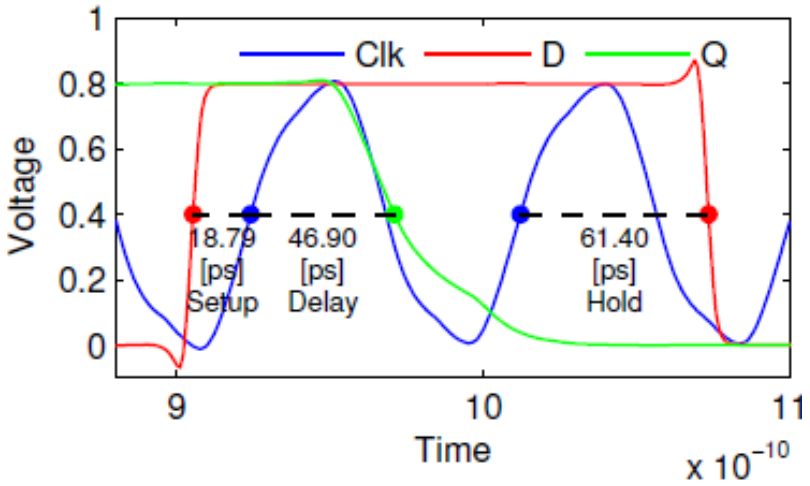
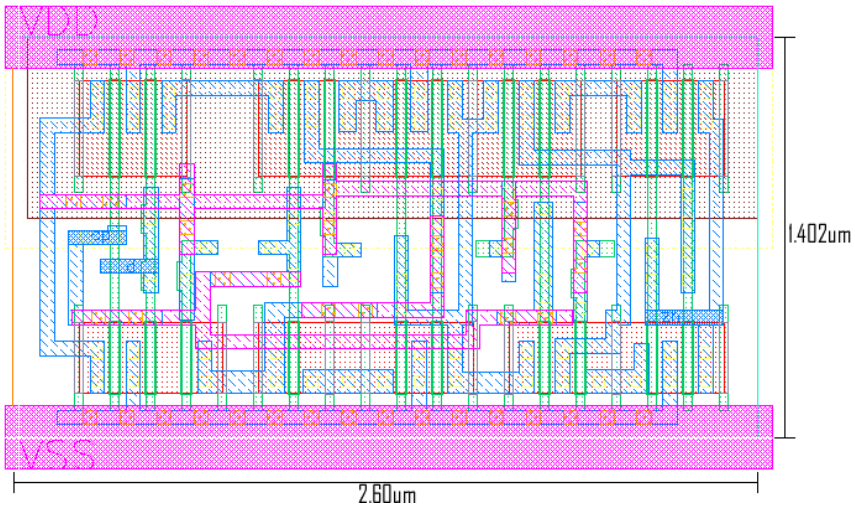



FIGURE 17 DFFRE LAYOUT




The implemented Pass gate based type Flip Flop (DFF) topology is based on latched inverters. During the simulation, it was noticed that a 1X configuration showed better frequency results than slightly modified version of the DFF's transistors. The characteristics of the pass gate flip flop can be seen at Figure 16 and Table 5, the layout view can be seen at Figure 17 DFFRE layout.

## 4.4 STRONG ARM FLIP FLOP

FIGURE 18 SAFF AT 18.3GHZ

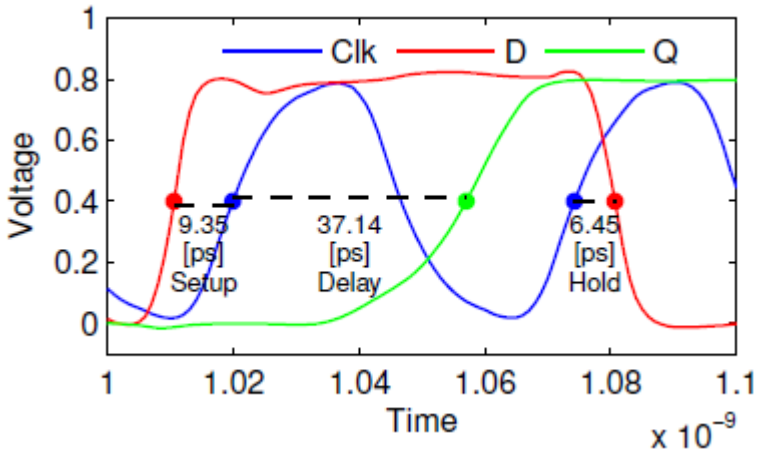
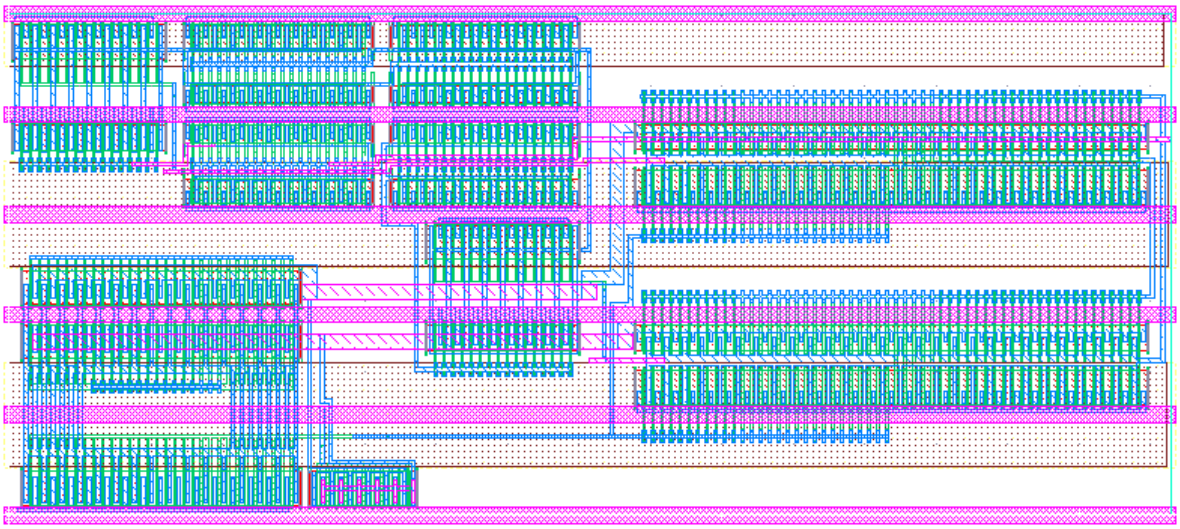



FIGURE 19 SAFF LAYOUT



The Strong Arm Flip Flop (SAFF) is a symmetric circuit by definition, and because of this, simulations were made by varying pairs of transistors. Additionally, simulations were made using a Fanout 1 (F01) setup. Initially, in order to reduce the input transistor's offset, the number of fingers for this pair was raised. As a consequence, the total resistance that these transistors showed was highly reduced, and the current flow through them was raised. With the purpose of balancing the circuit, all other transistors' finger number were raised, especially, those through which the current flow was as high as in the input transistor's (or

closer). Input and clocked transistors were the mostly affected. Due to the SAFF's size raise, NOT 1X gates weren't able to handle it as load and it was needed to realize fan out simulations with NOT 8X gates. The strong arm simulation results can be seen at Figure 18 and Table 7, As the strong arm flip flop size and power consumption are considerably higher an special multilevel layout was made in Figure 19.

# 5 SYNTHESIS OF A PRBS GENERATOR

FIGURE 20 PRBS GENERATOR SCHEMATIC

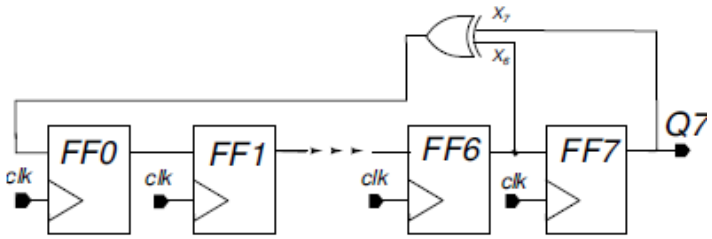
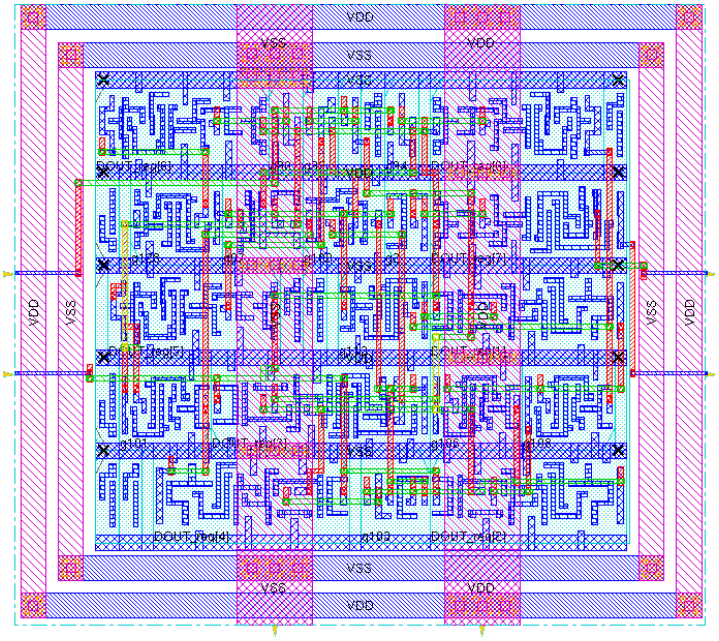



FIGURE 21 PRBS GENERATOR SYNTHESIS LAYOUT




An example of synthesis using standard cells can be seen at figure 18; an 8 bit pseudo random binary sequence (PRBS) generator is made using a linear feedback shift register (LFSR) in addition a XOR gates to disrupt the bit rotation. The location of the XOR gate is located in order to maximize the length of the PRBS. A polynomial can be used to represent the generating sequence:

$$Q7 = x^7 + x^6 + 1$$

The previous expression's schematic representation can is represented in Figure 20 and the result of the synthesis can be seen in Figure 21.

# 6 CONCLUTIONS

A Standard cell library developed in the state of the art 28nm technology is proposed. Library's cells include basic logical circuits such as NOT, NAND and NOR gates; and flip-flops such as Pass Gate Based, Strong Arm and True Single Phase Clock. A set of basic logic gates was designed. Four versions of the NOT gate were included with the purpose of giving the library the ability of handling higher loads. These versions are 1x, 2x, 4x and 8x NOT gates, which work with frequencies over 12.8 GHz and delays lower than 16 picoseconds. The proposed flip-flops reached a maximum frequency over 11 GHz each one; the strong arm and the TSPC flip-flops reached maximum frequencies of 18.3 GHz and 13.5 GHz, which is 61.95% and 13.5% faster than the Pass gate based flip-flop respectively. All flip-flops rising output and falling output delays were ranged from 30 to 40 picoseconds. Layout, schematic, and symbol views are available in the .library including simulation setups.

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