ADVANCED LAYOUT AND SENSITIVITY ANALYSIS OF A VOLTAGE COMPARATOR IN 28NM CMOS TECHNOLOGY

MICHEL YURANY SAENZ LOPEZ
DUVAN NICOLAS GOMEZ DIAZ

UNIVERSIDAD INDUSTRIAL DE SANTANDER
FACULTAD DE INGENIERÍAS FISICOMECÁNICAS
ESCUELA DE INGENIERÍA ELÉCTRICA, ELECTRÓNICA Y DE TELECOMUNICACIONES
BUCARAMANGA
2026

ADVANCED LAYOUT AND SENSITIVITY ANALYSIS OF A VOLTAGE COMPARATOR IN 28NM CMOS TECHNOLOGY

MICHEL YURANY SAENZ LOPEZ
DUVAN NICOLAS GOMEZ DIAZ

Degree work presented as a requirement to qualify for the title of Electronic Engineer

Advisor:
JAVIER FERNEY ARDILA OCHOA
PhD in Engineering

UNIVERSIDAD INDUSTRIAL DE SANTANDER
FACULTAD DE INGENIERÍAS FISICOMECÁNICAS
ESCUELA DE INGENIERÍA ELÉCTRICA, ELECTRÓNICA Y DE TELECOMUNICACIONES
BUCARAMANGA
2026

Dedicated to our families and friends.

And to our team, with whom we started and finished this amazing journey.

ACKNOWLEDGEMENTS

I would like to express my deepest gratitude to my parents Sonia and Edgar, and my sister Katheryn for the teachings they have instilled in me and for shaping the person I am today. Your unconditional support, love, and belief in me have been the foundation of this achievement; without your encouragement and example, this journey would not have been possible.

I am profoundly grateful to my partner Michel Saenz, who walked by my side throughout this entire process. Thank you for your constant company during long nights, for your patience, and for the encouragement you provided during every assignment, project, and challenge that led me to this point. Your support was invaluable in reaching this goal.

I extend my sincere thanks to the research group Onchip for providing the tools, spaces, and training that made the development of this project possible. I am deeply thankful to my advisor Javier Ardila and the friends who guided me. Thank you for your valuable insights, which significantly contributed to the completion of this work.

Finally, I wish to honor those who have been part of my life and influenced my path. Their memory and influence remain a constant reminder that life must be lived fully. To everyone who contributed to this work and supported me along the way, thank you for helping me close this chapter of my life today.

- Duván Nicolás Gómez Díaz

ACKNOWLEDGEMENTS

It is incredible how many people have been a fundamental part of this academic and formative journey. First and foremost, I am grateful to God for allowing me to gain so much knowledge during this stage of my life. I am deeply thankful to my grandfather Álvaro, who was a fundamental and motivational pillar at the beginning of this path; my sincerest gratitude goes to my mother Laura, who motivated me every day with her perseverance and courage; to my father Yimi, for instilling in me the values and principles that guide my life; and to my siblings Sheslly and Joel for being a constant source of support. Infinite thanks to my family for their unconditional support; they helped me countless times throughout this process and journey, supporting and backing everything I do.

I would like to thank my thesis advisor Javier Ardila, who, through his vocation, opened the doors to the fascinating world of microelectronics, sharing his knowledge in an inspiring way throughout his classes. I admire his vision and the passion with which he takes on challenges and achieves them.

A special thank you to my thesis partner Nicolás Gómez for his patience, collaboration, and discipline; his support was key in making this possible. It was a great pleasure for me to work in the OnChip group. I would like to thank all the current and former members of the group for the exchange of ideas.

Beyond the professional and research aspects, there are many friends who have enriched my daily life. They are Adriana Velásquez, Gabriela Tolosa, Daniela Mesa and Leidy Ramírez who have constantly been part of this process, providing me with emotional support, brightening my days, and helping me step away from the routine from time to time.

- Michel Yurany Saenz Lopez

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

Page.

RESUMEN

TÍTULO: DISEÑO AVANZADO DE LAYOUT Y ANÁLISIS DE SENSIBILIDAD DE UN COMPARADOR DE VOLTAJE EN TECNOLOGÍA CMOS DE 28NM [*]

AUTHORS: MICHEL YURANY SAENZ LOPEZ
DUVAN NICOLAS GOMEZ DIAZ [**]

PALABRAS CLAVE: Controlador PWM, CMOS, Comparador Estático, Análisis de Sensibilidad, Efectos Dependientes de Layout.

DESCRIPCIÓN:

Este trabajo aborda la mejora del diseño de un comparador de voltaje para disminuir variaciones en los parámetros de este mediante la aplicación de técnicas avanzadas de layout y análisis de sensibilidad, orientado a un controlador PWM analógico para un convertidor DC-DC reductor en tecnología CMOS de 28 nm. En nodos tecnológicos avanzados, la variabilidad del proceso y los efectos dependientes del layout (LDE), como Shallow Trench Isolation y Well Proximity Effect, afectan significativamente el comportamiento de los circuitos analógicos, impactando la precisión de conmutación, el retardo y la eficiencia energética. El comparador de referencia se caracteriza inicialmente mediante simulaciones PVT y Monte Carlo con el fin de evaluar su robustez, presentando una sensibilidad reducida ante las variaciones de los parametros de rendimiento. Posteriormente, se realiza un análisis de sensibilidad para identificar los parámetros más críticos que influyen en la velocidad de conmutación y la variabilidad. A partir de estos resultados, se procede al rediseño del circuito y a la implementación del layout empleando estrategias orientadas a mitigar LDE y el desajuste entre dispositivos. Finalmente, se lleva a cabo una verificación completa post-layout, que incluye extracción parasitaria, análisis PVT y simulaciones Monte Carlo, con el propósito de comparar cuantitativamente el rediseño frente al diseño de referencia, garantizando el cumplimiento de las especificaciones establecidas.

---

[*] Trabajo de Grado

[**] Facultad de Ingenierías Físico-Mecánicas. Escuela de Ingenierías Eléctrica, Electrónica y de Telecomunicaciones. Director: JAVIER FERNEY ARDILA OCHOA

ABSTRACT

TITLE: ADVANCED LAYOUT AND SENSITIVITY ANALYSIS OF A VOLTAGE COMPARATOR IN 28NM CMOS TECHNOLOGY [*]

AUTHORS: MICHEL YURANY SAENZ LOPEZ
DUVAN NICOLAS GOMEZ DIAZ [**]

KEYWORDS: PWM Controller, CMOS, Static Comparator, Sensitivity Analysis, Layout Depends Effects.

DESCRIPTION:

This work addresses the design improvement of a voltage comparator to reduce variations in its parameters through the application of advanced layout techniques and sensitivity analysis, oriented toward an analog PWM controller for a buck DC-DC converter in 28 nm CMOS technology. In advanced technology nodes, process variability and layout-dependent effects (LDE), such as Shallow Trench Isolation and Well Proximity Effect, significantly affect the behavior of analog circuits, impacting switching precision, delay, and energy efficiency. The baseline comparator is initially characterized using PVT and Monte Carlo simulations to evaluate its robustness, presenting a reduced sensitivity to variations in performance parameters. Subsequently, a sensitivity analysis is performed to identify the most critical parameters influencing switching speed and variability. Based on these results, the circuit is redesigned and the layout is implemented using strategies aimed at mitigating LDE and device mismatch. Finally, a complete post-layout verification is carried out, including parasitic extraction, PVT analysis, and Monte Carlo simulations, with the purpose of quantitatively comparing the redesign against the reference design, ensuring compliance with the established specifications.

---

[*] BSc Thesis

[**] Facultad de Ingenierías Físico-Mecánicas. Escuela de Ingenierías Eléctrica, Electrónica y de Telecomunicaciones. Advisor: JAVIER FERNEY ARDILA OCHOA

INTRODUCTION

System-on-Chip (SoC) architectures integrate multiple functional blocks that operate at different voltage levels to achieve optimal performance, which requires highly precise power management strategies. In this context, DC-DC buck converters are essential components, as they efficiently regulate and adapt voltage levels derived from a primary source, such as a battery, in order to meet system requirements while maintaining high energy efficiency. [1]

Within this power management architecture, DC-DC buck converters rely on closed-loop control architectures to ensure accurate voltage regulation. Specifically, this project is developed within the context of the TangaraR chip, a DC-DC converter block designed in 28 nm CMOS technology. The TangaraR circuit employs a control architecture based on a Pulse Width Modulation (PWM) controller, which determines the switching behavior of the power stage. The voltage comparator is one of the critical decision blocks within this control loop, as it defines the exact switching instant by converting analog differences between a reference ramp and an error signal into a digital output. [2]

In advanced technology nodes, such as 28 nm CMOS, the design of analog circuits faces heightened sensitivity to process variations and Layout-Dependent Effects (LDE). As the physical dimensions of transistors shrink, physical phenomena such as the Well Proximity Effect (WPE) and Shallow Trench Isolation (STI) stress become prominent. Because these effects alter carrier mobility and threshold voltages depending on the exact physical placement and spacing of the devices, they lead to increased mismatch and offset, ultimately degrading the circuit's accuracy and overall robustness. [3]

---

[1] Over Jose AMAYA AMAYA and Victor Hugo MUÑOZ LÓPEZ. "Design of Base-Band Circuits for a PWM Controller in a DC-DC Buck Converter in CMOS Technology node of 28nm". Bachelor's thesis. Universidad Industrial de Santander, 2024.

[2] Luigi Iannelli FRANCESCO VASCA. *Dynamics and Control of Switched Electronic Systems*. Prentice Hall, 2012.

Due to these challenges, this project focuses on improving the robustness and performance of the voltage comparator through the application of advanced layout techniques and sensitivity analysis. The objective is to identify the specific variables that induce variability in the switching speed, employing mitigation strategies such as common-centroid structures, the use of dummy devices, and guard rings to reduce mismatch and parasitic effects. Through a methodology that includes baseline design characterization, circuit redesign, and post-layout verification, the goal is to ensure that the comparator operates reliably under process, voltage, and temperature variations (PVT) and Monte Carlo simulations, while meeting the specified power consumption metrics and defined switching time requirements.

The remainder of this document is organized as follows. Chapter 1 presents the project overview, including the design specifications. Chapter 2 describes the sensitivity analysis. Chapter 3 details the circuit design methodology and the implementation of advanced layout techniques. Chapter 4 presents the simulation results. Finally, the main conclusions of this work are summarized.

[3] M. L. Kniffin P. G. DRENNAN and D. R. LOCASCIO. Implications of Proximity Effects for Analog Design. In: *IEEE Custom Integrated Circuits Conference (CICC)*. 2006, pp. 1–5.

1. OBJECTIVES

1.1. GENERAL OBJECTIVES

To enhance the robustness and performance of a Voltage Comparator by applying advanced layout techniques and sensitivity analysis in 28 nm CMOS technology.

1.2. SPECIFIC OBJECTIVES

Review and characterize the baseline Voltage Comparator design measuring robustness through PVT and Monte Carlo simulations .

Study and document the main advanced layout techniques to mitigate layout dependent effects (LDE) in advanced nodes.

Redesign the layout using advanced layout techniques.

Perform post-layout verification and comparison with the baseline design including PVT and Monte Carlo simulations.

2. PROJECT OVERVIEW

The central objective of this project is to improve the robustness and performance of a voltage comparator through advanced layout techniques and sensitivity analysis in 28 nm CMOS technology. This component is the critical decision block within a Pulse Width Modulation (PWM) controller, which is essential for voltage regulation in integrated DC-DC Buck converters for System-on-Chip (SoC) architectures.

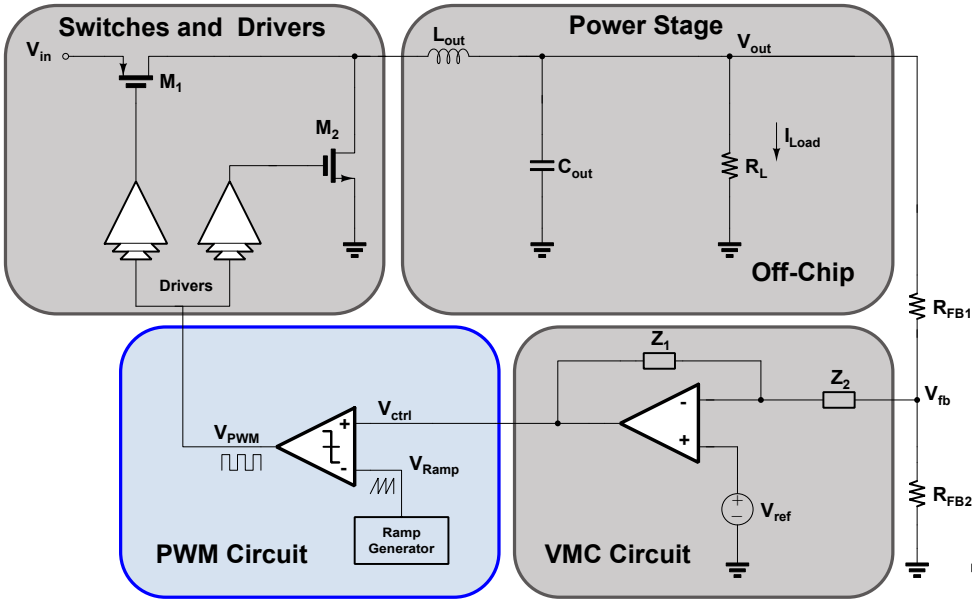
2.1. DC-DC BUCK CONVERTER

A DC-DC Buck converter transforms a DC input voltage into an output voltage of lower magnitude with high efficiency. To maintain this constant voltage against load variations, it utilizes a closed-loop control system, as shown in Figure **2.1**. This topology consists of a power stage composed of an LC filter, which supplies the regulated voltage to the load. A control loop operates through the Voltage Mode Control (VMC) block, processing the difference between the feedback signal and a precision reference. The resulting control signal is compared against a periodic ramp within the PWM circuit to define the duty cycle. Finally, this modulation drives the controllers (drivers) of the switching elements (PMOS and NMOS transistors) and an output filter, operating between two states: Mode 1, where the inductor is charged, and Mode 2, where it discharges toward the load. To maintain a constant voltage against variations in the load or the line, the converter requires a closed-loop control system that corrects deviations in real-time. [4]

---

[4] Yuan CHEN et al. A General Frequency-Domain Model of Trailing-Edge and Leading-Edge Carrier PWM dc–dc Converter Based on Hybrid Continuous and Discrete-Time Descriptions. In: *IEEE Journal of Emerging and Selected Topics in Power Electronics*. 2021, vol. 9. DOI: 10.1109/JESTPE.2020.2982179.

Figure 2.1. DC-DC Buck Converter.



Source [1].

2.2. PULSE WIDTH MODULATOR

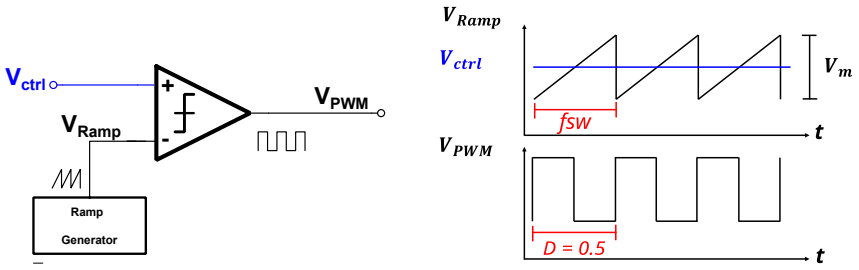
PWM is the predominant method for controlling power delivery in switching converters. It is generated by comparing an analog error signal (V_{ctrl}), which represents the output voltage deviation, with a periodic carrier signal (V_{ramp}), as seen in Figure **2.2**. The resulting duty cycle is the ratio of the time the switch is on, as defined in (1), where Vm is the amplitude of the ramp.[5]

$$D = \frac{V_{ctrl}}{V_m} \tag{1}$$

To achieve this duty cycle, there are various modulation techniques; however, falling-edge mod-

[5] Min-Chin LEE and Yi-Chiuan CHEN. Implementation of a ramp generator with Schmitt trigger circuit for PWM modulator applications. In: *2017 Progress in Electromagnetics Research Symposium - Fall (PIERS - FALL)*. 2017. DOI: 10.1109/PIERS-FALL.2017.8293500.

Figure 2.2. PWM Circuit and PWM signal.

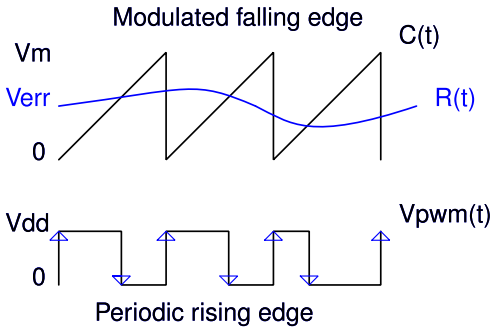


(a) PWM Circuit. (b) PWM Signal.

Source [1].

ulation is the most common in DC-DC converters [5] . The operation of this modulation is shown in Figure **2.3**.

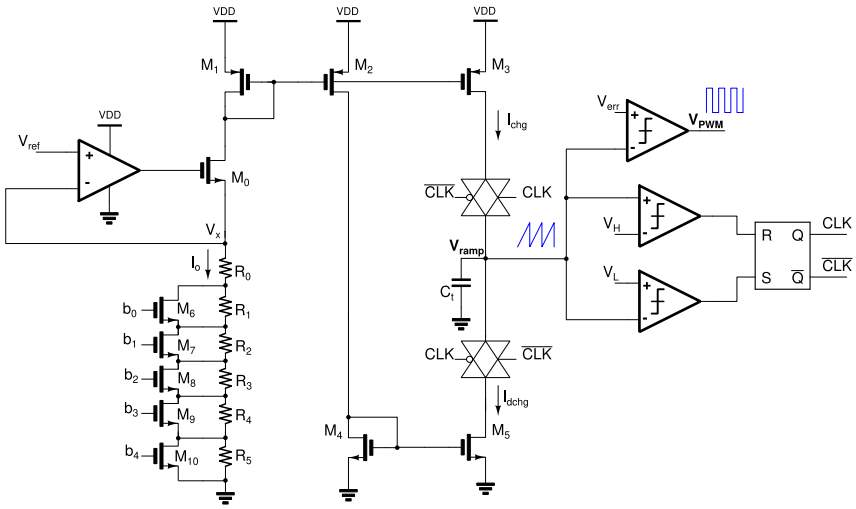
Figure 2.3. Constant-frequency trailing-edge modulation.



Source [1].

To generate this modulation, a topology is selected based on the principle of controlled charging and discharging of a capacitor (C_t) through current sources (see figure **2.4**). This method is capable of precisely regulating both the switching frequency and the duty cycle. [1]

Figure 2.4. Implemented PWM circuit.



Source [1].

This architecture operates by converting a stable reference voltage into a precise charging current through a voltage-to-current (V-I) converter. The key components and their functions are as follows:

- Current Generation: The V-I block, composed of an operational amplifier, a pass transistor (M_0), and a resistor (R_t), generates a current I_o proportional to V_{ref}.
- Current Mirrors: This current is replicated using PMOS and NMOS current mirrors to establish the charging current (I_{chg}) and the discharging current (I_{d_chg}).
- Slope Control: Unlike conventional topologies that discharge the capacitor directly to ground, this implementation uses a controlled discharge source designed to be 9 times greater than the charging source. This allows for superior control over the ramp slopes, reducing voltage errors due to delay without drastically increasing power consumption. [1]
- Oscillation Logic: A control block, integrating a window comparator and an SR Latch, governs the oscillation cycle. The SR Latch generates the necessary clock signals to

alternate between charging and discharging states upon detecting that V_{ramp} has reached the pre-established limits.

Within this system, the voltage comparator is the critical component that dictates the precision of the upper (V_H) and lower (V_L) thresholds. Its performance has a direct impact on the integrity of the carrier signal and defines the ramp's inflection points. Any sensitivity error or the presence of excessive offset voltage (V_{os}) will shift these thresholds, altering the ramp amplitude and, consequently, the final switching frequency. The propagation delay of the comparators introduces voltage errors proportional to the ramp slope. Since the discharge slope is significantly steeper, the delay of the low-level comparator (CMPL) is identified as the critical path that most affects frequency precision [1]. As seen in (2), the frequency (f_{sw}) depends critically on the precision of the thresholds (V_H–V_L) and the propagation delays (t_{dH} and t_{dL}), two factors that are the direct responsibility of the comparator.

$$f_{sw} = \frac{0.9 I_{\text{chg}}}{C_t \left(V_H - V_L\right) + I_{\text{chg}} \left(t_{dH} + 9 t_{dL}\right)} \tag{2}$$

2.3. COMPARATOR TOPOLOGY

The comparator implemented in this system is a high-speed static three-stage comparator: a pre-amplification stage, a decision stage, and an output buffer[1] (See Figure **2.5**).

Figure 2.5. Comparators Topology.

Source [1].

Preamplifier Stage: It consists of a differential amplifier with diode-connected loads. Its main function is to amplify the differential input signal to improve the comparator's sensitivity and, simultaneously, isolate the input terminals from switching noise generated by the positive feedback stage. Additionally, it provides initial gain, reducing the impact of the offset voltage

from subsequent stages when referred to the total system input. [6]

Decision Stage - Cross-Coupled Pair: This is the ”heart” of the comparator and uses a pair of cross-coupled transistors (Cross-Coupled Pair or XCP). Its operation is based on:

- Regeneration: The cross-coupled pair acts as an ”impedance negator,” presenting negative resistance between its drains. This creates positive feedback that allows for ”synchronous amplification” or regeneration, where even small voltage differences are exponentially amplified toward logic levels. [7]
- Hysteresis Control: In this static topology, diode-connected transistors ($M_{10,11}$) are added to prevent the loop from permanently locking (latch-up), allowing for continuous operation. The ratio between these transistors and the XCP pair ($M_{8,9}$) determines the presence and width of the hysteresis, which is necessary to filter noise during comparison. [7]

Post-amp Stage: The final stage is a differential-to-single-ended amplifier connected to an output inverter. Its purpose is to take the output from the decision stage and convert it into a pure rail-to-rail digital signal compatible with the subsequent CMOS logic. It increases the switching speed and provides the necessary current to drive capacitive loads without degrading the performance of the decision stage. [1]

2.4. ADVANCED LAYOUT CONSIDERATIONS IN 28 NM CMOS TECHNOLOGY

This section details the physical challenges and design techniques necessary to ensure the comparator’s robustness in the 28 nm CMOS technology node. As device dimensions shrink,

---

[6] Daniel Felipe BARRIOS RUEDA and Nestor Ivan MATAJIRA ORTIZ. “Design of Energy-Efficient Voltage Comparators for a System-on-Chip Using a CMOS Technology Node of 28nm”. Bachelor’s thesis. Universidad Industrial de Santander, 2024.

[7] B. RAZAVI. The Cross-Coupled Pair—Part I [A Circuit for All Seasons]. In: *IEEE Solid-State Circuits Magazine*. 2014, vol. 6, no. 3.

layout design transitions from a simple schematic translation to a highly interactive process where the physical environment of the device alters its electrical parameters. For a high-precision block like a voltage comparator, performance depends not only on electrical sizing but also on strict geometric implementation to reduce process, voltage, and temperature (PVT) variations. [8] [9]

2.4.1. Impact of Physical Effects on Precision Blocks: As technology scales toward the 28 nm node and channel length decreases, devices experience so-called Short-Channel Effects. As the distance between the source and drain shortens, the gate loses authority over the channel depletion region, leading to severe phenomena such as Drain-Induced Barrier Lowering (DIBL), subthreshold slope degradation, and channel length modulation. [8]

As a result, the threshold voltage (V_{th}) and mobility (μ) suffer enormous statistical variations (mismatch) even between identical adjacent transistors. In a voltage comparator, these variations translate directly into an increase in input offset, which degrades comparison precision, being unable to detect the high and low thresholds (V_H and V_L) of the ramp, directly modifying the switching frequency and the system resolution. Therefore, mitigating these effects at the design level is no longer optional, but an imperative requirement.

2.4.2. Layout Dependent Effects (LDE) and Mitigation: In 28 nm nodes, Layout Dependent Effects (LDE) transition from second-order variations to first-order factors that can deviate the bias current by more than 20% . [10] [11]

---

[8] A. PIPINO. *Design of Analog Circuits in 28nm CMOS Technology for Physics Applications*. Ph.D. Dissertation. Università degli Studi di Milano-Bicocca, 2016.

[9] A. HASTINGS. *The Art of Analog Layout*. 3rd ed. Pearson, 2024.

[10] M. SAHRLING. *Layout Techniques for Integrated Circuit Designers*. Artech House, 2020.

[11] J. LIENIG and J. SCHEIBLE. *Fundamentals of Layout Design for Electronic Circuits*. Springer International Publishing, 2020.

- Basic stress LDEs & STI: STI is silicon dioxide embedded in the substrate to electrically isolate the active regions of adjacent transistors. Because oxide and silicon have different thermal expansion coefficients, the creation of the STI induces strong mechanical stress on the transistor channel, altering the mobility of the charge carriers. Specifically, this mechanical stress is maximally concentrated when a transistor is located near a diffusion boundary. Consequently, the resulting magnitude in V_{th} and the drain current depends on the distance between the polysilicon gate and the edge of the STI. .[10] [11] How to mitigate them: By adding dummy transistors to the ends of matched arrays. This ensures that the "active" transistors in the center see exactly the same STI volume and, therefore, experience the same mechanical stress profile. [9] [10]

- Well Proximity Effect (WPE): During high-energy ion implantation to form wells, ions bounce (scatter) off the edges of the photoresist mask. These scattered ions end up being implanted near the well edges, altering the local doping profile and drastically changing the V_{th} of devices located in that area. [10] [11]

  How to mitigate it: By adding dummy transistors to the ends of matched arrays, allowing peripheral devices to have a distance to the well boundary. Another option is to move critical transistors (such as the comparator's differential pair) at least $1\,\mu m$ to $2\,\mu m$ away from the well edge. Alternatively, place all critical devices at exactly the same distance from the edge so that the variation affects all of them equally [3]

- Antenna Effect: During the plasma etching process in metal fabrication, long metal traces act as antennas that collect static charges. If this metal is connected solely to a polysilicon gate, the accumulated charge can generate a voltage high enough to break the thin gate oxide, permanently damaging the transistor [9] [11]. This occurs during routing when the exposed metal area exceeds the area ratio permitted by design rules (Antenna Ratio) relative to the connected gate area.

  How to mitigate it: By performing a "metal jumper" to a higher layer near the gate to break

the galvanic connection during early plasma stages, or by adding a reverse-connected diode near the gate to safely discharge the accumulated energy into the substrate. [9]

- Latchup: This is the accidental activation of a parasitic thyristor (PNPN structure) inherent to CMOS structures due to voltage drops in the substrate and the well. If activated, it creates a low-impedance short circuit between VDD and GND, which can melt the chip [9] [11]. It occurs during transient current spikes, minority carrier injection, or when the parasitic resistances of the substrate (R_{sub}) and the well (R_{well}) are very high.

  How to mitigate it: By surrounding all important blocks or devices with guard rings solidly connected to VDD (for N-Wells) and GND (for P-Sub). Minimize resistance by injecting as many well and substrate contacts (tap cells) as possible. [9]

2.4.3. Matching Techniques and Symmetrical Arrangements For the comparator to achieve high resolution and low offset voltage, symmetrical elements in the schematic (such as the input differential pair and current mirrors) must be electrically identical in the silicon. Due to process gradients during manufacturing (thermal variations, oxide thickness), devices cannot simply be drawn side by side. [9] [12]

- Interdigitated Arrangement: Consists of dividing large transistors into multiple fingers and alternating them in a one-dimensional pattern [9]. It is generally used for current mirrors or gain stages where the goal is to cancel linear gradients in a single direction along the chip. It offers a reasonable balance between good matching and ease of routing. [9].
- Common Centroid: This is a two-dimensional dispersion pattern where sub-devices are organized such that their geometric centers of mass (centroids) coincide at the exact same point [9]. Its application is mandatory for the input differential pairs of a high-precision comparator. Unlike interdigitated, common centroid cancels process gradients

[12] C. SAINT and J. SAINT. *IC Layout Basiscs: A practical guide*. McGraw-Hill, 2001.

in both directions (X and Y axes). It is the most robust technique against temperature and doping variations across the die, at the expense of much more complex routing. [9] [12]

- Symmetry in Routing (Symmetry Types):

  Axial Symmetry (Mirror Symmetry / Axis of Symmetry): Everything drawn on the left side of a virtual central axis must be the exact reflection of the right side. This ensures that parasitic routing capacitances to the substrate and between layers are identical for the positive and negative paths of the comparator, avoiding temporal imbalances (skew or phase delay) during high-speed switching. [12]

It is vital to accompany these arrangements with rings of dummy devices around the entire perimeter of the matched block. Dummies have no electrical function, but they ensure that edge devices experience the same optical etching conditions (microloading effects/lithographic density) and thermal/mechanical stress as the devices located in the center of the pattern [9], [10].

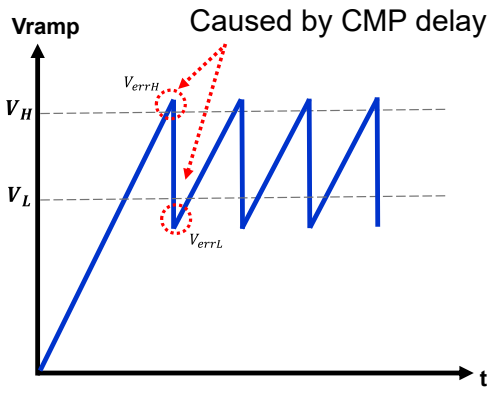
3. SENSITIVITY ANALYSIS

The design of the comparator requires a deep understanding of how the switching frequency (f_{sw}) of the PWM controller degrades. In this section, the impact of each independent circuit variable on system stability is quantified through a sensitivity analysis based on the linear approximation of the total error.

The ramp frequency is significantly affected by comparator delays, as these produce an error voltage that depends on the charging and discharging slopes of the ramp generator and the delay of each specific comparator. This phenomenon can be observed in Figure 3.1. Additionally, the input-referred offset of the comparators generates a comparison error voltage, affecting both the ramp amplitude and its frequency. The actual frequency of the ramp generator, accounting for these errors, is given by:

$$f_{sw} = \frac{0.9I_{chg}}{C_t(V_H - V_L \pm V_{os}) + I_{chg}(t_{dH} + 9t_{dL})} \tag{3}$$

Figure 3.1. Delay Errors.



Source [1].

3.1. FREQUENCY SENSITIVITY (f_{sw})

To evaluate the system's robustness against parameter variations, the total change in frequency (Δf_{sw}) is defined as the sum of the individual contributions of each variable, weighted by their respective partial derivatives. According to the sensitivity theory, the total variation is expressed through the following linear approximation:

$$\Delta f_{sw} = \frac{\partial f_{sw}}{\partial I_{chg}}\Delta I_{chg} + \frac{\partial f_{sw}}{\partial C_t}\Delta C_t + \frac{\partial f_{sw}}{\partial t_{dH}}\Delta t_{dH} + \frac{\partial f_{sw}}{\partial t_{dL}}\Delta t_{dL} + \frac{\partial f_{sw}}{\partial V_{os}}\cancelto{0}{\Delta V_{os}} \tag{4}$$

Each partial derivative represents the sensitivity of the system to a specific variable; a higher absolute value indicates that the switching frequency is more vulnerable to fluctuations in that parameter.

- **Sensitivity to lower delay (t_{dL}):**

$$\frac{\partial f_{sw}}{\partial t_{dL}} = \frac{-8.1 I_{chg}^2}{(C_t(V_H - V_L \pm V_{os}) + I_{chg}(t_{dH} + 9t_{dL}))^2} = -40 \times 10^{12} \left[\frac{Hz}{s}\right] \tag{5}$$

  This is identified as the most critical variable in the design. Since the ramp discharges 9 times faster than it charges to maintain the sawtooth waveform, any delay in the lower limit comparator (CMP_L) has a massive impact on the total period. This critical interaction occurs during the High-to-Low transition (discharge phase), corresponding to the t_{dHL} propagation time.

- **Sensitivity to upper delay (t_{dH}):**

$$\frac{\partial f_{sw}}{\partial t_{dH}} = \frac{-0.9 I_{chg}^2}{(C_t(V_H - V_L \pm V_{os}) + I_{chg}(t_{dH} + 9t_{dL}))^2} = -4.44 \times 10^{12} \left[\frac{Hz}{s}\right] \tag{6}$$

  The impact of the upper delay on frequency is nearly 10 times smaller than that of the lower delay (t_{dL}), which establishes a clear hierarchy for design priorities during the layout stage.

- **Sensitivity to offset (V_{os}):**

$$\frac{\partial f_{sw}}{\partial V_{os}} = \frac{\pm 0.9 C_t I_{chg}}{(C_t(V_H - V_L \pm V_{os}) + I_{chg}(t_{dH} + 9t_{dL}))^2} = \pm 4.69 \times 10^6 \left[\frac{Hz}{V}\right] \tag{7}$$

  This derivative represents the sensitivity to the offset voltage. It should be noted that the offset voltage error due to PVT variations is considered negligible in this deterministic analysis and is therefore excluded from the total frequency delta calculation.

Consequently, the frequency variation in the PWM controller imposed by the comparison blocks is defined as the Frequency Delta: [1]

$$\Delta f_{sw} = \frac{\partial f_{sw}}{\partial t_{dH}} \Delta t_{dH} + \frac{\partial f_{sw}}{\partial t_{dL}} \Delta t_{dL} \tag{8}$$

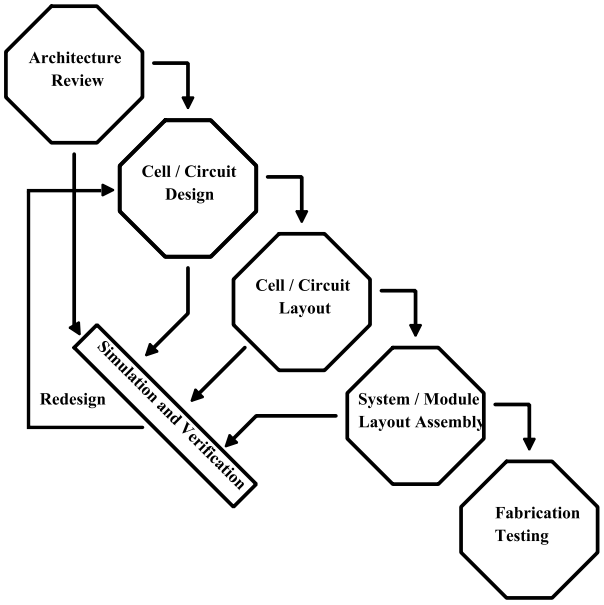
By substituting the calculated sensitivity values, the impact is quantified as:

$$\Delta f_{sw} = -4.44 \times 10^{12} \cdot \Delta t_{dH} + \left(-40 \times 10^{12}\right) \cdot \Delta t_{dL} \tag{9}$$

4. PWM CIRCUIT DESIGN METHODOLOGY

This chapter addresses the proposed design methodology for the voltage comparator, as shown in Figure 4.1. The methodology is structured as an iterative design flow, in which design specifications are verified; these are fundamental for decision-making throughout the stages of the design process.

Figure 4.1. Design methodology.



4.1. BASELINE DESIGN RESULTS

This section presents the performance metrics of the three-stage comparator proposed in [1], which serves as the starting point for this work. The results obtained from both schematic-level and post-layout simulations are detailed, highlighting the impact of parasitic elements on the design's performance.

Table 4.1. Schematic and Post-Layout Results of the Baseline Comparator

Parameter	Condition	Schematic			Post-Layout		
		Min	**Typ**	**Max**	**Min**	**Typ**	**Max**
A_o [dB]		80.55	88.70	93.29	77.52	89.31	94.12
BW[MHz]		4.60	12.82	23.50	3.58	10.19	18.48
td_{LH}[ns]	Vin = 5mV Low to High	1.59	2.35	3.08	1.99	2.77	3.48
td_{HL}[ns]	Vin = 5mV High to Low	1.59	2.33	3.59	2.22	3.30	9.36
td_{LH}[ns]	Vin = 20mV Low to High	1.18	1.67	2.39	1.45	2.03	2.84
td_{HL}[ns]	Vin = 20mV High to Low	1.12	1.61	2.63	1.39	2.05	3.47
Slew Rate [kV/us]	Vin = 1.8 V	1.40	2.38	3.57	1.30	2.18	3.31
Resolution [uV]		38.96	66.12	169.06	35.44	61.61	239.45
Static Current Low [uA]	Vinn = 900 mV Vout Low	34.82	50.46	67.34	35.35	51.66	69.11
Static Current High [uA]	Vinn = 900 mV Vout High	19.58	31.41	43.57	19.51	21.82	43.89
Dynamic Current [nA]	@2MHz	-0.02	1.32	3.07	-0.01	0.68	3.08
ICMR [V]		0.30	1.68	1.94	0.03	1.63	1.86
Input Noise [nV]	@20MHz	14.74	21.29	31.78	14.27	20.71	31.25
Pavg [uW]		57.98	79.30	119.18	52.41	80.61	120.96

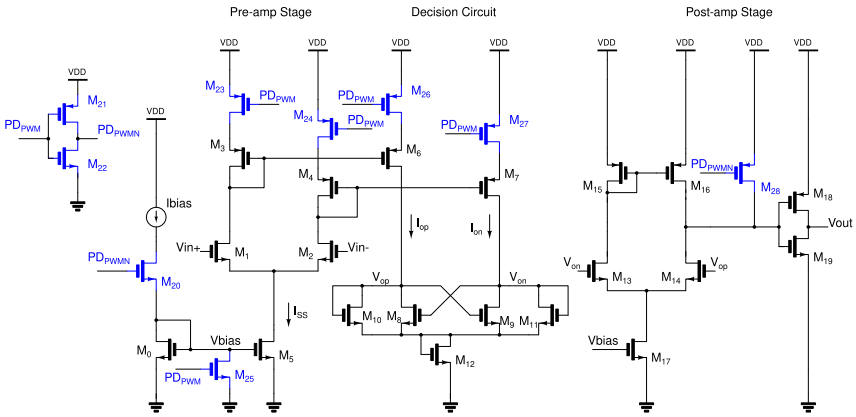
Table 4.2. Monte Carlo Simulation Results of the Baseline Comparator

Parameter	Condition	Unit	Schematic		Post-Layout	
			Mean	σ	Mean	σ
Input Referred Offset		[mV]	1.96	4.23	0.89	4.35
t_{dLH}	$V_{in} = 5$ mV	[ns]	2.15	1.00	3.50	1.66
t_{dHL}	$V_{in} = 5$ mV	[ns]	3.38	2.50	3.59	1.84

4.2. CIRCUIT DESIGN

This section describes the redesign process of the voltage comparator at the schematic level under Typical, Process, Voltage, and Temperature (PVT) variations, as well as Monte Carlo conditions. Design decisions were presented for each stage: pre-amplifier, decision, and post-amplifier, as shown in 4.2. Additionally, the figure also illustrates the implementation of a power-gating technique for the comparator, aimed at reducing energy consumption when the circuit is not in use, based on the method described in [6].

Figure 4.2. Power Down implementation Comparators.



Pre-amplification stage

In this first stage, it was established that the transistors operate in weak inversion to obtain maximum gain without modifying the current flowing through their branches. This was achieved

using the g_m/I_D property to correctly size the transistor widths. [13] Additionally, the channel length was reduced to maximize bandwidth [1].

Decision stage

For this stage, the following decisions were made: Transistors M_8, M_9, M_{10} and M_{11} are biased according to the operational principle described below:

- When $V_{in+} > V_{in-}$, transistor M_{10} operates in strong inversion and saturation, M_9 is in the triode region, M_8 remains in weak inversion, and M_{11} is off.
- When $V_{in+} < V_{in-}$, the operating conditions are swapped between M_{10} and M_{11}, as well as between M_8 and M_9 [6].

For sizing, transistors M_8, M_9, M_{10} and M_{11} were designed with equal dimensions to ensure regenerative behavior [14].

Post-amp stage

This stage take the information from the previous stage and outputs a digital signal. [15] To achieve this, the transistors must be biased as follows:

- If $V_{in+} > V_{in-}$, $M_{13,14}$ operate in the saturation region in weak inversion, $M_{15,17}$ operate in strong inversion and saturation, and M_{16} operates in the triode region.
- When $V_{in+} < V_{in-}$, $M_{14,17}$ operate in the triode region, $M_{13,16}$ operate in the saturation region in weak inversion, and M_{15} is off. [6]

The current in this stage was increased to improve the comparator speed. [1] Finally, minimum channel lengths were used in the inverter to reduce the comparator delay times. [6]

---

[13] Phillip E. ALLEN and Douglas R. HOLBERG. *CMOS Analog Circuit Design*. OXFORD UNIVERSITY PRESS, 2001.

[14] B. RAZAVI. The Cross-Coupled Pair—Part II [A Circuit for All Seasons]. In: *IEEE Solid-State Circuits Magazine*. 2014, vol. 6, no. 3.

[15] R. Jacob BAKER, Harry W. LI, and David E. BOYCE. *CMOS. Circuit design layout and simulation*. Fourth Edition. IEEE Press, 2019.

4.3. CIRCUIT LAYOUT

Layout development focused on Design for Manufacturability (DFM), ensuring physical integrity through strict adherence to Design Rule Checks (DRC) and Layout Versus Schematic (LVS) verification. A strategic floorplan was implemented to prioritize signal integrity and reduce critical path lengths, thereby minimizing parasitic effects. This methodology ensures the robustness of the voltage comparator against process variations.

Floorplanning

Floorplanning was performed by grouping the blocks most sensitive to noise sources and thermal gradients, such as the differential pair, the latch, and the current mirrors. For each of these blocks or "stacks," transistor combinations (fingers and multipliers). The design complies with maximum gate area and uniform density constraints. A uniform orientation was maintained for all gates to comply with lithography rules, prohibiting any device rotation to prevent threshold voltage (V_{th}) variations. [8]

Advanced Matching and Abutment Techniques

- Common-Centroid Matching: This technique was implemented to cancel linear temperature and mechanical stress gradients. [11] This ensures that the geometric centers of the matched transistors coincide, utilizing axial symmetry to guarantee that proximity effects affect the devices in each stack identically.
- Abutment: By integrating transistors into a single stack (abutment), junction parasitic capacitance was reduced by sharing diffusion regions (source/drain). Furthermore, dummy devices were included at the ends of each stack. These devices ensure that the active transistors see an identical environment, mitigating variations caused by etching.

Layout-Dependent Effect (LDE) Mitigation

- STI (Shallow Trench Isolation): The aforementioned dummy devices also function as spacers to ensure that the mechanical stress induced by trench isolation is uniform across

the central transistors, avoiding shifts in carrier mobility (μ).

- Well Proximity Effect (WPE): To mitigate ion scattering near the well edges, the PMOS transistor stacks were placed in N-wells with a minimum distance of $1\,\mu m$ from the active region to the well edge.
- Antenna Effect: Antenna rule verification was performed to prevent electrostatic charge buildup on the gates during fabrication. Since critical paths were kept short and routing in upper metal layers was prioritized, the insertion of protection diodes was not required.
- Latchup: Guard rings were designed for each stack, connected to V_{DD} for PMOS transistors and V_{SS} for NMOS. This reduces substrate resistance and prevents the triggering of parasitic BJT devices.

External Connections and Signal Integrity

The routing strategy was based on the following principles:

- Upper Metals: Upper metal layers (thicker and less resistive) were used for the longest and most critical signal paths, minimizing series resistance and IR drops.
- Via Stacks: Multiple parallel vias were implemented in the V_{DD} and V_{SS} power connections to reduce contact resistance.

Design Verification (DRC and LVS)

Each cell and block was verified prior to final integration:

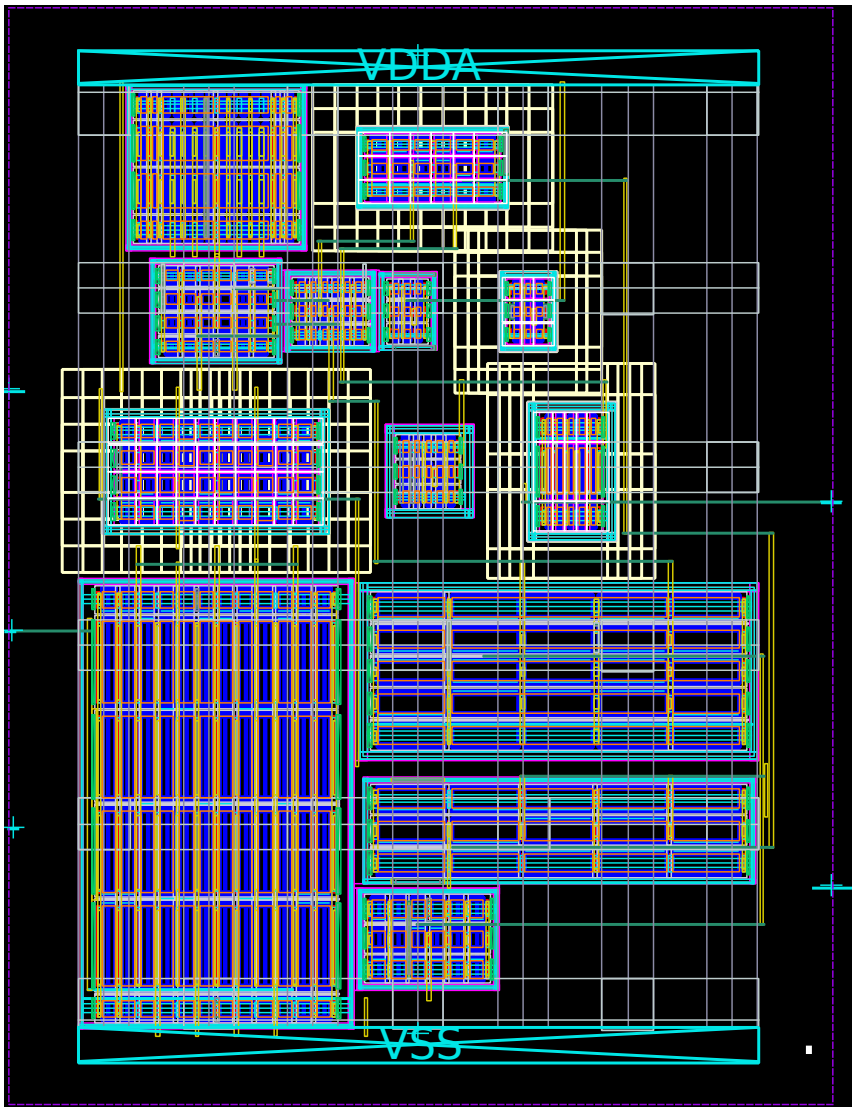
- Design Rule Check (DRC): Compliance with restricted metal and polysilicon density rules.
- Layout Versus Schematic (LVS): Guarantee of exact electrical correspondence between the topology and the physical implementation.
- Parasitic Extraction (PEX): The strategic distribution was validated through parasitic extraction (C+CC), allowing post-layout simulations (including Monte Carlo and PVT).

5. RESULTS

5.1. DEVICE SIZING

The comparator design, including the power-down implementation, was developed using TSMC's 28 nm CMOS technology. The specific transistor dimensions are detailed in Table 5.1, and the implemented circuit schematic is shown in Figure 4.2.

Figure 5.1. Layout of the proposed Comparator.



The implemented layout is shown in Figure 5.1, incorporating dummy devices, matching techniques, and guard rings for LDE mitigation. The design is DRC and LVS compliant, enabling the parasitic extraction required for the post-layout simulations.

Table 5.1. Comparator transistor sizing

Name	$W(\mu m)$	$Finger\_W(\mu m)$	$L(\mu m)$	$N_{Multiplier}$	N_{Finger}
M_0	0.54	0.54	2	1	1
M_{1-2}	2.4	2.4	0.4	16	1
M_{3-4}	0.4	0.4	0.4	2	1
M_5	0.5	0.5	0.4	2	1
M_{6-7}	0.4	0.4	0.4	2	1
M_8	0.3	0.3	0.35	1	1
M_9	0.3	0.3	0.35	1	1
M_{10}	0.3	0.3	0.35	1	1
M_{11}	0.3	0.3	0.35	1	1
M_{12}	5	1	0.15	4	5
M_{13-14}	0.3	0.3	0.15	1	1
M_{15-16}	0.3	0.3	0.45	1	1
M_{17}	1.65	0.55	2	3	3
M_{18}	1.35	1.35	0.15	1	1
M_{19}	0.35	0.35	0.15	1	1
M_{20}	0.55	0.55	2	1	1
M_{21-22}	0.27	0.27	0.15	1	1
M_{23-24}	0.4	0.4	0.4	1	1
M_{25}	0.55	0.55	2	1	1
M_{26-27}	0.4	0.4	0.4	1	1
M_{28}	0.3	0.3	0.45	1	1

Comparative Analysis of Schematic Design A comparative analysis at the schematic level was carried out to evaluate the improvements in the performance of the proposed comparator. This stage focused on the sizing of the transistors (W/L ratios) to address the balance between power consumption and switching times.

The results at the schematic level, summarized in Table 4.1 and Table 5.2, show an improvement of 43.88% in bandwidth and 85.49% in slew rate. The average power consumption was reduced from 79.30 μW to 42.25 μW, representing a savings of 46.72%, an improvement in low-state consumption current of 43.88% and in high-state current consumption of 41.83%.

Furthermore, schematic-level Monte Carlo simulations show an improvement in the offset mean from 1.96 mV to 0.16 mV, which shows that the transistor resizing managed to minimize systematic mismatch by 91.84%. On the other hand, a change in the mean of t_{dHL} from 3.38 ns to 3.18 ns and of t_{dLH} from 2.15 ns to 3.58 ns is observed for a 5 mV input, showing that the response speed in high-to-low transitions was optimized by 5.98%, while in t_{dLH} there is an increase of 66.51%.

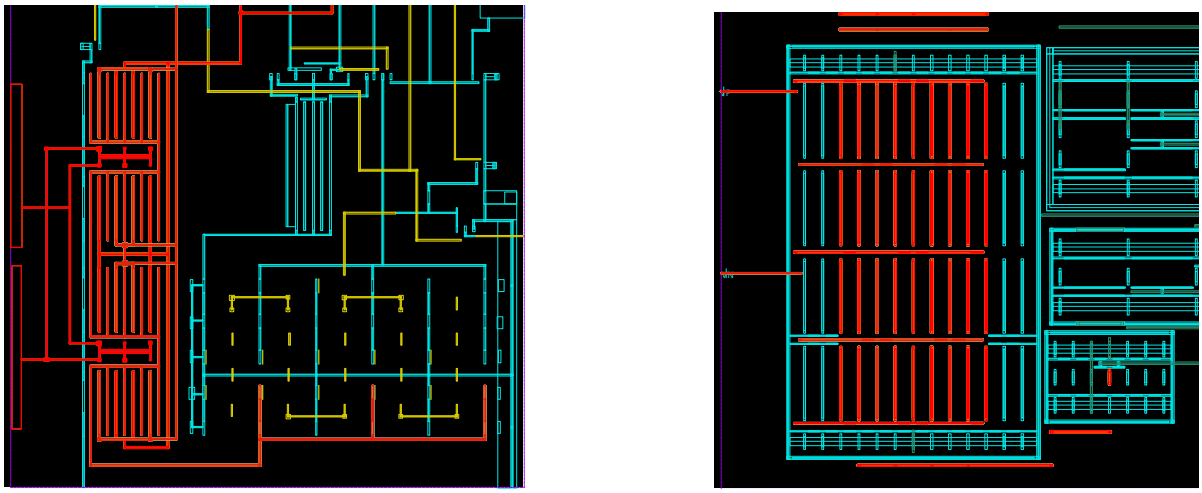
Comparative Analysis of Physical Implementation (Layout) A comparative analysis between the baseline layout and the proposed layout of the comparator is presented. It is important to highlight that the proposed design has been optimized considering robustness criteria for future silicon fabrication.

1. **Second-Order Effects (Matching)**

    - **Baseline Layout:** Transistors requiring critical matching present an asymmetric arrangement and are placed far apart from each other. This indicates that thermal gradients and manufacturing process variations were not considered in the original design (Figure 5.2(a)). Specifically, for the differential pair (M_1 and M_2), the internal connections highlighted in red reveal a lack of symmetry in the stack routing, which increases the circuit's vulnerability to mismatch.
    - **Proposed Layout:** Interdigitated and common-centroid structures were implemented to mitigate thermal and process gradients on the chip (Figure 5.2(b)). In the case

of the differential pair (M_1 and M_2), the internal connections are highlighted in red to demonstrate the high degree of symmetry achieved through the common-centroid configuration. This symmetric routing ensures that both transistors in the differential pair experience identical conditions, improving the comparator's precision.

Figure 5.2. Matching techniques for the differential pair.

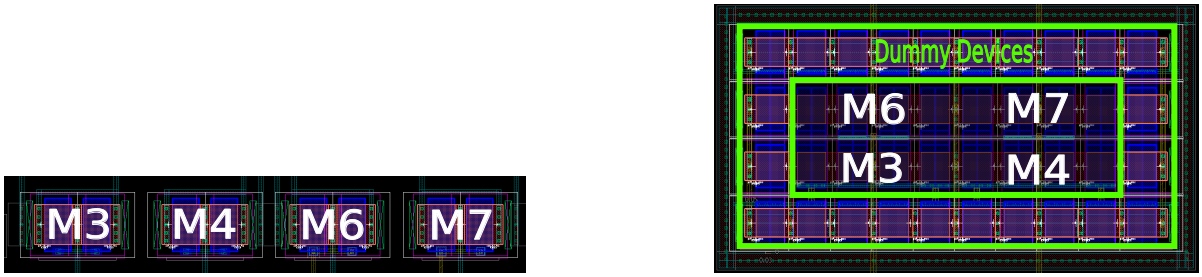


(a) Baseline (b) Proposed

2. **Use of Dummy Devices**

- **Baseline Layout:** In the baseline comparator, it is observed that critical arrays, such as the one formed by transistors M_3, M_4, M_6, and M_7, lack dummy devices at their ends. This absence leaves the active transistors exposed to variations in the etching process and WPE, compromising the uniformity of their electrical characteristics, as seen in Figure 5.3(a).
- **Proposed Layout:** Dummy transistors were added to the ends of the matched arrays to mitigate WPE effects, ensuring a constant distance to the well boundary and mitigating STI. Furthermore, these devices guarantee that the active transistors "see" the same environment during the etching process, which prevents over-etching at the edges and ensures geometric uniformity (see Figure 5.3(b)).

Figure 5.3. Use of dummy devices.

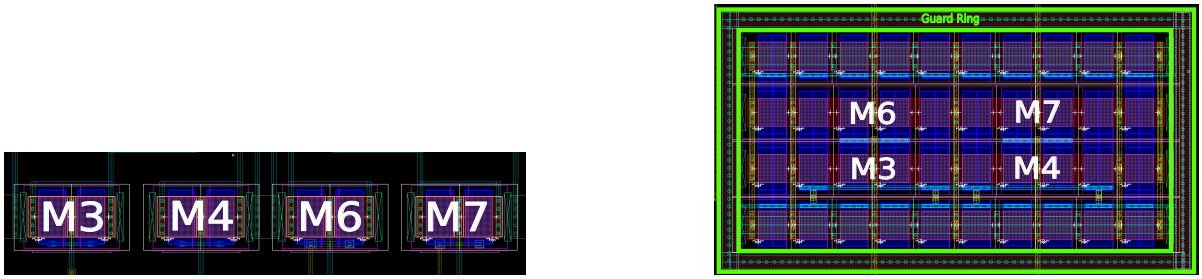


(a) Baseline (b) Proposed

3. **Use of Guard Rings**

- **Baseline Layout:** The design lacks dedicated guard rings around the transistor stacks. This absence increases the circuit's susceptibility to substrate-coupled noise and raises the risk of the Latch-up phenomenon, as there are no nearby low-impedance contacts to stabilize the well and substrate potentials, as seen in Figure 5.4(a).
- **Proposed Layout:** Unlike the baseline, this design incorporates full Guard Rings surrounding the transistor stacks. These structures act as isolation barriers that collect minority carriers and ensure a robust connection to the power rails (V_{DD} and V_{SS}), effectively preventing the Latch-up phenomenon and enhancing signal integrity against external noise (see Figure 5.4(b)).

Figure 5.4. Use of guard rings.

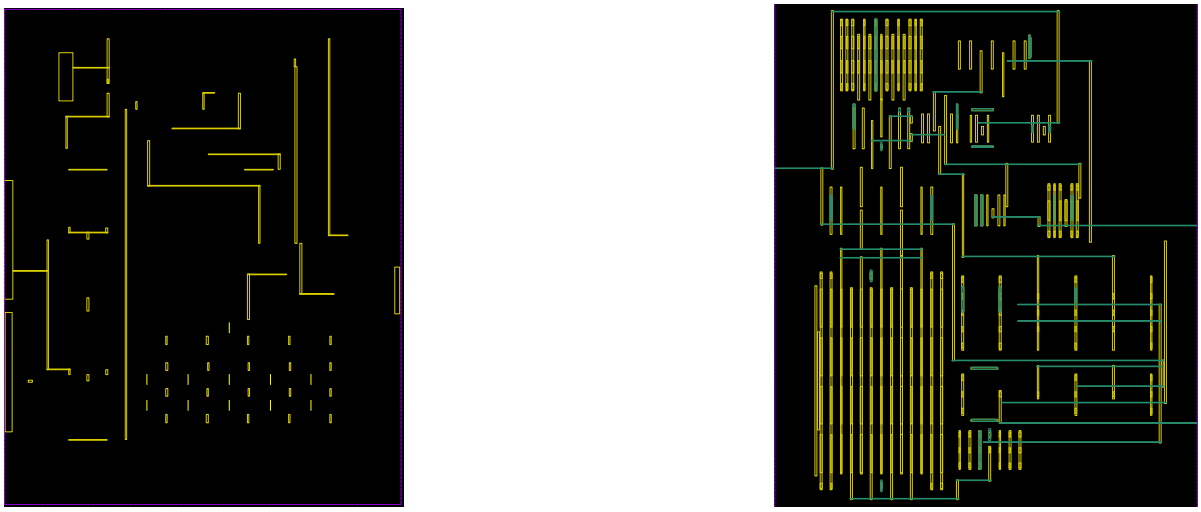


(a) Baseline (b) Proposed

4. **Optimization of Routing Strategy**

   - **Baseline Layout:** Routing is predominantly performed using a single metal layer (Metal 2) for both horizontal and vertical interconnections. This lack of planning in the metal hierarchy results in longer paths, increasing the risk of signal congestion and potential electrical failures due to the high density of crossings within the same metal level, as observed in Figure Figure 5.5(a).
   - **Proposed Layout:** A routing strategy is implemented using different metal layers for horizontal and vertical paths. This approach enables more direct and compact paths. By separating the routing directions into different metal levels, the risks of proximity-related short circuits are eliminated, and signal integrity is improved through a more organized and efficient layout topology (see Figure 5.5(b)).

Figure 5.5. Optimization of routing strategy.



(a) Baseline (b) Proposed

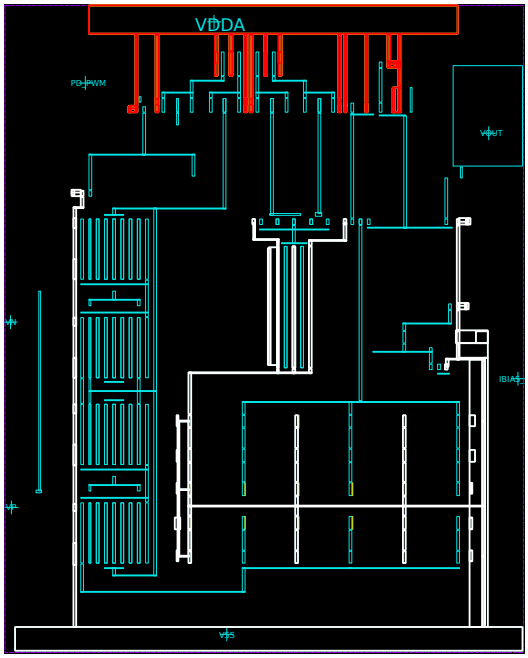
5. **Signal and Power Integrity (EM and IR Drop)**

   - **Baseline Layout:** It utilizes thin traces in Metal 1 and Metal 2 for V_{DD} and V_{SS} connections. Since these are lower metal layers, they exhibit higher sheet resistance and lower current-carrying capacity, which leads to significant voltage drops (IR drop)

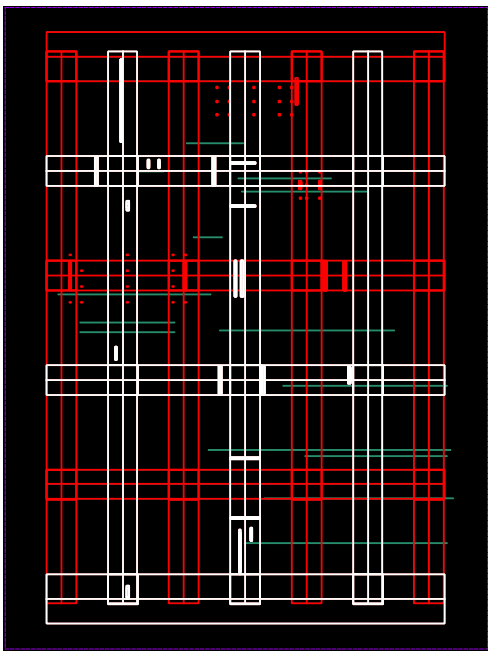
and increases electromigration (EM) risks. In Figure 5.6(a), the V_{SS} connections are highlighted in white and V_{DD} in red, illustrating a restrictive and high-resistance routing approach.

- **Proposed Layout:** This design implements a power grid structure to handle power distribution. As shown in Figure 5.6(b), the V_{DD} (in red) and V_{SS} (in white) connections are established through wider and more robust paths. This configuration minimizes series resistance, effectively reducing IR drop, and ensures both signal and power integrity by providing balanced impedances for the differential paths.

Figure 5.6. Signal and Power Integrity.



(a) Baseline



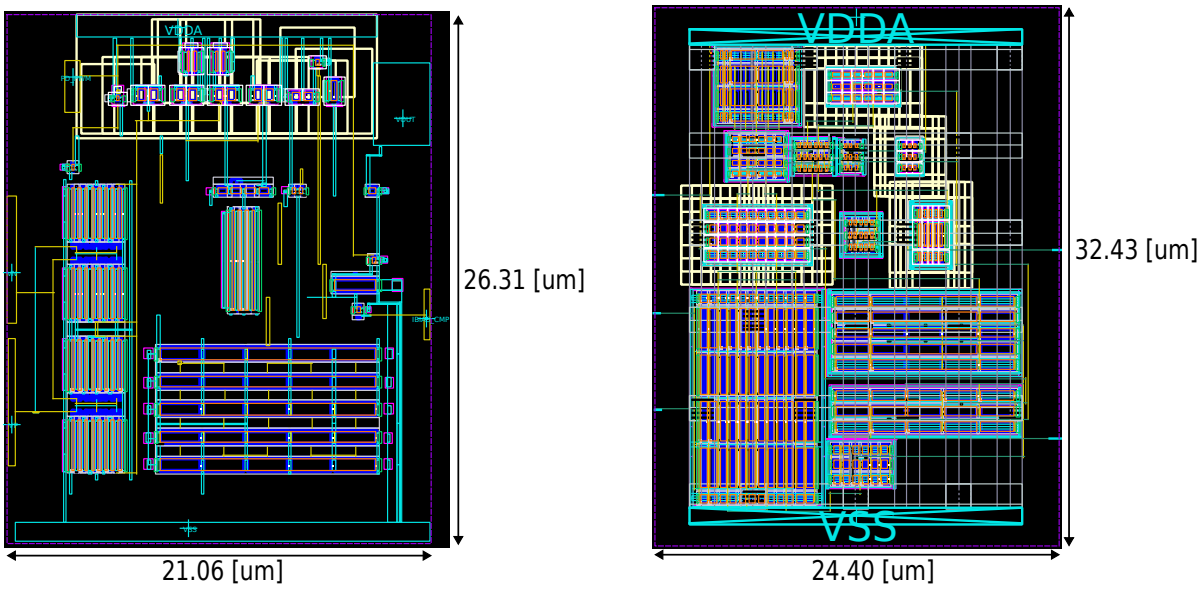
(b) Proposed

6. **Area Summary**

The physical implementation of the baseline layout is shown Figure 5.7(a), occupying a total area of 554.22 μm^2. Likewise, the proposed design is shown in Figure 5.7(b), with an area of 791.13 μm^2.

This 42.8% increase in area is due to the use of dummy devices, guard rings, and the circuit resizing performed to reduce power consumption.

Figure 5.7. Layout area comparison.



(a) Baseline (b) Proposed

5.2. SCHEMATIC AND POST-LAYOUT RESULTS

This section presents the simulation results for the baseline comparator at both the schematic and post-layout levels. The simulations were conducted using the TSMC 28 nm process corners to account for slow and fast variations in MOSFET transistors. The validation environment was defined to test the circuit's robustness under a supply voltage range from 1.6 V to 2.0 V and a temperature range from -40 ℃ to 125 ℃. Additionally, Monte Carlo (MC) statistical simulations were performed using 100 samples to characterize the impact of process variations and mismatch on the comparator's performance. A sample size of 100 was selected due to the high computational cost when simulating at both the schematic and post-layout levels.

Table 5.2. Schematic and Post-Layout Results of the proposed Comparator

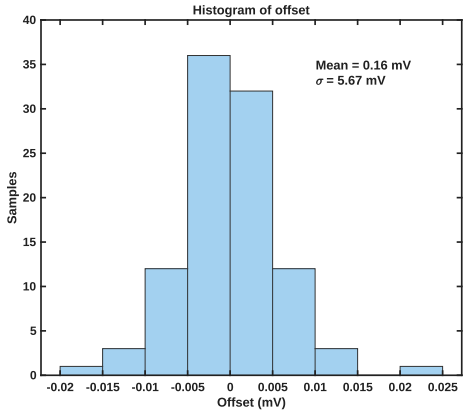
Parameter	Condition	Schematic			Post-Layout		
		Min	**Typ**	**Max**	**Min**	**Typ**	**Max**
A_o [dB]		77.54	84.81	89.45	78.36	87.32	94.94
BW [MHz]		11.89	23.78	36.44	7.37	15.35	24.25
td_{LH} [ns]	Vin = 5mV Low to High	2.28	3.19	4.43	3.47	4.91	7.25
td_{HL} [ns]	Vin = 5mV High to Low	2.15	3.07	4.76	3.06	4.44	7.23
td_{LH} [ns]	Vin = 20mV Low to High	1.69	2.38	3.47	2.37	3.34	5.04
td_{HL} [ns]	Vin = 20mV High to Low	1.48	2.14	3.23	1.97	2.86	4.41
Slew Rate [kV/us]	Vin = 1.8 V	2.65	3.71	5.61	1.85	3.02	4.33
Resolution [uV]		60.65	103.38	238.89	32.23	77.53	211.26
Static Current Low [μA]	VinP $<$ VinN Average Low	17.27	28.32	44.79	17.22	28.22	44.49
Static Current High [μA]	VinP $>$ VinN Average High	8.77	18.27	33.09	8.79	18.23	32.78
Dynamic Current [nA]	@2MHz	0.19	1.78	3.27	-0.61	0.42	2.10
ICMR [V]		1.31	1.67	1.93	1.32	1.68	1.92
Input Noise [nV]	@20MHz	21.63	29.54	40.77	21.45	29.36	40.58
Pavg [μW]		20.86	42.25	79.90	20.85	42.00	79.20

Table 5.3. Monte Carlo Simulation Results of the Comparator

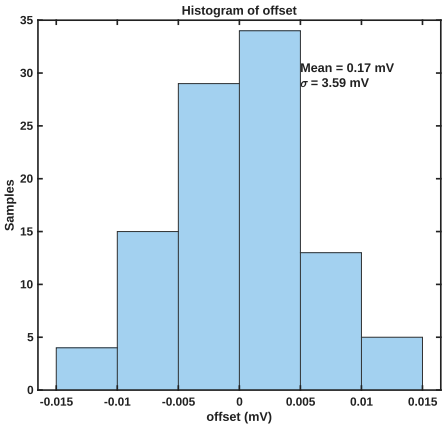
Parameter	**Condition**	**Unit**	**Schematic**		**Post-Layout**	
			Mean	σ	**Mean**	σ
Input Referred Offset		[mV]	0.16	5.67	0.17	5.59
t_{dLH}	$V_{in} = 5$ mV	[ns]	3.58	1.17	6.49	7.71
t_{dHL}	$V_{in} = 5$ mV	[ns]	3.18	1.66	5.82	5.64

Figure 5.8, 5.9 and 5.10 show the results of the statistical simulations at both the schematic and post-layout levels for offset, t_{dLH} and t_{dHL} respectively, where the mean and standard deviation for each specification can be seen.

Figure 5.8. Monte Carlo simulation results for offset.

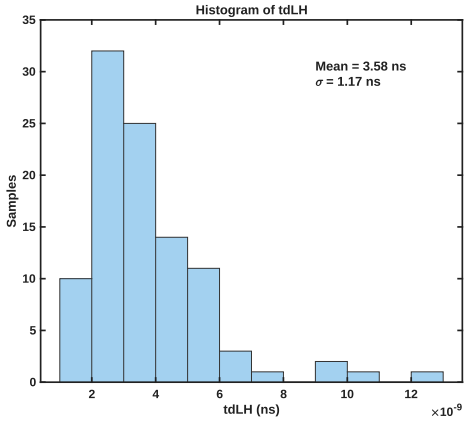


(a) Schematic

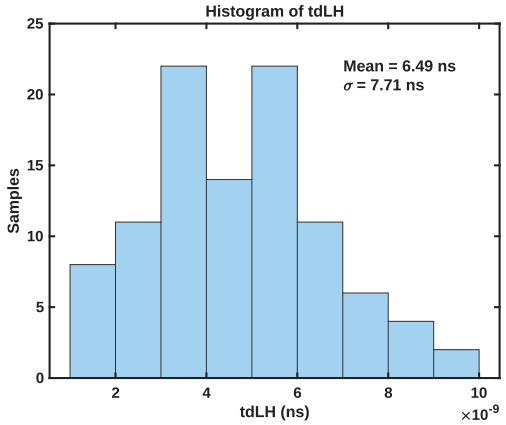


(b) Post-Layout

Figure 5.9. Monte Carlo simulation results for t_{dLH}.

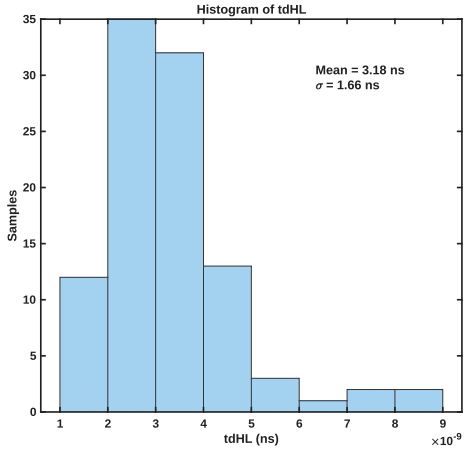


(a) Schematic

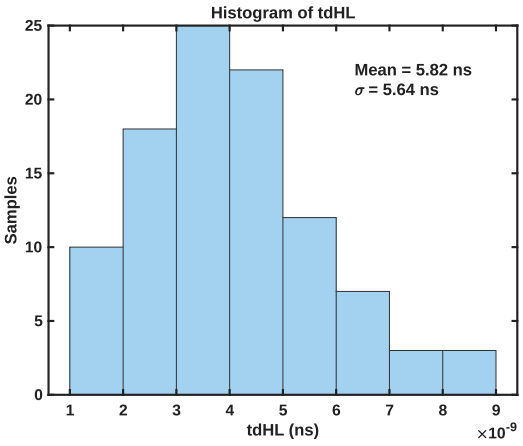


(b) Post-Layout

Figure 5.10. Monte Carlo simulation results for t_{dHL}.



(a) Schematic



(b) Post-Layout

A comparative analysis at the schematic level was carried out to evaluate the improvements in the performance of the proposed comparator. This stage focused on the sizing of the transistors (W/L ratios) to address the balance between power consumption and switching times.

The results at the schematic level, summarized in Table 4.1 and Table 5.2, show an improve-

ment of 43.88% in bandwidth and 85.49% in slew rate. The average power consumption was reduced from 79.30 μW to 42.25 μW, representing a savings of 46.72%, an improvement in low-state consumption current of 43.88% and in high-state current consumption of 41.83%. Furthermore, schematic-level Monte Carlo simulations show an improvement in the offset mean from 1.96 mV to 0.16 mV, which shows that the transistor resizing managed to minimize systematic mismatch by 91.84%. On the other hand, a change in the mean of t_{dHL} from 3.38 ns to 3.18 ns and of t_{dLH} from 2.15 ns to 3.58 ns is observed for a 5 mV input, showing that the response speed in high-to-low transitions was optimized by 5.98%, while in t_{dLH} there is an increase of 66.51%.

After performing the sensitivity analysis detailed in Chapter 4 , the robustness of the comparator is evaluated by measuring the reduction in total frequency deviation relative to the nominal target of 2 MHz. For this purpose, the performance of the proposed design (Table 5.2) is compared against the baseline design (Table 4.1) using the results from post-layout PVT simulations.
This robustness evaluation focuses specifically on a 5 mV input signal. This input level is critical as it allows for verifying whether the layout improvements maintain signal integrity against noise and parasitic effects at low operating levels.
The following frequency deviation calculations (Δf_{swmin}) are performed based on the frequency equation that incorporates delay and offset errors:

Results Baseline Comparator

$$\Delta f_{swmin} = (-4.44 \times 10^{12} \cdot 0.78 \times 10^{-9}) + (-40 \times 10^{12} \cdot 1.11 \times 10^{-9}) = -47.86 \text{ kHz} \quad (10)$$

$$\Delta f_{swmin} = (-4.44 \times 10^{12} \cdot 0.71 \times 10^{-9}) + (-40 \times 10^{12} \cdot 6.06 \times 10^{-9}) = -245.55 \text{ kHz} \quad (11)$$

Results Proposed Comparator

$$\Delta f_{swmin} = (-4.44 \times 10^{12} \cdot 1.44 \times 10^{-9}) + (-40 \times 10^{12} \cdot 1.38 \times 10^{-9}) = -61.59 \text{ kHz} \quad (12)$$

$$\Delta f_{swmin} = (-4.44 \times 10^{12} \cdot 2.34 \times 10^{-9}) + (-40 \times 10^{12} \cdot 2.79 \times 10^{-9}) = -121.98 \text{ kHz} \quad (13)$$

The deterministic error is quantified as the percentage deviation of the calculated frequency relative to the nominal design frequency:

$$\text{Error (\%)} = \frac{|\Delta f_{sw}|}{2 \text{ MHz}} \times 100 \quad (14)$$

The Table 5.4 summarizes the minimum and maximum frequency variations relative to the typical value and their associated error percentages. A design is defined as having greater robustness if the total error is minimized, ensuring that the switching frequency remains as close as possible to 2 MHz under all operating conditions.

Table 5.4. Comparative Analysis of Frequency Robustness

Parameter	**Baseline Comparator**		**Redesigned Comparator**	
	Min	**Max**	**Min**	**Max**
Δf_{sw} [kHz]	-47.86	-245.55	-61.59	-121.98
Deterministic Error [%]	2.39	12.27	3.08	6.02

Now, the robustness of the comparator is evaluated by measuring the variations between its schematic behavior and its post-layout performance for both the reference design and the proposed design, with the results shown in Table 4.1 and Table 5.2 respectively, through a quantitative analysis.

- **Propagation Delay ($V_{in} = 5$ mV):** The baseline comparator shows a typical delay increase of 41.63% and its worst-case corner (max), reaching 9.36 ns. In contrast, the

proposed comparator despite a typical PEX variation of 44.63$\%$, its worst-case delay is limited to 7.23 ns (a deviation of 51.89$\%$). Furthermore, the proposed design achieves near-perfect symmetry between the rising and falling edges, even in the slowest cases (7.25 ns and 7.23 ns).

- **Average Power Consumption (P_{avg}):** The baseline comparator shows sensitivity to layout parasitic effects, with a typical increase in consumption of 1.65% (from 79.30 μw to 80.61 μw) and reaching up to 120.96 μw in the worst case, which represents a 52.5% increase with respect to its schematic. Conversely, the proposed comparator shows a typical variation of 0.59% (from 42.25 μw to 42.00 μw), which shows that the parasitic impact is not as significant, since the post-layout results are close to the schematic results, and in the worst case, it showed an improvement, going from 79.90 μw to 79.20 μw (0.87% variation). Consequently, the redesign not only reduces nominal power by 47.9% compared to the reference design, but also ensures that its worst-case power consumption remains notably lower than the typical consumption of the original design.

- **Bandwidth (B_w):** The parasitic extraction shows that the baseline comparator suffers a 20.51% drop in typical bandwidth (from 12.82 MHz to 10.19 MHz), with a worst-case minimum that degrades from 4.60 MHz to 3.58 MHz (22.17% variation). While the proposed design shows a higher typical sensitivity to PEX with a 35.45% reduction (from 23.78 MHz to 15.35 MHz), it maintains a much higher upper operating limit, with a worst-case minimum from 11.89 MHz to 7.37 MHz (38.0% variation).

A comparative analysis between Table 4.2 and Table 5.3 reveals an offset mean variation of 1.07 mV for the baseline comparator when transitioning from schematic to post-layout, whereas in the proposed comparator, this variation is limited to only 0.1 mV, demonstrating the effectiveness of the matching techniques employed. Regarding propagation delays, the baseline comparator exhibits a variation of 1.35 ns in t_{dLH} and 0.21 ns in t_{dHL}, while the proposed design shows variations of 2.91 ns and 2.64 ns, respectively.

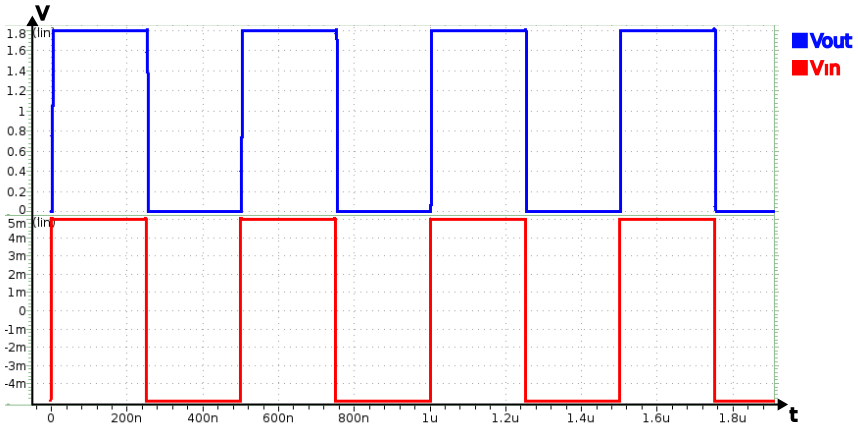
This discrepancy between schematic and layout results is primarily attributed to extracted parasitic capacitance. This was validated by extracting the critical capacitances from the signal

path in the layout and integrating their corresponding values into the schematic. The results of this simulation confirmed that the increase in delays is a direct consequence of these parasitic capacitances.

5.3. COMPARATOR CIRCUIT IN OPERATION

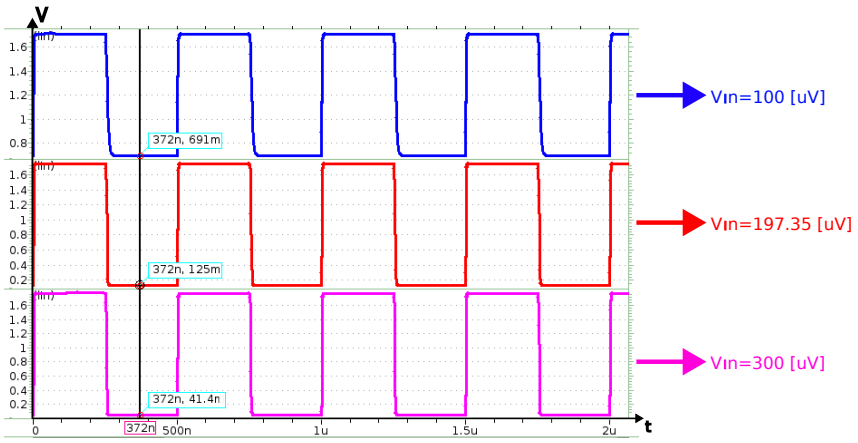
In this section, the functionality of the comparator is shown. The output signal (V_{out}) presents rail-to-rail transitions whenever the differential input signal (V_{in}) presents a minimal difference, as shown in Figure 5.11. It is evident that the proposed design maintains precise and stable switching even with an input signal of 5 mV.

Figure 5.11. Comparator input and output signals.



To evaluate the accuracy of the proposed comparator, a functional verification focused on its resolution capability was carried out. The target resolution for this design has been set at 103.38 μV, which represents the minimum differential input voltage that the architecture must distinguish to generate a rail-to-rail signal. However, both the input-referred offset and the input noise of the comparator is considered, resulting in a total resolution of 197.35 μV. To characterize the resolution and dynamic response near this threshold, the comparator was subjected to three differential input levels: 100 μV, 197.35 μV, and 300 μV. Figure 5.12 shows the response of the comparator to the three differential input levels.

Figure 5.12. Transient response of the proposed comparator for verifying resolution at different differential input levels.



Functional tests demonstrate that, with a differential input of 100 μV, the comparator detects the signal transition but does not reach the power rails, indicating that it has not exceeded the minimum differential voltage level for the correct operation of the comparator. However, starting from the 197.35 μV test, the output signal begins to show consistent rail-to-rail behavior. This transition confirms the real resolution of the comparator, effectively validating the design target of 197.35 μV. Consequently, the architecture demonstrates its ability to provide a well defined logic output for signals equal to or greater than the specified resolution, ensuring high-precision sensing .

6. CONCLUSIONS

The sensitivity analysis, supported by post-layout PVT results, confirms that the proposed comparator is more robust, achieving a 50% reduction in the maximum deterministic error—dropping from a 12.27% deviation in the baseline design to only 6.02%. This performance validates that the implementation of advanced layout techniques effectively mitigates parasitic and Layout-Dependent Effects (LDE) to the 28nm node, which otherwise triggered critical frequency instability in the reference design.

The implementation of matching structures such as Common-Centroid and Interdigitation mitigated layout-dependent effects (LDE), such as the Well Proximity Effect (WPE) and Shallow Trench Isolation (STI) stress. In addition, the strategic use of Dummy Devices and Guard Rings aims to promote etch uniformity and minimize the risk of latch-up, thereby reinforcing the physical integrity of the active stacks.

The layout redesign demonstrates physical robustness based on strict compliance with advanced design rules and DRC (Design Rule Check) and LVS (Layout Versus Schematic) verifications. This guarantees the electrical and structural integrity required for future silicon fabrication. The baseline comparator presents an offset mean variation of 1.07 mV when transitioning from schematic to post-layout, while this redesign shows a lower variation in results between schematic and post-layout of 0.1 mV. This result validates the effectiveness of the matching techniques.

The electrical performance of the block was improved, achieving a 47.9% reduction in average power consumption (from 80.61 μW to 42.00 μW), along with a 50.6% increase in bandwidth and 38.5% in Slew Rate. The increase in design area was a fundamental investment to achieve these improvements in efficiency and ensure less variation in the switching frequency, as supported by the results of Monte Carlo and PVT simulations.

BIBLIOGRAPHY

ALLEN, Phillip E. and Douglas R. HOLBERG. *CMOS Analog Circuit Design*. OXFORD UNIVERSITY PRESS, 2001.

AMAYA AMAYA, Over Jose and Victor Hugo MUÑOZ LÓPEZ. “Design of Base-Band Circuits for a PWM Controller in a DC-DC Buck Converter in CMOS Technology node of 28nm”. Bachelor’s thesis. Universidad Industrial de Santander, 2024 (cit. on pp. 12, 17–20, 27, 28, 31).

BAKER, R. Jacob, Harry W. LI, and David E. BOYCE. *CMOS. Circuit design layout and simulation*. Fourth Edition. IEEE Press, 2019.

BARRIOS RUEDA, Daniel Felipe and Nestor Ivan MATAJIRA ORTIZ. “Design of Energy-Efficient Voltage Comparators for a System-on-Chip Using a CMOS Technology Node of 28nm”. Bachelor’s thesis. Universidad Industrial de Santander, 2024 (cit. on pp. 20, 30, 31).

CHEN, Yuan et al. A General Frequency-Domain Model of Trailing-Edge and Leading-Edge Carrier PWM dc–dc Converter Based on Hybrid Continuous and Discrete-Time Descriptions. In: *IEEE Journal of Emerging and Selected Topics in Power Electronics*. 2021, vol. 9. DOI: 10.1109/JESTPE.2020.2982179.

FRANCESCO VASCA, Luigi Iannelli. *Dynamics and Control of Switched Electronic Systems*. Prentice Hall, 2012.

HASTINGS, A.. *The Art of Analog Layout*. 3rd ed. Pearson, 2024.

LEE, Min-Chin and Yi-Chiuan CHEN. Implementation of a ramp generator with Schmitt trigger circuit for PWM modulator applications. In: *2017 Progress in Electromagnetics Research Symposium - Fall (PIERS - FALL)*. 2017. DOI: 10.1109/PIERS-FALL.2017.8293500.

LIENIG, J. and J. SCHEIBLE. *Fundamentals of Layout Design for Electronic Circuits*. Springer International Publishing, 2020.

P. G. DRENNAN, M. L. Kniffin and D. R. LOCASCIO. Implications of Proximity Effects for Analog Design. In: *IEEE Custom Integrated Circuits Conference (CICC)*. 2006, pp. 1–5.

PIPINO, A.. *Design of Analog Circuits in 28nm CMOS Technology for Physics Applications*. Ph.D. Dissertation. Università degli Studi di Milano-Bicocca, 2016.

RAZAVI, B. The Cross-Coupled Pair—Part I [A Circuit for All Seasons]. In: *IEEE Solid-State Circuits Magazine*. 2014, vol. 6, no. 3.

RAZAVI, B. The Cross-Coupled Pair—Part II [A Circuit for All Seasons]. In: *IEEE Solid-State Circuits Magazine*. 2014, vol. 6, no. 3.

SAHRLING, M.. *Layout Techniques for Integrated Circuit Designers*. Artech House, 2020.

SAINT, C. and J. SAINT. *IC Layout Basiscs: A practical guide*. McGraw-Hill, 2001.