Control of Three Phase Inverters Under Voltage Sags

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Dedicatoria

Este trabajo está dedicado a mi hija Lucía. Esta aventura comenzó por ti, en busca de bienestar y un mejor futuro. Tú fuiste mi fuente de motivación durante estos cinco años. Eres una niña muy inteligente y capaz; has crecido demostrando independencia para realizar tus deberes y empatizas fácilmente con los demás. Por eso creo que te resulta sencillo relacionarte con la gente. El tener que separarme de ti durante un año fue una de las decisiones más difíciles que he tomado en mi vida, pero fue necesario. He terminado una etapa, pero espero poder cumplir con mi rol de padre durante muchos años más.

Luchi, este trabajo fue realizado por y para ti. Espero lo veas como un ejemplo de que las cosas que valen la pena requieren esfuerzo, sacrificio y perseverancia. Paradójicamente, para lograr objetivos y metas, también se debe aprender a soltar y decir "con esto es suficiente". Es la principal enseñanza que me deja este doctorado y te la quiero compartir. Todo en la vida se trata de un balance; ahora decirlo es fácil, lograrlo es otro cuento. Si bien la disciplina es necesaria, el ser demasiado rígida puede acabar contigo. Las pausas y el descanso son igual de importantes que el arduo trabajo. Esto pasa en el doctorado cuando te centras tanto en la solución que te olvidas del problema. Te vuelves ineficiente y se pierde la creatividad; se comienzan a complicar cosas que deberían ser sencillas. Ahí es donde compartir espacios diferentes ayuda a aclarar la mente.

Lograr ese equilibrio requiere criterio, autocrítica, compasión y autoestima. Recuerda, lo más importante siempre serás tú, tu salud y bienestar. Y si algún día llegas a ser madre, espero

logres entender que el sacrificio de un padre no es porque él crea que tú eres más importante, sino que desde ese momento en el que tomas su manita y prometes cuidarla por el resto de su vida, ese bebé pasa a ser parte de ti, de tu bienestar y felicidad. Pasas a compartir su dolor y alegría, y eso hace que el esfuerzo valga la pena. Te amo.

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Abbreviations

[BBTW] Butterworth filter

[CS] Current Strategy

[EKF] Extended Kalman Filter

[DSRF] Double Synchronous Reference Frame

[DDSRF] Double Decouple Synchronous Reference Frame

[DPGS] Distributed Power Generation Systems

[DSC] Delayed Signal Cancellation

[GC] Grid Code

[GGC] German Grid Code VDE-AR-N 4120

[GFL] Grid Following

[GFM] Grid Forming

[LVRT] Low-Voltage Ride-Through

[MAF] Moving Average Filter

[MPPT] Maximum Power Point Tracking

[PCC] Point of Common Coupling

[PI] Proportional-Integral

[PLL] Phase Locked-Loop

[PPT] Power Point Tracking

[PR] Proportional-Resonant

[PWM] Pulse With Modulation

[RCI] Reactive Current Injection

[RLMS] Recursive Least Mean Square

[SCC] Short Circuit Current

[SG] Synchronous Generator

[SRF] Synchronous Reference Frame

[SVM] Space Vector Modulation

[THD] Total Harmonic Distortion

[TRD] Total Radio Distortion

[TSSE] Two-Sample Sequence Extractor

Nomenclature

[C_{dc}] DC-link capacitor

[f_s] Sampling frequency

[θ^+] Argument of the positive sequence voltage

[θ^-] Argument of the negative sequence voltage

[i_{abc}] Phase currents in the *abc* frame

[I_{abc}] Amplitudes of the phase currents in the *abc* frame

[I_{nom}] Nominal current of the inverter

[I_p^+] Amplitude of the active positive sequence current

[I_p^-] Amplitude of the active negative sequence current

[I_q^+] Amplitude of the reactive positive sequence current

[I_q^-] Amplitude of the reactive negative sequence current

[L_g] Impedance of the line impedance

[p] Instantaneous active power injected to the grid

[P] Average component of the active power injected to the grid

[$\tilde{p}$] Oscillatory component of p

[$\tilde{P}$] Amplitude of $\tilde{p}$

[P_L] Maximum inverter losses

[q] Instantaneous reactive power injected to the grid

[Q] Average component of the reactive power injected to the grid

[$\tilde{q}$] Oscillatory component of q

[$\tilde{Q}$] Amplitude of $\tilde{q}$

[R_g] Resistance of the line impedance

[v_{dc}] Voltage at the DC-link

[V_{dc}] Nominal value of the DC-link voltage

[$\tilde{v}_{dc}$] Oscillatory component of the DC-link voltage

[V^+] Amplitude of the positive sequence voltage

[V^-] Amplitude of the negative sequence voltage

[v_{abc}] Phase voltages in the *abc* frame

[V_{abc}] Amplitudes of the phase voltages in the *abc* frame

[V_g] Voltage source of the grid model

[V_{nom}] Nominal voltage of the inverter

[φ^{+}] Phase of the positive sequence voltage

[φ^{-}] Phase of the negative sequence voltage

[Z_g] Line impedance of the grid model

[ω] Nominal angular frequency of the system

[ω_c] Cut-off frequency

[ω_s] Estimated angular frequency

Resumen

Título: Control of Three Phase Inverters Under Voltage Sags [*]

Autor: David Javier Rincón Adarme [**]

Palabras Clave: Algoritmo de sincronización, Estrategia de inyección corriente, Fuentes controladas de tensión, Hundimientos de tensión, Inversor de potencia.

Descripción:

Esta tesis doctoral se enfoca en mejorar el desempeño de inversores de potencia conectados a la red durante hundimientos de tensión. Se realizó una revisión de diferentes códigos de red (GC) para definir los requerimientos y las características de operación deseadas del convertidor durante hundimientos de tensión. Con base en esta revisión, esta tesis presenta dos contribuciones principales.

La primera contribución es un algoritmo de sincronización con un corto tiempo de stablecimiento, lo cual es crítico para la operación de inversores conectados a la red durante hundimientos de tensión. El algoritmo emplea un nuevo extractor de secuencias de dos muestras (TSSE) combinado con un seguidor de fase (PLL). El algoritmo TSSE extrae las componentes de secuencia positiva y negativa mientras que el PLL se usa para estimar la frecuencia fundamental de la red. Para mitigar el efecto de la distorsión armónica en la estimación del TSSE y del PLL, se utiliza un filtro Butterworht y un filtro de cancelación de señal retrasada (DSC), respectivamente. El desempeño del algoritmo de sincronización se evalúa a través de pruebas experimentales en lazo abierto y en lazo cerrado. Los resultados muestran la eficacia del TSSE-DCS en mejorar la estimación de las componentes de secuencia durante condiciones de red anormales para convertidores seguidores de red.

La segunda contribución es un algoritmo generador de la corriente de referencia o *estrategia de corriente*, que cumple con los requerimientos de la nueva generación de GC. Esta estrategia considera las condiciones pre falla para realizar la reducción de corriente, priorizando la inyección de corriente reactiva. Como objetivo segundario al soporte de tensión, la estrategia reduce las oscilaciones en la potencia activa instantánea y por ende en la tensión de la barra DC, al ajustar la inyección de corriente reactiva a través de la secuencia negativa de acuerdo al estándar alemán VDE-AR-N4120. El desempeño de la estrategia es validado por medio de simulaciones de un sistema de transmisión y pruebas experimentales en un modelo escalado. Los resultados confirman que la estrategia mitiga las oscilaciones en la potencia activa instantánea y permite incrementar la inyección de potencia activa proporcionando soporte de tensión a la red.

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[*] PhD Thesis

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Abstract

Title: Control of Three Phase Inverters Under Voltage Sags [*]

Author: David Javier Rincón Adarme [**]

Keywords: Low-Voltage Ride-Trough, Synchronization Algorithm, Current Strategy, Voltage Source Converter, Power Inverter.

Description:

The present doctoral thesis focuses on enhancing the performance of grid-connected inverters under voltage sags. A literature review on grid codes (GC) was conducted to define Low-Voltage Ride-Through (LVRT) requirements and desired converter operating characteristics. Based on those, this thesis presents two major contributions.

The first contribution is a synchronization algorithm that exhibits a short settling time, which is critical for the operation of grid-connected converters under voltage sags. The algorithm employs a novel two-sample sequence extractor (TSSE) combined with a phase-locked loop (PLL). The TSSE extracts the positive and negative sequences while the PLL is used to estimate the grid frequency. To mitigate harmonic distortion effects on the TSSE and PLL estimations, a third-order Butterworth filter and a Delayed Signal Cancellation (DSC) filter are used, respectively. The algorithm's performance is evaluated through experimental tests in open- and closed-loop configurations. Results underscore the efficacy of the DSC-TSSE in enhancing the estimation of the voltage sequences during grid abnormal conditions for grid-following converters.

The second contribution is a reference signal generator, or *current strategy*, that meets new generation GC requirements. This strategy incorporates pre-fault conditions to manage current scale down, prioritizing reactive current injection. As a secondary objective to the voltage support, it reduces the instantaneous active power oscillations and thus DC-bus voltage fluctuations, by adjusting the reactive negative sequence current injection in compliance with the German VDE-AR-N 4120 standard. The performance of the proposed strategy is validated through transmission system simulations and experimental tests in a scaled-down model. Results confirm that the strategy mitigates instantaneous active power oscillations and allows increased active power supply while voltage support is provided to the grid.

Overall, the proposed synchronization algorithm and current reference strategy address key challenges faced by grid-connected inverters under voltage sags. Together, they improve the converter's dynamic response, ensure compliance with evolving grid code requirements, and enhance fault ride-through capability. The thesis concludes by presenting conclusions and future research lines.

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Introduction

A reliable energy supply is crucial for the development of a society and its individuals. However, conventional power generation relies on finite resources such as coal and petroleum, which produce substantial greenhouse gas emissions, including carbon dioxide and methane. A sustainable alternative is renewable energy generation using wind, solar, low-carbon hydrogen, and other inexhaustible or naturally replenished resources [1]. Renewable energy sources are not only more environmentally friendly but also increasingly cost-effective compared to most of the conventional generation methods [2, 3].

As a result, renewable energy penetration into the power grid has grown significantly over the past decade [4, 5]. Wind and photovoltaic (PV) systems require power inverters to interface with the grid, offering improved controllability and operational efficiency [6]. However, unlike synchronous generators, power inverters lack inherent system inertia [3, 7], making them more susceptible to grid disturbances caused by the intermittent nature of renewable sources, faults, and other system events.

The intermittent nature of renewable sources introduces challenges such as supply-demand mismatches and generation fluctuations, which can lead to frequency instability [3, 6]. Additionally, voltage stability is influenced by power flow variations, potentially compromising grid reliability [8]. In the past, distributed power generation systems (DPGS) were allowed to disconnect during grid disturbances. However, as DPGS penetration increased, this approach raised concerns as widespread disconnections could trigger cascading failures compromising the grid stability [9].

To address these challenges, many countries have updated their grid codes (GCs) to regulate the interconnection of DPGS [1, 10]. A well-known GC requirement is the Low-Voltage Ride-Through (LVRT) capability, which states that DPGS must remain connected to the grid during voltage sags to prevent sudden tripping and loss of generation [11, 12]. The primary objective of LVRT is to support voltage recovery within the shortest possible time.

General criteria establish that the sag has to be quickly detected, and the full power capacity of the inverter must be exploited [12]. Additionally, three critical inverter quantities must be managed: 1) maximum AC output current, 2) maximum AC output voltage, and 3) maximum DC-link voltage [13]. Therefore, voltage support strategies must ensure these parameters remain within safe operational limits. Furthermore, GCs specify requirements like the minimum injection of reactive current and the maximum voltage level at the Point of common coupling (PCC). Other desirable secondary objectives include minimizing voltage oscillations on the DC-link and low harmonic content on the injected currents.

The control system of a power inverter consists of multiple loops, including synchronization, current control, and reference signal generation. For a correct operation of the inverter during voltage sags, the control strategy of each loop must take into account aspects that are not considered under normal operation conditions, i.e., the presence of negative sequence and phase shifts on the grid voltages [14]. Additionally, these strategies must comply with GCs and standards related to power quality, current injection, settling time, and measurement accuracy [15–18].

This thesis focuses on improving the performance of grid-connected power inverters under voltage sags. Specifically, it proposes a synchronization algorithm and a reference current strategy

that enhance the LVRT capabilities of the inverter. The rest of this doctoral thesis is organized as follows.

- **Chapter 1** provides an overview of three-phase grid-tie power converters, and outlines the objectives and contributions of the thesis.
- **Chapter 2** presents the first contribution of this thesis: a synchronization algorithm for rapid and accurate estimation of the positive- and negative-sequence voltages under abnormal grid conditions.
- **Chapter 3** discusses the second contribution: a reference current generator for grid-connected inverters under voltage sags, designed in compliance with modern grid code requirements.
- Finally, conclusions are presented summarizing this thesis findings and potential directions for future research.

1. Theoretical Framework

This chapter presents the main characteristics of voltage sags, reviews the LVRT requirements of different GCs, provides an overview of voltage support strategies, and describes the system model and its corresponding control loops. In addition, this chapter introduces the objectives and main contributions of the thesis.

1.1. Voltage Sags

A voltage sag is a short-time reduction in the RMS voltage value in one or more grid phases, typically caused by short circuits, overloads, or the start-up of large motors. Table 2 of Std IEEE 1159 classifies different electromagnetic phenomena, including voltage sags [19]. Although magnitude and duration are the main characteristics of voltage sags, other features like phase angle jumps and unbalance must be considered [14]. Symmetrical faults occur infrequently, accounting for only about 2-3 % of all grid faults [20]). Consequently, most grid faults are asymmetrical, leading to the presence of negative- and zero-sequence voltage components in the grid [21, 22].

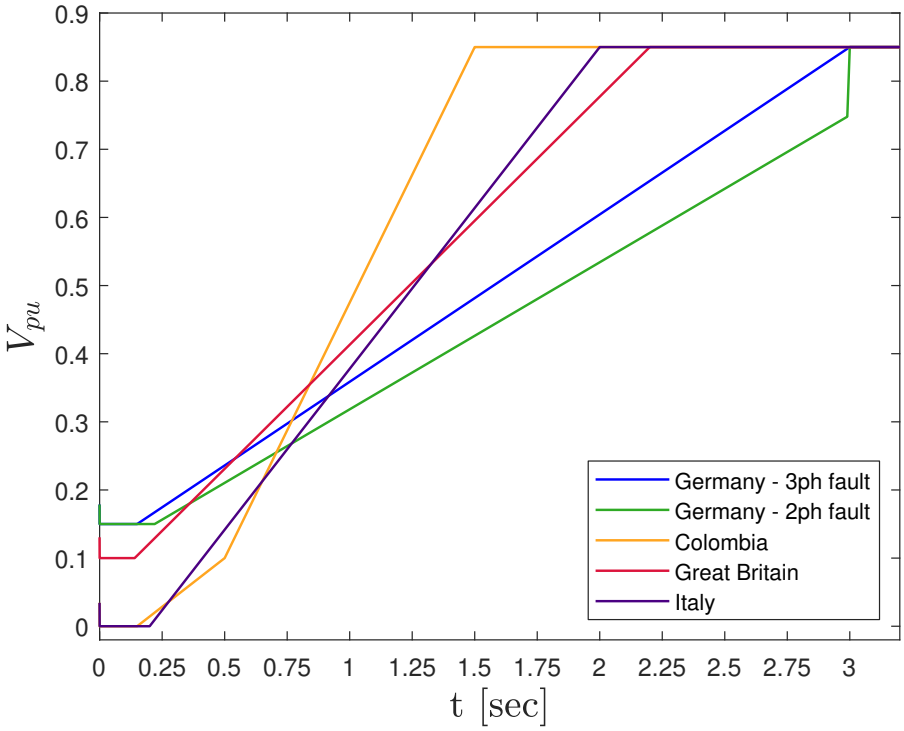
1.2. Grid Codes and Technical Requirements

GCs are technical regulations imposed by the transmission and distribution system operators seeking to guarantee the stability and regulation of the system frequency and voltage [23, 24]. Due to the substantial growth in renewable energy generation, DPGS requirements have become increasingly stringent in many countries over the past decade [25]. Specifically, GCs require DPGS to stay connected to the grid during voltage sags. Furthermore, maximum current and reactive current injection (RCI) are often requested to support the voltage recovery. Once the fault is cleared,

the DPGSs must resume active power supply [26]. A voltage versus fault duration profile is defined to consider the safety of the equipment. Figure 1.1 shows the profiles of different national GCs. Disconnection is allowed for voltages below these profiles [25, 27].

Figure 1.1

LVRT curves from selected countries

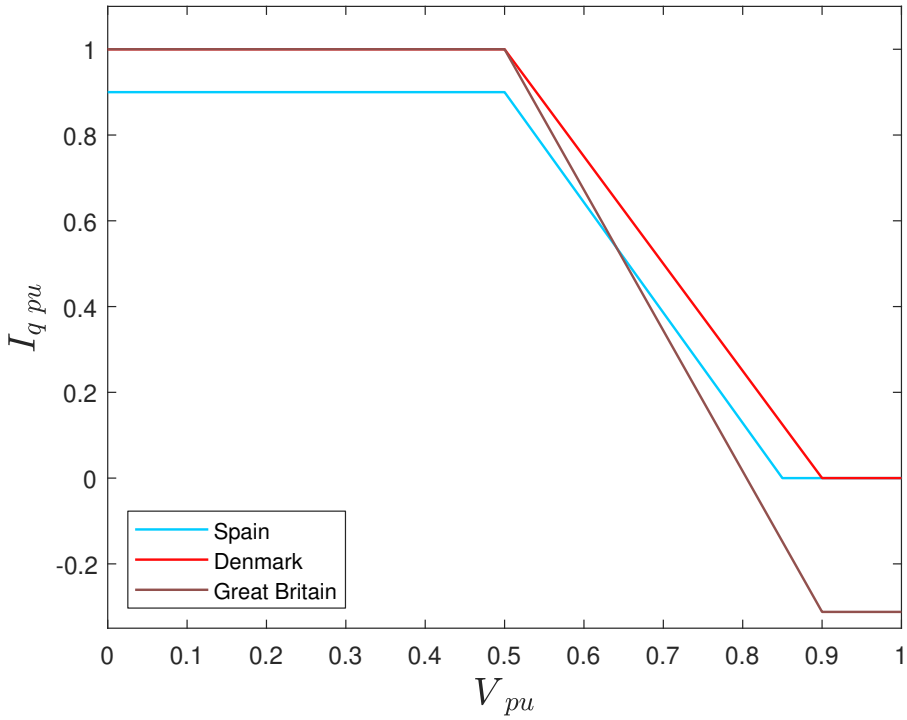


In the same way, some GCs define a minimum RCI profile to provide voltage support. Figure 1.2 shows traditional RCI requirements [27, 28]. These only considered the injection of current through the positive sequence component. The RCI requirement can also be determined based on the on-grid voltage reduction during the fault, e.g., GCs of Germany and Colombia [29, 30]. In this case, the RCI is defined in terms of the difference between the pre-fault and the fault voltages rather than just considering the last ones. Moreover, a new generation of GCs defines requirements

for the injection of current through the negative sequence component [31, 32]. A more detailed discussion of these requirements is provided in Chapter 3.

Figure 1.2

Reactive current injection required in different GCs



In addition, the maximum phase voltage must comply with the range established by the GC. International standards also define the requirements for DGPSs interconnection to the grid; as summarized in Table 1.1. These standards provide guidelines for desirable operation characteristics, which include reactive power injection, limits for the harmonic content of the voltages at the PCC and the injected currents, and voltage and frequency ride-through requirements. National GCs usually adopt or reference these international standards as a baseline to establish their

interconnection requirements.

Table 1.1

International standards related to the interconnection of DPGS to the grid.

Standard	Subject
IEEE Std 519 [15]	IEEE Standard for Harmonic Control in Electric Power Systems
IEEE Std 1547 [16]	IEEE Standard for Interconnection and Interoperability of Distributed Energy Resources with Associated Electric Power Systems Interfaces
IEEE Std 2800 [17]	IEEE Standard for Interconnection and Interoperability of Inverter-Based Resources (IBRs) Interconnecting with Associated Transmission Electric Power Systems
EN-50549 [33]	European Standard: Requirements for generating plants to be connected in parallel with distribution networks - Part 2: Connection to a MV distribution network - Generation plants up to and including Type B

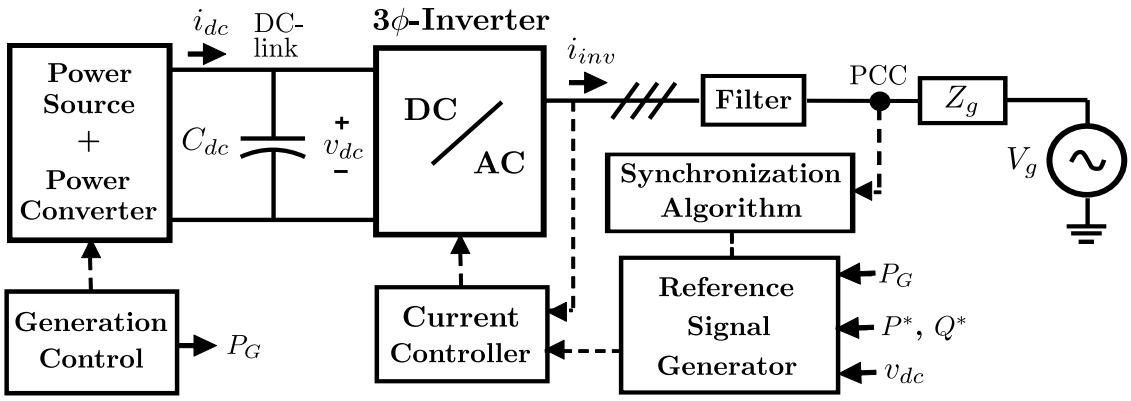
In general, for the inverter safety, three key technical limitations must be addressed: 1) maximum phase current limit, 2) maximum phase voltage limit, and 3) maximum DC-link voltage limit [13]. Additionally, secondary objectives such as minimizing DC-link voltage oscillations, the reduction of harmonic content on the injected currents, and the mitigation of power oscillations are also desired [34–38].

1.3. Grid-Connected Inverter

Fig. 1.3 shows a general scheme of a grid-connected inverter in DPGS applications. The Generation Stage consists of the power source (wind, solar, storage system, etc.) and a power

Figure 1.3

Scheme of a grid-connected inverter in DPGS applications



converter whose characteristics depend on the source type. For example, a photovoltaic system may employ a DC-DC converter to regulate voltage and control power output. A DC-link capacitor C_{dc} is used to balance the power exchange between the inverter and the Generation Stage. A filter is implemented at the output of the three-phase inverter to reduce the high-frequency harmonics. The grid is represented by a line impedance Z_g and a voltage source V_g. Although not included in the scheme, some loads could be connected at the point of common coupling (PCC), and Z_g can include the impedance of a power transformer between the inverter and the grid.

1.4. Control Loops

In general, power electronics converters used for DGPS can be classified into two types: Grid-Forming (GFM) and Grid-Following (GFL) converters [39, 40]. The main difference between them is how they synchronize with the grid [41]. GFM converters are designed to operate as an ideal source with constant voltage amplitude and frequency to form an AC voltage autonomously. However, when integrated with other GFM converters or synchronous generators (SG), a frequency

droop control (usually a P - ω droop) is necessary [39]. This emulates the rotor characteristics of an SG, enabling a power synchronization with the grid [41].

On the other hand, GFL converters use a synchronization algorithm, usually a phase-locked loop (PLL), to estimate the phase and the frequency of the PCC voltage, performing the synchronization with the grid. The estimated voltage parameters are then used to define a current vector that regulates the active and reactive power exchange [41]. Each converter type has benefits and drawbacks. GFM converters are an emerging technology that presents adequate operation for weak grids [39]. In contrast, GFL converters are adequate for strong grids operation but its stability could decrease in weak grids.

This thesis focused on GFL converters since these are widely used in practical applications across both small- and large-scale generation systems [39, 40]. The main control loops of a GFL converter are shown in Fig. 1.3. A description of each loop is presented below.

a) Synchronization Algorithm

For GFL converters, the synchronization algorithm must estimate the amplitude and phase of the PCC voltages. Additionally, symmetrical component calculation is essential for monitoring, diagnostics, and control purposes, particularly during asymmetrical fault conditions [42, 43]. Phase-Locked Loops (PLL) algorithms are the most widely adopted approach for grid-voltage synchronization, primarily due to ease of formulation and low computational burden [44].

The basic structure of a PLL consists of a phase detection block, a loop filter, and a

voltage-controlled oscillator [45]. The main difference among PLL algorithms is the phase detection method [44, 46]. The detection block is usually modified to deal with grid disturbances, e.g., voltage sags, phase jumps, and voltage unbalance, and to enhance the disturbance rejection capability of the PLL. Other proposals are based on extended Kalman filters, adaptive Notch filters and Least Mean Squares (LMS) Filters [47–49]. This thesis proposes a synchronization algorithm with desirable performance under voltage sags, which is developed in Chapter 2.

b) Reference Current Generator

This loop generates the reference current signals for grid injection; hence, it is also referred as the Current Strategy. Reference current generators are classified into two types based on their control approach. In the first type, the reference currents are generated using a close-loop control to regulate variables of the system like the DC-bus voltage or the PCC voltage level [50–52]. For the second type, instantaneous power theory approach is preferred to calculate the values of the currents [1, 34]. It is worth mentioning that it is usual to find strategies that combine the two mentioned types [36, 53].

Table 1.2 summarizes the characteristics of several LVRT reference current generators proposed in the last decade [54]. It begins with the Instantaneous Active Reactive Control strategy in which distorted currents are injected to guarantee constant power delivery [45]. However, the injection of high harmonic contents is not a common practice. Instead, the vast majority of the strategies opt to inject non-distorted currents and deal with active and reactive

power oscillations [54].

The review also reveals that over time, current strategies tend to include more aspects to improve the inverter performance. For instance, early works only contemplate the injection of P or Q during a voltage sag [55–58]. Although this simplifies the inverter control, injection of both components is desirable to provide major support to the grid. Furthermore, many studies adopt a flexible approach in which scalar coefficients are employed to adjust the current reference, enabling desired control characteristics such as distortion-free reference currents and mitigation of power oscillations [12, 26, 54, 56, 59].

In fact, multiple studies concluded that the grid impedance should be considered to enhance the voltage support, and these include the resistive component of Z_g in their analysis [60–63]. Nevertheless, grid impedance commonly changes during faults. Although real-time grid impedance estimation is a research area, current methods do not provide the rapid response needed to fulfill the LVRT current injection requirements [64, 65]. Consequently, treating Z_g as a known and constant parameter during a voltage sag is impractical for optimizing voltage support [54].

Moreover, Table 1.2 indicates that the GCs' RCI requirement is rarely contemplated [26, 66]. Additionally, most strategies do not consider the three technical restrictions mentioned for the converter. The majority focus only on the maximum current limitation. However, it is important to define how the current strategy addresses over-voltages or power curtailment scenarios to ensure an adequate operation of the converter. For example, if a current

strategy has a closed-loop that regulates the DC-link voltage, it must be coordinated with the generation control during the fault. Otherwise, poor power balance regulation can lead to undesirable DC-bus voltage behaviors.

To address practical applications, this thesis proposes a reference current generator based on the German GC VDE-AR-N 4120 standard [31]. The proposed strategy fulfills the German GC requirements and the technical restrictions of the converter. The strategy also minimizes active power oscillations within the constraints of the GC requirements. The proposal is later introduced in Chapter 3.

c) Current Controller

The current controller tracks the reference signal and generates the pulses for the inverter. A first type of controllers generate the pulses based on the current error; these are known as ON/OFF techniques and include the delta and hysteresis control [45]. A second type estimates the inverter voltage to track the reference current. In such cases, Space Vector Modulation (SVM) or Pulse-Width Modulation (PWM) techniques are used to generate the switching pulses based on the voltage reference. SVM techniques determinate the ON/OFF states combination and the switching periods based on the location of the reference voltage on the $\alpha\beta 0$ or the $dq0$ reference frames [67, 68].

Table 1.2

Characteristics of different reference current generators.

			Restrictions			**Secondary objectives**			**Control features**					
Control Strategy	Year	Flexible	Over Current Control[1]	Over Voltage Control[2]	Deals with Power Curtailment[3]	Osc. Control[4] $\tilde{p}_{2\omega}$	Osc. Control[4] $\tilde{q}_{2\omega}$	v_{dc} Osc. Control	Injection[5] P	Injection[5] Q	Grid Impedance[6] R_g	Grid Impedance[6] X_g	RCI-GC[7]	Complexity
[45]	*	×	✓	×	×	✓	✓	✓	✓	✓	×	×	×	Low
[55]	2012	✓	×	×	×	✓	×	✓	✓	×	×	✓	×	Low
[57]	2013	✓	○	✓	×	×	×	×	×	✓	×	✓	×	Low
[59]	2013	✓	✓	×	×	○	×	×	✓	✓	×	✓	×	Medium
[58]	2014	✓	✓	✓	×	×	×	×	×	✓	×	✓	✓	Medium
[56]	2014	✓	×	×	×	×	×	×	✓	×	✓	×	×	Low
[66]	2014	×	✓	✓	×	×	×	-	×	✓	×	✓	✓	Low
[11]	2015	✓	✓	×	✓	×	×	×	✓	✓	✓	✓	×	Low
[13]	2015	×	✓	✓	×	×	×	✓	×	✓	×	✓	×	Medium
[52]	2015	×	✓	✓	×	×	×	×	✓	✓	×	✓	×	Low
[60]	2016	×	×	×	×	○	○	○	✓	✓	✓	✓	×	Low
[10]	2016	✓	✓	×	×	✓	×	✓	✓	✓	×	×	×	Low
[12]	2017	✓	✓	×	✓	✓	×	✓	✓	✓	×	×	×	Medium
[26]	2018	✓	✓	×	×	○	×	○	✓	✓	×	×	✓	Medium
[34]	2018	×	✓	✓	✓	○	×	○	✓	✓	✓	✓	×	High
[61]	2018	×	✓	×	×	×	×	×	✓	✓	✓	✓	×	Low
[69]	2018	✓	✓	✓	×	×	×	-	✓	✓	×	✓	✓	Low
[70]	2019	✓	✓	×	×	○	○	○	✓	✓	×	×	×	Medium
[62]	2019	×	✓	×	×	×	×	×	✓	✓	✓	✓	×	Low
[71]	2020	✓	✓	✓	×	○	○	○	✓	✓	✓	✓	×	Medium
[63]	2020	✓	✓	×	×	✓	×	✓	✓	✓	✓	✓	×	Low
[72]	2021	○	✓	×	×	✓	○	✓	✓	✓	×	×	×	Low
[73]	2023	✓	✓	✓	×	×	×	×	✓	✓	×	×	✓	Medium
[74]	2024	✓	✓	✓	✓	×	×	×	✓	✓	✓	✓	×	Medium
[75]	2025	✓	✓	✓	✓	✓	×	✓	✓	✓	✓	✓	×	High

✓Achieved or partially covered × Not achieved ○ Achieved under certain conditions – Unable to determinate. [1] The table refers to limiting the maximum instantaneous phase current. [2] The table refers to limiting the maximum instantaneous phase voltage at the PCC. [3] The table refers to the capability of the control to deal with the extra energy on the Generation Stage caused by the power curtailment. Specifically, to the coordination between the generation loop and the current reference generator. [4] The table describes if instantaneous active or reactive power oscillations are canceled or mitigated. [5] The table shows if the algorithm can inject active and/or reactive power during the voltage sag. [6] The table shows whether the control strategy considers the line resistance or inductance. [7] Reactive current injection according to grid code.

On the other hand PWM techniques compares the voltage reference with a carrier signal to generate the switching pulses [76]. Examples of linear current control techniques are Proportional-Integral (PI), Dead-Beat, and Proportional-Resonant (PR) controls [45, 77]. Non-linear control approaches include Fuzzy logic and artificial neural networks [78].

As mentioned, a filtering stage is added at the output of the inverter to mitigate the harmonic content [79]. Consequently, the current controller must account for the phase shift and magnitude attenuation introduced by the filter impedance in order to ensure fast and accurate tracking of the reference current. In this thesis, a damped LCL configuration is selected as the grid connection filter due to its low cost and small size [79, 80]. A proportional-resonant (PR) controller is employed to generate the inverter voltage reference based on the injected current error [81, 82]. The PR controller parameters are tuned using the Ziegler-Nichols second method for PI controllers [83]. Then, a PWM scheme is then implemented to generate the switching signals.

e) Generation Control and Power Balance

Generation control depends on the type of renewable distributed source. In general, under normal operation the objective is to maximize power output. For PV generation, maximum power point tracking (MPPT) techniques include incremental conductance, Perturb and Observe, and Fuzzy logic algorithms [84, 85]. However, during voltage sags, the active power injection capability of the inverter could be reduced due to the current limitations. This constraint can lead to a mismatch between the generated power and the power delivered to the grid, which is reflected in the DC-link capacitor voltage. Specifically, over-voltage on

C_{dc} due to excess of generated power that cannot be injected into the grid is a major concern.

In such cases, generation control could be operated in a non-MPPT mode to maintain the power balance between the injected power and the source [12, 38]. However, the performance of a power point tracking (PPT) algorithm to deal with DC-link voltages oscillations is limited by the power generation scenario and the amplitude of the double-frequency active power oscillations. Another strategy involves using a bidirectional converter with a power storage element, like batteries or super-capacitors for power balancing [50, 53]. While this approach offers a better power regulation, it is more expensive and requires more complex control. A third option is to consume the excess generated power using a chopper resistor [11, 38]. The resistor can handle excess power but not power deficits. Consequently, negative DC-link voltage oscillations are not eliminated. Nevertheless, this is a cost-effective approach with a simple formulation.

1.5. Objectives

Considering the above, the main objective of this thesis is:

- To improve the LVRT capability of grid-tie inverters by designing a control strategy that upgrades state-of-the-art proposals.

Based on this, the following specific objectives were proposed for the research:

To identify the power inverter behavior and requirements during voltage sags, looking for improvement opportunities for the control scheme.

To design a control strategy that considers aspects like the type of voltage sag, the grid impedance, and the power generation scenario, aiming to enhance the voltage support.

To evaluate the performance of the proposed strategy by simulations in *Matlab*®- *Simulink*, verifying the results with experimental data.

1.6. Contributions

This thesis presents two major contributions to improve the performance of grid-tie inverters under voltage sags. The first contribution is a synchronization algorithm that provides a fast and accurate estimation of the positive- and negative-sequence components under voltage sags and highly distorted voltage conditions. The algorithm is based on a novel Two-Sample Sequence Extractor (TSSE). The TSSE is based on the definition of the voltages in the $\alpha\beta$ reference frame in terms of the symmetric voltage components [86]. Since a five-variables system with two equations arises, a linear approximation between two voltage samples is used to perform the estimation. Therefore, the TSSE can estimate the amplitude and phase of the positive- and negative-sequence components as long as the system frequency is known. Consequently, the primary challenge in implementing the TSSE was to find a suitable frequency extractor.

Initially, this thesis considered a scenario with non-distorted voltages under grid abnormal conditions such as phase jumps, unbalanced voltages, and frequency changes. In this context, the TSSE shows to be compatible with a Recursive Least Mean Square (RLMS) frequency estimator [86]. The RLMS accurately estimates the system fundamental frequency (ω). Moreover, a feedback configuration with the TSSE significantly accelerates the RLMS estimation speed.

The TSSE-RLMS algorithm demonstrates superior performance in estimating voltage pa-

rameters compared to algorithms like the Decoupled Double Synchronous Reference Frame - PLL (DDSRF-PLL) and the Dual Second Order Generalized Integrator - PLL (DSOGI-PLL), thanks to its rapid and accurate estimation [86]. Nevertheless, the TSSE-RLMS exhibits a high overshoot in the estimation of the amplitudes and phase jumps during transients, which is undesirable for grid synchronization. Due to the TSSE's linear approximation, estimation errors increase with large voltage variations. While the TSSE-RLMS performance could be improved by including a pre-filtering stage, this was not initially considered to ensure a fair comparison with the studied algorithms, none of which incorporate filters to mitigate noise or harmonics.

For the next step, highly distorted voltage conditions were considered [15]. As a result, a Butterworth filter in the *abc* frame was incorporated to the TSSE-RLMS. The filter not only mitigates harmonic content, but it also improves the system stability. Additionally, the amplitude attenuation and phase shift introduced by the filter on the estimated voltages can be compensated using the TSSE outputs, the filter's transfer function, and the fundamental frequency ω. However, the performance of the RLMS is deteriorated by the filter's action. Consequently, the TSSE-RLMS estimation with the Butterworth filter became unacceptably slow, and so, inadequate.

As an alternative, a SRF-PLL with a Delayed Signal Cancellation (DSC) filter was used to estimate ω. This change improved the TSSE's speed, enabling it to estimate the sequence voltage amplitudes and phases within 1.3 fundamental cycles of the signal. Other contemplated algorithms required at least two cycles to perform the estimation. Moreover, the incorporation of the Butterworth filter solves the overshoot and phase jumps issues of TSSE. Notably, the steady-state error of the proposed algorithm (DSC-TSSE) during voltage sags meets the criteria established in va-

rious standards for normal operation conditions, which are more stringent than those defined for fault conditions [16, 17]. For these reasons, the DSC-TSSE exhibits an enhanced voltage sequence estimation during grid abnormal conditions for grid-following converters. The complete algorithm formulation and further performance analysis are presented in Chapter 2.

The second contribution is a LVRT current strategy that satisfies new generation GC requirements. Specifically, the proposed strategy is designed to comply the VDE-AR-N 4120 (GGC), the German GC for grid connection of generation installations, storage facilities, and combinations of these, for a voltage range of 60 kV to 150 kV [31]. The GGC defines the amount of reactive current that must be injected through the positive- and negative-sequence based on the amplitude variation of the corresponding voltage sequence. Furthermore, the GGC establishes that any necessary reactive current limitation is preferably achieved by uniformly reducing the positive- and negative-sequence currents.

Once the reactive current requirement has been fulfilled, the remaining capacity of the inverter must be used to inject active power through the positive sequence component. It is important to note that the GGC does not allow active power injection through the negative-sequence component. The GGC also employs load notation for the system requirements, where currents and powers are positive when entering the facility. However, this thesis uses source notation, which is often used in the literature. These GGC requirements are all considered in the proposed strategy.

A common error in GGC compliance is scaling down the current by a constant reference signal reduction, neglecting pre-fault conditions [73]. Although GGC states that current limitation is preferably achieved by uniform reduction of the reactive currents, this should apply only to the

additional current injection. The goal is to emulate the behavior of synchronous generators (SG), maintaining similar positive- and negative-sequence impedances during faults [73].

Instantaneous active power oscillations ($\tilde{p}$) cause voltage fluctuations at the DC bus at twice the fundamental frequency, potentially leading to power quality issues [87, 88]. Based on the previous, this thesis proposes a current strategy that prioritizes reactive current injection and maximizes active power delivery during faults, with the secondary objective of minimizing active power oscillations. The strategy uses the GGC's negative-sequence reactive injection tolerance to reduce the $\tilde{p}$ injected into the grid. Usually, active and reactive negative-sequence currents are selected to mitigate $\tilde{p}$ [10, 12, 26, 63, 89]. However, the GGC does not contemplate injecting active current through the negative sequence. As a result, the oscillating component of the active power injected via positive sequence current cannot be compensated. Furthermore, the GGC defines negative sequence reactive current injection, but its tolerance range allows operational flexibility during sags, which is exploited by the proposed strategy. A detailed explanation and analysis of the strategy are presented in Chapter 3.

2. Synchronization algorithm: DSC-TSSE

Synchronization algorithms are required for stable and efficient operation of three-phase grid-following converters connected to the grid. These algorithms must provide fast and accurate estimations of the frequency and sequence voltages to allow a secure grid connection even under abnormal grid conditions. This chapter introduces a novel three-phase synchronization algorithm that employs a Two-Sample Sequence Extractor (TSSE) combined with a PLL algorithm for frequency estimation. The input signals for the TSSE and the PLL are filtered by a third-order Butterworth filter and a Delayed Signal Cancellation (DSC) filter, respectively, to mitigate the harmonic distortion effects on the voltage estimations. The performance of the DSC-TSSE is evaluated through two types of experimental tests. First, an open-loop test is conducted for measurement calibration, comparing the proposed algorithm with other techniques. Second, a closed-loop test is performed to analyze and validate the behavior of the DSC-TSSE and the overall power converter control operating as a distributed generator with Low-Voltage Ride-Through (LVRT) capabilities under highly distorted grid voltage conditions.

This chapter is organized as follows. State-of-the-art is introduced in Section 2.1. Section 2.2 details the algorithm formulation. Section 2.3 presents the experimental results and their analysis. The main conclusions are stated in Section 2.4.

2.1. State-of-the-art

PLL algorithms are the most widely adopted approach for grid-voltage synchronization, primarily due to ease of formulation and low computational burden [44]. The PLL algorithms

mainly differ according to the adopted phase detection method [44, 46]. Conceptually, there are two approaches to enhance the phase detector performance. The first approach deals with the PLL performance during grid disturbances, e.g., voltage sags, phase jumps, and voltage unbalances [44, 90, 91]. Traditionally, phase estimation is based on the use of the positive-sequence components. In this context, sequence extractors, such as the Decoupled Double Synchronous Reference Frame (DDSRF-PLL) and the Dual Second Order Generalized Integrator (DSOGI-PLL), have been widely adopted [92].

The second approach is based on enhancing the disturbance rejection capability of the PLL [90, 93], using filtering methods, e.g., Moving Average Filters (MAF), Adaptive Notch Filters (ANF), and Delayed Signal Cancellation (DSC) filters [90, 93]. Enhancement of disturbance rejection capability results in slower dynamic response.

A common consideration for a PLL algorithm is the trade-off between the desirable transient response and the acceptable steady-state estimation error [43, 91]. The PLL instability, particularly under weak grid conditions, has been widely reported [94–98]. It should be noted that sequence extractors based on the $dq0$-frame transformation require an additional PLL to accurately estimate the phase of the negative sequence component [99]. Since the negative sequence is not predominant, tuning the negative sequence PLL represents an additional challenge for this algorithm.

Other types of synchronization algorithms include Adaptive Notch Filtering and Extended Kalman Filters (EKF) [47–49]. Reference [100] compares the performance of different synchronization algorithms under non-distorted conditions. The results indicate that the EKF provides the best performance. However, the EKF's complex formulation and high computational requirements

can be problematic for some practical applications [101].

This thesis proposed a voltage estimator based on a Two-Sample Sequence Extractor (TSSE) and a Recursive Least Mean Square (RLMS) frequency estimator [86]. In this case, a slide window approach RLMS is used to estimate the system's frequency. The TSSE-RLMS demonstrates desirable performance by estimating system parameters accurately and swiftly under abnormal grid conditions. Nonetheless, it exhibits significant overshoot, which is a drawback for synchronization applications. Additionally, the TSSE-RLMS shows poor speed when pre-filtering is abecaudded for noise rejection.

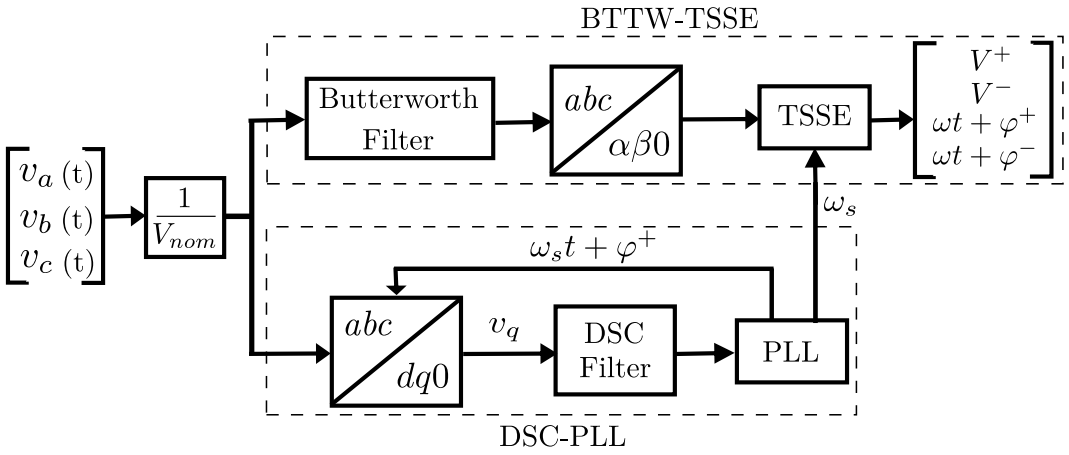
Considering the operational disadvantages of the previously mentioned techniques, this thesis proposes a Delayed Signal Cancellation Two-Sample Sequence Extractor (DSC-TSSE), which provides a fast and accurate estimation of the positive- and negative-sequence components under abnormal conditions and highly distorted voltages. The DSC-TSSE consists of two independent subsystems: a Two-Sample Sequence Extractor (TSSE) and a Synchronous Reference Frame Phase-Locked Loop (SRF-PLL). Both systems are filtered in order to deal with harmonic content. This filtering also addresses the TSSE's overshoot problem, making it suitable for grid synchronization. Furthermore, unlike sequence extractors based on the dq-frame transformation, the DSC-TSSE avoids the use of a secondary PLL to estimate the negative sequence argument. Additionally, the DSC-TSSE has a straightforward formulation and low computational burden, making it practical for practical applications.

2.2. Proposed DSC-TSSE algorithm

The proposed synchronization algorithm is illustrated in Fig. 2.1. It comprises two subsystems, the BTTW-TSSE, and a DSC-PLL. The BTTW-TSSE consists of a Butterworth filter and the TSSE. The filter mitigates the harmonic content of the PCC voltage signals, while the TSSE estimates the positive- and negative-sequence components. Additionally, an extra step is included in the TSSE to correct the Butterworth filter's amplitude gain and phase shift. The DSC-PLL comprises a SRF-PLL with a DSC pre-filtering stage and estimates the grid frequency rather than the phase of the positive sequence component. The components of the proposed algorithm are further elaborated as follows.

Figure 2.1

Black diagram of the DSC-TSSE



2.2.1. Butterworth Filter.

A Butterworth filter is characterized by its flat and linear phase response in the passband. This behavior is desirable to mitigate the impact on the magnitude and phase correction that the

TSSE performs. Nevertheless, a higher-order filter is necessary to attain a particular band-stop. In this sense, a third-order low-pass Butterworth filter with the transfer function

$$H(s) = \frac{\omega_c^3}{s^3 + 2\omega_c s^2 + 2\omega_c^2 s + \omega_c^3}, \tag{2.1}$$

is implemented, where ω_c denotes the cut-off frequency. This study assumes a nominal grid frequency of $f_0 = 60$ Hz. Considering that the IEC/IEEE 60255-118-1 suggests the frequency range of $f_0 \pm 5$ Hz for measurements, and a $\omega_c/2\pi$ close to f_0 increases the disturbances rejection and reduces the estimation speed, a value of $\omega_c = 160\pi$ rad/s is selected. The filter Bode plot is depicted in Fig. 2.2 and shows that the fundamental component of the filtered signal undergoes an amplitude attenuation and a phase shift. The phase shift is corrected by the TSSE, as explained in the subsequent section.

2.2.2. Two-Sample Sequence Extractor.

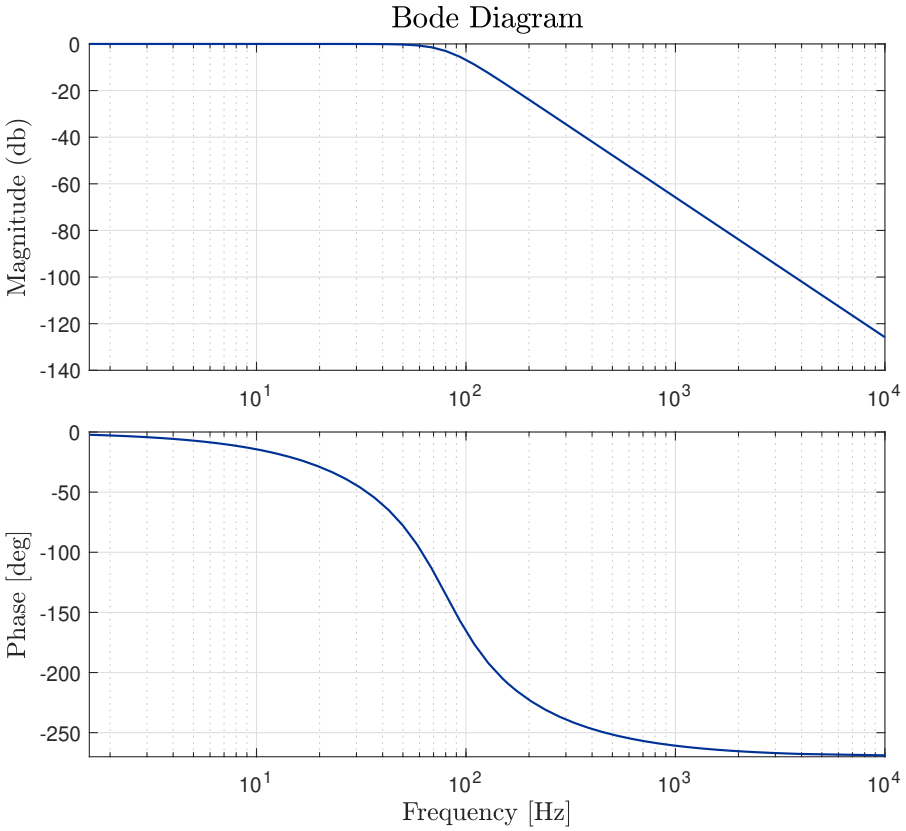
The TSSE operates on voltages represented in the $\alpha\beta$-frame, expressed in terms of their positive- and negative-sequence components [102]. These components can be expressed as

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \begin{bmatrix} V^+ cos(\omega t + \varphi^+) + V^- cos(\omega t + \varphi^-) \\ V^+ sin(\omega t + \varphi^+) - V^- sin(\omega t + \varphi^-) \end{bmatrix}, \tag{2.2}$$

where V^+, V^-, φ^+, and φ^- are the amplitudes and phases of the positive- and negative-sequences voltages, respectively, and ω is the grid angular frequency. Equation (2.2) is an undetermined system as it consists of two equations with four degrees of freedom, given that ω serves as an input provided by the PLL. To address this issue, the TSSE considers the samples taken at time instants

Figure 2.2

Bode diagram of (2.1) with $\omega_c = 160\pi$ *rad/s*



t_1 and t_2, i.e.,

$$\begin{bmatrix} v_\alpha(t_1) \\ v_\beta(t_1) \\ v_\alpha(t_2) \\ v_\beta(t_2) \end{bmatrix} = \begin{bmatrix} V^+cos(\omega t_1 + \varphi^+) + V^-cos(\omega t_1 + \varphi^-) \\ V^+sin(\omega t_1 + \varphi^+) - V^-sin(\omega t_1 + \varphi^-) \\ V^+cos(\omega t_2 + \varphi^+) + V^-cos(\omega t_2 + \varphi^-) \\ V^+sin(\omega t_2 + \varphi^+) - V^-sin(\omega t_2 + \varphi^-) \end{bmatrix}. \tag{2.3}$$

The system is reformulated by defining the variables Y_i and the coefficients B_j as:

$$\begin{bmatrix} Y_1 \\ Y_2 \\ Y_3 \\ Y_4 \\ B_1 \\ B_2 \end{bmatrix} = \begin{bmatrix} V^+cos(\omega t_2 + \varphi^+) \\ V^+sin(\omega t_2 + \varphi^+) \\ V^-cos(\omega t_2 + \varphi^-) \\ V^-sin(\omega t_2 + \varphi^-) \\ cos(\omega \Delta t) \\ sin(\omega \Delta t) \end{bmatrix}, \tag{2.4}$$

where $\Delta t = t_2 - t_1$. By substituting (2.4) in (2.3) the following system is obtained

$$\begin{bmatrix} v_\alpha(t_1) \\ v_\beta(t_1) \\ v_\alpha(t_2) \\ v_\beta(t_2) \end{bmatrix} = \begin{bmatrix} B_1 & B_2 & B_1 & B_2 \\ -B_2 & B_1 & B_2 & -B_1 \\ 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & -1 \end{bmatrix} \begin{bmatrix} Y_1 \\ Y_2 \\ Y_3 \\ Y_4 \end{bmatrix}. \tag{2.5}$$

From (2.5), the variables Y_i are defined as

$$\begin{bmatrix} Y_1 \\ Y_2 \\ Y_3 \\ Y_4 \end{bmatrix} = \frac{0.5}{B_2} \begin{bmatrix} 0 & -1 & B_2 & B_1 \\ 1 & 0 & -B_1 & B_2 \\ 0 & 1 & B_2 & -B_1 \\ 1 & 0 & -B_1 & -B_2 \end{bmatrix} \begin{bmatrix} v_\alpha(t_1) \\ v_\beta(t_1) \\ v_\alpha(t_2) \\ v_\beta(t_2) \end{bmatrix}. \tag{2.6}$$

An analysis of the TSSE's accuracy and guidelines for its tuning are presented in [86]. Additionally, to correct the amplitude attenuation and the phase shift caused by the Butterworth filter, it is necessary to calculate the gains of (2.1) at $s = j\omega_s$, where ω_s represents the PLL's estimated frequency, and thus the corrected variables Y_i^* are

$$\begin{bmatrix} Y_1^* \\ Y_2^* \\ Y_3^* \\ Y_4^* \end{bmatrix} = \begin{bmatrix} \dfrac{Y_1\cos(P_g) + Y_2\sin(P_g)}{M_g} \\ \dfrac{Y_2\cos(P_g) - Y_1\sin(P_g)}{M_g} \\ \dfrac{Y_3\cos(P_g) + Y_4\sin(P_g)}{M_g} \\ \dfrac{Y_4\cos(P_g) - Y_3\sin(P_g)}{M_g} \end{bmatrix}, \tag{2.7}$$

where M_g and P_g are the magnitude gain and the phase shift of the Butterworth filter, respectively. Then the amplitudes and the arguments of the positive- and negative-sequence components are calculated as

$$\begin{bmatrix} V^+ \\ V^- \\ \omega t + \varphi^+ \\ \omega t + \varphi^- \end{bmatrix} = \begin{bmatrix} \sqrt{(Y_1^*)^2 + (Y_2^*)^2} \\ \sqrt{(Y_3^*)^2 + (Y_4^*)^2} \\ atan(Y_2^*/Y_1^*) \\ atan(Y_4^*/Y_3^*) \end{bmatrix}. \tag{2.8}$$

To evaluate the TSSE estimation error, consider the set of measurements presented in (2.9), where $\omega_s = \omega - \omega_e$, $\Delta^+ = \Delta\varphi^+ + \Delta\omega\Delta t$, and $\Delta^- = \Delta\varphi^- + \Delta\omega\Delta t$, where ω_s is the estimated fre-

quency, ω_e is the error, and $\Delta\omega$ is the frequency variation. ΔV^+, ΔV^-, $\Delta\varphi^+$ and $\Delta\varphi^-$ are amplitude changes and phase signals shifts of the positive- and negative-sequences components, respectively. N_i represents the noise of each measurement.

$$\begin{bmatrix} v_\alpha(t_1) \\ v_\beta(t_1) \\ v_\alpha(t_2) \\ v_\beta(t_2) \end{bmatrix} = \begin{bmatrix} (V^+ - \Delta V^+)\cos(\omega(t-\Delta t)+\varphi^+ - \Delta^+) + (V^- - \Delta V^-)\cos(\omega(t-\Delta t)+\varphi^- - \Delta^-) + N_{v_{\alpha 1}} \\ (V^+ - \Delta V^+)\sin(\omega(t-\Delta t)+\varphi^+ - \Delta^+) - (V^- - \Delta V^-)\sin(\omega(t-\Delta t)+\varphi^- - \Delta^-) + N_{v_{\beta 1}} \\ (V^+)\cos(\omega(t)+\varphi^+) + N_{v_{\alpha 2}} \\ (V^-)\cos(\omega(t)+\varphi^-) + N_{v_{\beta 2}} \end{bmatrix}. \tag{2.9}$$

According to (2.4), estimated Y_1 is

$$Y_1 = 0.5\left[\frac{-v_\beta(t_1) + \sin(\omega_s\Delta t)v_\alpha(t_2) + \cos(\omega_s\Delta t)v_\beta(t_2)}{\sin(\omega_s\Delta t)}\right]. \tag{2.10}$$

Equation (2.10) can be expressed as

$$Y_1 = \frac{0.5}{\sin(\omega_s\Delta t)} \begin{pmatrix} V^+\cos(\omega t+\varphi^+)(\sin(\omega_s\Delta t) + \sin(\omega\Delta t - \Delta^+)) \\ +V^+\sin(\omega t+\varphi^+)(\cos(\omega_s\Delta t) - \cos(\omega\Delta t - \Delta^+)) \\ +V^-\cos(\omega t+\varphi^-)(\sin(\omega_s\Delta t) - \sin(\omega\Delta t - \Delta^-)) \\ +V^-\sin(\omega t+\varphi^-)(\cos(\omega_s\Delta t) - \cos(\omega\Delta t - \Delta^-)) \\ +\Delta V^+\sin(\omega t+\varphi^+)\cos(\omega\Delta t - \Delta^+) \\ -\Delta V^+\cos(\omega t+\varphi^+)\sin(\omega\Delta t - \Delta^+) \\ -\Delta V^+\sin(\omega t+\varphi^+)\cos(\omega\Delta t - \Delta^+) \\ +\Delta V^+\cos(\omega t+\varphi^+)\sin(\omega\Delta t - \Delta^+) \\ -N_{v_{\beta 1}} + \sin(\omega_s\Delta t)N_{v_{\alpha 2}} + \cos(\omega_s\Delta t)N_{v_{\beta 2}} \end{pmatrix}. \tag{2.11}$$

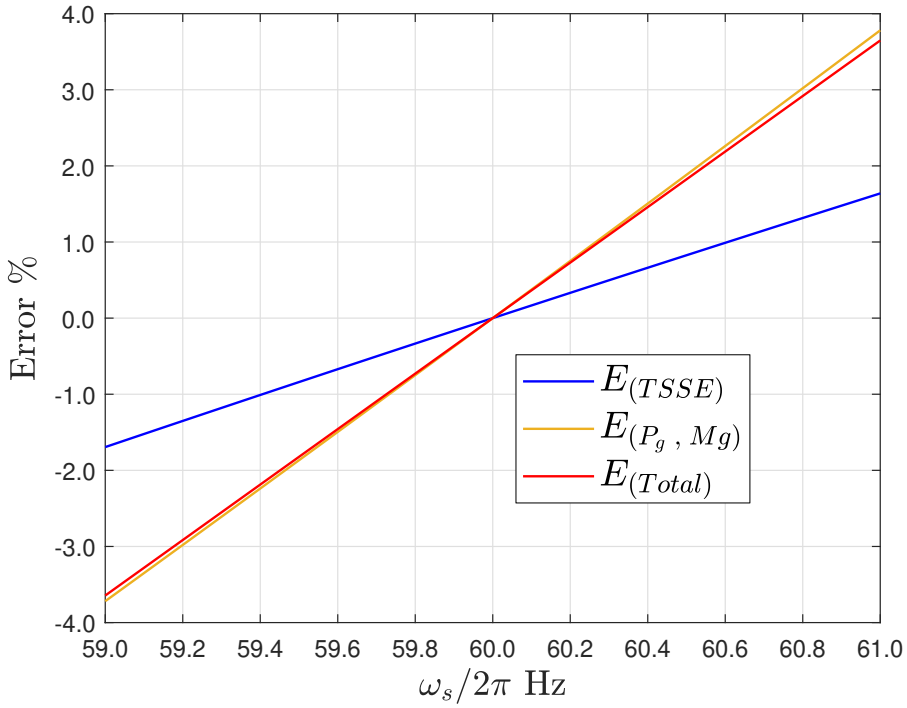
To analyze the TSSE accuracy, considering the error in the estimation of ω, the following assumptions are made: i) the signals' noise is negligible due to the Butterworth filter, ii) $\omega_s = \omega \pm (2\pi\times 1\text{ Hz})$, iii) $\Delta t = 1\times 10^{-4}$ s, and iv) the amplitude, phase, and frequency of voltages are constant. Under these assumptions, it can assume $\cos(\omega_s\Delta t) \simeq \cos(\omega\Delta t)$, and

$$Y_1 \simeq 0.5\begin{pmatrix} V^+\cos(\omega t+\varphi^+)\left(1 + \dfrac{\sin(\omega\Delta t)}{\sin(\omega_s\Delta t)}\right) \\ +V^-\cos(\omega t+\varphi^-)\left(1 - \dfrac{\sin(\omega\Delta t)}{\sin(\omega_s\Delta t)}\right) \end{pmatrix}. \tag{2.12}$$

Similar expressions are obtained for the states $Y_{2,3,4}$. Figure 2.3 shows the estimation error E_{Total} on Y_1^* considering ω_s deviation in (2.7) and (2.12). The results show that the TSSE achieves 99 % accurate for $\omega_s = \omega \pm (2\pi \times 0.6)$ when only (2.12) is considered, corresponding to a $E_{TSSE} < 1\,\%$. This accuracy justifies the suitability of the PLL to estimate ω_s as an input for the TSSE. Figure 2.3 also reveals that the main source of error, caused by the deviation in ω_s, is the correction performed at (2.7), which results in an error $E_{(P_g\,,\,Mg)}$ up to $\pm\,4\,\%$ for a 1 Hz deviation. Nevertheless, the overall estimation can reach an accuracy of 99.7 % as long as $\omega_s = \omega \pm (2\pi \times 0.1)$, which is a wide margin given that the typical error requirement for f estimation is $\pm$ 0.01 Hz [17].

Figure 2.3

Errors in the TSSE estimations due to ω_s deviation



2.2.3. Delayed Signal Cancellation Filter.

The proposed algorithm employs a PLL with a DSC filter stage. This type of filter performs the subtraction of the actual signal and its out-of-phase signal, i.e.,

$$x_{DSC}(t) = \frac{1}{2}\left[x(t) - x(t - \frac{T}{n})\right], \tag{2.13}$$

to achieve zero gain at frequencies $f_n = (n/T)(2k \pm 0.5)$ Hz for $k = 0, \pm 1, \pm 2, ...$, where n is referred as the delay factor and $T = 1/f$ denotes the fundamental period of the grid [103]. In practice, a cascade configuration of DSC is commonly used since a single filter will block specific harmonics [104]. The transfer function of an infinite cascade configuration of DSC filters is

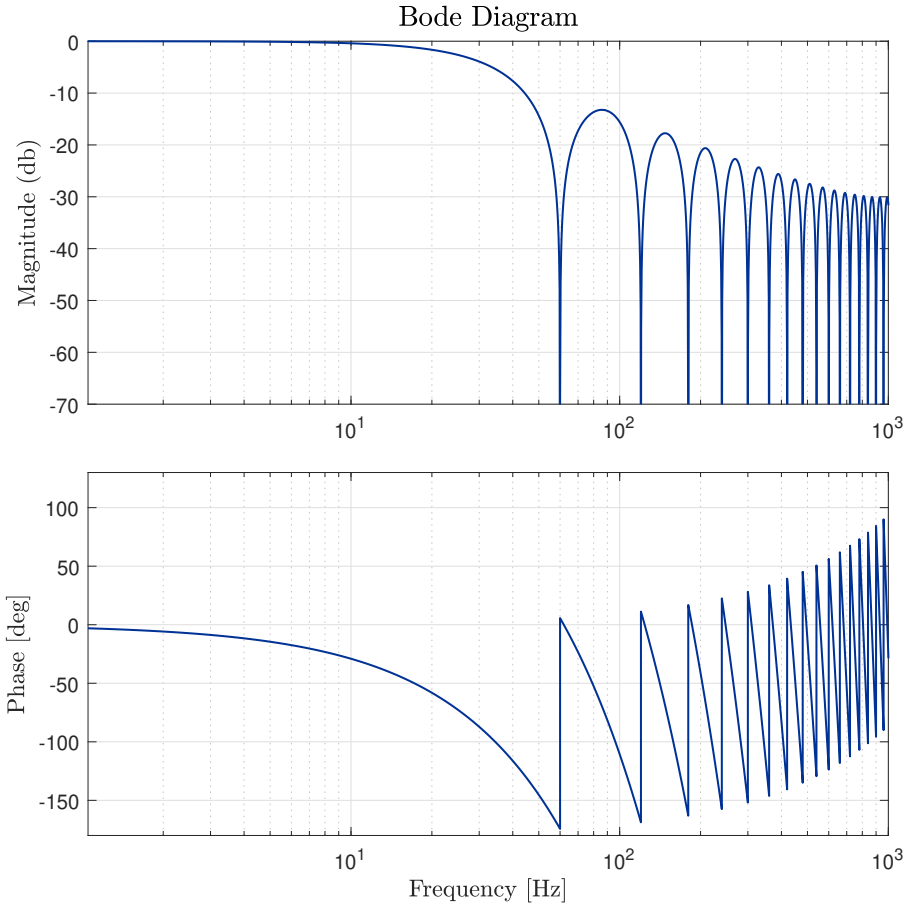
$$CDSC(s) = \frac{1}{2}\prod_{n=1}^{\infty}\left[x(t) - x(t - \frac{T}{n})\right]. \tag{2.14}$$

In this study, it is assumed that the harmonic pattern is unknown. Therefore, a cascade configuration with $n = 2, 4, 8, 16, 32$ is selected [103]. The Bode plot of the configuration is presented in Fig. 2.4.

Notably, an infinite cascade configuration of DSC filters is equivalent to a MAF filter, as demonstrated in [103]. Additionally, the synchronization of a grid-following inverter is performed with the cosine and sine functions of the positive and negative arguments, $\theta^+ = \omega t + \varphi^+$ and $\theta^- = \omega t + \varphi^-$, rather than with ω estimation. This is a salient feature of the proposed algorithm, as the estimation of these functions is conducted by the TSSE, avoiding using a second PLL for θ^- estimation [43, 92].

Figure 2.4

Bode diagram of a cascade DSC filter configuration with $n = 2,4,8,16,32$



2.2.4. Synchronous Reference Frame - PLL.

A traditional SRF-PLL is used to estimate the system frequency ω_s [105]. In this case, only the quadrature voltage v_q is calculated since the sequence components are estimated by the TSSE (see Fig. 2.1). Additionally, there is no need to separate the positive and negative sequences since v_q is filtered using the cascade DSC filter.

2.3. Performance evaluation

This section presents the test scenarios, a description of the experimental set-up, and the analysis of the obtained results.

2.3.1. Test Scenarios.

Six different scenarios of voltage sags subject to three different harmonic contents are considered for the performance evaluation. Table 2.1 presents the studied voltage sags scenarios, which can be separated into two types. Type I is focused on amplitude variations of the positive and negative sequences, whereas Type II presents voltage sags with changes in frequency and phase [14]. Scenario V_s-3 represents a voltage recovery defined by a ramp amplitude; Table 2.1 specifies the initial and final values of V^+ and V^-.

Table 2.1

Voltage sag test scenarios

Parameter	Scenarios Type I			Scenarios Type II		
	V_s-1	V_s-2	V_s-3	V_s-4	V_s-5	V_s-6
V^+ V_{pu}	0.3	0.4	0.4 - 0.9	0.7	0.7	0.7
V^- V_{pu}	0	0.4	0.1 - 0.21	0.2	0.2	0.2
f Hz	60	60	60	60	55	55
ϕ^+ rad	0	0	0	$\pi/12$	0	$\pi/12$
ϕ^- rad	0	0	$-\pi$	0	0	0
t s	0.3-0.6	0.9-1.2	1.5-1.8	2.1-2.4	2.7-3.0	3.3-3.6

Table 2.2 shows the voltage distortions applied to the voltage sags. Each case is defined based on the voltage distortion limits described in Table 1 of the IEEE Std 519 [15], and the technical literature [106–108]. The aim is to evaluate the performance of the algorithms under different types and levels of harmonic content.

Table 2.2

Harmonic distortion

Case	Harmonic distortion %						THD %
	3^{rd}	5^{th}	7^{th}	9^{th}	11^{th}	13^{th}	
0	0	0	0	0	0	0	0.00
1	2	5	4	0	3	0	7.35
2	0	5	5	0	5	5	10
3	0	10	5	0	5	5	13.23

2.3.2. Tests.

Open-loop and closed-loop tests are conducted to evaluate the performance of the DSC-TSSE. An open-loop test compares various synchronization algorithms with the DSC-TSSE. In the closed-loop test, the algorithm's behavior during inverter's current and power injection into the system is evaluated.

Open-loop test. In this case, an AC programmable source Chroma 61511 is used to generate the voltage profiles, the measurements are performed with a system based on LV 25-P LEM voltage sensors, and the synchronization algorithms are implemented in a dSPACE R&D Controller Board - DS1104. The performance of the synchronization algorithms is analyzed based on the requirements outlined in the IEEE-1547 and IEC/IEEE 60255-118-1 standards [16, 109], using the following criteria:

- Settling time (t_s): Desired t_s is set at 33.3 ms for voltage amplitudes and 100 ms for frequency. Additionally, the band error of t_s for voltage and frequency estimations are set at 2 % of V_{nom} and 0.1 Hz, respectively.

- Steady-state error (*SSE*): *SSE* should be less than 1 % of V_{nom} and 0.01 Hz for voltage amplitudes and frequency, respectively.

- Overshoot (*OS*): Limits for voltage and frequency overshoots are set at 5 % of V_{nom} and 1 % of f_{nom} (60 Hz), respectively.

The proposed algorithm is compared with a Double Synchronous Reference Frame PLL (DSRF-PLL) and an Adaptive Butterworth-Extended Kalman Filter (AB-EKF) based on the results provided in [86, 100]; These two algorithms adequately deal with harmonics by including a cascade DSC filter and an adaptive Butterworth prefiltering stage, respectively [49, 103]. Table 2.3 shows the parameters used for each algorithm, which are calculated following the design guidelines [43], [86], [91], and [110].

Table 2.3

Tuning parameters of the algorithms.

DSRF-PLL + CDSC [43, 91]	AB-EFK [110]	DSC-TSSE [86]
$k_p^+ = 100$	$Q = 0.2$	$k_p^+ = 100$
$k_i^+ = 2500$	$R = 0.01$	$k_i^+ = 2500$
$k_p^- = 500$	$P = 0.01$	$\triangle t_{TSSE} = 0.1$ ms
$k_i^- = 2500$	$\varepsilon = 1{\times}10^{-17}$	

Note. sample period and dSPACE execution time are 100 μs.

The DSRF-PLL comprises two independent PLLs to accurately estimate the arguments of the positive and negative sequences, $\theta^+ = \omega t + \varphi^+$ and $\theta^- = \omega t + \varphi^-$ [99]. The positive sequence PLL uses the traditional $dq0$ transform, while a transformation with clockwise rotation of the dq axes is required for the negative sequence. Additionally, the negative sequence PLL is activated

only when $V^- \geq 0.05V_{nom}$ to avoid errors in θ^- estimation. Hence, k_p^- is five times k_p^+ to compensate for the initial estimation time of the negative PLL. This issue does not arise for the DSC-TSSE or the AB-EKF, as the cosine and sine functions of θ^+ and θ^- are included in their formulation.

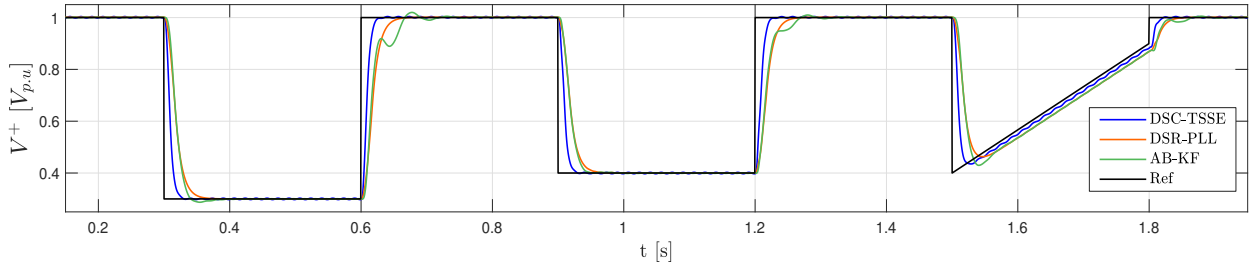
Figures 2.5 and 2.6 show the experimental results for the voltage sags described in Table 2.1, assuming non-distorted voltages (i.e., Case 0 of harmonic distortion content, THD = 0 %). Figures 2.7 and 2.8 show the experimental results for the voltage sags described in Table 2.1, assuming Case 3 of harmonic content, THD = 13.23 %.

Table 2.4 compares the results of the open-loop test. The results that meet the threshold, according to the specified criteria described in this subsection, are highlighted in green. In contrast, those not meeting the criteria are highlighted in orange. Figures and tables of the open-loop test for the harmonic distortion content cases 1 and 2 are presented in Appendix 1.

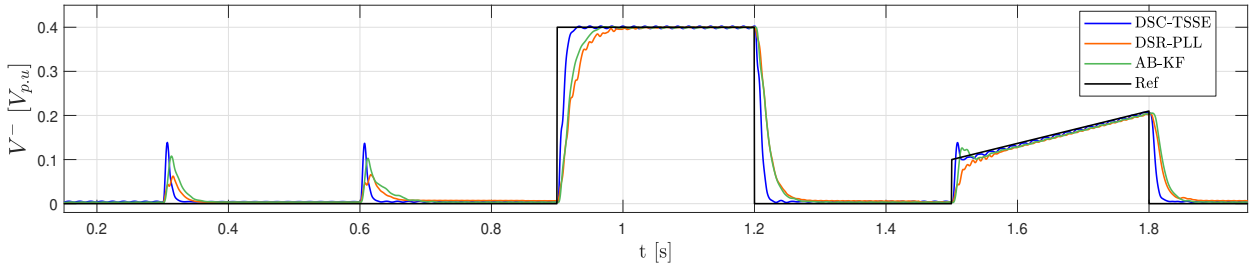
The first conclusion from Table 2.4 is that the introduction of harmonic distortion does not significantly affect the algorithms' performance. Only a slight deterioration for the estimations with THD = 13.23 % is observed. According to IEEE Std 519, a THD limit of 8 % is permitted for PCC voltages below 1 kV [15]. In this context, performing current injection based on the fundamental component of the voltage contributes to mitigating the harmonic content of the injected current and may also reduce the voltage distortion at the PCC. Consequently, the analysis of the results focuses on the performance of the algorithms in estimating each parameter, starting with the amplitudes of the sequence components.

Figure 2.5

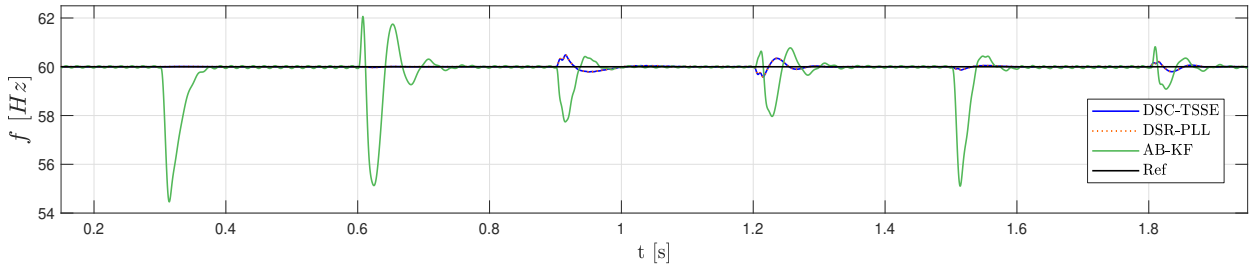
Open-loop test results corresponding to voltage sags scenarios Type I with THD = 0% a) V^+, b) V^-, c) $\omega/2\pi$, and d) θ^+



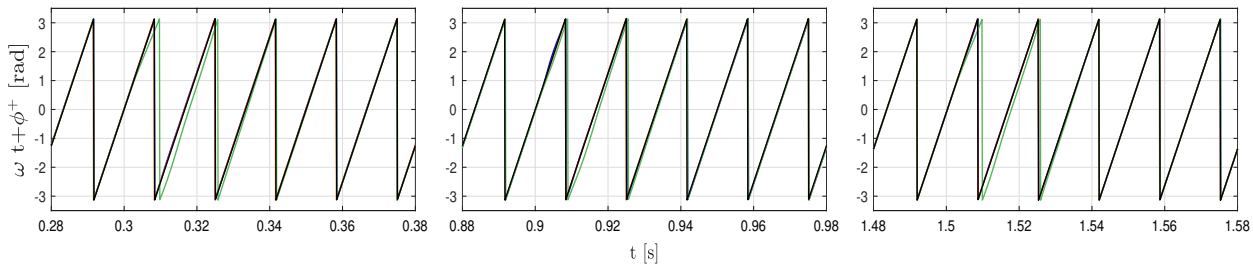
(a)



(b)



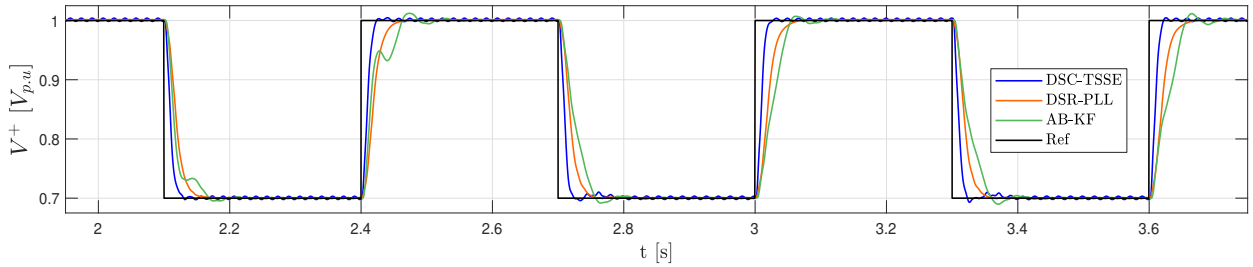
(c)



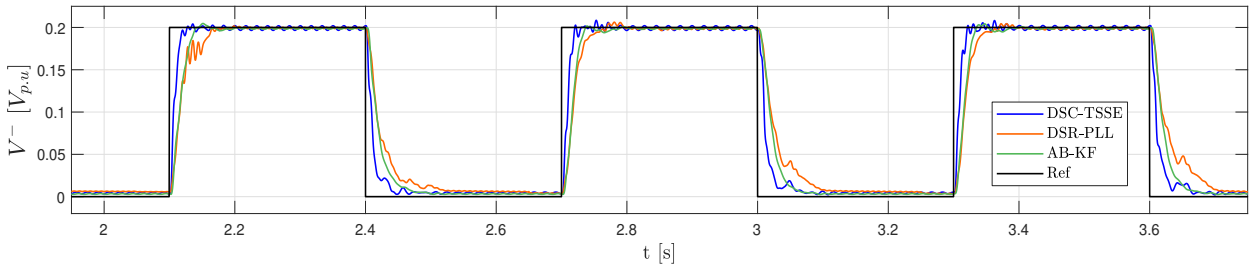
(d)

Figure 2.6

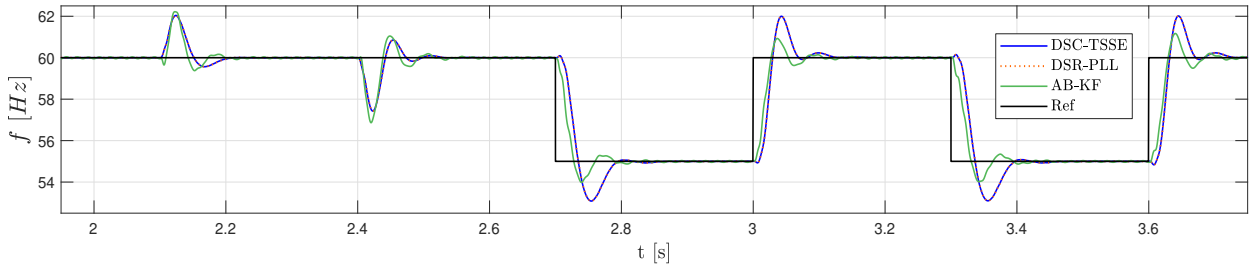
Open-loop test results corresponding to voltage sags scenarios Type II with THD = 0% a) V^+, b) V^-, c) $\omega/2\pi$, and d) θ^+



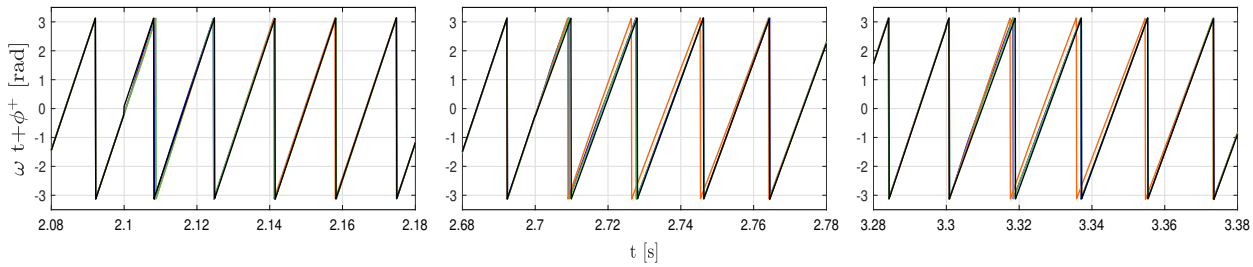
(a)



(b)



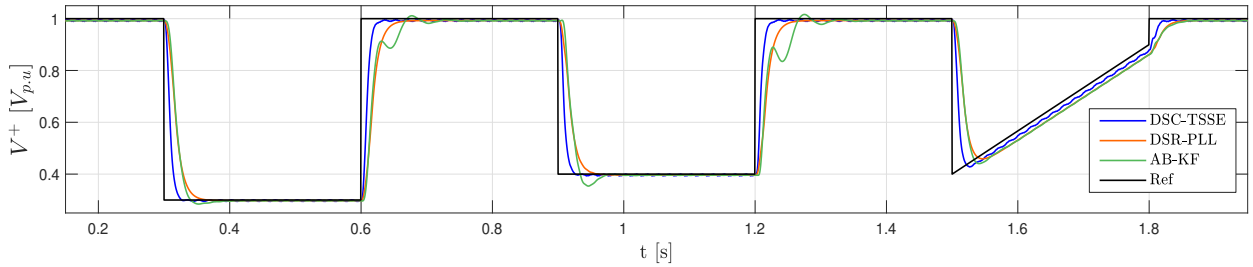
(c)



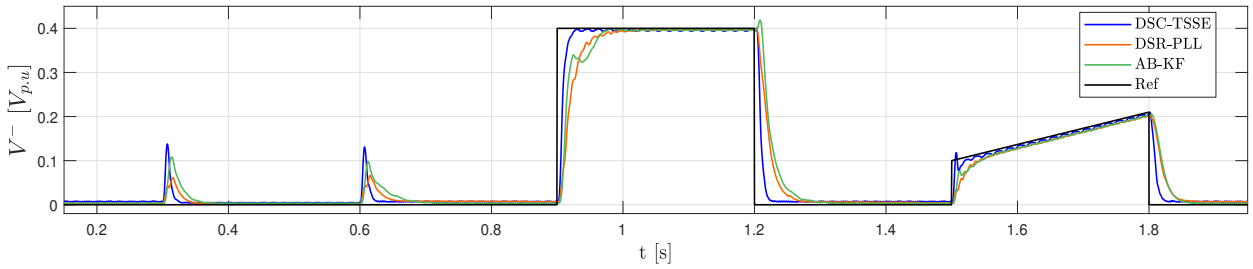
(d)

Figure 2.7

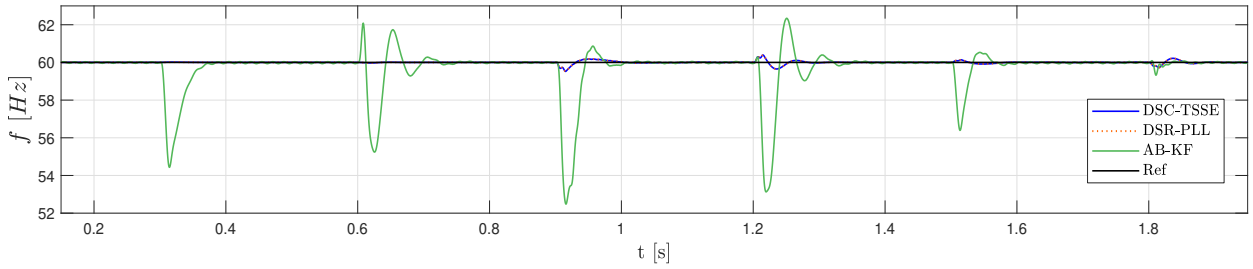
Open-loop test results corresponding to voltage sags scenarios Type I with THD = 13.23% a) V^+, b) V^-, c) $\omega/2\pi$, and d) θ^+



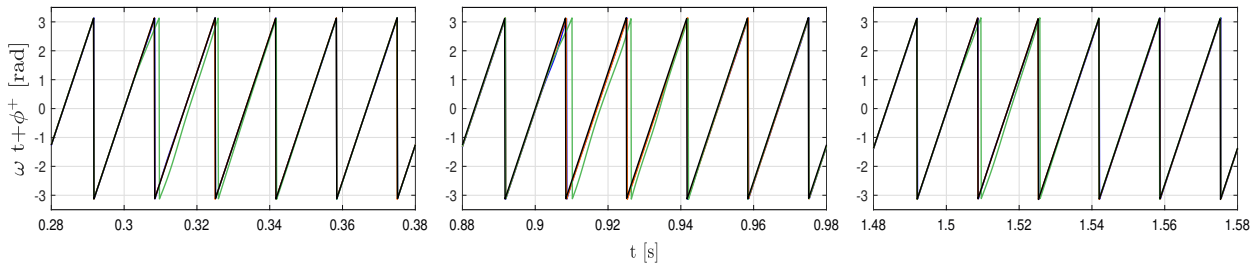
(a)



(b)



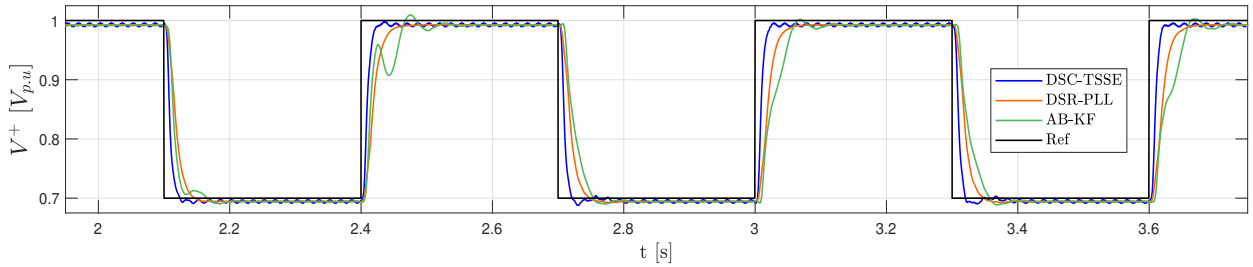
(c)



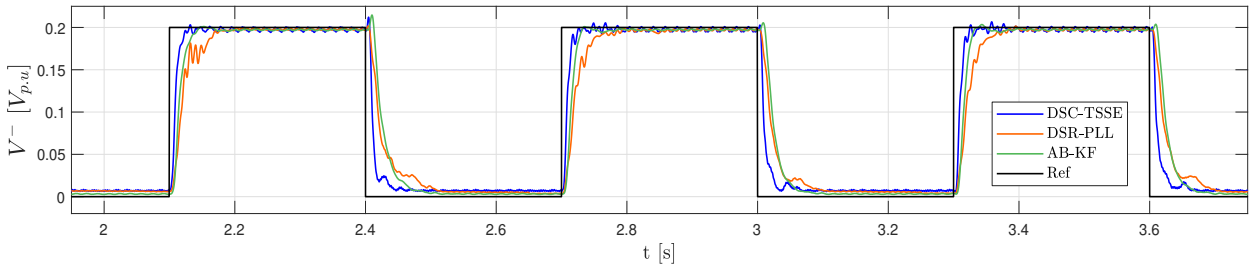
(d)

Figure 2.8

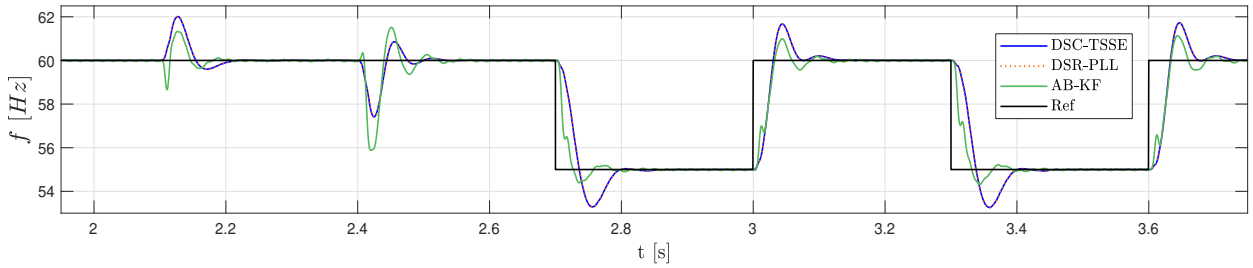
Open-loop test results corresponding to voltage sags scenarios Type II with THD = 13.23 % a) V^+, b) V^-, c) $\omega/2\pi$, and d) θ^+



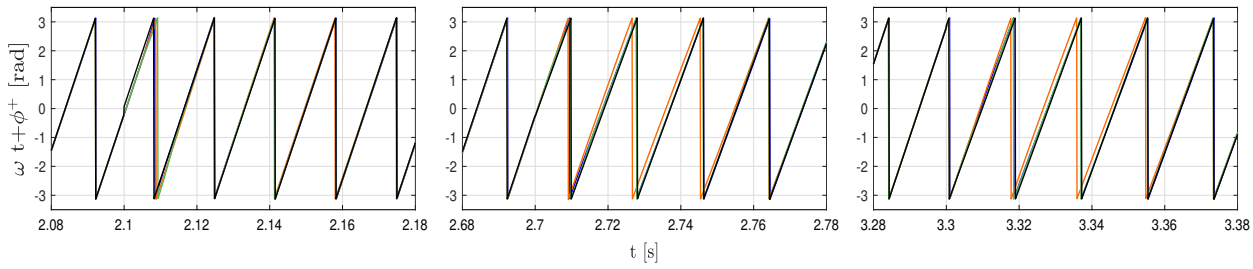
(a)



(b)



(c)



(d)

Table 2.4

Open-loop experimental results.

Algorithm		AB-EKF			DSRF-PLL			DSC-TSSE			AB-EKF			DSRF-PLL			DSC-TSSE		
Criteria		t_s ms	SSE $\times10^{-3}$	OS	t_s ms	SSE $\times10^{-3}$	OS	t_s ms	SSE $\times10^{-3}$	OS	t_s ms	SSE $\times10^{-3}$	OS	t_s ms	SSE $\times10^{-3}$	OS	t_s ms	SSE $\times10^{-3}$	OS
Scenario		THD = 0 %									THD = 13.23 %								
V_s-1	V^+	35.40	1.05	0.01	45.70	0.17	0.00	21.50	1.56	0.00	36.00	3.57	0.01	43.80	2.49	0.00	21.60	5.21	0.00
	V^-	38.60	3.18	0.11	30.40	2.95	0.06	17.40	2.59	0.14	39.60	3.63	0.11	29.30	2.05	0.06	16.40	5.14	0.14
	f	66.50	40.30	5.54	0.00	2.00	0.00	0.00	2.00	0.00	69.00	64.20	5.57	0.00	1.80	0.01	0.00	1.80	0.01
V_s-2	V^+	36.70	0.61	0.01	48.10	0.46	0.00	21.50	1.41	0.01	60.30	4.49	0.05	42.40	3.56	0.00	20.50	6.59	0.00
	V^-	47.70	1.25	0.00	66.10	0.58	0.00	19.50	1.32	0.00	63.40	4.73	0.00	61.50	3.99	0.04	19.90	6.46	0.00
	f	87.80	38.5	2.26	79.20	16.2	0.50	79.20	16.2	0.50	102.0	58.60	7.52	78.20	16.40	0.48	78.20	16.40	0.48
V_s-3	V^+	-	28.40	0.03	-	28.50	0.03	18.80	17.91	0.01	-	36.99	0.03	-	36.99	0.03	-	24.78	0.02
	V^-	15.40	5.95	0.02	29.50	7.63	0.01	11.20	4.95	0.02	36.40	6.88	0.02	33.3	9.36	0.02	12.60	7.01	0.02
	f	87.40	41.10	4.90	16.80	14.80	0.11	16.80	14.80	0.11	83.5	58.20	3.60	17.40	16.00	0.28	17.40	16.00	0.28
V_s-4	V^+	54.90	0.75	0.00	36.90	0.77	0.00	19.50	1.90	0.00	26.10	6.42	0.01	33.90	5.64	0.00	17.50	8.31	0.00
	V^-	29.30	1.51	0.00	51.70	1.31	0.09	15.37	1.99	0.00	28.30	3.74	0.00	56.80	3.17	0.06	18.10	5.82	0.00
	f	94.70	58.10	2.21	99.10	16.60	2.01	99.10	16.60	2.01	90.50	55.30	1.30	99.30	13.50	1.99	99.30	13.50	1.99
V_s-5	V^+	49.40	0.98	0.01	37.20	0.77	0.01	16.80	2.09	0.00	45.40	6.66	0.01	35.20	5.65	0.01	17.40	8.33	0.01
	V^-	27.70	1.51	0.00	34.40	2.09	0.01	17.90	2.02	0.01	24.70	3.72	0.00	46.10	3.79	0.05	15.20	5.19	0.02
	f	112.2	46.50	1.02	91.6	5.70	1.72	91.6	5.70	1.72	82.2	43.60	0.61	92.70	4.60	1.71	92.70	4.60	1.71
V_s-6	V^+	51.40	0.98	0.01	37.10	0.86	0.01	17.80	1.99	0.01	48.40	6.78	0.01	35.20	5.82	0.01	17.40	8.51	0.01
	V^-	26.60	1.81	0.00	34.80	1.91	0.01	18.40	2.18	0.01	25.70	3.72	0.00	45.20	3.68	0.04	16.20	5.19	0.02
	f	105.4	42.20	0.98	92.70	5.70	1.73	92.70	5.70	1.73	88.4	42.20	0.68	92.70	4.90	1.74	92.70	4.90	1.74

* Units for *SSE* and *OS* are V for the voltage amplitudes and Hz for the estimated frequency.

** A green highlight indicates that the estimation meets the comparison criteria, whereas an orange highlight indicates otherwise.

Table 2.4 highlights that the DSC-TSSE provides a desirable performance by estimating V^+ and V^- in less than two fundamental cycles of the signals. The DSRF-PLL and the AB-EKF generally exceed the established t_s criteria, requiring 2-3 cycles to estimate the positive- and negative-sequence amplitudes. The estimation error of the DSC-TSSE is below 2 % of V_{nom} (1.79 %) for the ramp voltage scenario under non-distorted conditions, and it also exhibits the lowest SSE for V^+ and V^- estimation during the ramp scenarios with harmonic contents. It is worth mentioning that the *OS* of the amplitude estimations is not significant for any of the algorithms.

A cascade DSC-PLL is used for frequency estimation for the DSRF-PLL and the DSC-TSSE. Since the DSC deals with the double-frequency oscillations caused by the negative sequen-

ce, the results are the same for both algorithms, as shown in Table 2.4. The DSC-PLL's frequency estimation meets the t_s and SSE criteria, yet it exceeds the overshoot requirement during voltage sag scenarios involving phase and frequency jumps. On the other hand, the frequency estimation of the AB-EKF shows higher values of t_s and SSE, often exceeding the performance criteria. This algorithm also shows high values of *OS* for type I voltage sags.

It should be noted that accurate estimation of θ^+ for the DSRF-PLL takes almost two cycles during frequency jumps, as can be seen in Figs. 1.7(d) and 1.9(d). Similarly, θ^+ estimation for the AB-EKF takes around the same time for type I voltage sag scenarios, as can be seen in Figs. 1.6(d) and 1.8(d). On the other hand, the proposed algorithm performs a faster estimation of θ^+ and θ^-, since the TSSE offers more freedom regarding ω_s [86] as stated in Section 2.2.2.

Computational burden is often expressed based on the computation time and memory resources needed to solve a problem. On a dSPACE R&D Controller Board (DS1104), both the DSC-TSSE and DSRF-PLL algorithms have an execution time of 53 μs, while the AB-EKF filter takes 63 μs. Furthermore, DSC-TSSE and DSRF-PLL have comparable memory usage, around 420 kB, indicating similar computational demands. However, the DSC-TSSE exhibits superior performance by estimating the voltage parameters faster and more accurately.

Table 2.5

Computational burden of the analized algorithms

Parameter	AB-EKF	DSRF-PLL	DSC-TSSE
Execution time μs	63	53	53
Memory usage kB	406	421	416

Closed-loop test. The closed-loop test emulates the behaviour of a DPGS with LVRT capabilities. The DSC-TSSE is tested under voltage sags type I considering the harmonic content cases described in Table 2.2. However, the parameters of the sags are changed as described in Table 2.6 to guarantee the safety of the equipment ($f = 60$ Hz).

Table 2.6

Voltage sags scenarios for the closed-loop test

Parameter	Scenarios Type I		
	V_s-1*	V_s-2*	V_s-3*
V^+ V_{pu}	0.5	0.7	0.5 - 0.8
V^- V_{pu}	0	0.2	0.13 - 0.21
f Hz	60	60	60
ϕ^+ rad	0	π/6	π/12
ϕ^- rad	0	0	π/12
t s	0.5-0.8	1.8-2.1	3.1-3.4

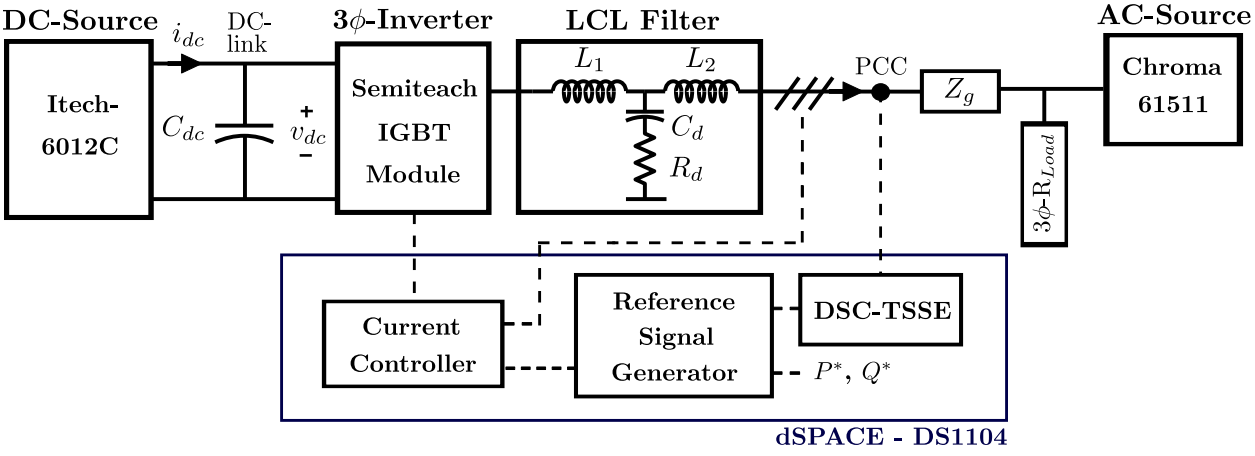
Figure 2.9 shows the hardware-based experimental set-up, and Fig. 2.10 provides a schematic representation of its main components. The set-up consists of a DC programmable source ITECH-6012C, a DC-link capacitor C_{dc}, a Semiteach IGBT module connected as a three-phase full-bridge inverter configuration, an LCL grid connection filter, a $Z_g = R_g + jL_g\omega$ representing the line impedance, a 3ϕ-resistive load, and an AC programmable source Chroma 61511 to emulate disturbances of the grid voltage (V_g).

Figure 2.9

Closed-loop experimental set-up

Figure 2.10

Schematic of the closed-loop experimental set-up



The PCC voltages and the injected currents to the grid are measured using systems based on

sensors LV 25-P and LA 25-NP from LEM, respectively. Parameters of the experimental set-up for the closed-loop test are given in Table 2.7, where P_g is the active power injected to the grid during normal operation and f_s is the switching frequency. The control algorithms are implemented in a dSPACE R&D Controller Board - DS1104.

Table 2.7

Parameters of the closed-loop test

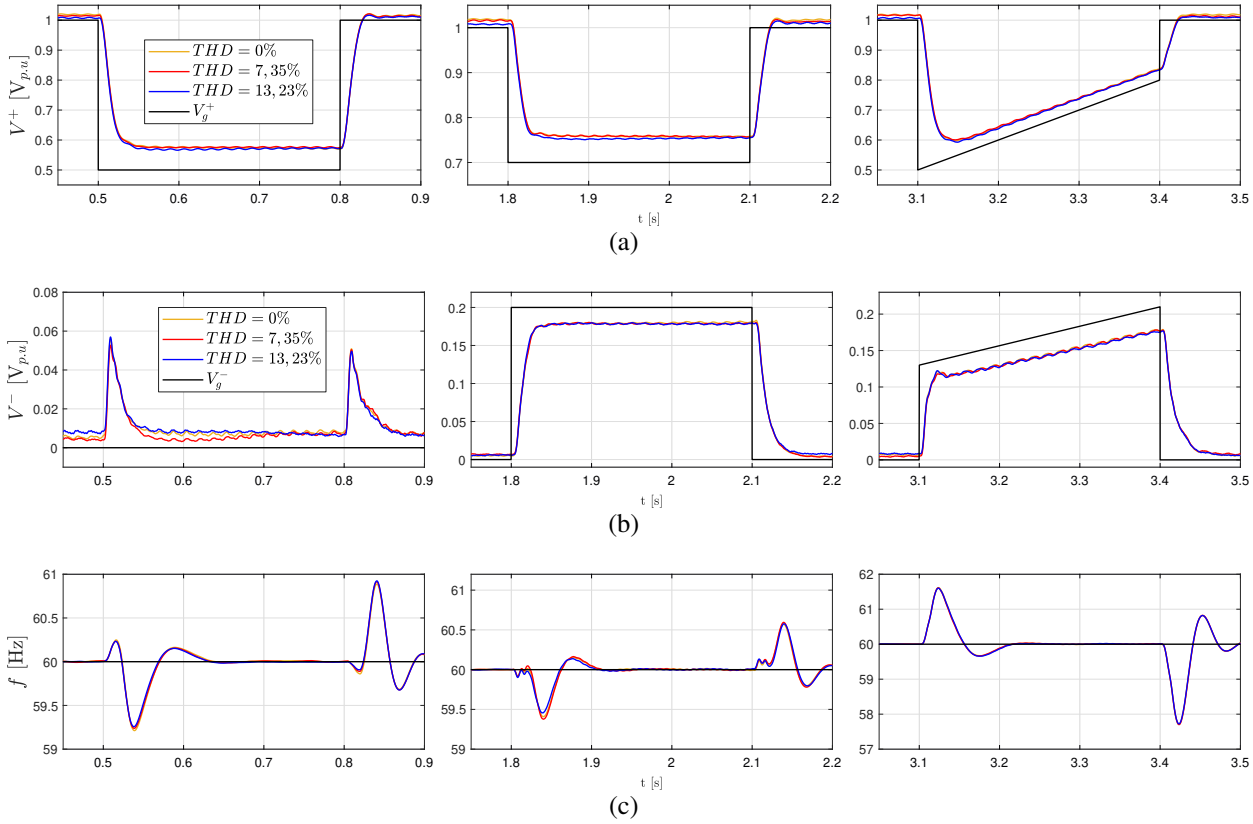
Parameter	Value	Parameter	Value
V_{nom}	110 Vrms	L_1	5 mH
f	60 Hz	L_2	5 mH
$I_{nom-peak}$	6.428 A_{peak}	C_d	4.7 μF
V_{dc}	450 V	R_d	5 Ω
C_{dc}	1.1 mF	P_g	1000 W
L_g	2.5 mH	S_{nom}	1.5 kVA
R_g	0.53 [Ω]	3ϕ- R_{Load}	12 Ω
f_s	10 kHz		

The inverter is synchronized using the DSC-TSSE. The reference currents are generated using the LVRT strategy proposed in [63]. This strategy is selected since the voltage support is optimized as long as Z_g's is known. Additionally, the strategy limits the injected current, increases V^+ and reduces V^-. A PIR controller with a pulse width modulation (PWM) technique generates the switching pulses for the inverter. Figures 2.11 and 2.12 present the closed-loop test results considering the different harmonic contents cases.

Figure 2.11 shows that the estimated voltage parameters are almost identical regardless of the harmonic contents. Figures 2.11(a) and 2.11(b) highlight how the voltage positive sequence increases while the negative sequence decreases. Additionally, the injected currents are limited to the safe operational ranges during the sags with $i_{abc} < 1.1 I_{nom}$ for steady-state conditions.

Figure 2.11

Closed-loop results for voltage sags scenarios type I a) V^+ at the PCC, b) V^- at the PCC, c) $\omega_s/2\pi$



The results also show that the frequency estimation presents major differences between the open-loop and the closed-loop test. Although the frequency SSE is less than 0.02 Hz for all the closed-loop cases, its OS is greater than the expected for voltage sags Type I according to the open-loop test, e.g., reaching more than 1 Hz for the ramp scenario (Figs. 1.6(c) and 1.12(c)). Moreover, the frequency estimation settling time is greater than 100 ms for the closed-loop tests (see Fig. 1.12(c)). This behavior does not affect the DSC-TSSE performance for the grid-following synchronization, yet it could have a negative impact on grid-forming operation during transient

conditions. For example, the IEEE Std 2800 establishes that the current settling time should be less than four fundamental cycles of the signal for all inverter-based resources except for the Type-III wind units [17].

Figure 2.12

Closed-loop results for voltage sags scenarios type I a) injected currents i_{abc} for voltage THD=0 %, b) injected currents i_{abc} for voltage THD=7.35 %, c) injected currents i_{abc} for voltage THD=13.23 %

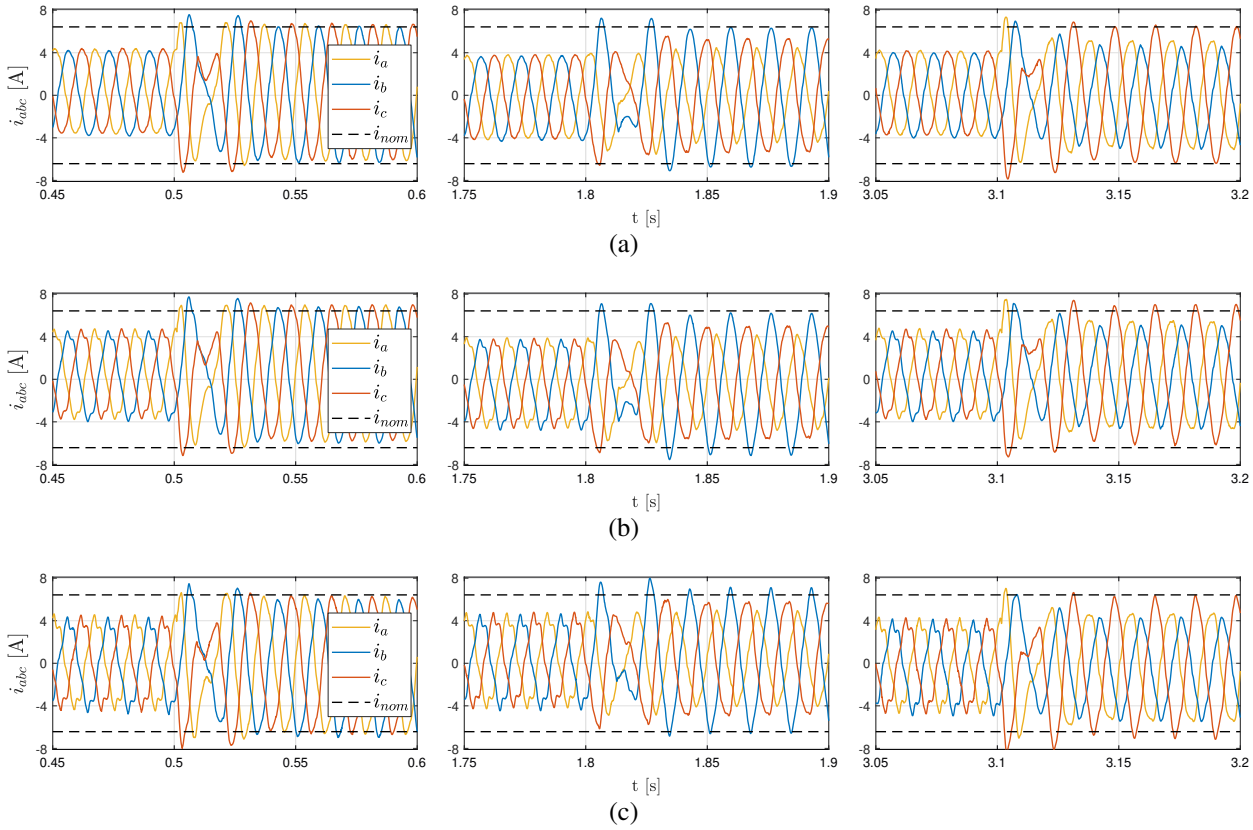


Table 2.8 presents the positive and negative sequences' amplitudes, their respective t_s, the THD of the PCC voltages, and the Total Ratio Distortion (TRD) of the injected currents for the closed-loop test [16]. The results show that V^+ and V^- estimations reach a steady state in less

than 2.5 and 2 cycles, respectively. These values are approximately one cycle greater than the ones obtained during the open-loop test for V^+ estimation. For the ramp voltage case, the settling time is defined at the moment that voltage difference remains constant compared to the reference, which is 0.04 V_{pu} above for V^+ and 0.03 V_{pu} below for V^-.

Table 2.8

Results of the closed-loop test

Harmonic distortion	THD=0 %			THD=7.35 %			THD=13.23 %		
Voltage sag	V_s-1*	V_s-2*	V_s-3*	V_s-1*	V_s-2*	V_s-3*	V_s-1*	V_s-2*	V_s-3*
V^+ [V_{pu}]	0.58	0.76	0.04†	0.57	0.76	0.04†	0.57	0.75	0.04†
t_{s-V^+} [ms]	39.3	23.8	47.6	38.4	24.9	43.1	36.1	24.2	42.2
V^- [V_{pu}]	0.01	0.18	0.03†	0.01	0.18	0.03†	0.01	0.18	0.03†
t_{s-V^-} [ms]	27.1	39.1	25.9	27.4	28.6	25.1	28.2	28.6	25.1
V_a THD %	3.00	1.76	1.96	5.53	4.61	3.69	9.13	7.25	5.59
V_b THD %	3.02	1.89	1.76	5.41	6.83	4.76	9.17	12.2	7.25
V_c THD %	3.15	2.21	2.29	5.21	4.13	6.81	9.31	6.33	12.5
i_a TRD %	3.56	3.68	6.27	4.37	4.14	6.01	5.47	4.68	7.57
i_b TRD %	3.56	3.68	4.53	4.37	4.24	4.26	5.47	6.04	6.60
i_c TRD %	3.56	6.55	3.40	4.75	6.53	4.00	5.47	7.72	5.88

† In the case of the ramp voltage scenario V_s-3*, the value correspond to $\Delta V^+ = V^+ - V_g^+$ and $\Delta V^- = V_g^- - V^-$.
Note. the reference to estimate t_s is changed to the steady state value of the corresponding sequence voltage during the sag.

The results also indicate acceptable performance of the inverter during harmonic distortion cases 0 and 1. According to IEEE Std 519, i.e., a maximum voltage THD of 8 % and a maximum current TRD of 5 % are acceptable for power systems with voltage levels below 1 kV [15]. During voltage sags V*s*-1 and V*s*-2 of Table 2.6, only one current TRD is beyond the 5 %. Nevertheless, that value is acceptable considering that the IEEE Std 519 increases the TRD maximum value by 1.5 for very short periods (<3 s) [15]. Thus, the test results validate the DSC-TSSE's robust

performance for sequence voltage estimation and demonstrate its suitability for grid-following converters under grid abnormal conditions.

2.4. Conclusions

This thesis introduces a synchronisation algorithm for the estimation of voltages parameters during the host grid abnormal conditions. The proposed DSC-TSSE is evaluated using an open-loop test for performance assessment and a closed-loop test to analyze its operational behavior. The study cases include voltage sags, voltage unbalances, frequency jumps and voltage distortion. Moreover, the proposed algorithm was rigorously compared with the DSRF-PLL and the AB-EKF algorithms.

The DSC-TSSE exhibits the shortest settling time among the studied algorithms, which is critical for the operation of the inverter during grid disturbances such as voltage sags. Moreover, even during abnormal conditions, the DSC-TSSE estimates voltage parameters in compliance with the IEEE-1547 standard. In addition, the proposed algorithm does not need an extra Park transformation to accurately estimate the negative sequence argument. These findings underscore the efficacy and efficiency of the DSC-TSSE in enhancing the voltage sequence estimation during grid abnormal conditions for grid-following converters. Future work will focus on improving the settling time and overshoot of the frequency estimation to develop an algorithm suitable for grid-forming converters.

3. Reference Current Generator

A new generation of grid codes (GC) requires that inverter-based resources inject positive- and negative-sequence currents during asymmetrical voltage sags. These prioritize the injection of reactive current. Once this requirement is fulfilled, GCs also demand to maximize the active power provision through the positive sequence. This chapter introduces a current strategy (CS) designed to meet GC requirements and the system constraints, while mitigating instantaneous active power oscillations and the resulting DC-bus voltage fluctuations. Furthermore, the proposed strategy exhibits an increased active power supply while voltage support is provided to the grid. The performance of the proposed strategy is validated through transmission system simulations and experimental tests in a scaled-down model.

This chapter is organized as follows. Section 3.1 introduces the State-of-the-art. Section 3.2 details the proposed current injection strategy. Section 3.3 presents the simulation and experimental results and their analysis. The main conclusions are stated in Section 3.4.

3.1. State-of-the-art

A new generation of GCs prioritizes the injection of reactive currents, requiring a supply proportional to the voltage change of the respective sequence, as defined by $\Delta I^{\pm} = K\Delta V^{\pm}\frac{I_{nom}}{V_{nom}}$ [31, 32]; where V_{nom} and I_{nom} are the nominal voltage and current of the DPGS, the superscripts + and - refers to the positive- and negative-sequence components, and K represents the curve's slope, usually between $2 \leq K \leq 6$. Once the reactive current requirement is satisfied, the remaining capacity of the inverter must be used to inject active power through the positive sequence component.

Furthermore, active power injection via negative-sequence current is not considered [31, 32].

In addition to current injection requirements, three main constraints must be considered for the inverter safety: 1) maximum phase current limit, 2) maximum phase voltage limit, and 3) maximum DC-link voltage limit [13]. Concerning power quality, reduction of harmonic content in the injected currents and mitigation of power oscillations are also desirable [34–38]. Oscillations in the instantaneous active power, from now on referred as active power oscillations, are of particular concern due to their direct influence on the DC-bus voltage stability [34, 111].

Over the past decade, several asymmetrical current strategies have been developed, as detailed in [7, 112]. This thesis also presents a review of flexible current strategies in [54]. Most of the studied strategies focus on improving the power converter performance without considering GC requirements. Some strategies prioritize minimizing active power oscillations while neglecting the requirements for the reactive negative-sequence current injection [10, 12, 34, 60]. Other approaches do not consistently prioritize reactive current injection over positive-sequence active current I_p^+ [61–63, 71]. Furthermore, most of the strategies do not comply new generation GCs since injection of active current through the negative-sequence I_p^- is considered [26, 113–115].

A current strategy S_I, based on the GGC is presented on [116]. In S_I, factors k_1 and k_2 are proposed to regulate active and reactive power injection via the positive and negative sequence components. However, S_I does not fully comply with the GGC, as it increases reactive current injection through the negative sequence. Furthermore, like other strategies designed according to new generation GCs, it fails to prioritize reactive current injection over I_p^+ injection [116, 117].

Current scaling is typically performed uniformly across all current components. However,

as explained by Azizi et al. in strategy S_{II}, current injection should prioritize reactive current variations ΔI_q^+ and ΔI_q^- over active current injection [73]. This prioritization aims to minimize deviations from the original reactive current demands. Azizi et al. have also demonstrated that the injection of I_p^+ is possible even when the current limit is already reached by the reactive current supply [73]. Nevertheless, S_{II} does not consider the power generation scenario which may result in over-currents if the injection of I_p^+ cannot be achieved.

This thesis presents a current strategy that prioritizes reactive current injection and maximizes I_p^+ to comply with the new generation GC requirements [31]. Moreover, the strategy mitigates active power oscillations while fulfilling the GC and system constraints [54]. Furthermore, the proposed strategy demonstrates that enhanced active power delivery is achievable without significantly impacting voltage support.

3.2. Proposed Strategy

The steps of the proposed algorithms are introduced below. The selected limits and values are based on the German Grid Code (GGC) VDE-AR-N 4120 [31]. Nevertheless, the proposed strategy is adaptable to analogous GC through appropriate adjustments of the corresponding factors and parameters [32].

3.2.1. Voltage sag detection.

The GGC stipulates that a voltage sag is detected when the minimum line-to-line voltage falls below 90 % of its nominal value, i.e. $V_{p-p}^{min} < 0.9\,V_{p-p}^{nom}$. The lowest line voltage amplitude can be found as

$$V_{min}^2 = 3\left(V^{+2} + V^{-2} + 2V^+V^- cos(\varphi^+ - \varphi^- + \varphi_{abc})\right), \tag{3.1}$$

where φ_{abc} is the value among $\{\pi/3, -\pi, -\pi/3\}$ that minimizes the cosine term, thus minimizing the resulting voltage amplitude.

3.2.2. Current definition according to GGC.

The current injection required by the GGC is defined as

$$\begin{aligned} I_q^+ &= I_{q0}^+ + \Delta I_q^+ \\ I_q^- &= I_{q0}^- + \Delta I_q^-, \end{aligned} \tag{3.2}$$

where I_q^+ and I_q^- are the required positive and negative sequences reactive currents, I_{q0}^+ and I_{q0}^- are the pre-fault positive- and negative-sequence reactive currents, and ΔI_q^+ and ΔI_q^- are the additional current injection required by the GGC. These are determined as

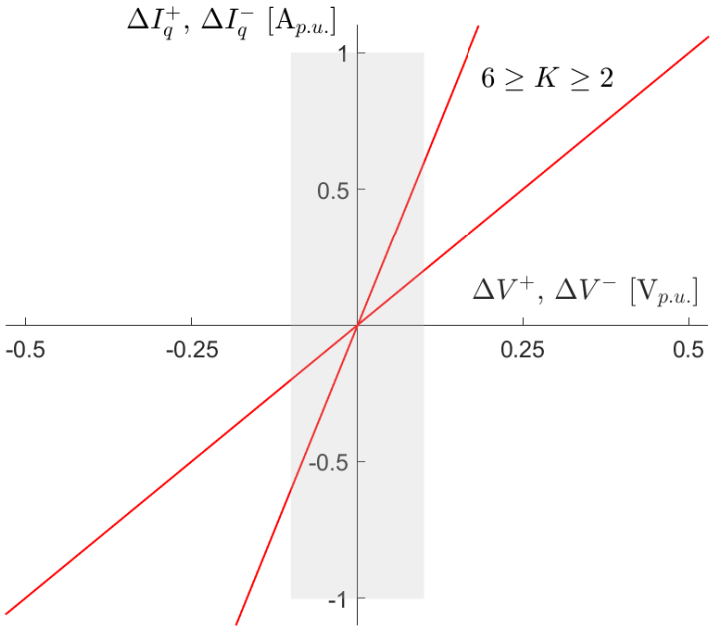
$$\begin{aligned} \Delta I_q^+ &= K \cdot \Delta V^+ \frac{I_{nom}}{V_{nom}} \\ \Delta I_q^- &= K \cdot \Delta V^- \frac{I_{nom}}{V_{nom}}. \end{aligned} \tag{3.3}$$

K is a constant defined in appendix B.6 of the GGC, whose value is among $2 \leq K \leq 6$ as shown in Fig 3.1 [31].

This analysis incorporates two key assumptions. First, since a transmission system is considered, it will be assumed that I_{q0}^- can be neglected. Secondly, the GGC uses load notation in which current is positive entering the element (e.g., source, load, filter, etc.), thus $\Delta I_q^+ \leq 0$ and $\Delta I_q^- \geq 0$. However, the proposed strategy adopts a source notation, in which current entering the grid is defined as positive. Consequently, the signs of both equations in (3.3) are reversed. Additio-

Figure 3.1

GGC K factor for additional LVRT reactive current injection



nally, the proposed algorithm is implemented in the $\alpha\beta 0$ frame. Therefore, it must be considered that Clark's transformation reverses the sign of the imaginary component of the negative sequence [102]. Consequently, the sign of ΔI_q^- is inverted again to inject a reactive current that mitigates V^-. Thus, the GGC's required currents are defined as

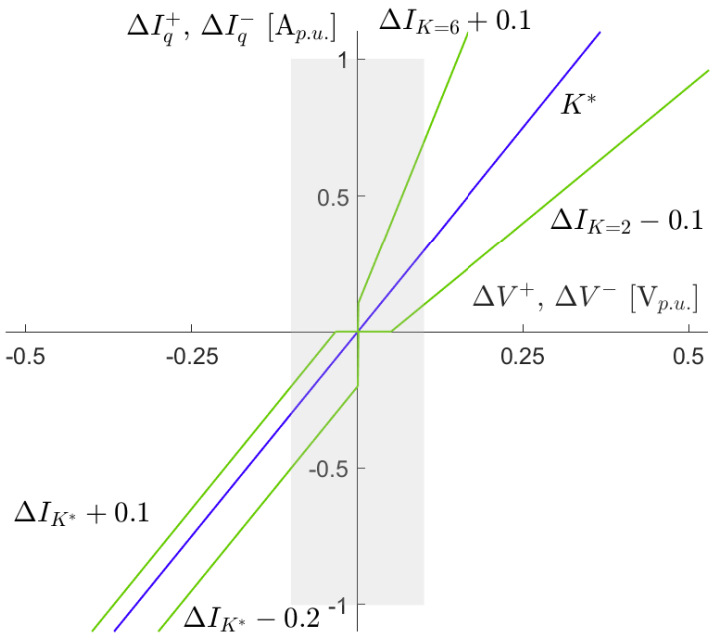
$$\begin{aligned} \Delta I_q^+ &= -K \cdot \Delta V^+ \frac{I_{nom}}{V_{nom}} \\ \Delta I_q^- &= K \cdot \Delta V^- \frac{I_{nom}}{V_{nom}} \end{aligned}. \tag{3.4}$$

3.2.3. Defining negative sequence reactive current injection to reduce active power oscillations.

Figure 3.2 illustrates the tolerance ranges for additional current injection ΔI_q^+ and ΔI_q^-, as specified in Annex C.1 of the GGC [31]. This annex defines a tolerance range for ΔI_q^- in terms of K with $2 \leq K \leq 6$. The proposed algorithm exploits this tolerance range to reduce the active power oscillations $\tilde{p}$.

Figure 3.2

GGC tolerance range for the additional LVRT reactive current injection



According to the instantaneous power theory, the reference currents can be defined in the $\alpha\beta$ frame as [63, 118]

$$\begin{aligned} i_\alpha &= I_p^+\left(\frac{v_\alpha^+}{V^+}\right)+I_p^-\left(\frac{v_\alpha^-}{V^-}\right)+I_q^+\left(\frac{v_\beta^+}{V^+}\right)+I_q^-\left(\frac{v_\beta^-}{V^-}\right) \\ i_\beta &= I_p^+\left(\frac{v_\beta^+}{V^+}\right)+I_p^-\left(\frac{v_\beta^-}{V^-}\right)-I_q^+\left(\frac{v_\alpha^+}{V^+}\right)-I_q^-\left(\frac{v_\alpha^-}{V^-}\right) \end{aligned}, \tag{3.5}$$

where

$$\begin{aligned} v_\alpha &= v_\alpha^+ + v_\alpha^- = V^+cos(\omega t+\varphi^+)+V^-cos(\omega t+\varphi^-) \\ v_\beta &= v_\beta^+ + v_\beta^- = V^+sin(\omega t+\varphi^+)-V^-sin(\omega t+\varphi^-) \end{aligned}', \tag{3.6}$$

and

$$\begin{aligned} I_p^+ &= \frac{2}{3}\frac{V^+P}{(V^+)^2+(V^-)^2} \;\; I_p^- = \frac{2}{3}\frac{V^-P}{(V^+)^2+(V^-)^2} \\ I_q^+ &= \frac{2}{3}\frac{V^+Q}{(V^+)^2+(V^-)^2} \;\; I_q^- = \frac{2}{3}\frac{V^-Q}{(V^+)^2+(V^-)^2} \end{aligned}. \tag{3.7}$$

In the same way, the instantaneous active and reactive powers injected to the grid, p and q, are expressed as

$$\begin{aligned} p &= P+\tilde{p} = P+\left(\frac{(I_p^+V^-+I_p^-V^+)cos(\delta)}{(V^+)^2+(V^-)^2}\right)P+\left(\frac{(I_q^+V^--I_q^-V^+)sin(\delta)}{(V^+)^2+(V^-)^2}\right)Q \\ q &= Q+\tilde{q} = Q+\left(\frac{(I_q^+V^-+I_q^-V^+)cos(\delta)}{(V^+)^2+(V^-)^2}\right)Q-\left(\frac{(I_p^+V^--I_p^-V^+)sin(\delta)}{(V^+)^2+(V^-)^2}\right)P \end{aligned}, \tag{3.8}$$

respectively, with $\delta = 2\omega t+\varphi^++\varphi^-$ [54]. From (3.8), it can be noticed that active power oscillations $\tilde{p}$ are composed of two terms, one depending on the active power injection P, and the other depending on the reactive power injection Q. To cancel $\tilde{p}$ due to Q, the negative sequence reactive current must be defined as

$$I_q^{-*} = \frac{V^-}{V^+} I_q^+. \tag{3.9}$$

Nevertheless, the following conditions must be established to accomplish the GGC requirements presented in Fig 3.1. If I_q^{-*} is lower than the minimum I_q^- defined in the GGC ($K = 2$), then

$$I_q^{-*} = \frac{2}{K} \Delta I_q^-. \tag{3.10}$$

On the other hand, if I_q^{-*} is greater than maximum tolerance of I_q^- ($K = 6$), then

$$I_q^{-*} = \frac{6}{K} \Delta I_q^-. \tag{3.11}$$

It should be noted that these limits do not account for the 10 % safety margin established by the GGC. Instead, this margin is treated as a tolerance between the reference and the injected values of I_q^{-*}.

3.2.4. Current limitation.

The amplitude of the injected currents in the *abc* frame is defined by

$$I_{abc} = \sqrt{(I_p^{+2} + I_q^{+2}) + (I_p^{-2} + I_q^{-2}) + 2Acos(x) + 2Bsin(x)}, \tag{3.12}$$

where $A = I_p^+ I_p^- - I_q^+ I_q^-$, $B = I_q^+ I_p^- + I_p^+ I_q^-$ and $x = \varphi^+ - \varphi^- + \varphi_{abc}^*$ with $\varphi_{abc}^* = \{0, -2\pi/3, 2\pi/3\}$ [54]. Since I_p^- injection is not considered in the GGC, the amplitude of the currents can be rewritten as

$$I_{abc} = \sqrt{I_q^{+2} + I_q^{-2} + I_p^{+2} - 2I_q^+ I_q^- cos(x) + 2I_p^+ I_q^- sin(x)}. \tag{3.13}$$

Analyzing (3.13), it is noticed that if the value of $sin(x)$ is negative, injecting I_p^+ may prevent exceeding the current limit [73]. Nevertheless, the current limit must be ensured for all phases. Therefore, three quadratic equations must be solved, as later explained in Section 3.2.5, to determine if I_p^+ injection is feasible. In this sense, the reactive currents definition should start by verifying if the injection of I_p^+ avoids surpassing the current limit, as proposed in [73]. However, if this is not the case, the reactive currents would need to be rescaled to comply with the current constraint, and I_p^+ must then be recalculated [73]. Therefore, the complexity and computational burden of the strategy would be increased. Furthermore, simulations were performed, obtaining that only on 1 % of the possible fault scenarios, the injection of I_p^+ will avoid over-current on all phases. For this reason, the proposed algorithm starts by calculating if the injection of I_q^+ and I_q^- surpass the current limit of the converter. Given that I_p^+ is initially set to zero, the maximum current amplitude is determined by the value of x that minimizes $cos(x)$, maximizing the expression

$$I_{max} = \sqrt{{I_q^+}^2 + {I_q^-}^2 - 2I_q^+ I_q^- cos(x)}. \tag{3.14}$$

If I_{max} exceeds I_{nom}, a current scale down is required. As defined by (3.2), only the values of $\Delta I_q^{\pm}$ can be reduced. Furthermore, the GGC establishes that the reactive current limitation is preferably achieved by uniformly scaling down the positive and negative sequence current. Therefore, the current limitation is performed by

$$\begin{aligned} {I_q^+}^* &= I_{q0}^+ + \rho \Delta I_q^+ \\ {I_q^-}^{**} &= \rho \Delta {I_q^-}^*, \end{aligned} \tag{3.15}$$

where ρ is the scalar factor defined to reduce the current injection and $\Delta {I_q^-}^* = {I_q^-}^*$. Substituting

(3.15) on (3.14) and solving it for ρ, it is obtained that

$$\begin{aligned} 0 =& \rho^2 \underbrace{\left[(\Delta I_q^+)^2 + (\Delta I_q^{-*})^2 - 2\eta \Delta I_q^+ \Delta I_q^{-*} Cos(x)\right]}_{\text{a}} \\ &+ \rho \underbrace{\left[2I_{q0}^+ \Delta I_q^+ - 2\eta I_{q0}^+ \Delta I_q^{-*} Cos(x)\right]}_{\text{b}} \\ &+ \underbrace{\left[(I_{q0}^+)^2 - (I_{nom})^2\right]}_{\text{c}}. \end{aligned} \tag{3.16}$$

Thus, ρ can be found for each phase as

$$\rho_{abc}^{max,min} = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a}. \tag{3.17}$$

Two conditions must be considered to solve (3.16), $I_{q0}^+ \geq 0$ and $I_{q0}^+ < 0$. If $I_{q0}^+ \geq 0$, then $I_q^{+*} \geq 0$ and $\eta = 1$. On the other hand, if $I_{q0}^+ < 0$ there are two possibilities, $I_q^{+*} \geq 0$ and $I_q^{+*} < 0$. In the first case, the amplitude $I_q^{+*} = I_{q0}^+ + \Delta I_q^+$ and $\eta = 1$. For the other case, $I_q^{+*} = -(I_{q0}^+ + \Delta I_q^+)$ and $\eta = -1$. In both possibilities, the value of ρ must satisfy the initial assumption ($I_q^{+*} \geq 0$ or $I_q^{+*} < 0$, respectively), to be a valid solution for the current limitation. Furthermore, ρ must be a value among $[0,1]$. Therefore, ρ is the minimum value among $\{\rho_a^{max}, \rho_b^{max}, \rho_c^{max}\}$ that fulfills these conditions.

3.2.5. Injection of I_p^+.

As previously stated, I_p^+ can be injected even when the maximum current limit is reached through the injection of I_q^+ and I_q^-. According to (3.13), I_p^+ injection is feasible as long as the term $I_p^{+2} + 2I_p^+ I_q^- sin(x)$ prevents over-currents in all the phases. The following equation must be solved to verify this condition for each phase

$$(I_p^+)^2 + \underbrace{2I_p^+ I_q^- sin(x)}_{b_2} + \underbrace{(I_{qi}^2 - I_{nom}^2)}_{c_2} = 0. \tag{3.18}$$

Where I_{qi} is obtained from (3.14) for the corresponding value of x with $i = a,b,c$. Therefore

$$I_{pi}^+ = \frac{-b_2 \pm \sqrt{b_2^2 - 4c_2}}{2}. \tag{3.19}$$

Based on equation (3.19), each phase will have a permissible range of I_{pi}^+ values, denoted as $\{I_{pi}^{+min}, I_{pi}^{+max}\}$ with $i = a,b,c$, where the current limit is not exceeded. Therefore, I_p^+ must be selected as the maximum value within the intersection of these three ranges, subject to the constraint $I_p^+ \geq 0$. Additionally, the power generation scenario and the converter losses must be considered in I_p^+ definition. Consequently, the maximum value of I_p^+ that should be injected is defined as

$$I_{pmax}^+ = \frac{2}{3} \frac{V^+(P_{gen} - P_L)}{(V^+)^2 + (V^-)^2}. \tag{3.20}$$

To ensure that the current limit is not going to be exceeded, I_{pmax}^+ must be greater or within the intersection of the I_p^+ ranges defined in this section. Otherwise, the value of I_p^+ must be set to zero.

3.2.6. DC voltage regulation.

A technical constraint of the system is the maximum DC bus voltage level $v_{dc} = V_{dc} + \tilde{v}_{dc}$. Maintaining v_{dc} as constant as possible is also desirable. Under normal operating conditions, a closed-loop control adjusts the inverter's active power injection to regulate v_{dc} [119]. However, during fault conditions, two factors must be considered. First, the current limitation could restrict

the injection of P. Secondly, without additional elements (i.e., use of batteries with a bidirectional converter), the injection of $\tilde{p}$ causes v_{dc} oscillations at twice of the system frequency [50, 53].

In this sense, v_{dc} over-voltage could be caused by an excess generated power that cannot be injected into the grid or by the oscillating component of p. Due to its simplicity and lower cost, this thesis employs a chopper resistor to consume excess power regulating v_{dc} maximum value. The limitation of this approach is that the resistor only handle excess power generation, not power deficits (i.e. super-capacitor in a bidirectional buck-boost configuration can deal with both).

Two actions are imposed to deal with v_{dc} voltage levels below its nominal value. First, I_p^+ injection is limited based on the power generation P_{gen} (3.20). Second, I_p^+ is adjusted considering the maximum losses of the inverter P_L, preventing control issues with the chopper resistor's ON/OFF states.

$$I_p^{+*} = I_p^+ + \frac{2}{3}\frac{V^+ P_L}{(V^+)^2 + (V^-)^2}. \tag{3.21}$$

It is important to note that while these two actions address v_{dc} reduction from generation deficits, they do not mitigate oscillations caused by $\tilde{p}$. Therefore, oscillations $\tilde{v}_{dc}$ below the nominal value V_{dc} persist.

3.2.7. Over-voltage.

Different studies present cases in which one of the phases reaches over-voltage during voltage support [59, 69, 114]. This over-voltage is mainly caused by substantial or complete positive-sequence current injection during asymmetrical faults. To mitigate this, the GGC mandates a minimum negative-sequence current injection during voltage sags. Suppose the GGC current injection

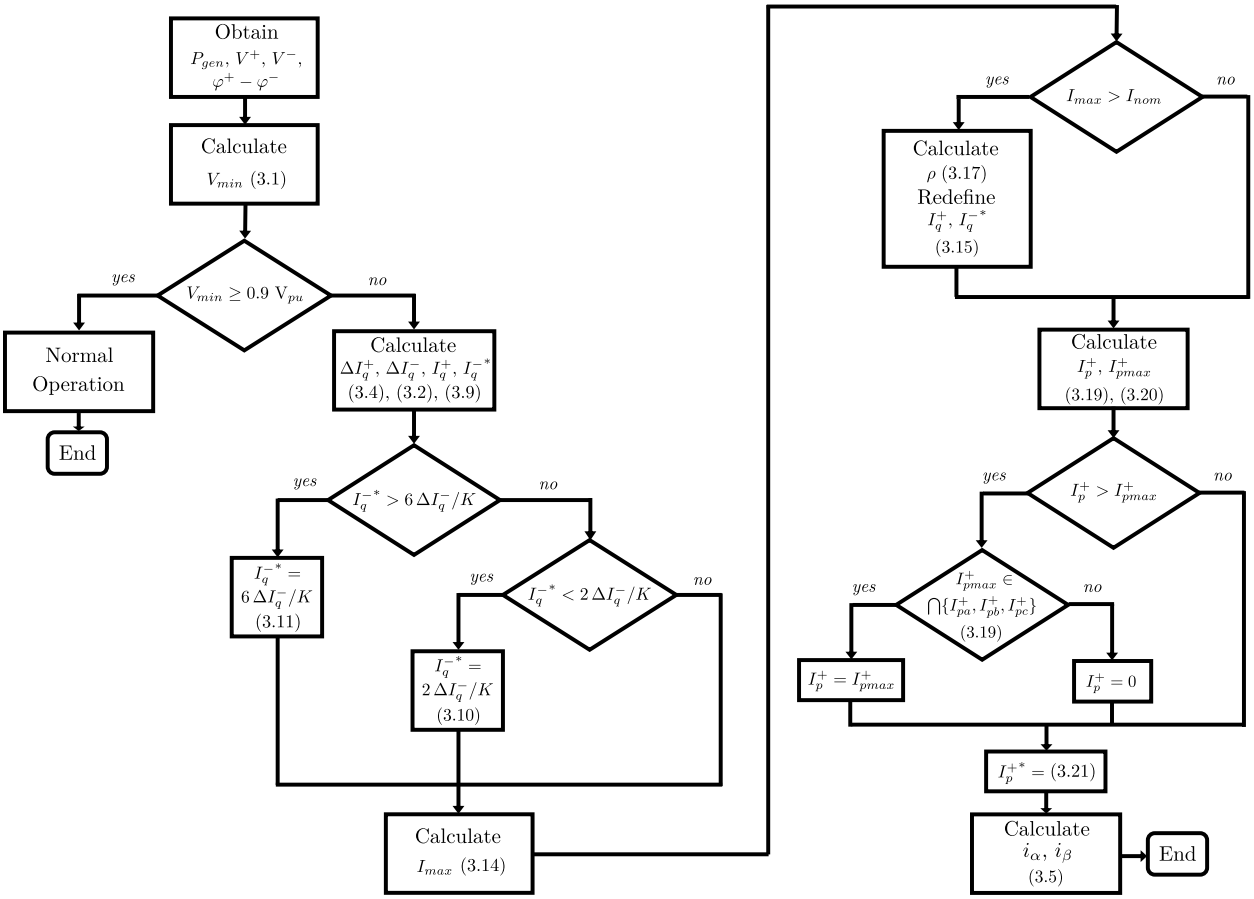
requirement is fulfilled. In that case, the conditions required for a grid-connected power inverter to present over-voltage during a voltage sag are extremely weird and so uncommon in practice.

3.2.8. Block diagram of the proposed algorithm.

The steps of the proposed algorithm are presented in Fig.3.3.

Figure 3.3

Block diagram of the proposed algorithm



3.3. Performance evaluation

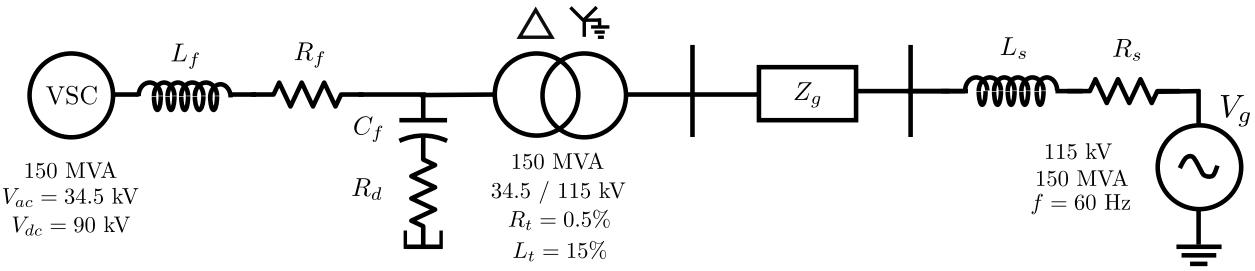
The proposed strategy, S_p, is evaluated through simulations and experimental tests. Its performance is compared with the strategies proposed in [116] and [73], referred to as S_I and S_{II}. These comparative strategies are chosen because they also adhere to the GGC requirements.

3.3.1. Simulations.

Simulations are conducted using *Matlab - Simulink* to evaluate the performance of the proposed strategy. Given that the GGC applies to high-voltage systems ranging from 60 kV to 150 kV, a 115 kV transmission system is selected for the simulations [31]. Figure 3.4 shows the single-line diagram of the system, which is composed of a voltage source converter (VSC) connected to the utility grid through an LC filter and a $\Delta - Y_n$ transformer. The grid is modeled as a line impedance $Z_g = R_g + j\omega L_g$ and a voltage source V_g.

Figure 3.4

Single-line diagram of a distributed generation system connected to a transmission system



In this thesis, the VSC model includes an ideal DC current source and a chopper resistor representing the Generation Stage, a DC-link capacitor C_{dc}, and a three-phase full-bridge inverter (see Fig. 3.5) [119]. For the control system, the inverter is synchronized using the algorithm pro-

posed in Chapter 2. During normal operation a PI control is used to regulate v_{dc}. A PR controller with a pulse-width modulation (PWM) technique is used to generate the switching pulses for the inverter [81, 82]. The signal S_{crc}, which activates the breaking chopper resistor to handle DC-bus over-voltage, is generated by a power control strategy based on a PI control that dissipates excess power that cannot be injected into the grid.

Figure 3.5

Model of the VSC

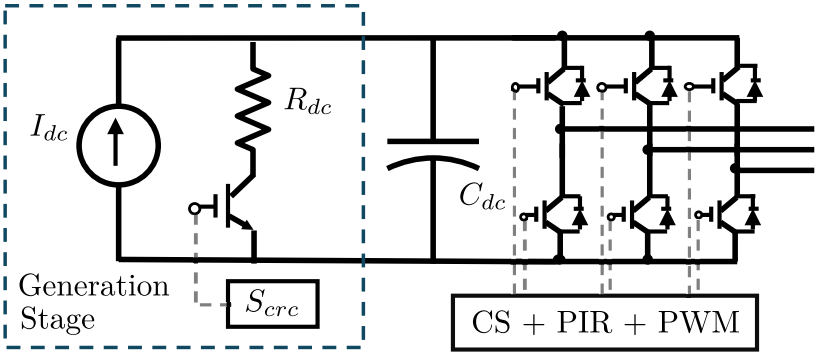


Table 3.1 shows the simulation parameters. According to these, the system has a short circuit ratio (SCR) of 6 [120]. This value is selected considering that the GGC establishes that voltage sags must not lead to instability or disconnection as long as the SCR at the PCC is greater than 6.

The strategies performance is compared under four different cases, these are shown in Table 3.2. Next, a description of each case is introduced:

Table 3.1

Parameters of the simulations

Parameter	Value	Parameter	Value
R_{dc}	18 Ω	R_g	1.5 Ω
C_{dc}	0.9 mF	L_g	32 mH
R_f	3.7 Ω	R_s	0.18 Ω
L_f	2.1 mH	L_s	7 mH
C_f	167 μF	f_s	10 kHz

Table 3.2

Simulations cases

Cases	P_{gen} MW	Q_{pf} MVAR	V_g^+ $V_{p.u}$	V_g^- $V_{p.u}$	φ_g^+ rad	φ_g^- rad	K
0	-	-	1	0	0	0	-
I	150	0	0.808	0.177	-1.3142	1.9076	2.5
II	100	0	0.7	0.2	0	0	3
III	10	30	0.7	0.4	0.2618	-0.2618	4
IV	10	-30	0.7	0.4	0.2618	-0.2618	4

a) Case 0 - This case represents the pre-fault condition of the source voltage V_g, characterized by its positive- and negative-sequence components V_g^+, V_g^-, and their corresponding phase angles φ_g^+, φ_g^-.

b) Case I - In this case, the injection of I_q^+ and I_q^- do not reach the nominal current of the inverter I_{nom}. Therefore, active power injection is possible even for current strategies that do not consider the condition established in Section 3.2.5.

c) Case II - For this case the injection of I_q^+ and I_q^- surpass I_{nom}, so power curtailment must be performed. Additionally, for this case, the condition of Section 3.2.5 is satisfied. Therefore,

the injection of I_p^+ is possible even if the reactive current injection already exceeds I_{nom}.

d) Case III - For cases III and IV, reactive power is injected into the grid before the sag. For Case III, this corresponds to a reactive power of $Q_{pf} = 30$ MVAR. Additionally, a low active power generation level is assumed to highlight the active power oscillations primarily induced by injection of Q. This type of oscillations are the ones attenuated by S_p.

e) Case IV - In this case, a $Q_{pf} = -30$ MVAR is injected before the sag. Strategies S_p and S_{II} emulate synchronous generator behavior by considering the pre-fault reactive currents. As a result, the amount of I_q^+ injected during the sag will be lower than in Case III. The reason is that ΔI_q^+ remains the same in both cases, while the pre-fault currents I_{q0}^+ differs [73].

Figures 3.6 to 3.9 present the simulation results for cases I to IV, respectively.

Figure 3.6

Simulation results for case I a) V^+, V^- and v_{dc} b) Injected active and reactive powers c) Injected currents d) Voltages at the PCC

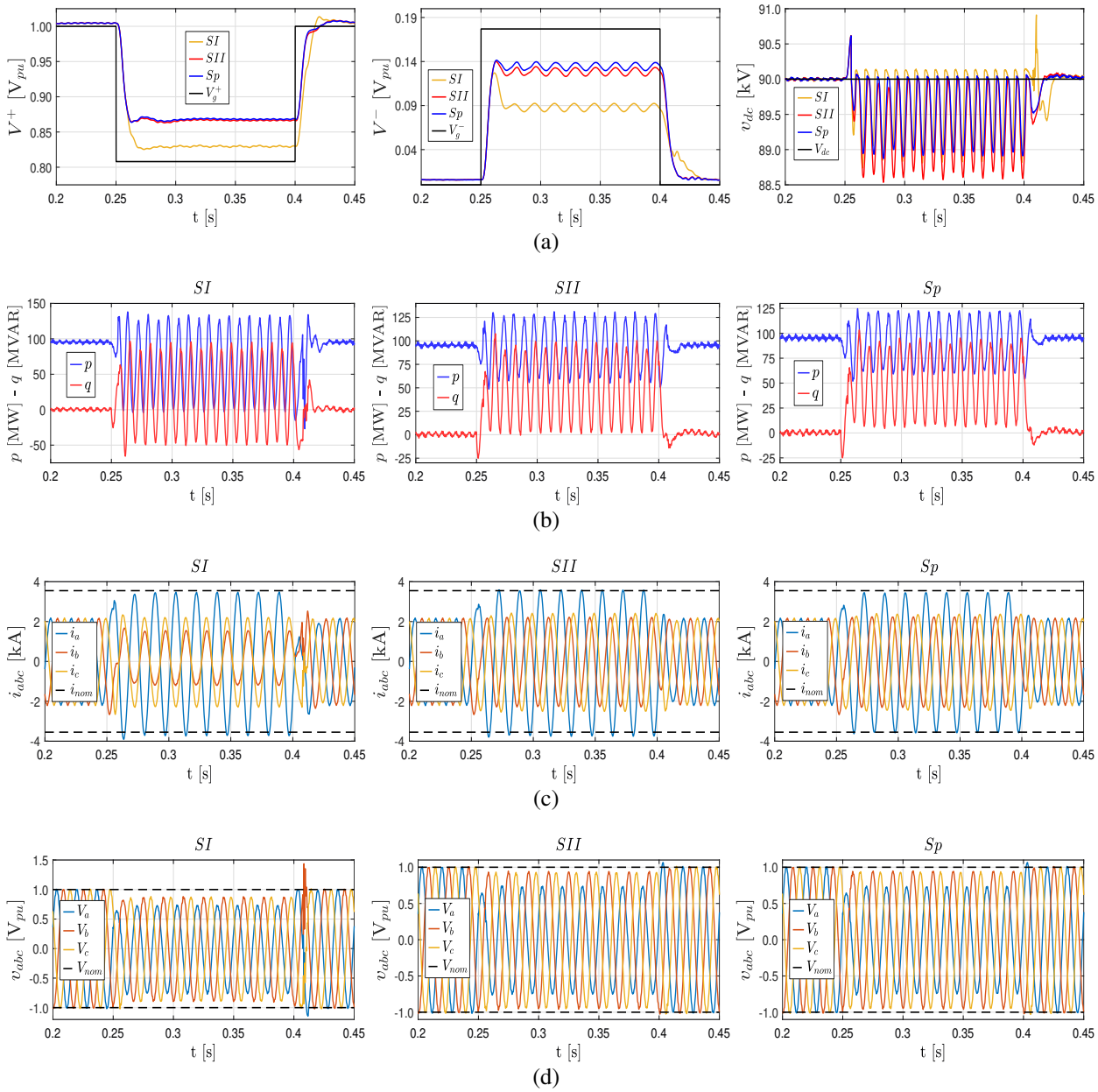


Figure 3.7

Simulation results for case II a) V^+, V^- and v_{dc} b) Injected powers p and q c) Injected currents d) Voltages at the PCC

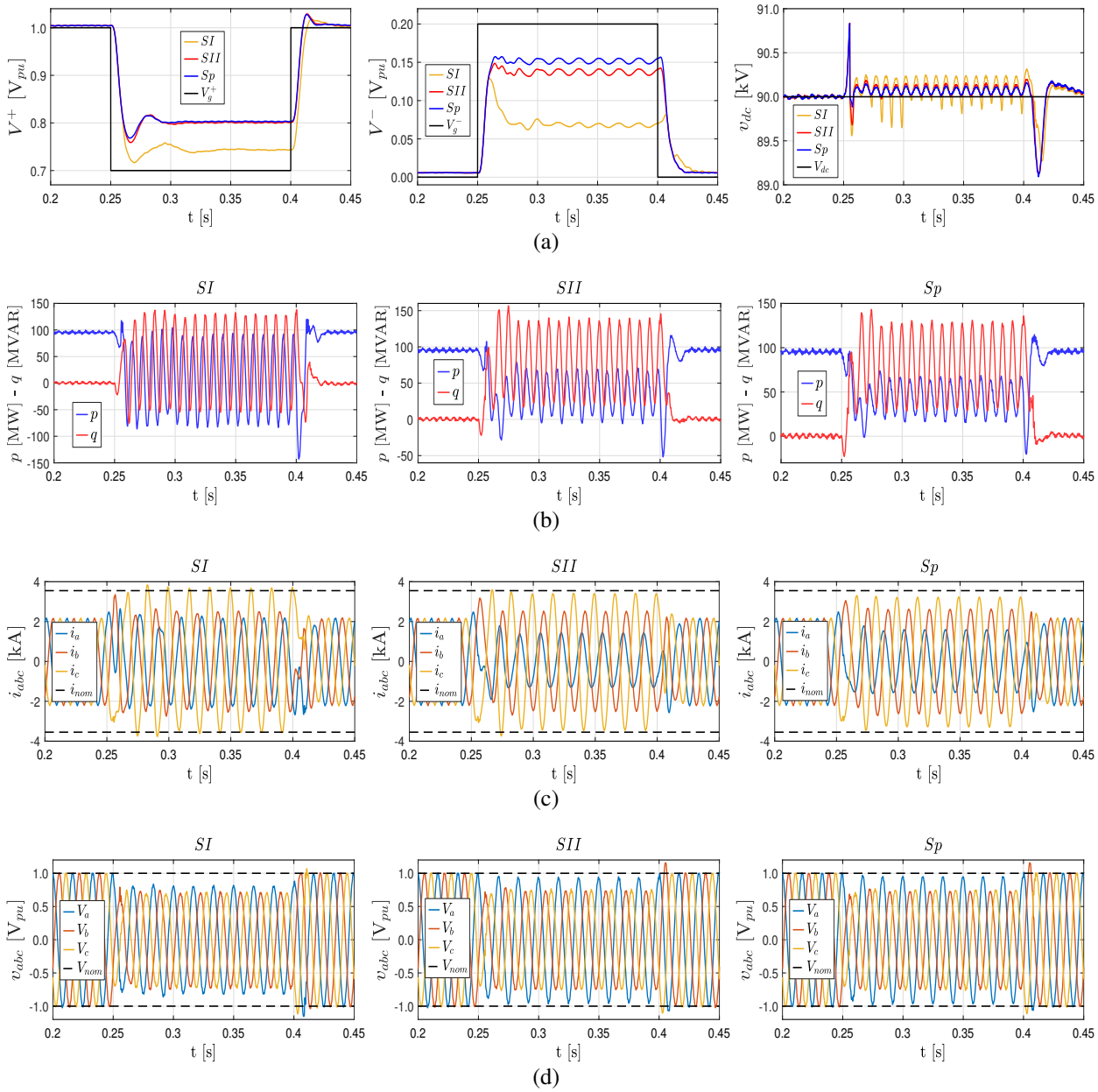


Figure 3.8

Simulation results for case III a) V^+, V^- and v_{dc} b) Injected powers p and q c) Injected currents d) Voltages at the PCC

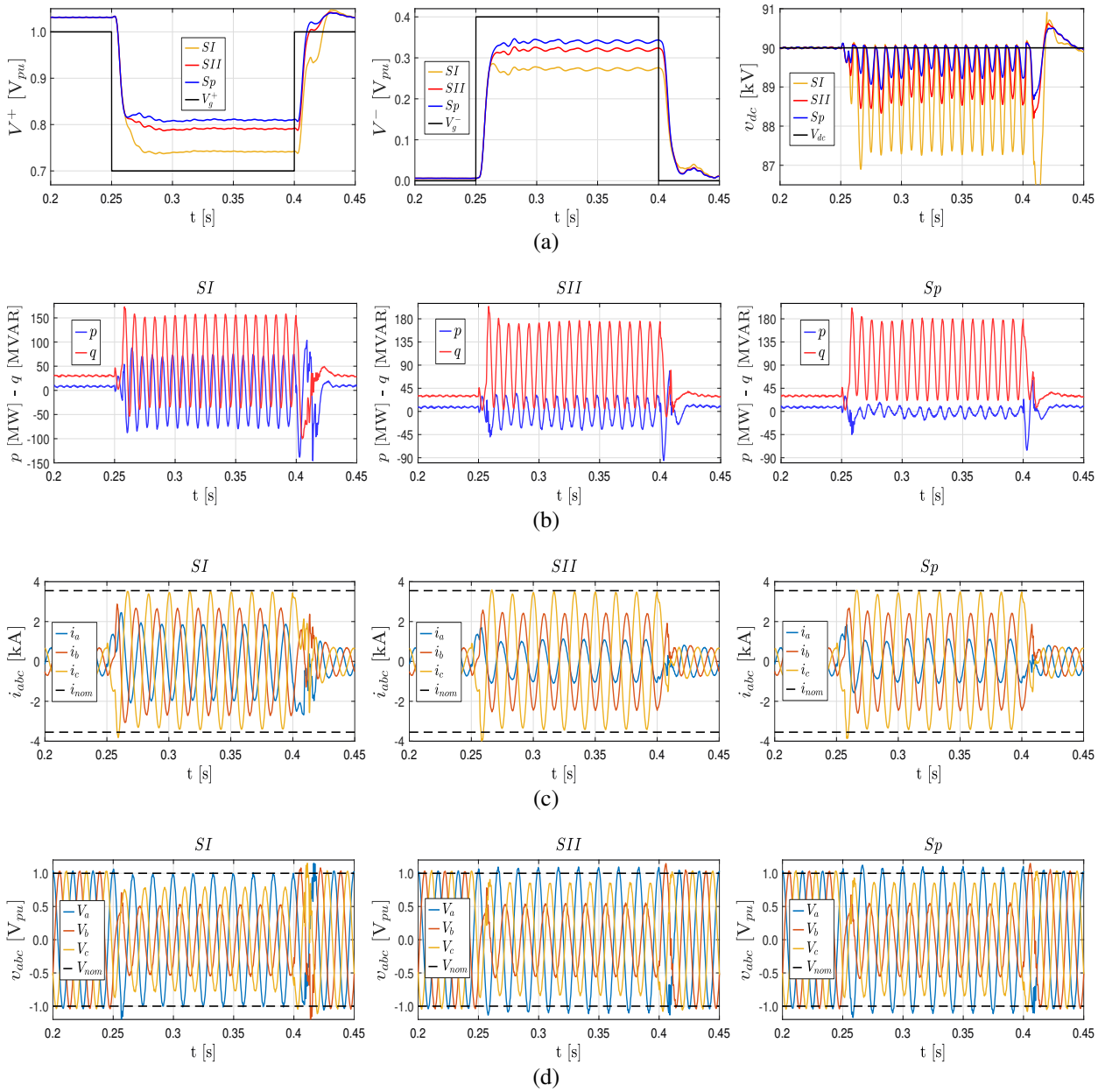


Figure 3.9

Simulation results for case IV a) V^+, V^- and v_{dc} b) Injected powers p and q c) Injected currents d) Voltages at the PCC

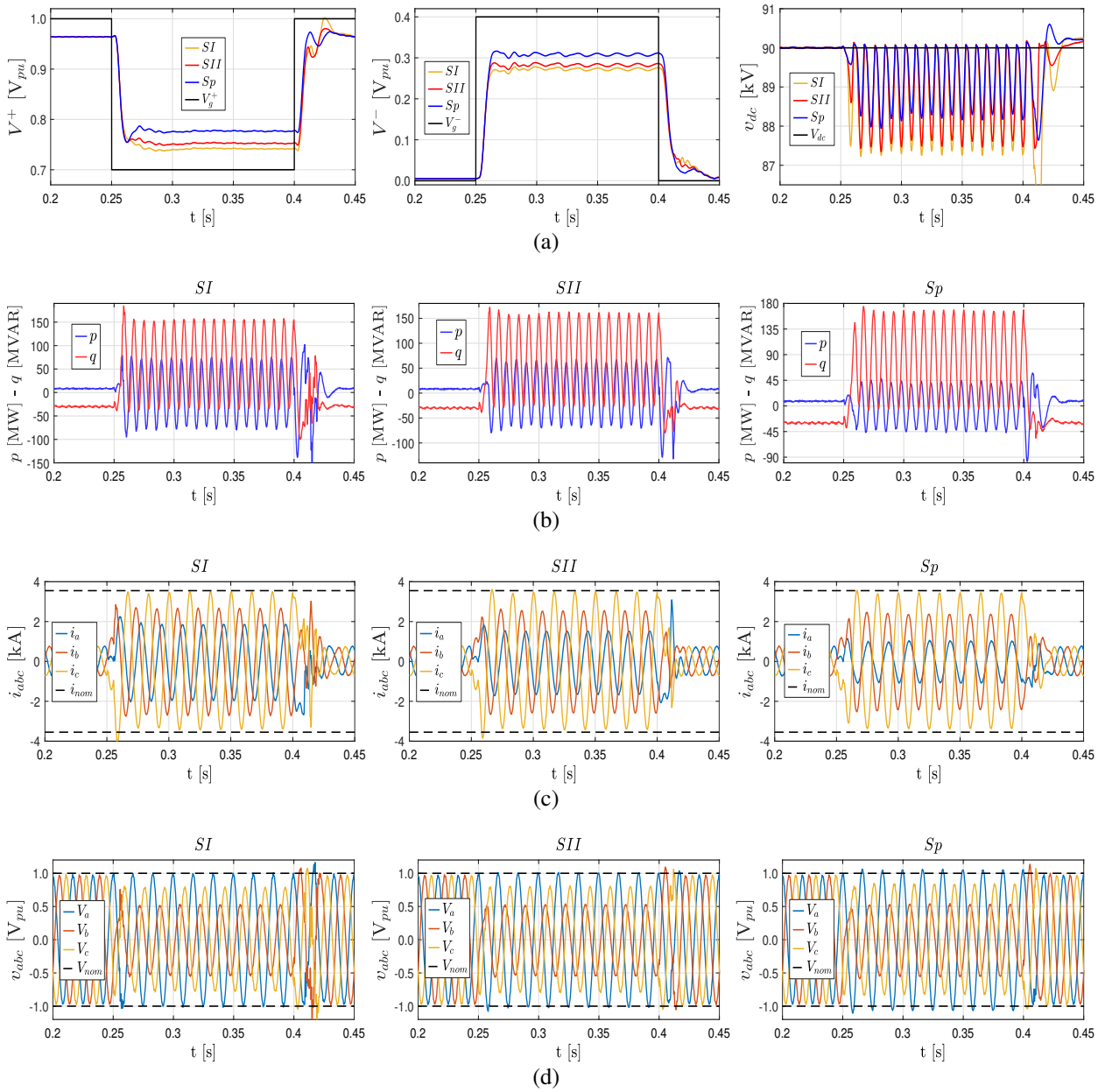


Table 3.3 shows the behavior of the voltage support, the DC-bus voltage, and the power

injection of the strategies for the studied cases.

Table 3.3

Simulations results

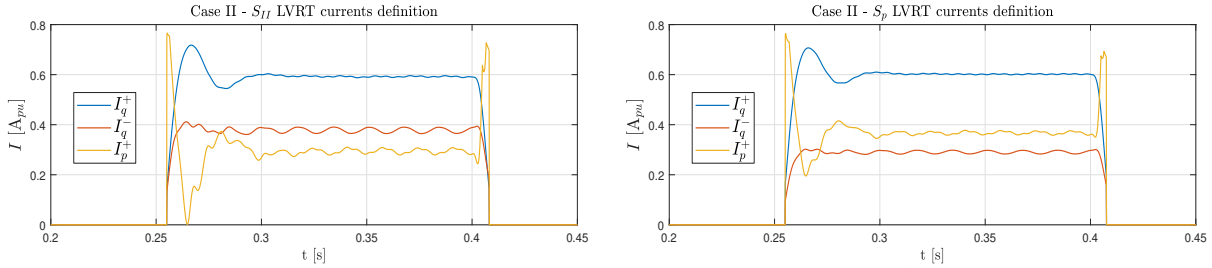
Parameter	Case I			Case II			Case III			Case IV		
Strategy	S_I	S_{II}	S_p	S_I	S_{II}	S_p	S_I	S_{II}	S_p	S_I	S_{II}	S_p
V^+ [V_{pu}]	0.829	0.866	0.869	0.743	0.801	0.803	0.742	0.791	0.810	0.742	0.752	0.779
V^- [V_{pu}]	0.087	0.128	0.134	0.066	0.137	0.152	0.273	0.321	0.341	0.272	0.282	0.308
$\tilde{V}_{dc}$ [kV]	1.47	1.20	1.10	0.25	0.14	0.10	2.70	1.40	0.72	2.75	2.51	1.80
P [MW]	65.9	95.2	91.5	6.6	31.5	42.5	-1.12	1.15	-1.71	-3.00	-3.4	-2.07
$\tilde{P}$ [MW]	34.0	36.8	31.3	88.3	35.6	25.1	71.8	30.2	12.2	76.4	66.4	43.8
Q [MVAR]	25.3	48.4	51.7	10.0	82.3	81.0	60.9	90.9	103.2	70.0	67.6	82.7
$\tilde{Q}$ [MVAR]	70.0	48.0	46.3	91.7	57.5	49.0	94.9	84.2	76.81	103.2	94.8	88.0
V_a [V_{pu}]	0.740	0.735	0.732	0.816	0.950	0.955	1.005	1.097	1.103	1.000	1.007	1.058
V_b [V_{pu}]	0.875	0.942	0.946	0.722	0.737	0.736	0.527	0.547	0.550	0.536	0.543	0.541
V_c [V_{pu}]	0.870	0.932	0.937	0.708	0.744	0.748	0.779	0.845	0.850	0.776	0.796	0.829

It can be observed that strategy S_I prioritizes I_q^- injection, which leads to a greater reduction in V^-. However, this also results in a significant reduction of V^+. Consequently, P and Q injected into the grid are significantly lower than those of strategies S_{II} and S_p, as appreciated in Cases I and II. Furthermore, this strategy presents greater oscillations in the injected powers $\tilde{p}$ and $\tilde{q}$, and thus in the DC-bus voltage $\tilde{v}_{dc}$.

Strategies S_{II} and S_p show a similar behavior for Case I. In Case II, the proposed strategy injects 35 % of additional active power than S_{II}. The reason is that the additional injectable active power is determined by the term $2I_p^+I_q^-sin(x)$. In this case, S_p minimizes the value of I_q^- according to (3.10). As a result, a higher value of I_p^+ can be injected into the grid, as shown in Fig 3.10. It should be noticed that the value of I_q^+ is practically the same for both strategies since S_p only modifies I_q^-'s value.

Figure 3.10

LVRT current definition for Case II a) S_{II} b) S_p (only the calculated values of the current during the sag are shown)



(a) (b)

Reduction of DC-voltage oscillations by S_p is not notable in Fig. 3.8(a). This is attributed to the chopper resistor R_{dc}, which dissipates excess energy when the generated power cannot be fully injected into the grid, thereby preventing DC bus over-voltage. However, S_p significantly reduces active power oscillations $\tilde{p}$ by approximately 30 % compared to S_{II}. This reduction is notable because $\tilde{p}$ is proportional to P, which is higher for S_p than for S_{II} for case II, as previously stated. Conversely, S_p exhibits a 0.015 V$_{pu}$ increase in V^- compared to S_{II} for this scenario.

Figures 3.8 and 3.9, illustrate that strategies S_{II} and S_p utilize the pre-fault value I_{q0}^+ to determine current injection, effectively emulating this synchronous generator behavior during voltage sags. In contrast, S_I presents the same results for cases III and IV. Furthermore, S_p also reduces $\tilde{V}_{dc}$ by 50 % in Case III and in 30 % for Case IV compare to S_{II}. Similarly, S_p achieves a 60 % and 35 % reduction in the amplitude of the active power oscillations $\tilde{P}$ compared to S_{II} in these respective cases.

In cases III and IV, S_p also provides enhanced V^+ support and a lower reduction of V^- com-

pared to S_{II}. However, the amplitude of the V_{abc} voltages for both strategies are nearly identical for both strategies in cases I, II, and III. In Case IV, S_p exhibits higher amplitudes for V_a and V_b, while V_c remains consistent with S_{II}. Therefore, despite the importance of V^+ and V^- in characterizing voltage sag profiles, effective support strategies must consider the amplitude and phase of v_{abc}, which are the actual voltages at the PCC.

3.3.2. Experimental tests.

The current strategies are implemented on the experimental set-up described in Section 2.3.2. Table 3.4 presents the parameters for the experimental test cases. These are similar to those used in the simulations. However, in the experimental set-up, P_{gen} represents the power generation value assumed during the fault. Under normal operation, an injection of 1 kW is considered for all the strategies to guarantee an adequate tracking of the reference signals by the current control. Furthermore, V^- for cases III and IV is reduced to 0.3 V_{pu} for safety reasons.

Table 3.4

Experimental cases

Cases	P_{gen} W	Q_{pf} VAR	V_g^+ $V_{p.u}$	V_g^- $V_{p.u}$	φ_g^+ rad	φ_g^- rad	K
0	1000	-	1	0	0	0	-
I	1000	0	0.808	0.177	-1.3142	1.9076	2.5
II	1000	0	0.7	0.2	0	0	3
III	0	300	0.7	0.3	0.2618	-0.2618	4
IV	0	-300	0.7	0.3	0.2618	-0.2618	4

Figures 3.11 to 3.14 presents the experimental results for cases I to IV, respectively.

Figure 3.11

Experimental results for case I a) V^+, V^- and v_{dc} b) Injected powers p and q c) Injected currents d) Voltages at the PCC

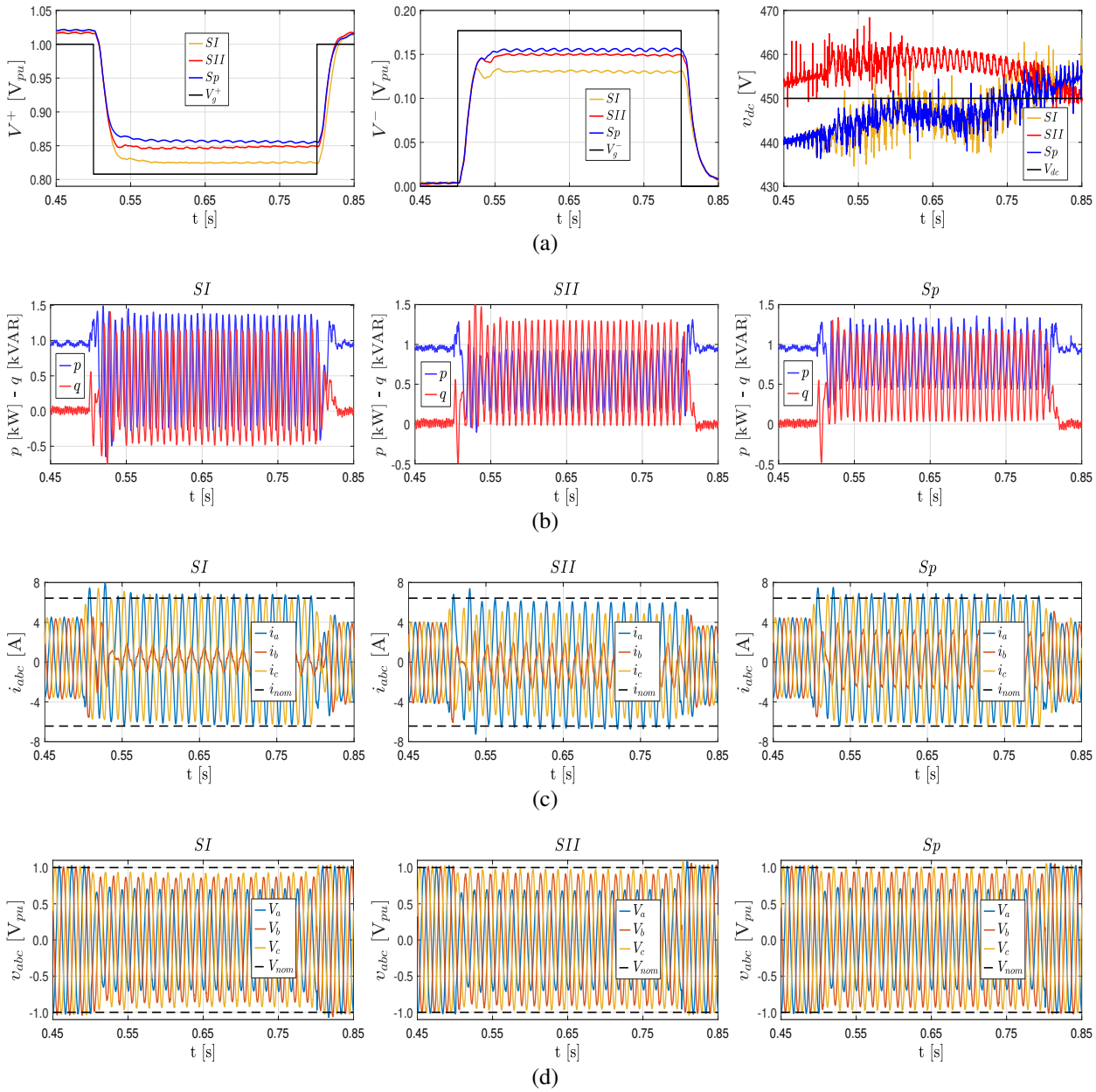


Figure 3.12

Experimental results for case II a) V^+, V^- and v_{dc} b) Injected powers p and q c) Injected currents d) Voltages at the PCC

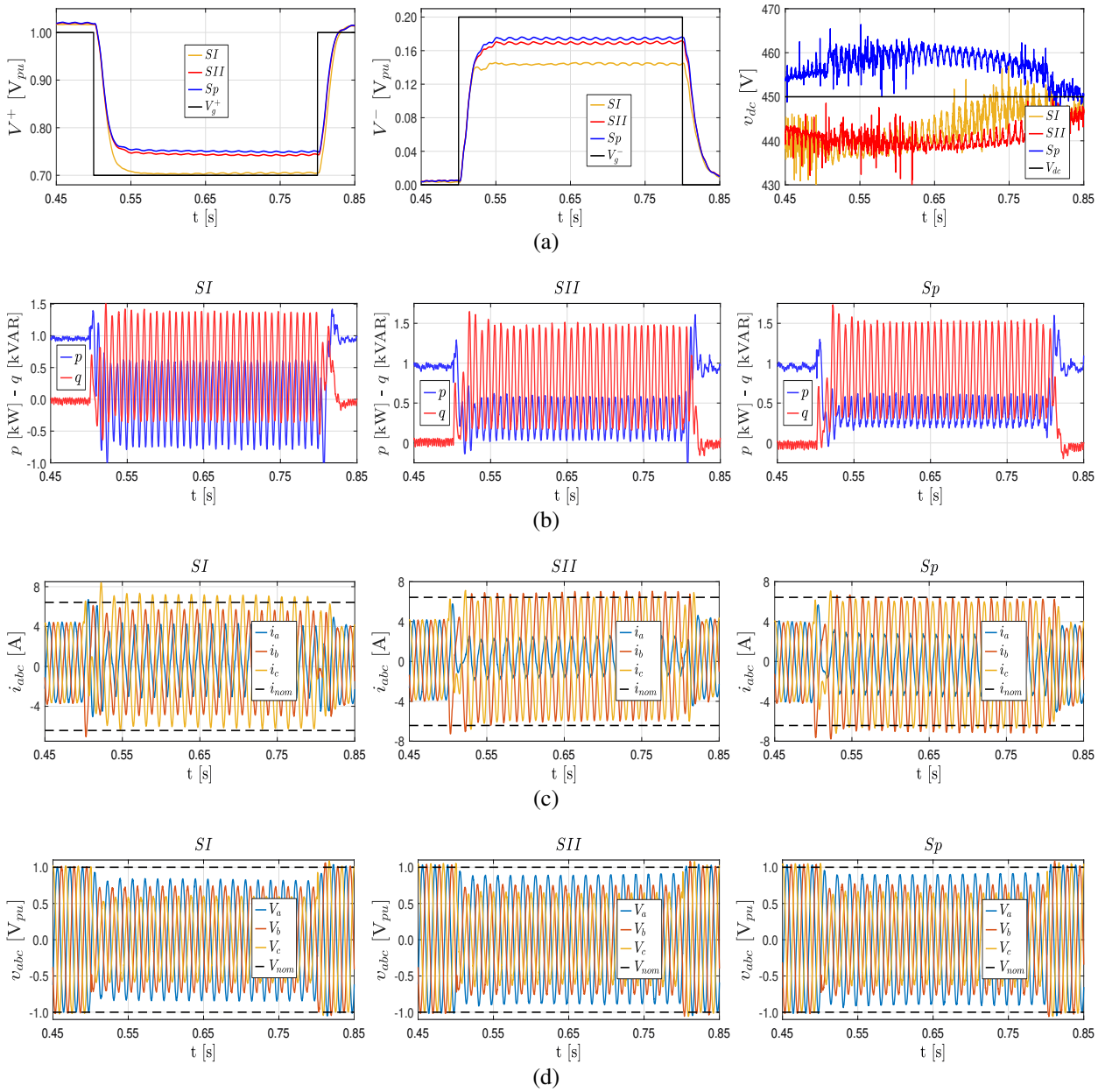


Figure 3.13

Experimental results for case III a) V^+, V^- and v_{dc} b) Injected powers p and q c) Injected currents d) Voltages at the PCC

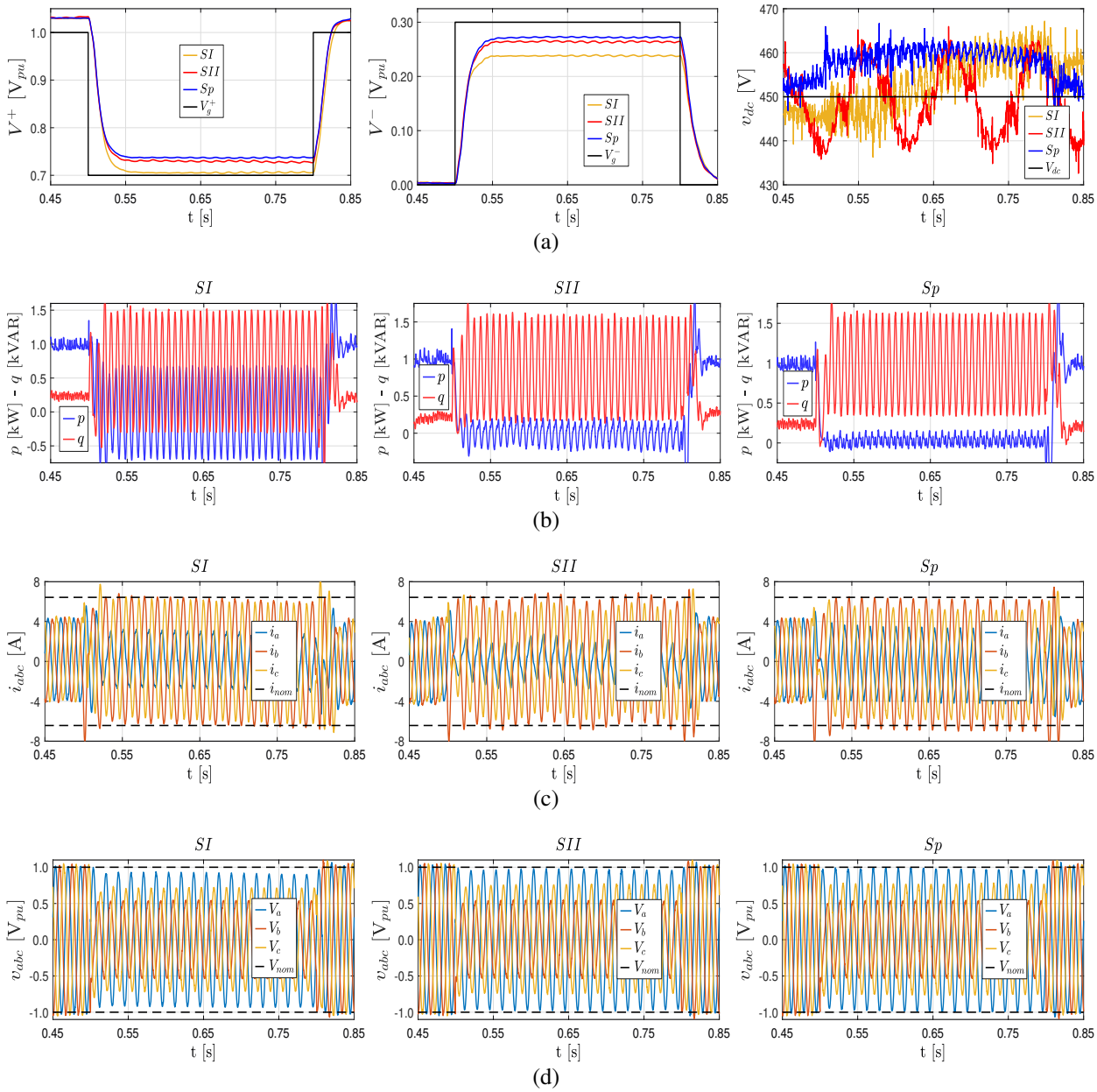


Figure 3.14

Experimental results for case IV a) V^+, V^- and v_{dc} b) Injected powers p and q c) Injected currents d) Voltages at the PCC

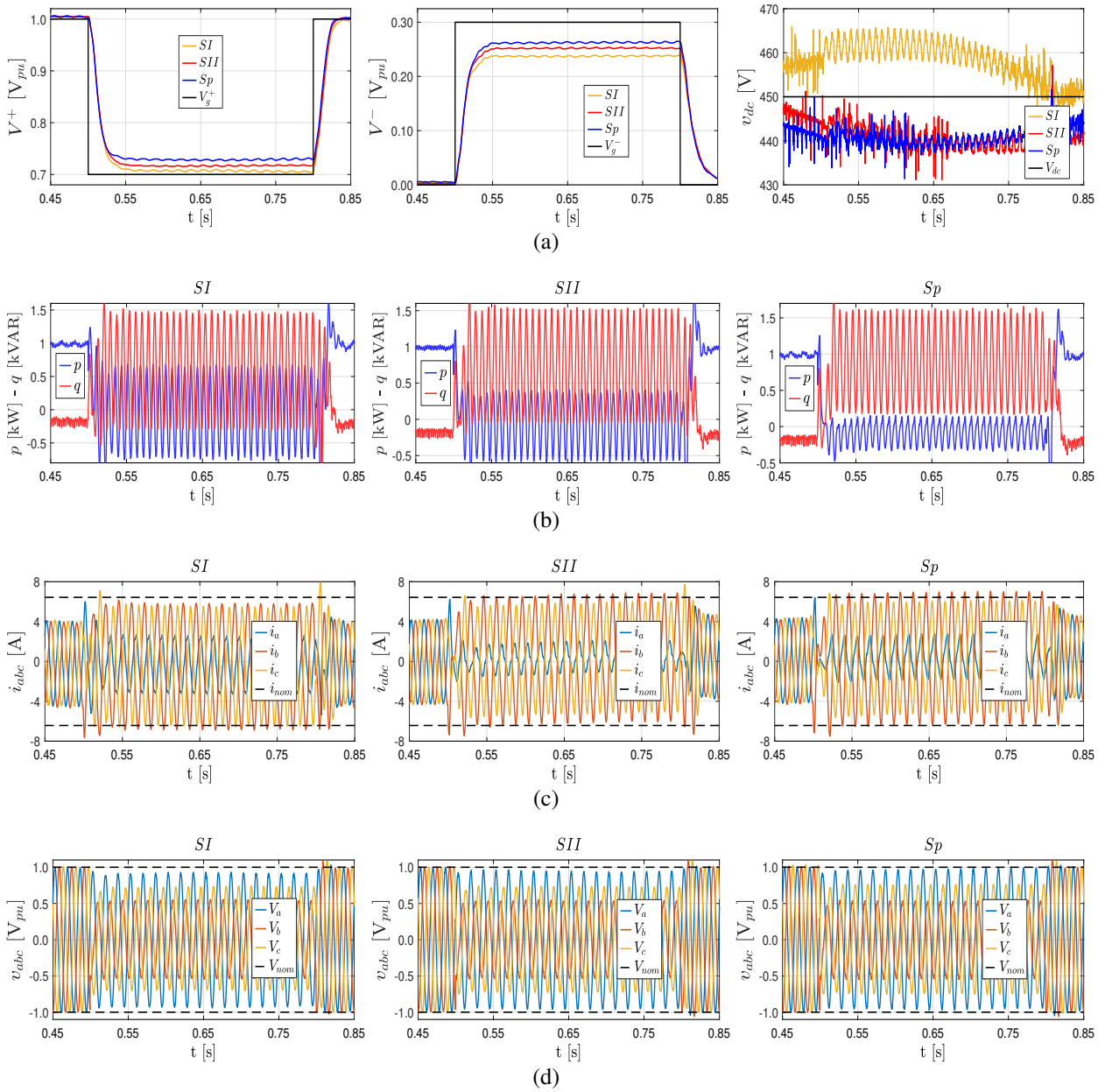


Table 3.5 presents the sequence voltage amplitudes and the power injection scenarios for

the experimental tests during the sags. In this context, $\tilde{v}_{dc}$ is not considered relevant because the generation stage is emulated using a DC programmable source ITECH-6012C (see Fig. 2.10). This source is configured in constant voltage mode with a reference voltage $V_{dc} = 450$ [V]. As a result, no additional components or control mechanisms, such as the chopper resistor, are required.

Table 3.5

Experimental results

Parameter	Case I			Case II			Case III			Case IV		
Strategy	S_I	S_{II}	S_p	S_I	S_{II}	S_p	S_I	S_{II}	S_p	S_I	S_{II}	S_p
V^+ [V_{pu}]	0.825	0.848	0.856	0.704	0.742	0.750	0.706	0.727	0.737	0.706	0.718	0.729
V^- [V_{pu}]	0.130	0.149	0.155	0.144	0.169	0.174	0.238	0.263	0.272	0.237	0.252	0.263
P [kW]	0.55	0.54	0.83	-0.1	0.32	0.59	0.00	-0.03	0.06	-0.02	-0.07	-0.07
$\tilde{P}$ [kW]	0.81	0.37	0.44	0.67	0.29	0.40	0.68	0.18	0.09	0.68	0.48	0.21
Q [kVAR]	0.37	0.64	0.63	0.53	0.81	0.81	0.60	1.06	0.99	0.60	0.75	0.91
$\tilde{Q}$ [kVAR]	0.79	0.65	0.60	0.85	0.85	0.78	0.89	0.88	0.64	0.89	0.79	0.71
V_a[V_{pu}]	0.710	0.689	0.692	0.832	0.895	0.905	0.918	0.966	0.976	0.919	0.948	0.971
V_b[V_{pu}]	0.624	0.903	0.912	0.727	0.755	0.759	0.536	0.530	0.538	0.539	0.533	0.534
V_c[V_{pu}]	0.862	0.962	0.971	0.590	0.640	0.645	0.712	0.748	0.760	0.713	0.721	0.752

Experimental results validate S_p performance derived from the simulations analysis. In cases I and II, the proposed strategy injects more active power while reducing its oscillatory component. This effect is particularly pronounced in Case I, where S_p injects around 50 % more active power compared to the other strategies, with an 53 % of oscillations amplitude ($\tilde{P}$). Conversely, the oscillatory components for S_I and S_{II} were 147 % and 68 % of their respective P. Although $\tilde{v}_{dc}$ behavior cannot be directly studied on the experimental set-up, a reduction in $\tilde{p}$ implies that DC-link voltage oscillation would be reduced due to their direct correlation. In Case II, S_I does not inject active power because it does not utilize I_p^+ to mitigate over-current resulting from the injection of I_q^+ and I_q^-. In contrast, S_p injects 27 % more active power with 68 % of $\tilde{p}$, compared

with S_{II} whose $\tilde{p}$ reach 80 % of the injected P.

Cases III and IV demonstrated that S_p and S_{II} consider the pre-fault values to perform reactive current injection during the fault. On the other hand, results for S_p are consistent for both cases. Experimental results confirm that S_p presents greater support on V^+ and a lower reduction of V^- compare to S_{II}. Consistent with the simulations, S_p exhibits similar or greater phase voltages amplitudes V_{abc} than those of S_{II}. Therefore, the proposed strategy demonstrates effective voltage support, injecting more active power than the compared strategies in most of the Cases. Furthermore, S_p reduces active power oscillations caused by the injection of I_q^+ and I_q^-, thereby mitigating fluctuations in the DC-bus voltage.

3.4. Conclusions

This thesis presents a LVRT current strategy aligned with new generation GCs requirements, specifically the German GC VDE-AR-N 4120. The proposed strategy S_p prioritizes reactive current injection and maximizes active power delivery during faults, with the secondary objective of minimizing active power oscillations. Comparative analysis with strategies S_I and S_{II}, both also based on the German GC, is conducted through simulations and experimental validation.

The results demonstrated that S_p effectively reduces DC-voltage oscillations and active power oscillations, while consistently enabling greater active power injection compared to S_I and S_{II}. Furthermore, S_p maintains or increases phase voltage amplitudes during faults, providing robust voltage support. For these reasons, S_p is a strong alternative to comply the GGC, particularly in applications where minimizing DC-bus voltage fluctuations is desirable.

4. Conclusions and Future Work

Conclusions

This doctoral thesis focused on improving the performance of grid-connected converters under voltage sags. The following conclusions are drawn from this research:

- A comprehensive literature review of grid code requirements and power converter control was conducted. This review revealed that LVRT requirements for distributed power generation systems (DPGS) tend to be more stringent with time. Initially, converter disconnection was permitted under grid abnormal conditions. However, GCs have evolved, requiring DPGS to remain connected and provide voltage support. Nowadays, GCs have started to incorporate negative sequence requirements to improve the LVRT capabilities of the converter. It is anticipated that LVRT requirements will continue to evolve, potentially including parameters such as fault impedance, to further enhance voltage support. The successful implementation of these requirements depends on the developing of the converter's technical characteristics and control systems.

- The synchronization algorithm presented in Chapter 2 achieves a short settling time which is critical for the operation of grid-connected converters during voltage sags. Moreover, it estimates the voltage parameters in compliance with the IEEE-1547 standard. As a result, the DSC-TSSE provides enhanced performance compared to traditional PLL formulations for voltage sequence estimation during grid abnormal conditions.

- The current strategy presented in Chapter 3 fulfills the LVRT requirements of new generation grid codes, specifically the German VDE-AR-N 4120 standard. The strategy incorporates pre-fault conditions to scale down the current while prioritizing reactive current injection. Furthermore, it reduces the instantaneous active power oscillations by adjusting the negative sequence reactive current injection within the VDE-AR-N 4120 tolerance. The strategy demonstrates that active power injection can be increased without significantly compromising voltage support.

- This thesis developed a synchronization algorithm and a current strategy that improve the performance of grid-connected converters during voltage sags. The synchronization algorithm provides rapid and accurate voltage parameter estimation, reducing converter reaction time under fault conditions. The current strategy complies with new generation grid codes, enabling its practical implementation. Additionally, it provides complementary desirable features by mitigating instantaneous active power oscillations and reducing DC-link voltage fluctuations.

Future Works

Potential research directions for future work include:

- The DSC-TSSE demonstrates high performance in estimating voltage parameters for grid-following converters. However, its frequency estimation exhibits a settling time that is too long for grid-forming strategies. Therefore, a promising research direction is to adapt the DSC-TSSE from a phase estimator to a frequency-locked loop (FLL) algorithm that is better

suited for grid-forming operation.

- Stability of powers converters connected to the grid depends on the synchronization algorithm and the current control loops. As the synchronization algorithm was addressed in this thesis, future work should focus on improving current control to ensure accurate tracking of reference currents for various grid and filter configurations.

- Voltage sags are usually characterized by the amplitude of the positive- and negative-sequences. However, the angle between these sequences also affects the amplitude of the *abc* voltages and currents. Future research could investigate how this angle influences the injected currents and, consequently, the voltage support.

- Numerous studies have shown that grid impedance consideration optimizes voltage support. However, the computational time of existing impedance estimation techniques is insufficient to meet the LVRT requirements of grid-connected converters during voltage sags. Therefore, real-time impedance estimation remains a significant area of research.

Discussion

The synchronization algorithm proposed in this thesis meets the IEEE 1547 measurement requirements, achieving steady-state accuracy during voltage sags with high harmonic content. Moreover, the proposed current injection strategy not only complies with the German grid code but also provides additional benefits, such as minimizing active power oscillations during voltage sags. Therefore, its implementation improves inverter performance during voltage sags compared with commercial solutions.

The primary challenge in implementing the proposed algorithms in commercial inverters is the computational burden, as both algorithms must be executed within a sampling period. In this thesis, two dSPACE DS1104 control boards operating in parallel were required to achieve this. Consequently, the use of FPGAs or higher-performance control platforms is necessary for practical implementation. Given the increased cost of such solutions, a cost-benefit analysis is required.

Finally, it is worth recalling that the proposed control was designed for grid-following converters. Therefore, its performance degrades as the grid becomes weaker. In such cases, grid-forming converters are a more suitable option.

Academic Contributions and Professional Development

Journal Papers.

- D. J. Rincón, M. A. Mantilla, J. M. Rey, M. Garnica, and D. Guilbert, *"An Overview of Flexible Current Control Strategies Applied to LVRT Capability for Grid-Connected Inverters"*, Energies, vol. 16, no. 3, p. 1052, Jan. 2023, doi: 10.3390/en16031052.

- D. J. Rincon, W. A. Sotelo, M. A. Mantilla, J. M. Rey, and R. Iravani, *"A two-sample algorithm for three-phase voltage parameters estimation under abnormal grid conditions",* International Journal of Electrical Power Energy Systems, vol. 157, p. 109834, 2024, https://doi.org/10.1016/j.ijepes 2024.109834.

Conferences Papers.

- D. J. Rincón, M. A. Mantilla, J. M. Rey and M. Garnica, *"DC Stage Modelling for LVRT Capability in Photovoltaic Systems",* IECON 2021 - 47^{th} Annual Conference of the IEEE Industrial Electronics Society, Toronto, ON, Canada, 2021, pp. 1-7, doi: 10.1109/IECON48115.2021.9589955.

- W. A. Sotelo, D. J. Rincón, M. A. Mantilla, J. M. Rey and Z. Zheng, *"Performance Analysis of Three-Phase Synchronization Algorithms Under Voltage Sags",* IECON 2022 - 48^{th} Annual Conference of the IEEE Industrial Electronics Society, Brussels, Belgium, 2022, pp. 1-6, doi: 10.1109/IECON49645.2022.9968855.

- I. J. Moreno, M. A. Mantilla, A. Esparza, J. M. Rey and D. J. Rincón, *"Flexibilities of a Voltage Support Control Strategy for Grid-Connected Inverter-Interfaced Distributed Generators during Voltage Sags",* 2023 IEEE 14th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), Shanghai, China, 2023, pp. 645-650, doi: 10.1109/PEDG56097.2023.10215232.

- Liceth T. León, Yolanda Rodríguez, David J. Rincon, María A. Mantilla and Javier E. Solano, *"Comparative Analysis of MPPT Algorithms for PV Systems Under Partial Shading Conditions",* Simposio Internacional sobre la Calidad de la Energía Eléctrica - SICEL, Pereira, Colombia, 2021, https://revistas.unal.edu.co/index.php/SICEL/article/view/97092/87474.

Book Chapters.

- Jersson García-García, Andrés Salinas, David Rincón and Agustín Bucciarelli, *"Laboratorios de microrredes en América Latina y el resto del mundo",* in *Microrredes eléctricas con alta penetración de energías renovables*, Universidad Distrital Francisco José de Caldas - First Edition, pp. 19-52, 2024.

- David Rincón and Miguel Garnica, *"Estrategias de control flexible para inversores ante hundimientos de tensión en redes eléctricas con alta integración de generación distribuida",* in *Microrredes eléctricas con alta penetración de energías renovables*, Universidad Distrital Francisco José de Caldas - First Edition, pp. 185-228, 2024.

Research Internships.

- Research internship at Optical Materials, Photonics and Systems Laboratory (LMOPS), University of Lorraine, Metz, France, under the supervision of Prof. Zhixue Zheng. From January 25^{th} to July 25^{th}, 2022.

- Research internship program in the *Energy System Group of the Department of Electrical and Computer Engineering*, University of Toronto, Toronto, Canada, under the supervision of Prof. Reza Iravani. From January 25^{th} to June 28^{th}, 2023.

References

[1] Rodriguez P, Timbus AV, Teodorescu R, Liserre M, Blaabjerg F. Flexible Active Power Control of Distributed Power Generation Systems During Grid Faults. IEEE Trans Ind Electron. 2007;54(5):2583-92.

[2] Guo X, Liu W, Lu Z. Flexible Power Regulation and Current-Limited Control of the Grid-Connected Inverter Under Unbalanced Grid Voltage Faults. IEEE Transactions on Industrial Electronics. 2017;64(9):7425-32.

[3] Alam MS, Al-Ismail FS, Salem A, Abido MA. High-Level Penetration of Renewable Energy Sources Into Grid Utility: Challenges and Solutions. IEEE Access. 2020;8:190277-99.

[4] Chen X, Mcelroy MB, Wu Q, Shu Y, Xue Y. Transition towards higher penetration of renewables: an overview of interlinked technical, environmental and socio-economic challenges. Journal of Modern Power Systems and Clean Energy. 2019;7(1):1-8.

[5] REN21. Renewables 2024 global status report - renewables in energy supply. REN21 Secretariat; 2024.

[6] Peyghami S, Palensky P, Blaabjerg F. An Overview on the Reliability of Modern Power Electronic Based Power Systems. IEEE Open Journal of Power Electronics. 2020;1:34-50.

[7] Jia J, Yang G, Nielsen AH. A Review on Grid-Connected Converter Control for

Short-Circuit Power Provision Under Grid Unbalanced Faults. IEEE Trans Power Del. 2018;33(2):649-61.

[8] Iweh CD, Gyamfi S, Tanyi E, Effah-Donyina E. Distributed Generation and Renewable Energy Integration into the Grid: Prerequisites, Push Factors, Practical Options, Issues and Merits. Energies. 2021;14(17).

[9] Tse CK, Huang M, Zhang X, Liu D, Li XL. Circuits and Systems Issues in Power Electronics Penetrated Power Grid. IEEE Open Journal of Circuits and Systems. 2020;1:140-56.

[10] Sosa JL, Castilla M, Miret J, Matas J, Al-Turki YA. Control Strategy to Maximize the Power Capability of PV Three-Phase Inverters During Voltage Sags. IEEE Trans Power Electron. 2016;31(4):3314-23.

[11] Camacho A, Castilla M, Miret J, Borrell A, de Vicuña LG. Active and Reactive Power Strategies With Peak Current Limitation for Distributed Generation Inverters During Unbalanced Grid Faults. IEEE Trans Power Electron. 2015;62(3):1515-25.

[12] Afshari E, Moradi GR, Rahimi R, Farhangi B, Yang Y, Blaabjerg F, et al. Control Strategy for Three-Phase Grid-Connected PV Inverters Enabling Current Limitation Under Unbalanced Faults. IEEE Trans Ind Electron. 2017;64(11):8908-18.

[13] Milicua A, Abad G, Rodríguez Vidal MA. Online Reference Limitation Method of Shunt-Connected Converters to the Grid to Avoid Exceeding Voltage and Current Limits Under Unbalanced Operatio - Part I: Theory. IEEE Trans Energy Convers. 2015;30(3):852-63.

[14] Bollen MH. Understanding Power Quality Problems: Voltage Sags and Interruptions. Press I, editor. John Wiley& Sons, Inc; 2000.

[15] IEEE Standard for Harmonic Control in Electric Power Systems. IEEE Std 519-2022 (Revision of IEEE Std 519-2014). 2022:1-31.

[16] IEEE Standard for Interconnection and Interoperability of Distributed Energy Resources with Associated Electric Power Systems Interfaces. IEEE Std 1547-2018 (Revision of IEEE Std 1547-2003). 2018:1-138.

[17] IEEE Standard for Interconnection and Interoperability of Inverter-Based Resources (IBRs) Interconnecting with Associated Transmission Electric Power Systems. IEEE Std 2800-2022. 2022:1-180.

[18] IEEE/IEC International Standard - Measuring relays and protection equipment - Part 118-1: Synchrophasor for power systems - Measurements. IEC/IEEE 60255-118-1:2018. 2018:1-78.

[19] IEEE Recommended Practice for Monitoring Electric Power Quality. IEEE Std 1159-2019 (Revision of IEEE Std 1159-2009). 2019:1-98.

[20] Garnica M, García de Vicuña L, Miret J, Camacho A, Guzmán R. Voltage Support Experimental Analysis of a Low-Voltage Ride-Through Strategy Applied to Grid-Connected Distributed Inverters. Energies. 2018;11(8).

[21] Swagata Das SS, Ananthan SN. Fault Location on Transmission and Distribution Lines: Principles and Applications. Press WI, editor. John Wiley & Sons; 2022.

[22] Tleis N. Power Systems Modelling and Fault Analysis. Elsevier, editor. ACADEMIC PRESS; 2022.

[23] Tarafdar Hagh M, Khalili T. A review of fault ride through of PV and wind renewable energies in grid codes. International Journal of Energy Research. 2019;43(4):1342-56.

[24] Yadav M, Pal N, Saini DK. Low voltage ride through capability for resilient electrical distribution system integrated with renewable energy resources. Energy Reports. 2023;9:833-58.

[25] Buraimoh E, Davidson IE. Overview of Fault Ride-Through Requirements for Photovoltaic Grid Integration, Design and Grid Code Compliance. In: 2020 9th International Conference on Renewable Energy Research and Application (ICRERA); 2020. p. 332-6.

[26] Garnica López MA, García de Vicuña JL, Miret J, Castilla M, Guzmán R. Control Strategy for Grid-Connected Three-Phase Inverters During Voltage Sags to Meet Grid Codes and to Maximize Power Delivery Capability. IEEE Trans Power Electron. 2018;33(11):9360-74.

[27] Zheng Q, Li J, Ai X, Wen J, Fang J. Overview of grid codes for photovoltaic integration. 2017:1-6.

[28] Sarkar MNI, Meegahapola LG, Datta M. Reactive Power Management in Renewable Rich Power Grids: A Review of Grid-Codes, Renewable Generators, Support Devices, Control Strategies and Optimization Algorithms. IEEE Access. 2018;6:41458-89.

[29] Duong MQ, Leva S, Mussetta M, Le KH. A Comparative Study on Controllers for Improving Transient Stability of DFIG Wind Turbines During Large Disturbances. Energies. 2018;11(3).

[30] Resolucion No 60 del 2019: Modificaciones al Reglamento de Operación para permitir la conexión y operación de plantas solares fotovoltaicas y eólicas en el SIN. Comisión de Regulación de Energía y Gas CREG. 2019.

[31] Technical requirements for the connection and operation of customer installations to the high voltage network (TAR high voltage), VDE-AR-N 4120; 2018.

[32] UNE-EN 50549-2 Requirements for generating plants to be connected in parallel with distribution networks Part 2: Connection to a MV distribution network Generating plants up to and including Type B. Asociación Española de Normalización, España. 2019.

[33] European Standard: Requirements for generating plants to be connected in parallel with distribution networks - Part 2: Connection to a MV distribution network - Generation plants up to and including Type B. EN 50549-2:2019/A1:2023. 2023:1-85.

[34] Shabestary MM, Mohamed YAI. Advanced Voltage Support and Active Power Flow Control in Grid-Connected Converters Under Unbalanced Conditions. IEEE Trans Power Electron. 2018;33(2):1855-64.

[35] Tafti HD, Maswood AI, Konstantinou G, Pou J, Townsend CD. Low-voltage ride-through

capability of full-row connected cascaded H-bridge converters. In: 2016 IEEE Region 10 Conference (TENCON); 2016. p. 984-7.

[36] Afshari E, Moradi GR, Yang Y, Farhangi B, Farhangi S. A review on current reference calculation of three-phase grid-connected PV converters under grid faults. In: 2017 IEEE Power and Energy Conference at Illinois (PECI); 2017. p. 1-7.

[37] Xu C, Xuehua W, Xinbo R, Cheng W, Huanyu W. A Low-Voltage Ride-Through Control Strategy for Two-Stage T-Type Three-Level Photovoltaic Inverters Limiting DC-Link Overvoltage and Grid-Side Overcurrent. In: 2018 20th European Conference on Power Electronics and Applications (EPE'18 ECCE Europe); 2018. p. P.1-P.10.

[38] Naresh P, Sravan Kumar VS. Analysis of Low Voltage Ride Through Techniques for Grid-Connected Photovoltaic Systems. In: 2020 IEEE International Conference on Power Electronics, Smart Grid and Renewable Energy (PESGRE2020); 2020. p. 1-7.

[39] Zhang H, Xiang W, Lin W, Wen J. Grid Forming Converters in Renewable Energy Sources Dominated Power Grid: Control Strategy, Stability, Application, and Challenges. Journal of Modern Power Systems and Clean Energy. 2021;9(6):1239-56.

[40] Li Y, Gu Y, Green TC. Revisiting Grid-Forming and Grid-Following Inverters: A Duality Theory. IEEE Transactions on Power Systems. 2022;37(6):4541-54.

[41] Wang X, Taul MG, Wu H, Liao Y, Blaabjerg F, Harnefors L. Grid-Synchronization Stability

of Converter-Based Resources - An Overview. IEEE Open Journal of Industry Applications. 2020;1:115-34.

[42] Roncero-Sanchez P, del Toro Garcia X, Torres AP, Feliu V. Fundamental Positive- and Negative-Sequence Estimator for Grid Synchronization Under Highly Disturbed Operating Conditions. IEEE Transactions on Power Electronics. 2013;28(8):3733-46.

[43] Rodriguez P, Pou J, Bergas J, Candela JI, Burgos RP, Boroyevich D. Decoupled Double Synchronous Reference Frame PLL for Power Converters Control. IEEE Transactions on Power Electronics. 2007;22(2):584-92.

[44] Mohammad Reza MM. Performance Comparison of Synchronous Reference Frame-Based PLLs Topologies Under Power Quality Disturbances. Iranian Journal of Science and Technology, Transactions of Electrical Engineering. 2018.

[45] Remus Teodorescu PR Marco Liserre. Grid Converters for Photovoltaic and Wind Power Systems. Sons JW, editor. Wiley-IEEE Press; 2011.

[46] Aljarrah R, Fawaz BB, Salem Q, Karimi M, Marzooghi H, Azizipanah-Abarghooee R. Issues and Challenges of Grid-Following Converters Interfacing Renewable Energy Sources in Low Inertia Systems: A Review. IEEE Access. 2024;12:5534-61.

[47] Yazdani D, Mojiri M, Bakhshai A, Joós G. A Fast and Accurate Synchronization Technique for Extraction of Symmetrical Components. IEEE Trans Power Electron. 2009;24(3):674-84.

[48] Sun M, Sahinoglu Z. Extended Kalman filter based grid synchronization in the presence of voltage unbalance for smart grid. In: ISGT 2011; 2011. p. 1-4.

[49] Mantilla MA, Petit JF, Ordóñez G. Control of multi-functional grid-connected PV systems with load compensation under distorted and unbalanced grid voltages. Electric Power Systems Research. 2021;192:106918.

[50] Mohammedsaeed EK, Jia K. Comparison of some low voltage ride-through strategies. In: IECON 2017 - 43rd Annual Conference of the IEEE Industrial Electronics Society; 2017. p. 152-7.

[51] Lin X, Han Y, Yang P, Wang C, Xiong J. Low-Voltage Ride-Through Techniques for Two-Stage Photovoltaic System under Unbalanced Grid Voltage Sag Conditions. In: 2018 IEEE 4th Southern Power Electronics Conference (SPEC); 2018. p. 1-8.

[52] Mirhosseini M, Pou J, Agelidis VG. Individual Phase Current Control With the Capability to Avoid Overvoltage in Grid-Connected Photovoltaic Power Plants Under Unbalanced Voltage Sags. IEEE Trans Power Electron. 2015;30(10):5346-51.

[53] Talha M, Raihan SRS, Rahim NA. PV inverter with decoupled active and reactive power control to mitigate grid faults. Renewable Energy. 2020;162:877-92.

[54] Rincón DJ, Mantilla MA, Rey JM, Garnica M, Guilbert D. An Overview of Flexible Current Control Strategies Applied to LVRT Capability for Grid-Connected Inverters. Energies. 2023;16(3).

[55] Miret J, Castilla M, Camacho A, Vicuña LGd, Matas J. Control Scheme for Photovoltaic Three-Phase Inverters to Minimize Peak Currents During Unbalanced Grid-Voltage Sags. IEEE Trans Power Electron. 2012;27(10):4262-71.

[56] Guo X, Zhang X, Wang B, Wu W, Guerrero JM. Asymmetrical Grid Fault Ride-Through Strategy of Three-Phase Grid-Connected Inverter Considering Network Impedance Impact in Low-Voltage Grid. IEEE Trans Power Electron. 2014;29(3):1064-8.

[57] Miret J, Camacho A, Castilla M, de Vicuña LG, Matas J. Control Scheme With Voltage Support Capability for Distributed Generation Inverters Under Voltage Sags. IEEE Trans Power Electron. 2013;28(11):5252-62.

[58] Castilla M, Miret J, Camacho A, Matas J, García de Vicuña L. Voltage Support Control Strategies for Static Synchronous Compensators Under Unbalanced Voltage Sags. IEEE Trans Power Electron. 2014;61(2):808-20.

[59] Camacho A, Castilla M, Miret J, Vasquez JC, Alarcon-Gallo E. Flexible Voltage Support Control for Three-Phase Distributed Generation Inverters Under Grid Fault. IEEE Trans Ind Electron. 2013;60(4):1429-41.

[60] Jin P, Li Y, Li G, Chen Z, Zhai X. Optimized hierarchical power oscillations control for distributed generation under unbalanced conditions. Applied Energy. 2017;194:343-52.

[61] Camacho A, Castilla M, Miret J, de Vicuña LG, Guzman R. Positive and Negative Sequence

Control Strategies to Maximize the Voltage Support in Resistive-Inductive Grids During Grid Faults. IEEE Trans Power Electron. 2018;33(6):5362-73.

[62] Shuvra MA, Chowdhury B. Distributed dynamic grid support using smart PV inverters during unbalanced grid faults. IET Renewable Power Generation. 2019.

[63] Garnica M, de Vicuña LG, Miret J, Castilla M, Guzmán R. Optimal Voltage-Support Control for Distributed Generation Inverters in RL Grid-Faulty Networks. IEEE Trans Power Electron. 2020;67(10):8405-15.

[64] Yang H, Tang Y. A Noninvasive Grid Impedance Estimation Method With Phase-Lock Loops. IEEE Transactions on Power Electronics. 2024;39(8):9059-65.

[65] De Meerendre MK, Prieto-Araujo E, Ahmed KH, Gomis-Bellmunt O, Xu L, Egea-Alvarez A. Review of Local Network Impedance Estimation Techniques. IEEE Access. 2020;8:213647-61.

[66] Camacho A, Castilla M, Miret J, Guzman R, Borrell A. Reactive Power Control for Distributed Generation Power Plants to Comply With Voltage Limits During Grid Faults. IEEE Trans Power Electron. 2014;29(11):6224-34.

[67] Rodriguez J, Lai JS, Peng FZ. Multilevel inverters: a survey of topologies, controls, and applications. IEEE Transactions on Industrial Electronics. 2002;49(4):724-38.

[68] Zhou K, Wang D. Relationship between space-vector modulation and three-phase carrier-

based PWM: a comprehensive analysis [three-phase inverters]. IEEE Transactions on Industrial Electronics. 2002;49(1):186-96.

[69] Miret J, Garnica López M, Vicuña L, Camacho A. PI-based controller for low-power distributed inverters to maximize reactive current injection while avoiding over voltage during voltage sags. IET Power Electronics. 2018 10;12.

[70] Celik D, Meral ME. A flexible control strategy with overcurrent limitation in distributed generation systems. International Journal of Electrical Power & Energy Systems. 2019;104:456-71.

[71] Celik D, Meral ME. Voltage Support Control Strategy of Grid-connected Inverter System Under Unbalanced Grid Faults to Meet Fault Ride Through Requirements. IET Generation, Transmission & Distribution. 2020.

[72] Meral ME, Celik D. Mitigation of DC-link voltage oscillations to reduce size of DC-side capacitor and improve lifetime of power converter. Electric Power Systems Research. 2021;194:107048.

[73] Azizi A, Banaiemoqadam A, Hooshyar A, Patel M. A Blind Spot in the LVRT Current Requirements of Modern Grid Codes for Inverter-Based Resources. IEEE Transactions on Power Delivery. 2023;38(1):319-34.

[74] Feng Y, Huang W, Jin Z, Li Y, Shen ZJ, Shuai Z. Voltage Support Strategy for Improving Po-

wer Transfer Capability of Grid-Connected Converter Under Unbalanced Conditions. IEEE Transactions on Power Electronics. 2024;39(7):7863-75.

[75] Wang Y, Zhao Q, Zhang W, Zhang T, Sun X, Wei M. A Multi-Objective Bi-Level LVRT Control Strategy for Two-Stage PV Grid-Connected System Under Asymmetrical Faults. IEEE Transactions on Sustainable Energy. 2025;16(2):1467-82.

[76] Holmes DG. Pulse Width Modulation For Power Converters>Principles and Practice. on Power Engineering IS, editor. IEEE PRESS; 2003.

[77] Alzate RE, Posada J. Design and implementation of proportional-resonant controller for 3-phase current source inverter in Dspace DS1104. In: 2017 IEEE Workshop on Power Electronics and Power Quality Applications (PEPQA); 2017. p. 1-6.

[78] Kazmierkowski MP, Malesani L. Current control techniques for three-phase voltage-source PWM converters: a survey. IEEE Transactions on Industrial Electronics. 1998;45(5):691-703.

[79] Solatialkaran D, Khajeh KG, Zare F. A Novel Filter Design Method for Grid-Tied Inverters. IEEE Transactions on Power Electronics. 2021;36(5):5473-85.

[80] Yagnik UP, Solanki MD. Comparison of L, LC & LCL filter for grid connected converter. In: 2017 International Conference on Trends in Electronics and Informatics (ICEI); 2017. p. 455-8.

[81] Pal B, Sahu PK, Mohapatra S. A review on feedback current control techniques of grid-connected PV inverter system with LCL filter. In: 2018 Technologies for Smart-City Energy Security and Power (ICSESP); 2018. p. 1-6.

[82] Timbus A, Liserre M, Teodorescu R, Rodriguez P, Blaabjerg F. Evaluation of Current Controllers for Distributed Power Generation Systems. IEEE Transactions on Power Electronics. 2009;24(3):654-64.

[83] Ogata K. Modern Control Engineering. Hall P, editor. Pearson; 2010.

[84] Mahela OP, Shaik AG. Comprehensive overview of grid interfaced solar photovoltaic systems. Renewable and Sustainable Energy Reviews. 2017;68:316-32.

[85] Islam H, Mekhilef S, Shah NBM, Soon TK, Seyedmahmousian M, Horan B, et al. Performance Evaluation of Maximum Power Point Tracking Approaches and Photovoltaic Systems. Energies. 2018;11(2).

[86] Rincón DJ, Sotelo WA, Mantilla MA, Rey JM, Iravani R. A two-sample algorithm for three-phase voltage parameters estimation under abnormal grid conditions. International Journal of Electrical Power & Energy Systems. 2024;157:109834.

[87] Tang F, Zhou J, Xin Z, Huang S, Loh PC. An Improved Three-Phase Voltage Source Converter With High-Performance Operation Under Unbalanced Conditions. IEEE Access. 2018;6:15908-18.

[88] Letaief F, Hamouda M, Belaid MA, Al-Haddad K. A Comprehensive Approach to Flexible LVRT Strategies for Inverter-Based PPMs Enhancing Voltage-Support, Overcurrent Protection, and DC-Link Voltage Quality. IEEE Access. 2024;12:52990-3017.

[89] Huka GB, Li W, Chao P, Peng S. A comprehensive LVRT strategy of two-stage photovoltaic systems under balanced and unbalanced faults. International Journal of Electrical Power & Energy Systems. 2018;103:288-301.

[90] Zunaib Alia NC, Lenos Hadjidemetrioub YY Elias Kyriakidesb, Blaabjerg F. Three-phase phase-locked loop synchronization algorithms for grid-connected renewable energy systems: A review. Renewable and Sustainable Energy Reviews. 2018;90:434-52.

[91] Guerrero-Rodríguez NF, Rey-Boué AB, Bueno EJ, Ortiz O, Reyes-Archundia E. Synchronization algorithms for grid-connected renewable systems: Overview, tests and comparative analysis. Renewable and Sustainable Energy Reviews. 2017;75:629-43.

[92] Meral ME, Celik D. Minimisation of power oscillations with a novel optimal control strategy for distributed generation inverter under grid faulty and harmonic networks. IET Renewable Power Generation. 2020 November;14:3010-22(12).

[93] Golestan S, Guerrero JM, Vasquez JC. Three-Phase PLLs: A Review of Recent Advances. IEEE Transactions on Power Electronics. 2017;32(3):1894-907.

[94] Xu J, Ling Z, Luo Y, Kan J, Diao H, Xie S. Synchronization Stability Analysis and Parameter Design of Grid-Following Inverters Considering the Interactions of Current Control and

Phase-Locked Loop. IEEE Journal of Emerging and Selected Topics in Power Electronics. 2024;12(5):5013-27.

[95] Liu Y, Yao J, Pei J, Zhao Y, Sun P, Zeng D, et al. Transient Stability Enhancement Control Strategy Based on Improved PLL for Grid Connected VSC during Severe Grid Fault. IEEE Transactions on Energy Conversion. 2021;36(1):218-29.

[96] Achlerkar PD, Panigrahi BK. New Perspectives on Stability of Decoupled Double Synchronous Reference Frame PLL. IEEE Transactions on Power Electronics. 2022;37(1):285-302.

[97] Wang Z, Guo L, Li X, Pang X, Li X, Zhou X, et al. PLL Synchronization Transient Stability Analysis of a Weak-Grid Connected VSC During Asymmetric Faults. IEEE Transactions on Power Electronics. 2024;39(2):2140-54.

[98] Zhao J, Huang M, Zha X. Nonlinear Analysis of PLL Damping Characteristics in Weak-Grid-Tied Inverters. IEEE Transactions on Circuits and Systems II: Express Briefs. 2020;67(11):2752-6.

[99] Guan L, Yao J. A Novel PLL Structure for Dynamic Stability Improvement of DFIG-based Wind Energy Generation Systems During Asymmetric LVRT. Journal of Modern Power Systems and Clean Energy. 2023;11(4):1149-64.

[100] Sotelo WA, Rincón DJ, Mantilla MA, Rey JM, Zheng Z. Performance Analysis of Three-Phase Synchronization Algorithms Under Voltage Sags. In: IECON 2022 â€“ 48th Annual Conference of the IEEE Industrial Electronics Society; 2022. p. 1-6.

[101] Reza MS, Ciobotaru M, Agelidis VG. A Modified Demodulation Technique for Single-Phase Grid Voltage Fundamental Parameter Estimation. IEEE Transactions on Industrial Electronics. 2015;62(6):3705-13.

[102] O´ Rourke CJ, Qasim MM, Overlin MR, Kirtley JL. A Geometric Interpretation of Reference Frames and Transformations: dq0, Clarke, and Park. IEEE Transactions on Energy Conversion. 2019;34(4):2070-83.

[103] Golestan S, Ramezani M, Guerrero JM, Monfared M. dq-Frame Cascaded Delayed Signal Cancellation- Based PLL: Analysis, Design, and Comparison With Moving Average Filter-Based PLL. IEEE Transactions on Power Electronics. 2015;30(3):1618-32.

[104] Wang YF, Li YW. Grid Synchronization PLL Based on Cascaded Delayed Signal Cancellation. IEEE Transactions on Power Electronics. 2011;26(7):1987-97.

[105] Golestan S, Guerrero JM. Conventional Synchronous Reference Frame Phase-Locked Loop is an Adaptive Complex Filter. IEEE Transactions on Industrial Electronics. 2015;62(3):1679-82.

[106] Rodríguez P, Luna A, Candela I, Mujal R, Teodorescu R, Blaabjerg F. Multiresonant frequency-locked loop for grid synchronization of power converters under distorted grid conditions. IEEE Transactions on Industrial Electronics. 2010;58(1):127-38.

[107] Golestan S, Guerrero JM, Abusorrah AM. MAF-PLL with phase-lead compensator. IEEE Transactions on Industrial Electronics. 2014;62(6):3691-5.

[108] Hui N, Xu H, Feng Y. A high performance grid synchronization method for renewable energy grid-connected applications. Energy Reports. 2021;7:388-94. 2021 The 4th International Conference on Electrical Engineering and Green Energy.

[109] IEEE Standard for Synchrophasor Measurements for Power Systems. IEEE Std C371181-2011 (Revision of IEEE Std C37118-2005). 2011:1-61.

[110] Bittanti S, Savaresi SM. On the parametrization and design of an extended Kalman filter frequency tracker. IEEE Transactions on Automatic Control. 2000;45(9):1718-24.

[111] Just H, Gentejohann M, Eggers M, Dieckerhoff S. Analysis and Control of DC-link Oscillations of Voltage Source Inverters during Unbalanced Grid Faults. In: 2019 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe); 2019. p. P.1-P.10.

[112] Joshi J, Swami AK, Jately V, Azzopardi B. A Comprehensive Review of Control Strategies to Overcome Challenges During LVRT in PV Systems. IEEE Access. 2021;9:121804-34.

[113] Shin D, Lee KJ, Lee JP, Yoo DW, Kim HJ. Implementation of Fault Ride-Through Techniques of Grid-Connected Inverter for Distributed Energy Resources With Adaptive Low-Pass Notch PLL. IEEE Transactions on Power Electronics. 2015;30(5):2859-71.

[114] Castilla M, Camacho A, Miret J, Guzmán R, Vicuña L. Avoiding overvoltage problems in three-phase distributed-generation systems during unbalanced voltage sags. IET Power Electronics. 2020 June;13:1537-45(8).

[115] Iñiguez JI, Duarte JN, Camacho A, Miret J, Castilla M. Voltage Support Provided by Three-Phase Three-Wire Inverters With Independent Reactive Phase-Current Injection. IEEE Transactions on Industrial Electronics. 2024;71(10):11806-16.

[116] Graungaard Taul M, Wang X, Davari P, Blaabjerg F. Current Reference Generation Based on Next-Generation Grid Code Requirements of Grid-Tied Converters During Asymmetrical Faults. IEEE Journal of Emerging and Selected Topics in Power Electronics. 2020;8(4):3784-97.

[117] Abubakar M, Renner H, Schurhuber R. Development of a Novel Control Scheme for Grid-Following Converter under Asymmetrical Faults. Energies. 2023;16(3).

[118] Akagi H, Watanabe EH, Aredes M. Instantaneous Power Theory and Applications to Power Conditioning. Sons JW, editor. Wiley-IEEE Press; 2017.

[119] Rincón DJ, Mantilla MA, Rey JM, Garnica M. DC Stage Modelling for LVRT Capability in Photovoltaic Systems. In: IECON 2021 â€“ 47th Annual Conference of the IEEE Industrial Electronics Society; 2021. p. 1-7.

[120] Damanik O, Sakinci OC, Grdenic G, Beerten J. Evaluation of the use of short-circuit ratio as a system strength indicator in converter-dominated power systems. In: 2022 IEEE PES Innovative Smart Grid Technologies Conference Europe (ISGT-Europe); 2022. p. 1-5.

Appendix

Appendix A. Additional results for the synchronization experimental tests

This appendix shows complementary results for the open- and closed-loop tests performed on the DSC-TSSE. The results do not add relevant information for the performance analysis of the proposed algorithm. However, they are useful for validating the algorithm's behavior under different harmonic distortion content.

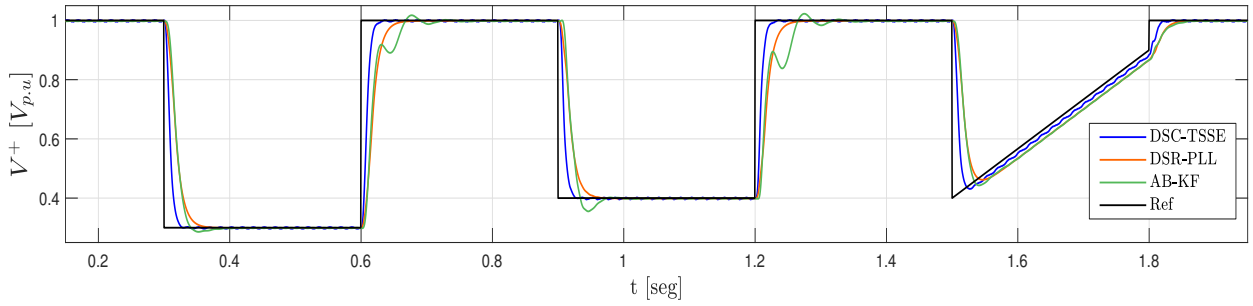
Open-loop complementary results

Figures A.1 and A.2 show the open-loop experimental results for the different voltage sags described in table 2.1, considering case 1 of harmonic distortion content, THD=7,35 %. In the same way, figures A.3 and A.4 exhibit the results considering a THD=10,0 % which corresponds to harmonic distortion content case 2. Table A.1 presents the open-loop test's comparison results for harmonic distortion cases 1 and 2, respectively. The results that meet the threshold according to the specified criteria described in Section 2.3.2 are highlighted in green, while those that do not meet the criteria are highlighted in orange.

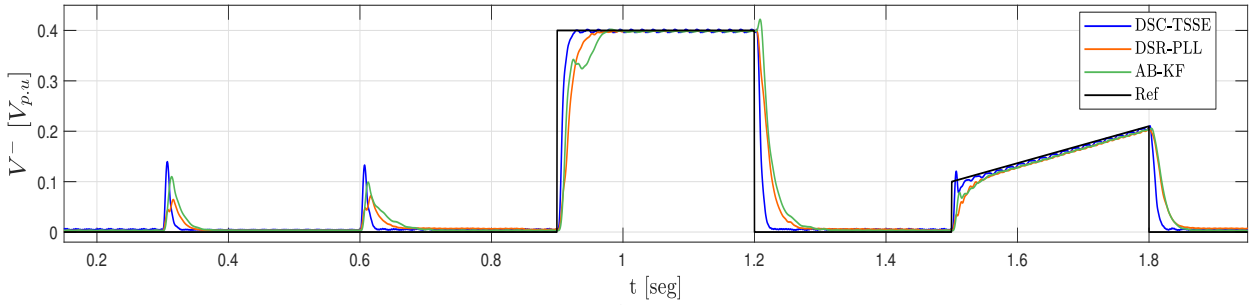
Table A.1 shows that the color highlight is almost the same for the harmonic distortion cases 1 to 3, only with four exceptions. The most relevant is that the DSC-TSSE reaches an accuracy of 2 % estimating V^+ under the ramp voltage scenario, considering a THD=7,35 % and obtaining a $t_s = 19,3$ [ms]. For the open-loop test considering harmonic distortion, this is the only time that one of the algorithms reach the mentioned criteria, validating again the superior performance of the DSC-TSSE.

Figure A.1

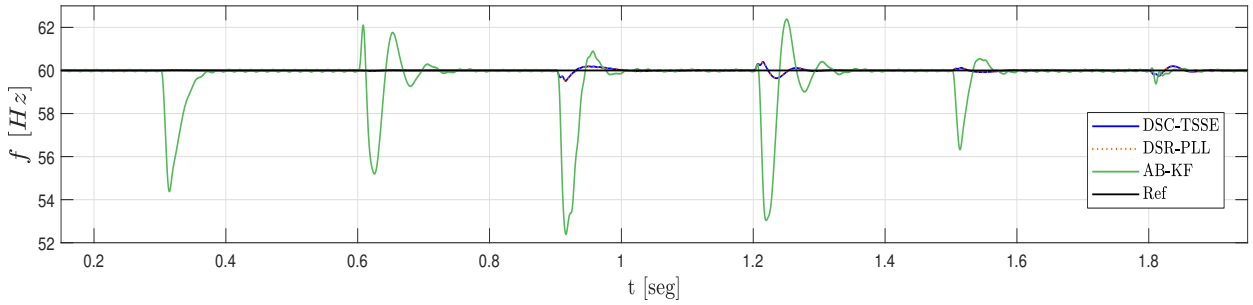
Results voltage sags scenarios type I with THD = 7,35% a) V^+, b) V^-, c) ω, and d) θ^+



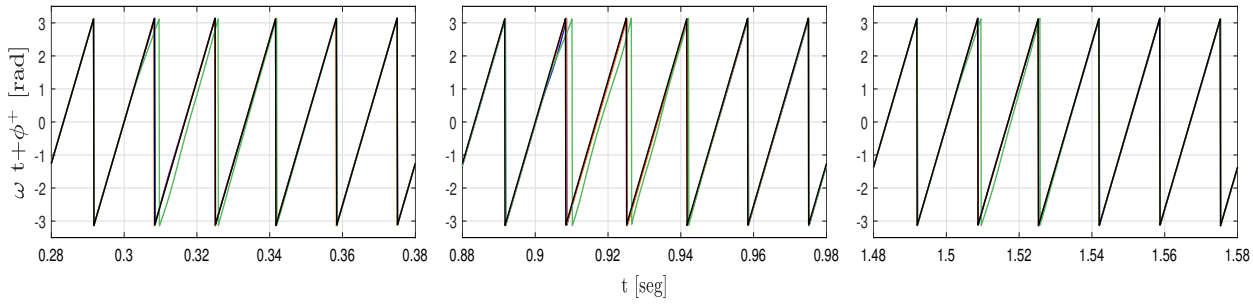
(a)



(b)



(c)



(d)

Figure A.2

Results voltage sags scenarios type II with THD = 7,35% a) V^+, b) V^-, c) ω, and d) θ^+

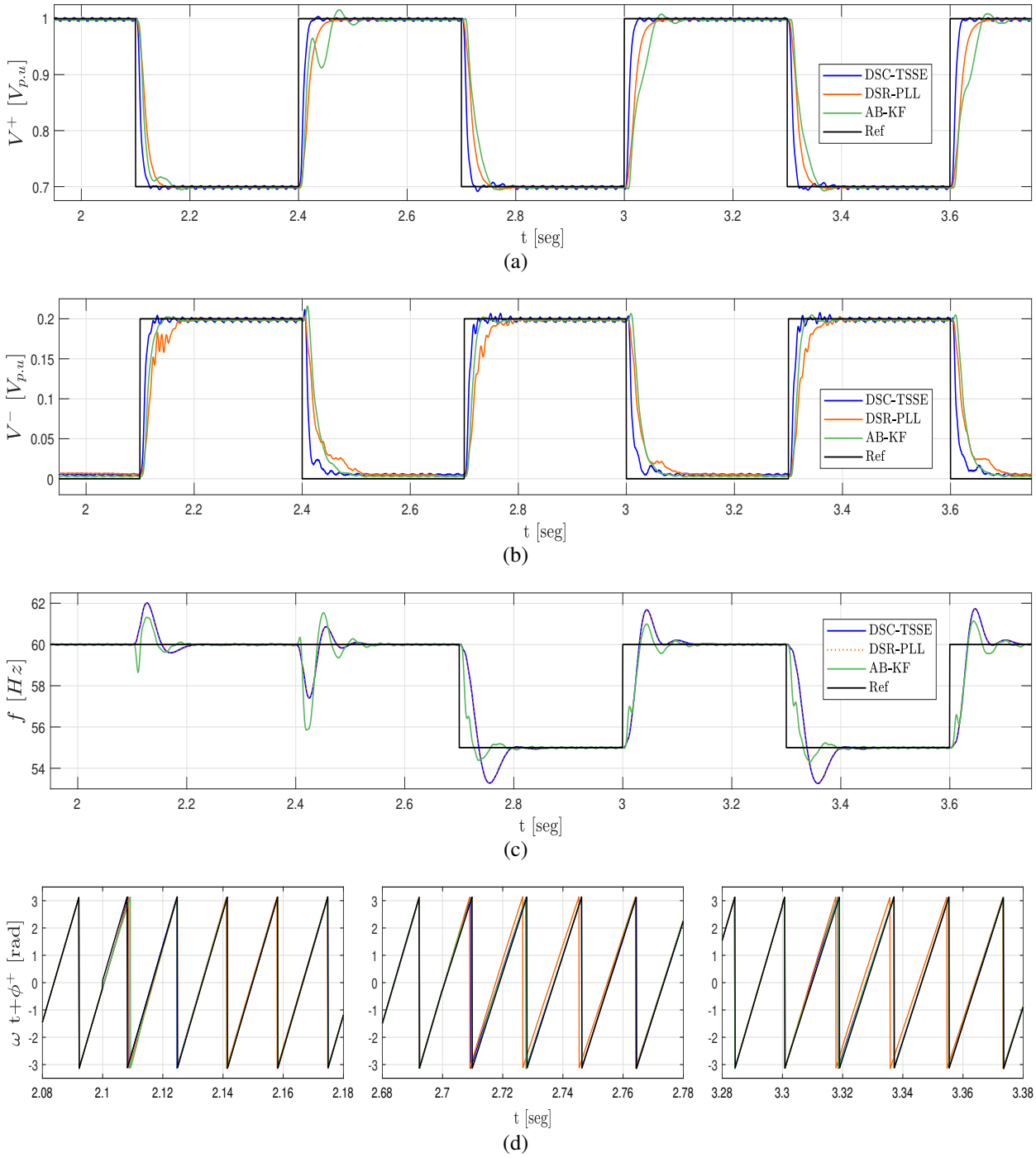


Figure A.3

Results voltage sags scenarios type I with THD = 10,0% a) V^+ b) V^- c) ω and d) θ^+

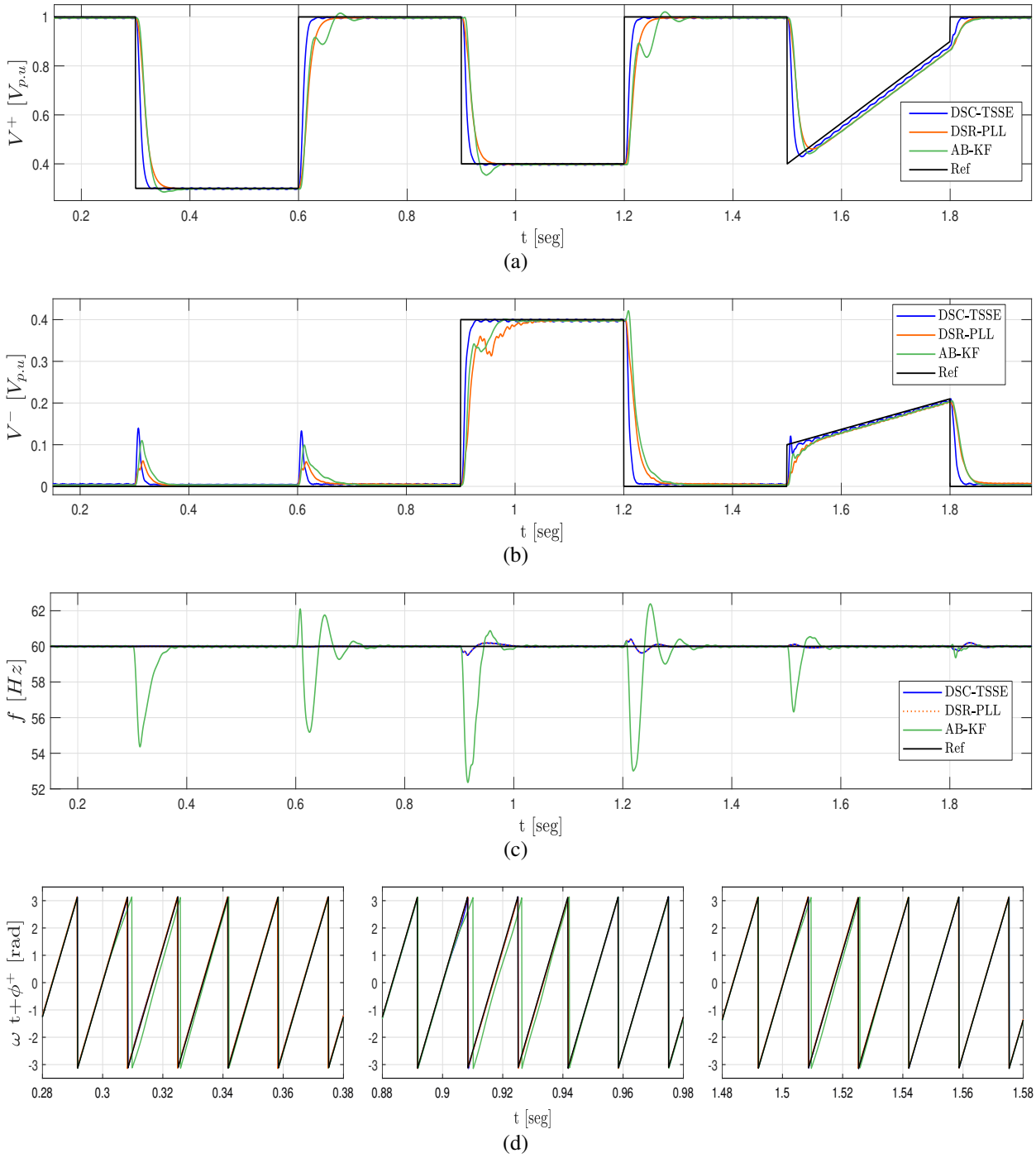


Figure A.4

Results voltage sags scenarios type II with THD = 10,0% a) V^+, b) V^-, c) ω, and d) θ^+

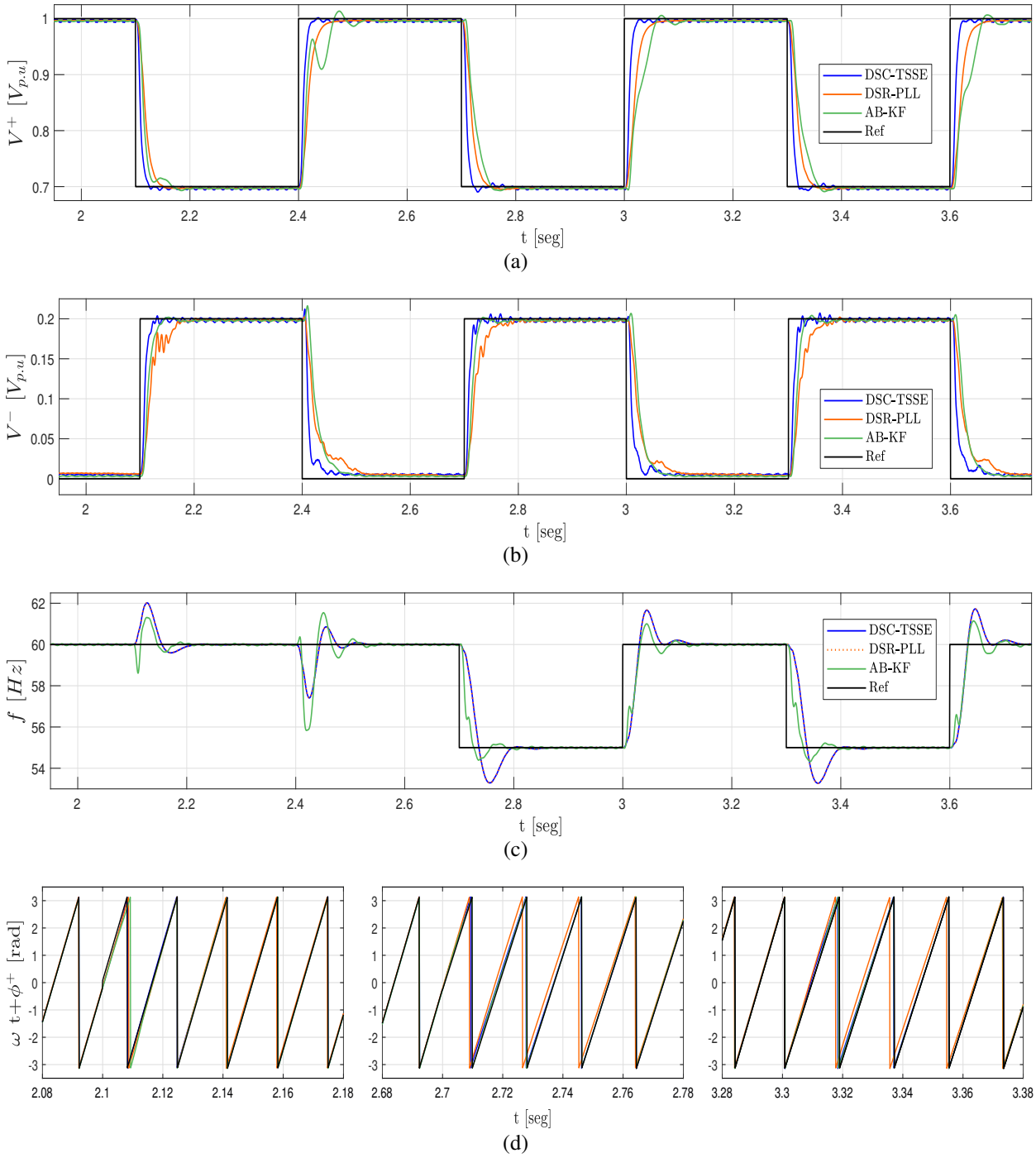


Table A.1

Open-loop experimental results

Algorithm		AB-EKF			DSRF-PLL			DSC-TSSE			AB-EKF			DSRF-PLL			DSC-TSSE		
Criteria		t_s ms	SSE $\times 10^{-3}$	OS	t_s ms	SSE $\times 10^{-3}$	OS	t_s ms	SSE $\times 10^{-3}$	OS	t_s ms	SSE $\times 10^{-3}$	OS	t_s ms	SSE $\times 10^{-3}$	OS	t_s ms	SSE $\times 10^{-3}$	OS
Scenario		THD = 7.35 %									THD = 10 %								
V_s-1	V^+	36,10	1,77	0,01	45,20	0,68	0,00	21,20	2,13	0,00	35,00	2,46	0,01	44,80	1,34	0,00	21,20	4,05	0,00
	V^-	38,60	3,41	0,11	32,10	3,13	0,06	16,40	4,64	0,14	35,60	3,63	0,11	30,30	2,37	0,06	16,40	4,84	0,14
	f	89,70	62,4	5,63	0,00	2,20	0,00	0,00	2,20	0,00	68,90	64,20	5,61	0,00	1,60	0,00	0,00	1,60	0,00
V_s-2	V^+	59,20	2,41	0,03	41,90	1,61	0,00	20,50	4,50	0,00	60,30	3,30	0,04	43,10	2,37	0,00	20,50	4,83	0,00
	V^-	62,40	2,66	0,00	39,90	1,25	0,00	19,50	3,90	0,00	62,40	3,73	0,00	91,60	2,62	0,08	19,50	4,90	0,00
	f	102,1	52,50	7,58	78,80	16,90	0,48	78,80	15,90	0,48	101,8	58,60	7,64	79,20	16,40	0,50	79,20	16,40	0,50
V_s-3	V^+	-	27,47	0,03	-	27,40	0,03	19,30	19,91	0,02	-	35,09	0,03	-	34,60	0,03	-	21,80	0,02
	V^-	36,90	7,51	0,02	33,3	8,18	0,01	12,20	7,65	0,02	33,40	6,88	0,02	33,10	8,76	0,04	12,60	7,01	0,02
	f	83,70	46,70	3,68	17,90	15,60	0,12	17,90	15,60	0,12	83,50	58,20	3,65	17,40	15,30	0,12	17,40	15,30	0,12
V_s-4	V^+	27,80	2,93	0,01	35,10	1,65	0,00	18,50	4,32	0,00	24,80	4,12	0,01	34,60	3,21	0,00	18,50	5,84	0,00
	V^-	29,30	2,50	0,00	56,80	1,98	0,04	16,37	4,61	0,00	25,30	3,01	0,00	57,10	2,48	0,06	17,10	4,82	0,00
	f	90,60	58,60	1,36	98,20	15,40	2,12	98,20	15,40	2,12	90,30	55,30	1,39	99,30	13,50	2,01	99,30	13,50	2,01
V_s-5	V^+	47,40	2,53	0,01	37,20	1,56	0,01	17,40	4,69	0,01	46,40	4,13	0,01	36,20	3,17	0,01	17,40	5,59	0,01
	V^-	24,70	2,51	0,00	46,10	2,67	0,05	15,20	4,62	0,01	24,70	2,98	0,00	46,40	3,29	0,05	15,20	4,38	0,01
	f	104,9	46,60	0,62	92,70	5,70	1,72	92,70	5,70	1,72	81,80	43,60	0,61	92,70	4,60	1,71	92,70	4,60	1,71
V_s-6	V^+	49,40	0,98	0,01	37,10	1,65	0,01	17,80	4,94	0,01	47,70	4,13	0,01	36,40	3,26	0,01	17,80	5,59	0,01
	V^-	25,70	2,51	0,00	40,50	2,49	0,04	16,20	4,62	0,01	25,00	2,89	0,00	44,40	2,99	0,04	16,20	4,46	0,01
	f	88,00	42,20	0,70	92,70	5,50	1,74	92,70	5,50	1,74	88,00	42,20	0,68	92,70	4,90	1,73	92,70	4,90	1,73

Units for *SSE* and *OS* are V for the voltage amplitudes and Hz, respectively.

The other two exceptions correspond to overshoot values on V^-'s estimation for the DRSF-PLL in voltage sags cases V_s-2 and V_s-4. For voltage sag V_s-2 considering a THD=7,35 % the *OS* of V^- accomplishes the established criteria. However, this is not true for harmonic distortion cases 2 and 3 in which an $OS = 0,06$ [V_{pu}] is obtained. Similarly, V^-'s *OS* for voltage sag V_s-4 considering a THD=10,0 %, surpass the *OS* limit with a value of $0,08$ [V_{pu}]. On the contrary, the *OS* of V^-'s estimation for harmonic distortion cases 1 and 3 meet the established criteria.

The last difference in the highlight of the table corresponds to the t_s of the AB-EKF frequency estimation for voltage sag case V_s-5 considering a THD=7,35 %, in which this value exceeds the 100 [ms]. Nevertheless, t_s meets the established criteria for harmonic distortion cases 2 and 3. To conclude, the *SSE* is the parameter whose performance degraded the most as the harmo-

nic distortion content increased.

Close-loop complementary results

Figure A.5 presents the experimental results for the closed-loop test considering harmonic distortion case 2, THD=10,0%. Results for non-harmonic distortion content are included to facilitate the analysis and comparison among the two cases. Figure A.5 shows that the results for a THD=10,0% are almost the same as the non-harmonic distortion case. Therefore, it is concluded that the voltage parameters estimation of the DSC-TSSE is slightly affected by the harmonic distortion as stated in Section 2.3.2.

Table A.2 presents the positive and negative sequences' amplitudes, their respective t_s, the THD of the PCC voltages, and the TRD of the injected currents for the closed-loop test considering harmonic distortion cases 0 and 2.

Figure A.5

Close-loop results for voltage sags scenarios type I a) V^+, b) V^-, c) ω, d) i_{abc} for voltage THD=0 %, e) i_{abc} for voltage THD=10,0 %*

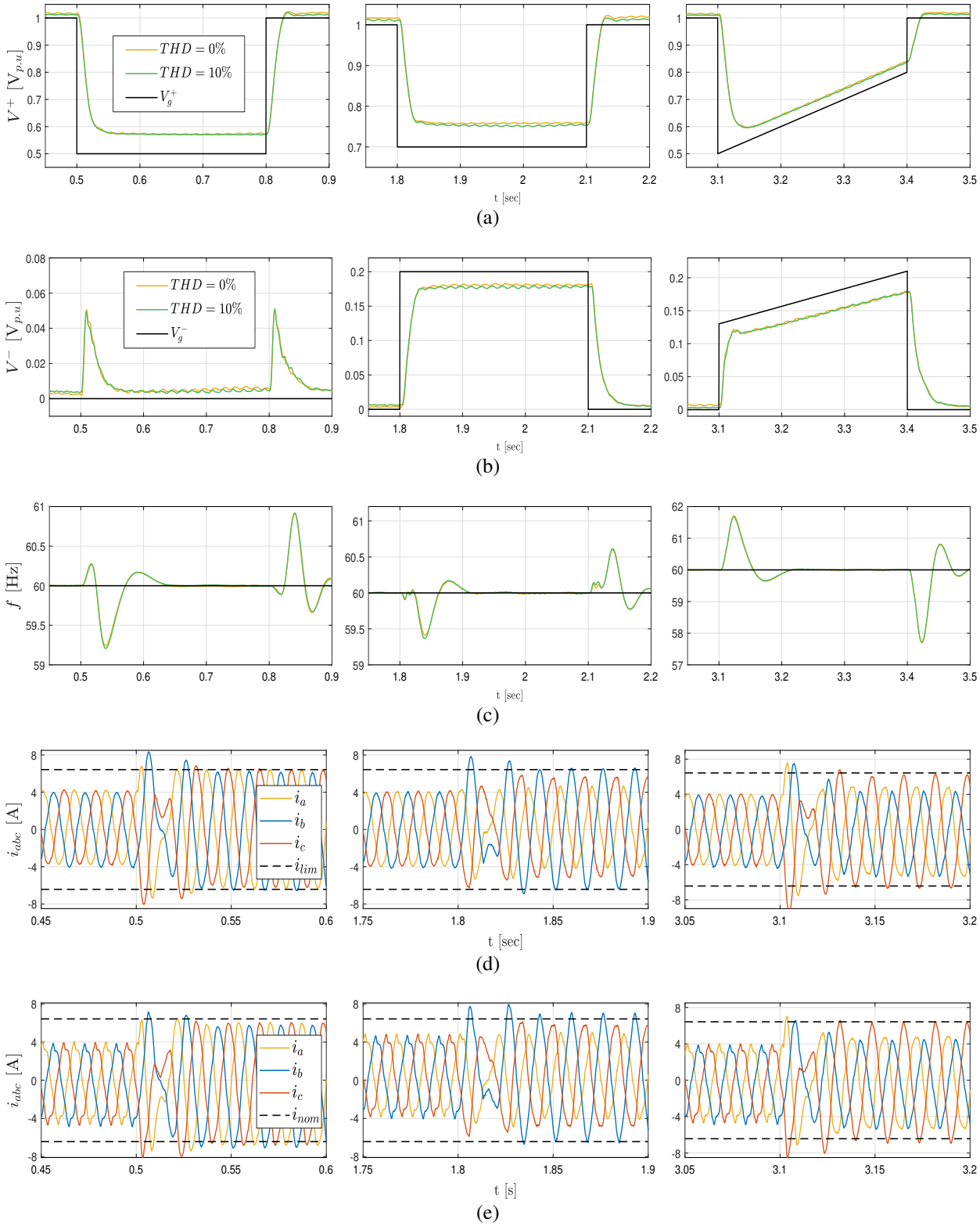


Table A.2

Results of the close-loop test

Harmonic distortion	THD=0 %			THD=7,35 %			THD=10,0 %		
Voltage sag	V_s-1*	V_s-2*	V_s-3*	V_s-1*	V_s-2*	V_s-3*	V_s-1*	V_s-2*	V_s-3*
V^+ [V_{pu}]	0,58	0,76	0,04†	0,57	0,76	0,04†	0,57	0,75	0,04†
t_{V^+} [ms]	39,3	23,8	47,6	38,4	24,9	43,1	35,4	25,8	43,5
V^- [V_{pu}]	0,01	0,18	0,03†	0,01	0,18	0,03†	0,01	0,18	0,03†
t_{V^-} [ms]	27,1	39,1	25,9	27,4	28,6	25,1	24,2	30,6	25,1
V_a THD %	3,00	1,83	1,94	5,49	4,56	3,49	7,59	6,46	4,84
V_b THD %	3,00	2,28	1,60	5,29	6,80	4,94	7,55	9,14	6,40
V_c THD %	2,74	2,28	2,30	5,29	4,08	6.84	7,55	5,56	8,38
i_a TRD %	3,35	4,16	6,18	4,32	4,00	6,12	4,29	3,96	6,58
i_b TRD %	3,35	4,20	4,72	4,32	4,26	4,14	4,29	4,50	4,13
i_c TRD %	3,35	6,73	3,12	3,75	6,53	4,00	4,29	7,03	3,80

† In the case of the voltage sag scenario 3, the voltage support value correspond to $\Delta V^+ = V^+ - V_g^+$ and $\Delta V^- = V_g^- - V^-$.
Note: t_s reference is changed to the steady state value of the corresponding sequence voltage during the sag.

According to Table A.2, results for a THD=10,0 % are more similar to harmonic content case 1 than to case 3 [15]. One possible explanation is that harmonic content case 3 (THD=13,23 %) is the only case in which the distortion limit of 5,0 % per individual harmonic is exceeded. Nevertheless, it should be mentioned that for a THD=10,0 %, the injected currents TRD surpass 5,0 % normal operation, which is the limit established in the IEEE Std 519. This limit infringement is reasonable since the TRD limit considers a maximum voltage THD=8,0 % [15]. Therefore, the inverter exhibits adequate performance only in cases where the voltages THD accomplish the IEEE Std 519 criteria.