Design and implementation of SRAM, DAC and ADC interfaces for APB and AHB-LITE buses

Camilo Eduardo Rojas Ortiz

Trabajo de Grado para optar por el título de ingeniero Electrónico

Director

Ckristian Ricardo Esteban Duran Blanco

MSC en Telecomunicaciones

CO-Director

Elkim Felipe Roa Fuentes

Ingeniero Electricista, PhD

Universidad Industrial de Santander

Facultad de Ingeniería Físico-Mecánicas

Escuela de Ingenierías Eléctrica, Electrónica y de Telecomunicaciones

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Título Diseño e implementación de las interfaces SRAM para AHB-LITE, DAC y ADC Para APB[*]

Autor Camilo Eduardo Rojas Ortiz[**]

Palabras claves SRAM, interfaz, bus de comunicación, Chisel, internet de las cosas.

DESCRIPCIÓN

Este trabajo presenta tres diferentes interfaces para la segunda versión del microcontrolador Open-V: AMBA High-performance Bus Lite (AHB-Lite) para una SRAM, y Advanced Peripheral Bus (APB) para un ADC y un DAC. Las interfaces propuestas son el puente de comunicación entre el bus de los periféricos y la instanciación del periférico analogico, estableciendo la manera en la cual cualquier maestro (como un procesador RISC-V) los controla.. Las interfaces fueron descritas en Chisel, el mismo HDL en el cual serán descritos todos los bloques del microcontrolador, tomando ventaja de sus capacidades para facilitar la integración de todos los bloques digitales.

Se explica detalladamente el funcionamiento de cada una de las interfaces y se presenta su circuito digital, así como la interconexión con el respectivo bus de comunicaciones dentro del integrado. Resultados de síntesis en 180nm son mostrados, realizando una comparación entre la interfaz para el DAC y para el ADC en la versión uno y versión dos, mostrando la ganancia en área y consumo potencia obtenidas en la versión dos, así como el reporte de síntesis para la interfaz de la SRAM. Adicionalmente se muestran algunas generalidades de los protocolos de comunicación AMBA diseñados por ARM como son: AXI, AHB y APB, mostrando algunas aplicaciones para cada uno de ellos.

[*] Trabajo de grado

[**] Facultad de Ingenierías Físico-Mecánicas. Escuela de ingeniería Eléctrica, Electrónica y Telecomunicaciones. Director: Ckristian Ricardo Esteban Duran Blanco Elkim Felipe Roa Fuentes

Abstract

Title Design and implementation of SRAM, DAC and ADC Interfaces for APB and AHB-lite buses[*]

Author Camilo Eduardo Rojas Ortiz[**]

Keywords SRAM, interface, communication bus, Chisel, internet of things.

DESCRIPTION

This paper presents three different interfaces for the second version of Open-V microcontroller: AMBA High-performance Bus Lite (AHB-Lite) for a SRAM, and Advanced Peripheral Bus (APB) for an ADC and a DAC. The proposed interfaces are the communication bridge between the peripherals bus and the analog peripheral instantiation, establishing the way in which any master (like a RISC-V processor) handle them. The interfaces were described in Chisel, the same HDL where all digital blocks of the microcontroller were described, taking advantage of their capabilities to facilitate the integration of all digital designs.

It explains in detail the operation of each of the interfaces and presents its digital circuit, as well as the interconnection with the respective on-chip communication bus. Synthesis results in 180 nm are shown, making a comparison between the interface for the digital to analog converter (DAC) and for the analog to digital converter (ADC) in version one and version two, showing the area gain and power consumption obtained in version two, as well as the synthesis report for the interface of the static random access memory (SRAM). In addition, some generalities of the AMBA communication protocols designed by ARM are shown: AXI, AHB and APB, showing some applications for each of them.

[*] Bachelor degree

[**] Faculty of Physic-Mechanical Engineering. School of Electrical Engineering, Electronics and Telecommunications. Advisor Ckristian Ricardo Esteban Duran Blanco Elkim Felipe Roa Fuentes

Introduction

Nowadays, the electronic industry has had a strong role in the society, supplying the needs of consumers and industries, presenting solutions to improve people's life. An important part of these technological advances is due to innovations in semiconductor industry, some of the most important advances in this area are: cheaper manufacturing process, low and ultra low-power consumption System-on-Chips (SoCs) that works with higher frequencies, and sensors for all type of variables. These advances have contributed to the development of the Internet of Things (IoT).

The second version of the Open-V microcontroller buses are designed to be a medium and low complexity bus interfaces, optimized for low-power consumption in Always-On (AON) applications. The Open-V microcontroller architecture, shown in Fig.1, has a new 32-bit processor, three-stage Single Issue In Order (SIIO) pipelined based on RISC-V ISA, a single core named Olinguito, which is was development by Onchip group from Universidad Industrial de Santander, with deferents peripherals such as: SPI, I2C, USB, and worked by this project: a SRAM, a DAC and an ADC, the last two in the AON module. Peripheral interfaces are important parts in microcontrollers, since they handle the off-processor communication with analog or external peripherals.

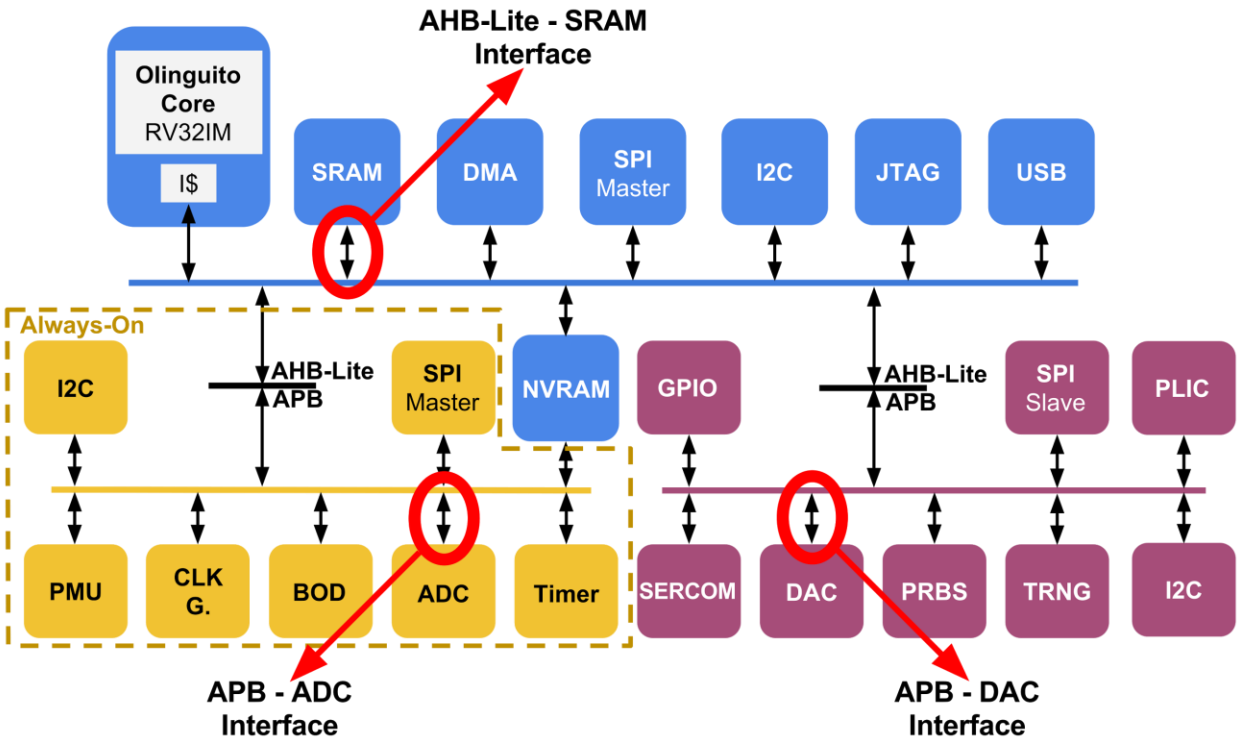

Figure 1 Open-V microcontroller architecture v.2.

The interfaces will be integrated with the processor and for this reason, those were described using Chisel Hardware Description Languages (HDL) as well as Olinguito. Chisel is an open-source hardware construction language developed at UC Berkeley that supports advanced hardware design using highly parameterized generators and layered domain-specific hardware languages (Jonathan B,, Huy V., Krste A. 2016).

This work presents the design and implementation of three on-chip bus-peripherals interfaces, one for medium and two for low-power consumption, to be used as part of the connection between the processor and the peripheral. These interfaces will be used in the integration of Open-V microcontroller to be tape-out in September 2017 in a Multi-Project-Wafer (MPW) in collaboration with SiFive, a fabless from San Francisco, California.

1. AMBA Protocols

On-chip interconnections represent a challenge for SoC designs, since they directly affect their performance and power consumption. Therefore, bus protocols must be carefully selected according to the SoC proposed. AMBA (Advance Microcontroller Bus Architecture) is a set of standard protocol buses for microcontrollers developed by ARM (AMBA SPECIFICATIONS. 2017), in order to show alternatives for several types of applications by their processing capacity and complexity. Some of the most outstanding protocol buses are:

1.1.Advanced eXtensible Interface (AXI)

The AXI is the most widespread AMBA interface, it can connect

hundreds of Masters and Slaves in complex SoCs. AXI is Designed for high-performance and high-frequency systems] (AMBA axi and ace protocol specification. 2011)..

The most outstanding features that have AXI is the separation address/control signals and data phases, burst-based transactions with only the start address issued. AXI separates read and write data channels, providing flexibility in the implementation of interconnect architectures.

The first version of Open-V microcontroller development by Onchip group (Duran, C., Rueda, D. L., Castillo, G., Agudelo, A., Rojas, C., Chaparro, L., ... & Ardila, J. 2016), uses the AMBA AXI4-Lite as its main bus.

1.2 Advanced High-performance Bus (AHB)

The AHB is a bus interface suitable for high-performance synthesizable designs, defining the connections among slaves, masters and bridge interconnect. AHB implements features like burst transfer, single clock-edge operation, a configurable wide data bus.

In order to provide multi-master designs, AHB needs an interconnect component that provides arbitration and routing signals from different masters to the appropriate slaves. Such as AXI, AHB has a reduced implementation named AHB-Lite (Amba ahb-lite specification. 2008), which reduces not only performance but also power consumption and complexity.

1.3 Advanced Peripheral Bus (APB)

The APB protocol was designed for low-frequency operations peripherals, it is optimized for minimal power consumption and reduced interface complexity (Amba apb specification. 2008). APB protocol is frequently used for controlling peripherals like the register map in a SoCs for AON applications. The APB protocol is not pipelined, this is used to connect to low-bandwidth peripherals which do not require the high performance of the AXI or AHB protocol.

2. SRAM interface for AHB-LITE

The SRAM will be used as one of the on-chip storage options for the Open-V v.2, which makes one of the most important peripherals in the implementation. The desired memory block to be instantiated manages 32-bit wide data and 1024 address (4kB). Fig.2 shows the signals of the AHB-Lite bus through SRAM Interface and finally to SRAM block.

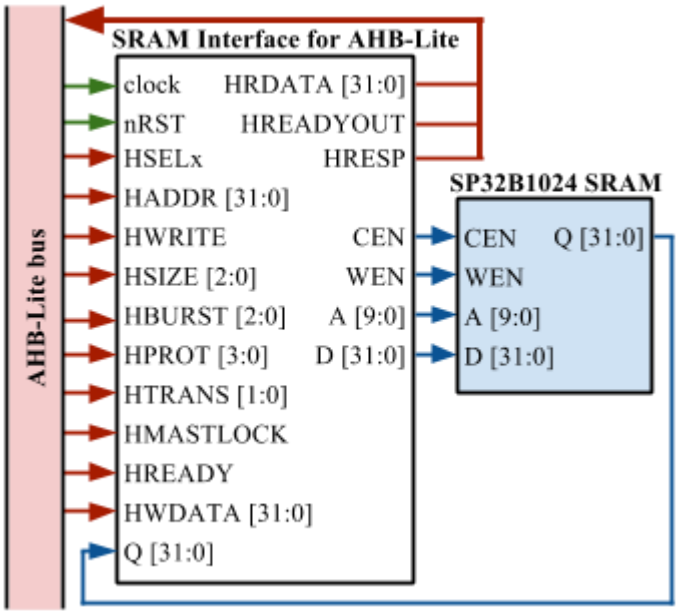

Figure 2. SRAM interface for AHB-Lite connections.

The SRAM interface shown in Fig.3, constituted by three registers to storages HADDR, Q, and HWDATA when a transaction is required for the bus, this happens when HSElx and HREADY are high and HTRANS is equal to two. Once the data is stored, a little state-machine is enabled to do the write or read transactions in order to generate the appropriated signals to CEN (Control

Enable) and WEN (Write Enable), then, the mux writes the data with the desired bytes according to the HSIZE signal.

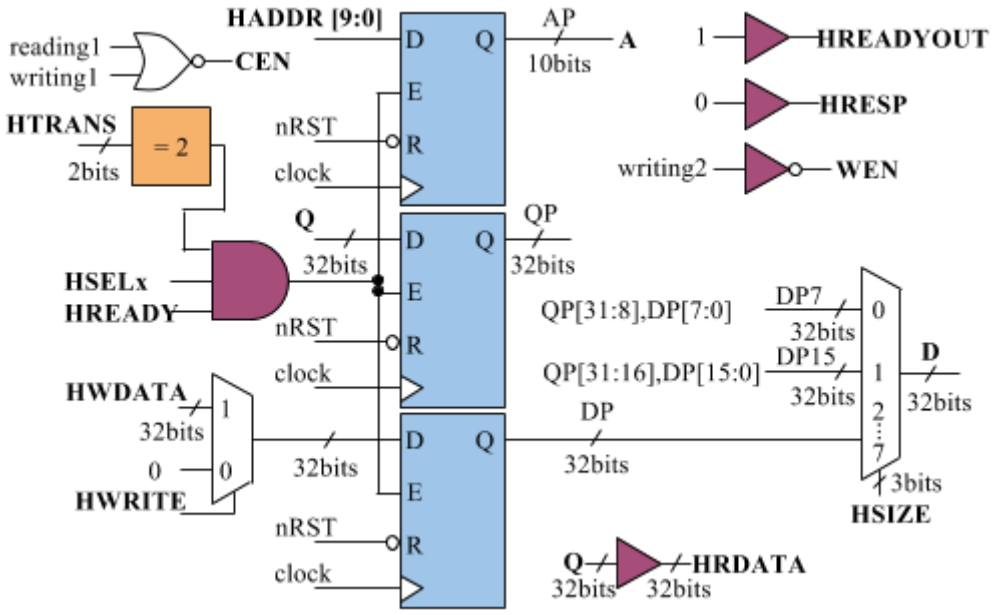

Figure 3. SRAM interface circuit diagram.

HREADYOUT signal is always high and HRESP is always low, due to the address capturing is a single clock operation. HRDATA is always Q, thanks to the CEN and WEN signals, which will avoid erroneous data from the SRAM block.

3. DAC and ADC interfaces for APB

Digital to analog and analog to digital converters, are some of the most used peripherals currently, offering connections between the digital and analog world, making it possible the data analysis at every moment. To handle this peripherals, an interface is needed to control and to obtain the best performance of them.

This project has as main objective the low-power consumption, AMBA APB was selected by the low-bandwidth operations peripherals, due to it provides minimum complexly design and high efficiently operation compared to AMBA AXI or AMBA AHB.

3.1 DAC interface for APB

The selected DAC is based in R2R architecture with 12-bit resolution, rail to rail output voltage and a typical settling time of 100 [ns].

To design the interface, it was necessary to know the correct operation in normal conditions of the DAC, having knowledge of a the number of bits for each one of the pins and their function, the time delay of the DAC conversion, max frequency operations and general restrictions of its functionality. On the other hand, it was necessary a study of the AMBA APB bus protocol, each of its characteristics and restrictions.

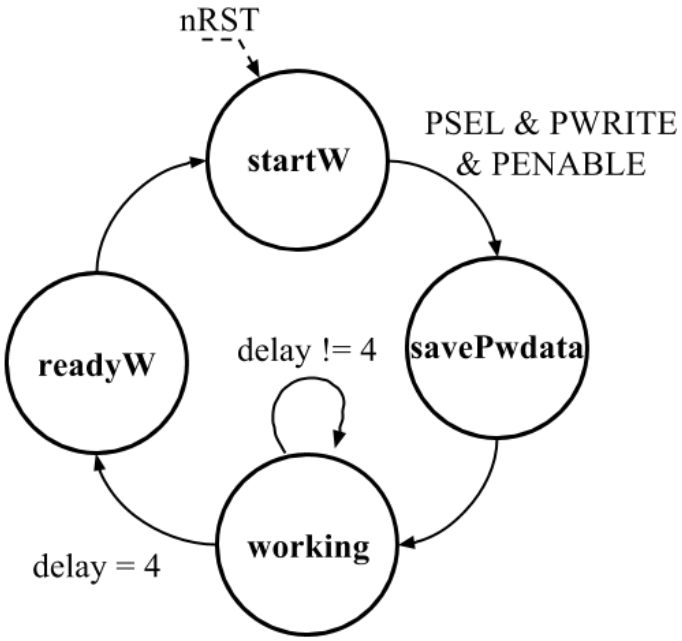

Figure 4. Writing control FSM.

DAC interface for APB is defined by the operation of the FSM shown in Fig.4. Waiting in "startW" state until PSEL, PWRITE, and PENANLE signals are high, to save PWDATA from the APB bus on the registers in "savePwdata" state, and in the next state of the FSM "working", activate the mux of the DATA, which is directly connected to the DAC, and waiting four clock cycles at 100 [MHz], then, sending to the bus PREADY in high in "readyW" state to indicate a transaction success.

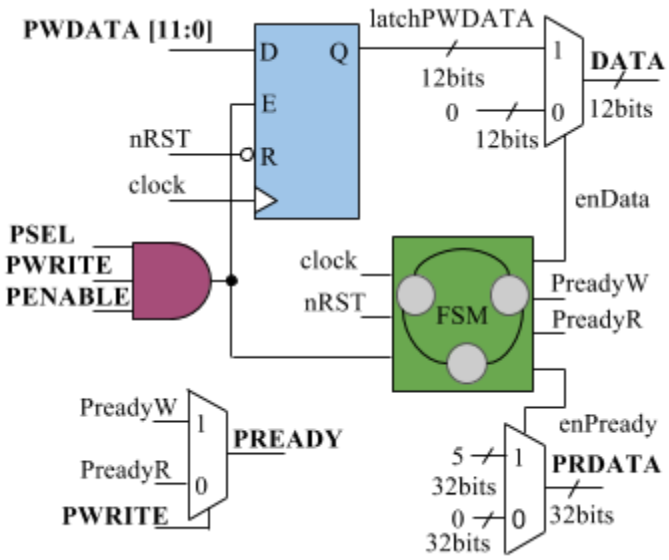

Figure 5. DAC interface for APB.

For reading transactions, the interface sends to the bus a five number in PRDATA, to indicate an erroneous order, as shown in Fig.5. Depending on whether it is a transaction of write or read (PWRITE), PREADY is selected between PreadyW and PreadyR from FSM.

3.2 ADC interface for APB

The selected ADC is a successive approximation register (SAR) ADC, 10-bit resolution converter, and operates at maximum sampling frequency of 10 [MHz]. The ADC interface for APB shown in Fig.6, is similar to the DAC interface in Fig.5, both interfaces have a register, an output data mux controlled by an FSM, and the same mux for PREADY signal, but since the function of this interface is to collect data from the ADC, the enable signal in register is BUSY from ADC, meaning that the interface will not catch the entire microcontroller operation while the ADC process the data.

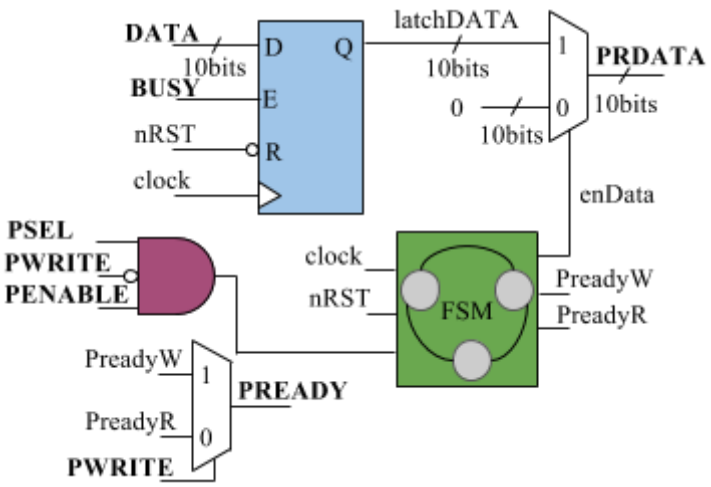

Figure 6. ADC interface for APB.

The FSM presented in Fig.7, controls the mux of PRDATA, writing the data in the bus in "process" state, and PreadyW or PreadyR signals in high in "startR" state.

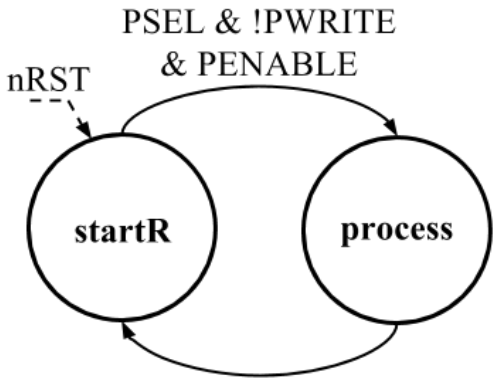

Figure 7. Control FSM.

4. Verifications and results

Using a testbench described in Chisel, verification of overall functionality interfaces has been performed. Ones the design in Chisel is finished, a Verilog file is generated from Chisel using SBT, a Chisel compiler. Signal generation, interfaces, peripherals and communications transactions are shown in Fig.8. Each interface was tested separately, with their corresponding peripherals and signals.

The testbench of the DAC interface for APB sends to the interface read and write request, and the signal scoreboard registers all the incoming information flow, of the whole trajectory until the peripheral, to verify the correct data in the input of the DAC.

On the other hand, the testbench of SRAM interface for AHB-Lite sends to the interface different values of HSIZE, and the signal scoreboard verify the correct data in the input and output of SRAM block.

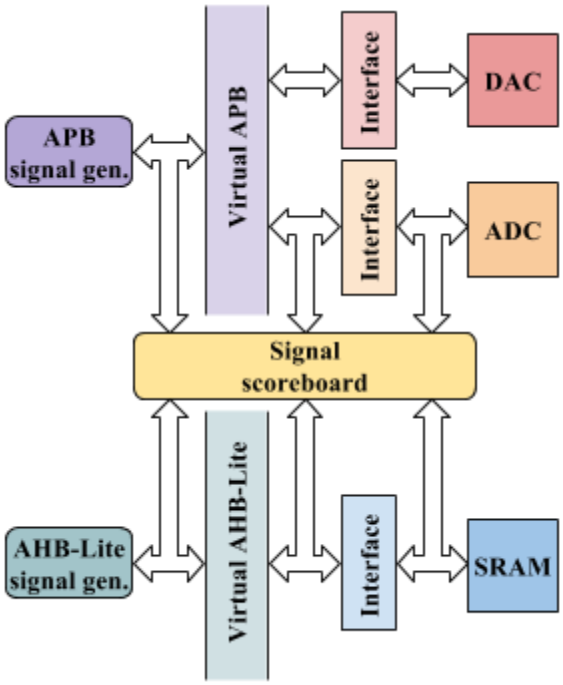

*Figure 8.*Testbench signaling.

The interfaces was fully-synthesized in TSMC 180 [nm] CMOS technology. Synthesis results are shown in Table.1 for each interface. For the second version of Open-V microcontroller, the SRAM interface for AHB-Lite occupies almost nine times the area of ADC interface for APB, and a little more than four times the area of DAC interface for APB.

The highest power consumption density comes from the SRAM interface. In synthesis production, the maximum operation frequency is determined by the SRAM, which operates at 100 [MHz]. However, the interfaces has been able to operate at higher frequency.

Table.1.

Synthesis report in TSMC 180nm, typical case.

Interface	Power [nW/Mhz]	Time Slack [ps @ 100Mhz]	Area [µm 2]
ADC - APB v.1	304.98	9402	946
ADC - APB v.2	209.81	9523	904
DAC - APB v.1	1042.71	8931	1793
DAC - APB v.2	394.68	8548	1747
SRAM - AHB-Lite	3540.46	8391	7180

5. Conclusions

This work offers a research work, design and implementation of three different interfaces for the second version of Open-V microcontroller developed by Onchip Group. The implemented interfaces were designed with all requirements from the protocol specifications, and functionality of the peripherals.

Due to the compatibility with AMBA AHB-Lite and AMBA APB, the implemented interfaces can be reused in future works focused in low-power and minimal area consumption.

The comparison between synthesis result of version one and version two, shows a small reduction in area and power consumption.

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